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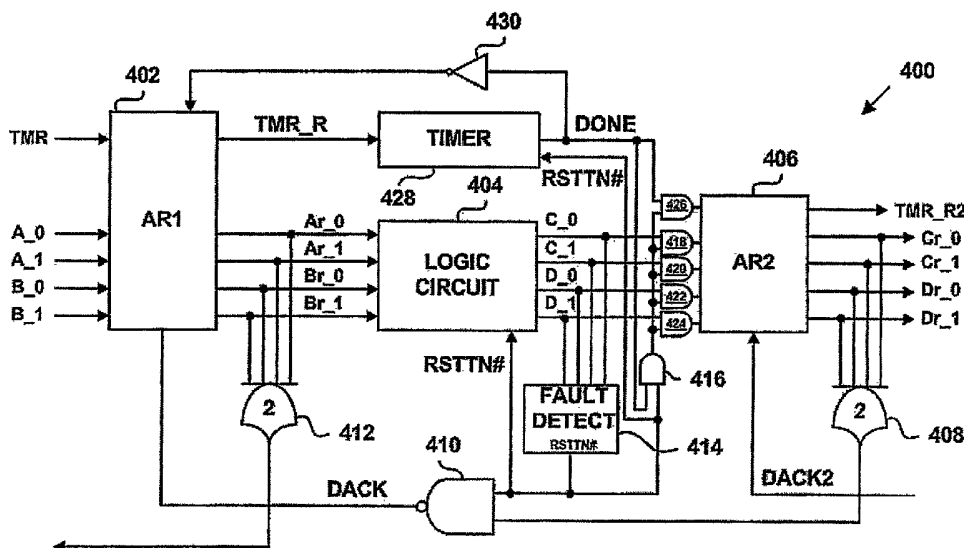
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[Continued on next page]

(54) Title: SYSTEM LEVEL HARDENING OF ASYNCHRONOUS COMBINATIONAL LOGIC CIRCUITS



(57) Abstract: A system and method for hardening an asynchronous combinational logic circuit against Single Event Upset (SEU) is presented. The asynchronous combinational logic circuit is located between two asynchronous registers. A fault detector is used to detect a fault at an output of the asynchronous combinational logic circuit caused by SEU. If the fault detector detects a fault, a first asynchronous register is prevented from clearing stored data and a second asynchronous register is prevented from loading data from the asynchronous combinational logic circuit until the fault is cleared. Further, a timer circuit is used to ensure enough time elapses to allow the asynchronous combinational logic circuit to reevaluate itself. The asynchronous combinational logic circuit reevaluates itself by first propagating a NULL wave front to clear the fault and then propagating the data stored in the first asynchronous register to its outputs.

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	KOL R ET AL: "STATECHART METHODOLOGY FOR THE DESIGN, VALIDATION, AND SYNTHESIS OF LARGE SCALE ASYNCHRONOUS SYSTEMS" IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS, INSTITUTE OF ELECTRONICS INFORMATION AND COMM. ENG. TOKYO, JP, vol. E80-D, no. 3, March 1997 (1997-03), pages 308-314, XP000723717 ISSN: 0916-8532 the whole document ----- -/--	1-10
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Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	HAUCK S: "ASYNCHRONOUS DESIGN METHODOLOGIES: AN OVERVIEW" PROCEEDINGS OF THE IEEE, IEEE. NEW YORK, US, vol. 83, no. 1, January 1995 (1995-01), pages 69-93, XP000495022 ISSN: 0018-9219 page 72, left-hand column - page 76, left-hand column; figures 3-7 -----	1-10