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(54) **Title:** POWER SEMICONDUCTOR APPARATUS

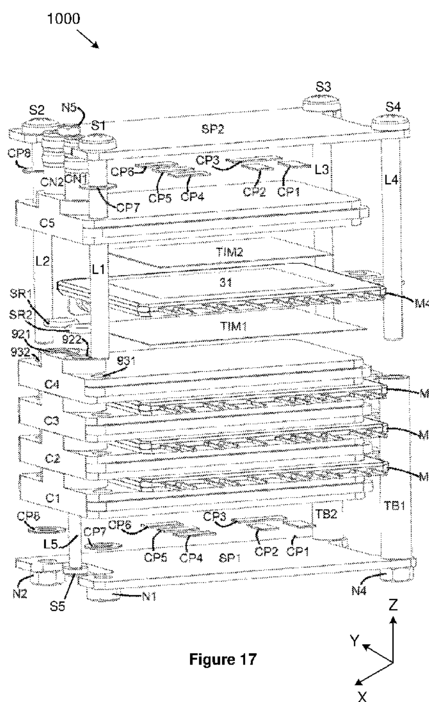
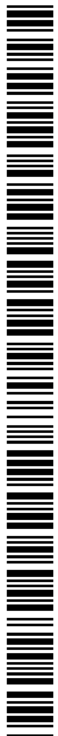


Figure 17

(57) **Abstract:** There is provided a power semiconductor apparatus 1000, comprising: a plurality of power semiconductor modules M1 to M4, each of which comprises at least one semiconductor chip; a plurality of coolers C1 to C5 stacked with the power semiconductor modules along a stacking direction Z, wherein each of the power semiconductor modules is thermally coupled to at least one of the coolers; first and second structural plates SP1, SP2 arranged on opposite sides of the stacked coolers and power semiconductor modules in the stacking direction, wherein the first and second structural plates are configured to pressurise the stacked coolers and power semiconductor modules in the stacking direction; a plurality of compliant components CP1 to CP8 arranged between at least one of the first and second structural plates and the stacked coolers and power semiconductor modules; and a pressure controller comprising first and second ends N1-N4, S1-S4 coupled to the first and second structural plates respectively, wherein a distance between the first and second ends is adjustable so as to control a pressure applied by the structural plates to the stacked coolers and power semiconductor modules in the stacking direction.



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Power Semiconductor Apparatus

Technical Field

The present disclosure relates to a power semiconductor apparatus. More
5 particularly, but not exclusively, the present disclosure relates to a power semiconductor apparatus which comprises a stack arrangement of power semiconductor modules and coolers and a pressure controlling mechanism for controlling a pressure applied to the stack arrangement.

10 Background

Power semiconductor modules have been considered as one of the most delicate components in electric control systems of electric vehicles (EVs) and hybrid electric vehicles (HEVs). For such applications, there has been an increasing demand for power semiconductor modules with increased power density, improved electrical performance
15 and thermal performance, high reliability and reduced costs. In particular, an electric control system for EV/HEV applications typically comprises three and more power converters which are constructed based upon power semiconductor modules. There is generally a limited space to accommodate the power semiconductor modules and their associated connections in the electric control system of an EV/HEV. It is known to stack
20 the power semiconductor modules and coolers, so as to allow the power semiconductor modules to be installed into the limited space allocated for the electric control system.

US 2015/0214205 A1 discloses a power semiconductor module with a reduced wiring inductance and an integrated cooler. The power semiconductor module comprises a single half-bridge switch and is integrated with a cooler having fin-formed base plates
25 and flat walls on both sides. Three such modules can be stacked together to form a three-phase inverter. However, in each module, the insulation between the power semiconductor devices and the cooler is achieved by encapsulation resin, which may degrade the thermal conductance of the relevant heat-flow paths. On the other hand, all of the power terminals and signal/control terminals are protruded from the same side of
30 the module. This would complicate the electrical connections and require a relatively large space to connect the terminals to a power source, power generation/delivery connectors, passive components, and control/drive printed circuit boards (PCBs).

US 2016/0192539 A1 discloses a stack unit where several power cards and
35 coolers are stacked one by one alternately to cool a large number of semiconductor devices. Each power card comprises a single half bridge switch which is sealed in a resin package with two additional insulating plates on both sides to provide the electrical

insulation between the power card and its neighbouring coolers. Each cooler includes a body made of resin, a pair of metal plates and a pair of gaskets. The stack of power cards and coolers are bound together by an outer steel frame which applies pressure to seal the coolers and to ensure intimate contact between the coolers and the insulating plates of the power cards. However, the insulating plates placed between the resin packages and the coolers may degrade the thermal conductance of the relevant heat-flow paths. Further, the outer steel frame which binds the stack needs to be installed with special machines or equipment, which presses the stack with a suitable pressure before the outer steel frame is securely welded around the stack. After the special machines or equipment is removed, the pressure applied by the outer steel frame may differ from the pressure applied by the special machines or equipment, depending upon the quality of the welding process, and cannot be re-adjusted. Therefore, it is generally difficult to control the pressure exerted by the outer steel frame to the stack. Furthermore, due to the spatial restriction imposed by the outer steel frame, the DC power terminals and the output AC terminal extended from the same side of the stack unit, with the signal/control signals extending from an opposite side of the stack unit. Having the DC power terminals and the AC terminal extending from the same side may also complicate the electrical connections and require a relatively large footprint to connect these terminals to the power source, power generation/delivery connectors and passive components.

US 2018/0026533 A1 discloses a boost converter which contains an intelligent power module. The intelligent power module includes a frame holder, semiconductor modules and a cooling portion. The semiconductor modules and the cooling plates of the cooling portion are alternately stacked and are pressurized by the frame holder. However, each of the semiconductor modules is formed by sealing a semiconductor element in a plate-like member with an insulating portion, and comprises a single power transistor in antiparallel connection with a diode. A total of thirty such semiconductor modules are inserted into fifteen slits between sixteen cooling plates to provide a booster converter. With the frame holder to hold such a large number of semiconductor modules and cooling plates, it would be rather tricky to achieve a specified pressure between the semiconductor modules and the cooling plates. Further, external electrical connections would be extremely complicated and would require a large footprint to implement the circuit topology of the boost converter.

It is an object of the present disclosure, among others, to provide an improved power semiconductor apparatus, which solves at least some of the problems associated with known semiconductor devices, whether identified herein or otherwise.

Summary

According to a first aspect of the present disclosure, there is provided a power semiconductor apparatus, comprising: a plurality of power semiconductor modules, each of which comprises at least one semiconductor chip; a plurality of coolers stacked with the power semiconductor modules along a stacking direction, wherein each of the power semiconductor modules is thermally coupled to at least one of the coolers; first and second structural plates arranged on opposite sides of the stacked coolers and power semiconductor modules in the stacking direction, wherein the first and second structural plates are configured to pressurise the stacked coolers and power semiconductor modules in the stacking direction; a plurality of compliant components arranged between at least one of the first and second structural plates and the stacked coolers and power semiconductor modules; and a pressure controller comprising first and second ends coupled to the first and second structural plates respectively, wherein a distance between the first and second ends is adjustable so as to control a pressure applied by the structural plates to the stacked coolers and power semiconductor modules in the stacking direction.

Advantageously, the pressure controller allows the pressure applied by the structural plates to the stack of coolers and power semiconductor modules to be easily established and adjusted to reach a desired level, and the compliant components are useful for distributing the pressure appropriately within the stack so as to improve the reliability of joints within the power semiconductor modules and also to improve the thermal coupling between the power semiconductor modules and the coolers. With the compliant components and the pressure controller, the power semiconductor apparatus eliminates the need of special machines/equipment required by prior apparatuses to apply the pressure to the stack, and also allows the pressure applied to be easily adjusted after the power semiconductor apparatus has been assembled.

The pressure controller may also be referred to as a “pressure adjusting mechanism” or a “pressure regulator”.

It would be understood that the structural plates would have sufficient mechanical strength in order to pressurise the stack without experiencing noticeable deformation in itself. The structural plates may be made of steel.

It would be understood that the expression “first and second ends coupled to the first and second structural plates respectively” encompasses the ends being directly or indirectly coupled to the structural plates, or the ends being integrally formed with the respective structural plates.

The structural plates and the pressure controller may collectively form a supporting frame of the stacked coolers and power semiconductor modules.

The term “compliant components” is intended to mean that the components have mechanical compliance (e.g., malleability, pliability, deformability, softness, shearability, compressibility, stretchiness, and/or geometric reactiveness to external forces applied to the exterior of the components). In an example, the components are able to achieve force and motion transmission through elastic body deformation. The compliant components may be made of a mechanically compliant material (e.g., silicone rubber), or alternatively may obtain compliance due to its structure (e.g., disk spring, coil spring, etc.). The term “compliant components” may be used interchangeably with “mechanically compliant components”.

The term “thermally coupled” used in the present disclosure means that one or more intervening elements may be connected between the coupled elements.

The plurality of compliant components may have a smaller area than at least one of the first and second structural plate (when viewed along the stacking direction). Further, the plurality of compliant components may have a smaller area than at least one of the coolers (when viewed along the stacking direction).

The pressure controller may comprise a linkage member extending between the first and second ends.

The first end may be rotatably coupled to the linkage member. A rotation of the first end with respect to the linkage member may be configured to adjust the distance between the first and second ends.

The linkage member may extend along the stacking direction.

The second end may be securely coupled to the linkage member.

The second end and the linkage member may form a bolt, and the first end may form a nut.

The linkage member may extend through at least some of the plurality of coolers. By extending through at least some of the plurality of coolers, the linkage member is useful for aligning and maintaining the positions of the coolers.

The power semiconductor apparatus may further comprise a tube arranged between the first and second structural plates. The tube may surround at least a part of the linkage member.

The power semiconductor apparatus may further comprise a plurality of the pressure controllers each arranged at a respective corner of the first and second structural plates.

The first and/or second ends of the pressure controller may have a smaller area than the first and/or second structural plates, respectively.

The area of the first/second end may be less than one fifth of the area of the first/second structural plate. The pressure controller may be removable from the first and second structural plates.

The plurality of compliant components may comprise a set of compliant component(s) which overlap the at least one semiconductor chip.

The plurality of compliant components may comprise a further set of compliant component(s) which at least partially surround the linkage member.

The compliant components may be securely attached to an inner surface of the first and/or second structural plates which faces the stacked coolers and power semiconductor modules.

At least one of the coolers may comprise: a main body defined by a first cold plate and a second cold plate securely bonded to one another; and a coolant inlet and a coolant outlet. The main body may comprise a flow channel of coolant therein between the coolant inlet and the coolant outlet.

The first and second cold plates may provide two cooling surfaces arranged at opposite sides of the respective cooler.

At least one of the coolers may further comprise first and second sealing rings surrounding the coolant inlet and coolant outlet, respectively. The first and second sealing rings may provide a seal between the at least one of the coolers and its neighbouring cooler around the coolant inlet and the coolant outlet, and the seal may be secured by the pressure applied by the structural plates.

The first cold plate may comprise a connection region, with the coolant inlet and outlet extending through the connection region and the second cold plate. The connection region may protrude over the remaining of the first cold plate. The connection region may be configured to contact a second cold plate of the neighbouring cooler via the sealing rings under the pressure applied by the structural plates.

The connection region may comprise recesses around the coolant inlet and outlet to hold the sealing rings.

The power semiconductor apparatus may further comprise thermal interface material arranged between at least one of the power semiconductor modules and its neighbouring cooler(s).

Each of the plurality of power semiconductor modules may comprise DC power terminals, AC output terminal(s) and control terminals, wherein: the DC power terminals are arranged at a first side of the respective power semiconductor module; the AC output terminal(s) are arranged at a second side of the respective power semiconductor module; the control terminals are arranged at a third side of the respective power semiconductor module; and no terminals are arranged at a fourth side of the respective power

semiconductor module; and wherein the coolant input and the coolant outlet are arranged at the fourth side of the respective power semiconductor module.

It would be appreciated that the first to fourth sides of the power semiconductor module are defined by a boundary of a substrate of the power semiconductor module.

5 At least one of the power semiconductor modules may comprise a first half-bridge switch and a second half-bridge switch.

The first half-bridge switch and the second half-bridge switch may be electrically connected in parallel between a DC positive power terminal and a DC negative power terminal of the power semiconductor module. The first half-bridge switch may comprise 10 a first high side device, a first low side device and a first output terminal connected therebetween. The second half-bridge switch may comprise a second high side device, a second low side device and a second output terminal connected therebetween.

The at least one of the power semiconductor modules may comprise a first substrate and a second substrate arranged at opposite sides of the power semiconductor 15 module.

The first substrate may comprise a first insulating layer and a first patterned conductive layer arranged on a surface of the first insulating layer which faces the half-bridge switches.

The second substrate may comprise a second insulating layer and a second 20 patterned conductive layer arranged on a surface of the second insulating layer which faces the half-bridge switches.

One or more of the first and second insulating layers may be made of an electrically insulating and thermally conductive material.

The first patterned conductive layer may comprise a first conductive track which 25 electrically connects high side terminals of the first and second high side devices to the DC positive power terminal.

The second patterned conductive layer may comprise a second conductive track which electrically connects low side terminals of the first and second low side devices to the DC negative power terminal.

30 At least three of the power semiconductor modules may each comprise a first half-bridge switch and a second half-bridge switch, and wherein: the first half-bridge switches of the at least three power semiconductor modules collectively form a generator inverter for driving a first electric motor; and the second half-bridge switches of the at least three power semiconductor modules collectively form a motor inverter for driving a 35 second electric motor.

According to a second aspect of the present disclosure, there is provided an electric vehicle comprising a power semiconductor apparatus according to the first aspect.

According to a third aspect of the present disclosure, there is provided a hybrid electric vehicle comprising a power semiconductor apparatus according to the first aspect.

According to a fourth aspect of the present disclosure, there is provided a method of assembling a power semiconductor apparatus, the method comprising:

stacking a plurality of power semiconductor modules and a plurality of coolers along a stacking direction, and wherein each of the power semiconductor modules comprises at least one semiconductor chip and is thermally coupled to at least one of the coolers;

arranging first and second structural plates on opposite sides of the stacked coolers and power semiconductor modules in the stacking direction;

arranging a plurality of compliant components between at least one of the first and second structural plates and the stacked coolers and power semiconductor modules; and

controlling a pressure applied by the first and second structural plates to the stacked coolers and power semiconductor modules in the stacking direction, by adjusting a distance between first and second ends of a pressure controller, wherein the first and second ends are coupled to the first and second structural plates respectively.

The first and/or second ends of the pressure controller may have a smaller area than the first and/or second structural plates, respectively.

Adjusting the distance between the first and second ends may comprise rotating at least one of the first and second ends around a linkage member of the pressure controller, wherein the linkage member extends between the first and second ends.

According to a fifth aspect of the present disclosure, there is provided a method of operating a power semiconductor apparatus, comprising:

pressurising a stack of power semiconductor modules and coolers along a stacking direction with first and second structural plates arranged on opposite sides of the stack, wherein each of the power semiconductor modules comprises at least one semiconductor chip and is thermally coupled to at least one of the coolers; and

adjusting a pressure applied by the first and second structural plates to the stack in the stacking direction, by adjusting a distance between first and second ends of a pressure controller, wherein the first and second ends are coupled to the first and second structural plates respectively.

Adjusting the distance between the first and second ends may comprise rotating at least one of the first and second ends around a linkage member which extend between the first and second ends.

Where appropriate any of the features described above in relation to any aspect of the present disclosure may be applied to any other aspect of the disclosure.

It would also be understood that the terms “first”, “second”, etc. are simply used in the present disclosure to label the relevant elements for the ease of description, and do not imply any limitations to the sequence or locations of the relevant elements.

Brief Description of the Drawings

In order that the disclosure may be more fully understood, a number of embodiments of the disclosure will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 schematically illustrates a circuit diagram of an electric control system for use in EV and HEV applications;

Figure 2 schematically illustrates a circuit diagram of a power semiconductor module for use in a power semiconductor apparatus according to an embodiment of the present disclosure;

Figure 3 schematically illustrates a top perspective view of a power semiconductor module which implements the circuit diagram of Figure 2;

Figure 4 schematically illustrates a bottom perspective view of the power semiconductor module of Figure 3;

Figure 5 schematically illustrates a side view of the power semiconductor module of Figure 3;

Figure 6 schematically illustrates a top perspective view of the power semiconductor module of Figure 3 with an encapsulant and a top substrate being invisible;

Figure 7 schematically illustrates a plan view of the power semiconductor module of Figure 6;

Figure 8 schematically illustrates a bottom perspective view of the top substrate of the power semiconductor module of Figure 3;

Figure 9 schematically illustrates a plan view of the top substrate of Figure 8;

Figure 10 schematically illustrates a spatial relationship between a patterned conductive layer on the bottom of the top substrate and conductive shims used in the module;

Figure 11 schematically illustrates a top perspective view of a power semiconductor apparatus according to an embodiment of the present disclosure;

Figure 12 schematically illustrates a top plan view of the power semiconductor apparatus of Figure 11;

Figure 13 schematically illustrates a bottom perspective view of the power semiconductor apparatus of Figure 11;

5 Figure 14 schematically illustrates a top perspective view of a cooler used in the power semiconductor apparatus of Figure 11;

Figure 15 schematically illustrates a bottom perspective view of the cooler of Figure 14;

Figure 16 schematically illustrates a bottom perspective view of the cooler of
10 Figure 14 but with a bottom cold plate being invisible;

Figure 17 schematically illustrates an exploded view of the power semiconductor apparatus of Figure 11;

Figure 18 schematically illustrates a spatial relationship between compliant components, on the one hand, and the semiconductor chips of the power semiconductor
15 module and through holes of the cooler, on the other hand;

Figure 19 shows process steps of a method for operating a power semiconductor apparatus according to an embodiment of the present disclosure;

Figure 20 shows processing steps of a method for assembling a power semiconductor apparatus according to an embodiment of the present disclosure.

20 In the figures, like parts are denoted by like reference numerals. It will be appreciated that the drawings are for illustration purposes only and are not drawn to scale.

<u>Detailed Description of the Preferred Embodiments</u>

25 Figure 1 shows a high-level circuit diagram of an electric control system 800 which is suitable for use in EV and HEV applications. The electric control system 800 incudes, from left to right, a battery, a variable voltage converter (also called “VVC”) 820, and a dual 3-phase inverter circuit (also called “dual inverter circuit”) which drives two electric motors. The two electric motors generally comprise a generator motor (shown
30 as “G”) and a traction motor (shown as “M”). The generation motor may be for example an integrated starter generator. However, in some cases, both of the electric motors may be traction motors if needed.

The VVC is a bi-directional DC/DC boost converter which boosts up an input voltage from the battery to a system required level. The VVC includes an input capacitor
35 C1, an inductor Lin, and a half-bridge IGBT power module based converter.

The dual inverter circuit includes two independent inverters, i.e., a generator inverter 840 and a motor inverter 860, each providing three-phase AC output for driving

a respective electric motor. The DC-link capacitor C2 supports both inverters by providing a stable input voltage. Both inverters are bi-directional.

During the start, acceleration and cruising operations of HEV/EV, the VVC 820 boosts up the input voltage from the battery to the system required level, and electric
5 power flows from the battery, through the VVC 820 and the dual inverter circuit 840, 860, to one or both of the motors G, M. The dual inverter circuit converts DC power to AC power for driving the motor(s).

During the braking operation of HEV/EV, a propulsion system (not shown in Figure 1) of the HEV/EV will have a slower speed than a rotation speed of the
10 electromagnetic field within the traction motor. This means that the traction motor is charging the battery. The inverter then converts AC power to DC power and utilities the VVC to reduce the converted DC voltage level before charging the battery. During this process, power/energy flows from the traction motor back to the battery through the corresponding inverter.

15 In a typical electric control system in HEV/EV applications, the VVC may handle a higher current than the generator inverter or the motor inverter. This is because the VVC aims to provide power for both the traction motor and the generator motor during the maximum power output operations. However, in some cases, the traction motor can be designed to have higher power output by using the generator motor as part of the
20 input source. Although the generator inverter and the motor inverter are illustrated as three-phase inverters in Figure 1, it would be understood that one or more of the inverters may be a multi-phase inverter.

Figure 2 shows a circuit diagram of a power semiconductor module 100 (also referred to as “power module” for brevity) according to an embodiment of the present
25 disclosure.

The power module 100 comprises a first half-bridge switch 110 and a second half-bridge switch 120 electrically connected in parallel between a DC positive power terminal DC+ and a DC negative power terminal DC- of the power module 100. The first half-bridge switch 110 comprises a first high side device 112, a first low side device 116
30 and a first output terminal AC1 connected therebetween. The second half-bridge switch 120 comprises a second high side device 122, a second low side device 126 and a second output terminal AC2 connected therebetween.

The power module 100 provides one phase of the generator inverter 840 and one phase of the motor inverter 860 as shown in Figure 1. Three instances of the power
35 module 100 shown in Figure 2 can be connected together to provide the generator inverter 840 and the motor inverter 860. In an example, the first half-bridge switch 110 belongs to the generator inverter 840, and the second half-bridge switch 120 belongs to

the motor inverter 860. In a typical electric control system of HEV/EV applications, the generator inverter handles a lower current than the motor inverter. Therefore, each of the first high side device 112 and the first low side device 116 comprises one power transistor chip (i.e., T1 or T2) in anti-parallel connection with one diode chip (i.e., D1 or D2), and each of the second high side device 122 and the second low side device 126 comprises two power transistor chips (i.e., T3&T4, or T5&T6) in anti-parallel connection with two diode chips (i.e., D3&D4 or D5&D6). Further, the power module 100 may also provide the half-bridge structure of the VVC 820. While Figure 1 shows that the VVC 820 is constructed with two half-bridge switches, it would be appreciated that the VVC 820 may alternatively be constructed with a single half-bridge switch. In a typical electric control system of HEV/EV applications, the VVC 820 may handle the highest current. Accordingly, if the power module 100 is used to construct the VVC 820, the two half-bridge switches 110, 120 of one IGBT module 100 may be connected in parallel by external connections to form the single half-bridge switch of the VVC 820.

In an example, the power transistor chips T1 to T6 of Figure 2 are insulated gate bipolar transistor (IGBT) chips, and the diode chips D1 to D6 are fast recovery diode (FRD) chips. It would be appreciated that depending on power and current ratings, each of the half-bridge switches 110, 120 may have different numbers of power transistor chips and diode chips from those shown in Figure 2. Further, the power transistor chips and diode chips may be wide bandgap semiconductor power chips, such as silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET), and Schottky diode chips. Furthermore, the body diodes of the SiC MOSFETs may be used such that the Schottky diode chips may be eliminated. A negative temperature coefficient (NTC) thermistor 130 is integrated in the module 100 as a temperature sensor.

The first high side device 112 has a high side power terminal 113 (also referred to herein as "collector terminal" and "collector/cathode terminal") that is coupled to DC+ terminal, a low side power terminal 114 (also referred to herein as "emitter terminal" and "emitter/anode terminal") that is coupled to the first output terminal AC1, and control terminals G1, C1 and E1 for switching on and off its power transistor chip T1. Similarly, the first low side device 116 has a high side power terminal 117 that is coupled to the first output terminal AC1, a low side power terminal 118 that is coupled to the DC- terminal, and control terminals G2, C2 and E2 for switching on and off its power transistor chip T2. The second high side device 122 has a high side power terminal 123 that is coupled to DC+ terminal, a low side power terminal 124 that is coupled to the second output terminal AC2, and control terminals G3, C3 and E3 for switching on and off its power transistor chips T3 and T4. The second low side device 126 has a high side power terminal 127 that is coupled to the first output terminal AC2, a low side power terminal

128 that is coupled to the DC- terminal, and control terminals G4, C4 and E4 for switching on and off its power transistor chips T5 and T6.

The physical structure of the power module 100 that implements the circuit diagram of Figure 2 is shown in Figures 3 to 10. In the physical structure, the power transistor chips T1 to T6 are embodied as IGBT chips, and the diode chips D1 to D6 are embodied as FRD chips.

The power module 100 has a bottom substrate which comprises an electrically insulating layer 20 (Figures 6 and 7), a patterned electrically conductive layer arranged on an inner surface of the insulating layer 20, and another electrically conductive layer 21 (Figure 4) arranged on an outer surface of the insulating layer 20. The "outer surface" used in the present disclosure refers to a surface which faces away from the IGBT chips or the FRD chips and is typically exposed to an exterior of the power module 100. The "inner surface" used herein refers to a surface opposite to the outer surface, and is typically encapsulated by an encapsulant 80 (Figure 3). The patterned electrically conductive layer of the bottom substrate forms conductive tracks 201 to 215 on the inner surface of the insulating layer 20. The conductive tracks 201 to 215 are separated, thus electrically isolated, from one another. Each of the conductive tracks 201 to 215 is a single continuous (i.e., unbroken) track.

With reference to Figures 6 and 7, collector pads of the IGBT chips T1, T3 and T4 and cathode pads of the FRD chips D1, D3 and D4 (i.e., the high side terminals 113, 123 of Figure 2) are securely attached (or bonded) to the conductive track 205 of the bottom substrate. Terminal 15 (i.e., the DC+ terminal of Figure 2) is further bonded to the conductive track 205 which also holds Terminal 5 (i.e., the C1/C3 terminal of Figure 2). The collector pad of the IGBT chip T2 and the cathode pad of the FRD chip D2 (i.e., the high side terminal 117 of Figure 2) are attached to the conductive track 213. Terminal 13 (i.e., the AC1 terminal) is bonded to the conductive track 213. Collector pads of the IGBT chips T5, T6 and cathode pads of the FRD chips D5, D6 (i.e., the high side terminal 127 of Figure 2) are attached to the conductive track 212. Terminal 12 (i.e., the AC2 terminal) is further bonded to the conductive track 212.

With further reference to Figures 6 and 7, a wire bond 71 is used to connect the gate pad of the IGBT chip T1 to the conductive track 201 holding Terminal 1 (i.e., the G1 terminal of Figure 2). Wire bonds 73, 74 are used to connect the gate pads of the IGBT chips T3 and T4 to the conductive track 203 holding Terminal 3 (i.e., the G3 terminal). A wire bond 72 is used to connect the gate pad of the IGBT chip T2 to the conductive track 206 holding Terminal 6 (i.e., the G2 terminal). Wire bonds 75, 76 are used to connect the gate pads of the IGBT chips T5 and T6 to the conductive track 208 holding Terminal 8 (i.e., the G4 terminal).

Conductive shims 41 to 46, 51 to 56 and 601 to 610 in combination with conductive tracks 301 to 303 of a top substrate are used to achieve the remaining interconnections required by the circuit diagram of Figure 2.

With reference to Figures 6 and 7, conductive shims 41 to 46 are bonded to topside bond pads (i.e., power emitter pads) of IGBT chips T1 to T6, respectively, and conductive shims 51 to 56 are bonded to topside bond pads (i.e., anode pads) of FRD chips D1 to D6, respectively. The topside bond pads of the IGBT chips T1 to T6 and the FRD chips D1 to D6 correspond to the low side terminals 114, 124, 118 and 128 of Figure 2.

The conductive shims 601 to 603 and 606 to 608 are bonded to conductive tracks 204, 207, 209, 213, 215, 202, respectively. Conductive shims 604, 605 and Terminal 14 are both bonded to the conductive track 214. Terminal 16 is bonded to the conductive track 215. As described below in more detail, Terminals 14, 16 collectively provide the DC- terminal of Figure 2. Conductive shims 609, 610 are both bonded to the conductive track 212.

As shown in Figure 6 which is a perspective view of the power module 100 with the top substrate and the encapsulant 80 being invisible, the conductive shims 41 to 46, 51 to 56 and 601 to 610 extend upwards along a direction that is generally perpendicular to the insulating layer 20 of the bottom plate. A height of each of the conductive shims 601 to 610 is substantially the same as a sum of a height of each IGBT chip T1 to T6 and a height of each of the conductive shims 41 to 46, and also substantially the same as a sum of a height of each FRD chip D1 to D6 and a height of each of the conductive shims 51 to 56. In this way, the top surfaces of the conductive shims 41 to 46, 51 to 56 and 601 to 620 are generally aligned at the same level with respect to the bottom substrate. It would be understood that the height of each of the conductive shims 601 to 610 is greater than a thickness of each of Terminals 1 to 16, such that Terminals 1 to 16 would not directly contact conductive tracks on the top substrate of the power module 100.

The top substrate of the power module 100 comprises an electrically insulating layer 30 (Figures 8 and 9), a patterned electrically conductive layer (Figures 8 and 9) arranged on an inner surface of the insulating layer 30, and another electrically conductive layer 31 (Figure 3) arranged on an outer surface of the insulating layer 30. As shown in Figures 8 and 9, the patterned electrically conductive layer of the top substrate forms conductive tracks 301 to 303 on the inner surface of the insulating layer 30. The conductive tracks 301 to 303 are separated, thus electrically isolated, from one another. Each of the conductive tracks 301 to 303 is a single continuous (i.e., unbroken) track.

In Figures 6 and 7, the encapsulant 80 and the top substrate have been omitted from the drawings in order to clearly illustrate the layout of the IGBT chips, the FRD chips and the conductive shims with respect to the bottom substrate. To assemble the power module 100, the top substrate shown in Figure 9 is flipped over with the conductive tracks 301 to 303 facing the structure as shown in Figure 7, and the conductive tracks 301 to 303 are then bonded to the top surfaces of the conductive shims 41 to 46, 51 to 56 and 601 to 610. The spatial relationship of the conductive tracks 301 to 303 and the conductive shims is schematically illustrated by Figure 10. It would be understood that in reality, once the top substrate is placed on top of the conductive shims, the components between the top and bottom substrates would not be visible as they would be covered by the top substrate. The diagram of Figure 10 is provided to conceptually illustrate how the conductive tracks 301 to 303 are aligned with the conductive shims 41 to 46, 51 to 56 and 601 to 610.

With reference to Figure 10, the conductive shims 42, 45, 46, 52, 55, 56 are bonded to the conductive track 301, and thus electrically connect the emitter pads of the IGBT chips T2, T5, T6 and the anode pads of the FRD chips D2, D5, D6 to the conductive track 301. The conductive shims 604, 605 and 607 are further bonded to the conductive track 301 and thus electrically connect the conductive track 301 to Terminals 14 and 16 (i.e., the DC- terminal of Figure 2). The conductive shims 602 and 603 are also bonded to the conductive track 301, and thus electrically connect the conductive track 301 to the conductive tracks 207 and 209 of the bottom substrate, respectively. The conductive track 207 holds Terminal 7 (i.e., the auxiliary emitter terminal E2 of Figure 2). The conductive track 209 holds Terminal 9 (i.e., the auxiliary emitter terminal E4 of Figure 2). The term “auxiliary emitter terminal” refers to a control terminal of an IGBT, and differs from a power emitter terminal where power current flows through (e.g., the low side terminals described above). It is generally desirable to separate the auxiliary emitter terminal from the power emitter terminal, so as to avoid the power circuit from influencing the control circuit.

The conductive shims 41, 51 are bonded to the conductive track 303, and thus electrically connect the emitter pad of the IGBT chip T1 and the anode pad of the FRD chip D1 to the conductive track 303. The conductive shim 606 is further bonded to the conductive track 303, and thus electrically connect the conductive track 303 to the conductive track 213 of the bottom substrate (which holds Terminal 13, the AC1 terminal). The conductive shim 608 is also bonded to the conductive track 303, and thus electrically connect the conductive track 303 to the conductive track 202 of the bottom substrate. As shown in Figure 7, the conductive track 202 holds Terminal 2 (i.e., the auxiliary emitter terminal E1 of Figure 2).

The conductive shims 43, 44, 53, 54 are bonded to the conductive track 302, and thus electrically connect the emitter pads of the IGBT chips T3, T4 and the anode pads of the FRD chips D3, D4 to the conductive track 302. The conductive shims 609, 610 are further bonded to the conductive track 302, and thus electrically connect the conductive track 302 to the conductive track 212 of the bottom substrate (which holds Terminal 12, the AC2 terminal). The conductive shim 601 is also bonded to the conductive track 302, and thus electrically connect the conductive track 302 to the conductive track 204 of the bottom substrate. As shown in Figure 7, the conductive track 204 holds Terminal 4 (i.e., the auxiliary emitter terminal E3 of Figure 2). The bottom substrate and the top substrate may also be referred to as “first substrate” and “second substrate”, respectively. The conductive tracks 205 and 301 may be referred to as “first conductive track” and “second conductive track”, respectively.

Conventional power modules house either a single switch, a single half-bridge switch, two-phase half-bridge switches or three-phase half-bridge switches. The single switch and single half-bridge switch modules would readily be designed and manufactured using the conventional techniques while maintaining sufficient reliability. This is because small numbers of power semiconductor chips are involved in these modules and the footprints of these modules are small so that the bending/warpage and thermo-mechanical stress/strain developments of these modules could be at a relatively low level. It is generally critical to arrange the layouts of power semiconductor chips, internal wiring and terminals, design the packaging structures and select the assembling processes of the two-phase and three-phase half bridge switch modules with large footprints for achieving good electrical performance and thermal performance while maintaining sufficient thermo-mechanical reliability. For this reason, even though the two-phase and three-phase half-bridge switch modules house more than one half-bridge switch, each half-bridge switch owns its independent conductive tracks and power terminals.

Unlike the conventional power modules in which each half-bridge switch owns its independent conductive tracks and power terminals, the power module 100 of the present disclosure comprises two (or more) half-bridge switches 110, 120 sharing conductive tracks and power terminals. In particular, the high side power terminals 113, 123 of the high side devices 112, 122 (i.e., the bottom pads of the IGBT chips T1, T3 and T4 and the FRD chips D1, D3 and D4 as shown in Figures 6 and 7) within each of the two half-bridge switches 110, 120 are attached to the same conductive track 205 of the bottom substrate. The low side power terminals 118, 128 of the low side devices 116, 126 (i.e., the top pads of the IGBT chips T2, T5 and T6, and the FRD chips, D2, D5 and D6 as shown in Figures 6 and 7) within each of the two half-bridge switches 110, 120

are connected to the same conductive track 301 of the top substrate (through six conductive shims 42, 45, 46, 52, 55 and 56). Furthermore, the two half-bridge switches 110, 120 share the same DC positive power terminal (i.e., Terminal 15) and DC negative power terminal (i.e., collectively provided by the Terminal 14 and Terminal 16).

5 The shared conductive tracks and power terminals lead to not only reduced volume and weight of the power module 100 but also simplified connections to an external DC power supply. Specifically, by utilising the conductive tracks formed on both of the bottom and the top substrates to electrically connect the components of the half-bridge switches, the power module 100 becomes more compact and achieves a smaller 10 dimension than conventional power modules. This means that the power module 100 provides an increased power density than conventional power modules. An external DC power supply may be connected to Terminals 14 to 16 by screw connections or a bonding technology such as laser welding. With simplified connections to the external DC power supply, multiple instances of the power module 100 can be easily connected to construct 15 a multi-inverter system (e.g., the dual-inverter system shown in Figure 1). The conductive shims 41 to 46, 51 to 56 and 601 to 610 have the ability of carrying significantly higher level current than the wire bonds attached to the top surfaces of the IGBT and FRD chips as used in the conventional power modules, and thus are useful for improving the reliability of the power module 100.

20 The conductive layer 21 on the outer surface of the bottom substrate and the conductive layer 31 on the outer surface of the top substrate can be used as the two cooling surfaces to achieve double side cooling. They can be sealed on two heat sinks in direct contact with coolant or mounted on the cold plates of two heat sinks with thermal interface material (TIM) and/or bonding technology such as lead-free soldering or 25 sintering technology. Accordingly, the power module 100 achieves an improved thermal performance.

As shown in Figure 7, the power terminals of the power module 100 include two interconnected Terminals 14 and 16 (DC-), which are provided at the two sides of Terminal 15 (DC+). The arrangement of Terminals 14 to 16 achieves local anti-parallel 30 current flows. More specifically, because Terminals 14 to 16 are arranged at the same side of the power module 100 (i.e., at the top side with reference to the orientation shown in Figure 7), and Terminal 15 (DC+) is sandwiched by Terminals 14 and 16 (DC-), the power current flowing through the conductive track 205 from Terminal 15 flows in a direction substantially opposite to that of the power current flowing through the 35 conductive track 301 into Terminals 14 and 16. The opposite flowing directions of the power currents cause cancellation of magnetic fluxes generated by the power currents, thereby reducing the wiring inductances of Terminals 14 to 16. Further, providing one

extra DC negative power terminal allows the power current flowing through the conductive track 301 to branch into two paths. The current branching avoids concentration of the power current in a limited part of the conductive track 301, thereby effectively reducing the wiring inductance of Terminals 14 and 16. The reduction is more
5 than 30% in an example as compared to a scenario where only Terminal 14 is used as the DC negative power terminal.

As shown in Figure 2, the second half-bridge switch 120 contains two IGBT chips (i.e., T3 and T4 or T5 and T6) and two FRD chips (i.e., D3 and D4 or D5 and D6), which are connected in parallel in each of its high side and low side devices 122 and 126. The
10 IGBT chips connected in parallel and their gate wire bonds (i.e., 73 and 74 or 75 and 76) are arranged in such a way that the conducting loops between the gate and auxiliary emitter terminals of each IGBT chip have similar parasitic inductance and resistance values. For example, as shown in Figure 7, the wire bonds 73, 74 are arranged substantially symmetrically between the IGBT chips T3, T4, and the wire bonds 75, 76
15 are arranged substantially symmetrically between the IGBT chips T5, T6. It would be appreciated that in the event that more than two IGBT chips (or SIC MOSFET chips) are connected in parallel, the gate wire bonds may be surrounds by the chips such that each chip experiences gate control loops with similar parasitic inductance and resistance values.

20 With reference to Figure 7, it can be seen that Terminals 14 to 16 (DC+ and DC-) are placed at a first, top, side of the power module 100, and that Terminals 1 to 11 (i.e., the signal and control terminals) are placed at a second, bottom, side of the power module 100. The signal and control terminals are organized into five groups: (i) Terminal 1 (G1) and Terminal 2 (E1/C2); (ii) Terminal 3 (G3) and Terminal 4 (E3/C4); (iii) Terminal
25 5 (C1/C3); (iv) Terminal 6 (G2), Terminal 7 (E2), Terminal 8 (G4) and Terminal 9 (E4); and (v) Terminal 10 (N1) and Terminal 11 (N2). Here the symbols in the parentheses stand for the ports illustrated in Figure 2. Terminals 10 and 11 are two nodes of the NTC thermistor 130. It would be understood that sufficient physical distances should be maintained between the terminals of the different groups. These terminals with such
30 placement and organization can be connected to a drive and control printed circuit board (PCB) with relatively simple structure while still keeping sufficient insulating and creepage distances. In particular, no additional consideration of insulating and creepage distances is needed for the PCB.

Both of the AC output terminals - Terminal 12 (AC2) and Terminal 13 (AC1) - of
35 the two half-bridge switches 110, 120 are placed at a third, right, side of the power module 100. No terminals are placed at a fourth, left, side of the power module 100. The power terminals 12 to 16 can be connected to external DC source and electric motors

by screw connections or a bonding technology such as laser welding. The above-described arrangement of Terminals 1 to 16 may facilitate the sealing or mounting of double side heat sinks on the top surface (i.e., a surface of the conductive layer 31 as shown in Figure 3) and bottom surface (i.e., a surface of the conductive layer 21 as shown in Figure 4) of the power module 100. This is because the inlets and outlets of the double side heat sinks may be conveniently placed at the fourth, left, side of the power module 100.

As shown in Figures 3 to 5, the encapsulant 80 fills the gaps between the top and bottom substrates, and encapsulates the semiconductor chips T1-T6 and D1-D6, the wire bonds 71-76, the conductive shims, and the joints between Terminals 1 to 16 and the conductive tracks of the bottom substrate. In this way, the encapsulant 80 protects the internal components of the power module 100. The encapsulant 80 is made of an electrically insulating but preferably thermally conductive material. It would be understood that a majority (if not all) of the conductive layer 21 of the bottom substrate and a majority (if not all) of the conductive layer 31 of the top substrate are exposed from the encapsulant 80 in order to form a direct contact with two-side heat removal bodies (e.g., heat sinks).

The encapsulant 80 may be made of a moulding compound, rather than conventionally used silicone gel. Using a moulding compound as the encapsulant 80 is useful for improving the reliability of the power module 100.

More specifically, silicone gel is a soft material and would not be able to improve the strength of the power module when used alone. Thus, a rigid plastic housing is typically used to further enclose the silicone gel. A moulding compound can eliminate the use of the plastic housing. Hence, using the moulding compound allows the volume (in particular, the thickness) of the power module 100 to be reduced as compared to using the silicone gel, or provides better insulation with similar dimensions or volume of the power module. The moulding compound, once cured, may lead to additional compressive stresses for enhancing the joints between the chips, shims and substrates in the module, and hence reduce the formation and growth of fatigue cracks which are due to shear and/or tensile stress and strain developments. Accordingly, using a moulding compound may improve the reliability of the power module 100.

The moulding compound may comprise epoxy, other polymer based materials, or inorganic materials with high insulating strength. Preferably, a polymer-based moulding compound may contain fillers such as silica, aluminium nitride or boron nitride fillers having high thermal conductivity and low coefficient of thermal expansion (CTE) to improve the thermal conductivity and constrain the CTE of the moulding compound. The curing temperature of the moulding compound may be at least 20°C lower than the

lowest melting point of the solder alloys used to attach the semiconductor chips and bond the conductive shims and terminals.

One or both of the bottom substrate and the top substrate of the power module 100 may be chosen from direct bonded copper (DBC), directed bonded aluminium (DBA) or active brazed metal (ABM) substrates. In that case, one or each of the insulating layers 20, 30 may comprise 0.2 mm to 1 mm thick alumina, aluminium nitride or silicon nitride ceramic tiles. The conductive layers on both sides of the insulating layers may comprise 0.1 mm to 1 mm thick pure copper, pure aluminium, copper-molybdenum alloy, copper-tungsten alloy, or other pure metals or alloys with similar thermal, electrical and thermo-mechanical properties. The conductive layer on one side of the top substrate may be patterned (e.g., by dry or wet etching) to form the conductive tracks 301 to 303. The conductive layer on one side of the bottom substrate may be patterned (e.g., by dry or wet etching) to form the conductive tracks 201 to 215.

Alternatively, one or each of the bottom substrate and the top substrate may be an insulated metal substrate (IMS). In that case, one or each of the insulating layers 20, 30 may comprise 0.05 mm to 0.25 mm thick resin compound, or other organic-based materials with high insulating strength and high thermal conductivity. The conductive layers on both sides of the insulating layers are in general made of pure copper, pure aluminium, copper alloy, aluminium alloy, or other pure metals or alloys with similar thermal, electrical and thermo-mechanical properties, and may have the same or different thicknesses in the range of 0.05 mm to several millimetres.

Of the above-described DBC, DBA, ABM substrates and IMSs, silicon nitride based ABM substrates may be used for high performance and high reliability applications. This is because silicon nitride based ABM substrates have high mechanical strength and can withstand high mechanical stresses for sealing or mounting the double side heat sinks and have good thermo-mechanical reliability.

The conductive shims 41 to 46, 51 to 56 and 601 to 610 may be made of pure metal (such as pure copper and pure aluminium), alloy (such as copper-molybdenum alloy and copper-tungsten alloy), metal-matrix composite (such as copper-graphite composite and aluminium-carbon fibre composite), or other materials with high thermal conductivity and high electrical conductivity. Preferably, the conductive shims are made of materials with CTEs matched or close to those of the substrates and/or semiconductor chips.

The semiconductor chips, T1 to T6 and D1 to D6, and the NTC thermistor may be attached to the conductive tracks of the bottom substrate with lead-free solder alloys (such as tin-silver, tin-copper, tin-silver-copper, tin-antimony, bismuth-silver solder alloys). Alternatively, they may be attached to the bottom substrate with sintering

technologies (such as silver sintering and copper sintering technologies). Similarly, the conductive shims 41 to 46, 51 to 56 and 601 to 610 may be bonded between the top surfaces of the semiconductor chips and the conductive tracks of the top substrate or between the conductive tracks of the bottom substrate and the conductive tracks of the top substrate with lead-free solder alloys or the sintering technologies. It would be understood that the conductive shims 41 to 46, 51 to 56 and 601 to 610 may be bonded with the same solder alloy or several solder alloys with different melting points, or combined sintering technology and solder alloys.

The power terminals 12 to 16 and the signal/control terminals 1 to 11 may be made of materials similar to those of the conductive shims with high thermal conductivity and high electrical conductivity. They may be bonded on the corresponding conductive tracks of bottom substrate with solder alloys or sintering technologies in a way similar to attaching the semiconductor chips and bonding the conductive shims. Alternatively, they may be bonded on the conductive tracks of bottom substrate with ultrasonic welding technology. Preferably, the terminals 1 to 16 may be made of metals or alloys such as pure copper, pure aluminium, copper alloy or aluminium alloy with sufficient strength and good ductility.

Using lead-free solder joints to attach the semiconductor chips and to bond the conductive shims and the terminals is preferred for low cost applications where the junction temperatures of the semiconductor chips are in general lower than 150 °C. Using sintered silver or copper joints to attach the semiconductor chips and to bond the conductive shims and the terminals is preferred for high temperature and high reliability applications where the junction temperatures of the semiconductor chips may be higher than 150 °C.

As described above, the power module 100 has integrated two half-bridge switches 110, 120 which share conductive tracks of the substrates and also share power terminals 14 to 16. In this way, the volume and weight of the power module 100 can further be reduced, and better layout of the power terminals can be realized for achieving low wiring inductance and resistance. Further, conductive shims 41-46 and 51-56 are used to replace conventional wire bonds for topside interconnection of semiconductor chips and are able to carry higher currents. The moulding compound not only ensures sufficient insulating and creepage distances between the related conductive tracks and between the terminals, but also adds mechanical support and hence improves reliability of the power module 100. All these factors contribute to the power module 100 with further improved power density, electrical/thermal performance and thermo-mechanical reliability, and benefit the construction of smaller and lighter dual-inverter systems for EV and HEV electric drive applications.

Figures 11 to 13 show the physical structure of a power semiconductor apparatus 1000 which comprises a stack of power semiconductor modules and coolers. Figure 17 shows an exploded view of the power semiconductor apparatus 1000. The power semiconductor apparatus 1000 is a main component of the electric control system 800 shown in Figure 1.

The power semiconductor apparatus 1000 comprises four instances (labelled as M1 to M4) of the same power semiconductor module 100. The power modules M1 to M4 are inserted between five coolers (labelled as C1 to C5) to form a stacked structure (referred to as "stack" for brevity). A Z direction in Figures 11 to 17 corresponds to a stacking direction along which the power modules M1 to M4 and the coolers C1 to C5 are stacked. The power modules M1 to M4 and the coolers C1 to C5 are alternately stacked one by one. Two coolers are respectively in contact with both sides of each power module. Each of the coolers C2 to C4 has both faces in contact with power modules. Each of the coolers C1 and C5 which are located at two ends of the stack only has one face in contact with a corresponding power module.

Either the power module M1 or M4 may be used for constructing the VVC 820, with the remaining three power modules being used for constructing the generator inverter 840 and the motor inverter 860. It would be understood that the power module for constructing the VVC 820 may have a different topology and/or a different physical structure than the other three power modules for the inverters 840, 860. However, it is preferable that the power module for the VVC 820 has the same outer dimension as the other three power modules, and thus can still be inserted into the space between adjacent coolers.

Because each of the power modules has integrated two half-bridge switches as described above, only four such power modules M1 to M4 (inserted between five coolers C1 to C5) would be sufficient to form the electric control system 800 shown in Figure 1. This is in contrast to prior techniques which would require eight or sixteen power modules (each of which includes either a single half-bridge switch or a single power transistor) inserted between nine or seventeen coolers in order to construct the same electric control system 800. Thus, for an electric control system with two or more power converters, the power semiconductor apparatus 1000 includes reduced numbers of power semiconductor modules and coolers and hence has a much reduced volume and weight as compared to prior techniques.

Each of the coolers C1 to C5 is integrated with pin fins, coolant channels, two-side cold plates, and inlet/outlet connectors. The coolers C2 to C4 share the same physical structure which is shown in Figures 14 to 16. Figures 14 and 15 are a top perspective view and a bottom perspective view of one such cooler, respectively, while

Figure 16 is a bottom perspective view of the cooler but with the bottom cold plate being invisible. Each of the coolers C2 to C4 comprises a top cold plate 901 and a bottom cold plate 902. The top cold plate 901 is integrated with a partition 903 and pin fins 904s on its bottom side (Figure 16), a connection region 91 on its top side (Figure 14), and two through holes 931 and 932 (Figure 14) extending through two corners of the top cold plate 901. The pin fins 904s are cooling-enhanced features, and the gaps between the pin fins 904s are cooling channels. It would be understood that the cooling-enhanced features may take a different form. In the connection region 91, there are three through holes 911, 912 and 933, and two cut-outs (or recesses) 921 and 922 which surround the through holes 911, 912, respectively. The bottom cold plate 902 is relatively simple and has three through holes 941, 942 and 943. The through holes 911 and 912 of the top cold plate 901 are co-axial with the through holes 941 and 942 of the bottom cold plate 902, respectively, and extend along the stacking direction. The through holes 911, 912, 941, 942 are in fluid communication with the cooling channels. In use, coolant can flow through the through holes 911, 912, 941, 942 and the cooling channels between the pin fins 904s. The two cut-outs 921 and 922 are made to hold sealing rings SR1, SR2 (Figure 17) so as to provide sealing between two adjacent coolers.

In the bottom cooler C1, the two through holes 941 and 942 are omitted from its bottom cold plate 902. In the top cooler C5, there are two connecting tubes CN1 and CN2 which extend from the connection region 91 of its top cold plate 901. The coolers C1 and C5 are identical to the coolers C2 to C4 in all other aspects. The connecting tubes CN1 and CN2 may be integrally formed with the top cold plate 901 of the cooler C5, or may be separately supplied and bonded to the top cold plate 901. In use, the two connecting tubes CN1 and CN2 are connected to a coolant supply and act as the coolant inlet and the coolant outlet for all of the coolers C1 to C5. Accordingly, the through holes 912 and 911 may be respectively regarded as the coolant inlet and coolant outlet of each cooler.

The top cold plate 901 and the bottom cold plate 902 of each cooler are preferably made of pure aluminium or aluminium alloy, so as to have light weight and low costs (due to low costs of both the raw materials and the manufacturing processes). Alternatively, they can be made of other pure metal (such as pure copper), alloy (such as copper-molybdenum alloy and copper-tungsten alloy), metal-matrix composite (such as copper-graphite composite, aluminium-silicon carbide composite and aluminium-carbon fibre composite), or other materials with high thermal conductivity. The top cold plate 901 and the bottom cold plate 902 of each cooler may be manufactured by using casting, machining or other metalworking processes, and are bonded together to form an integrated cooler by using, for example, welding, brazing or other bonding

technologies. Because only two small sealing rings SR1, SR2 (Figure 17) are used to provide sealing between the adjacent coolers, it is relatively easy to secure the sealing of the coolers within the power semiconductor apparatus 1000.

As described above, in the power module 100 (which is identical to each of the power modules M1 to M4 in an example), the power semiconductor devices T1 to T6 and D1 to D6 are bonded between a top substrate and a bottom substrate, and each of the top and the bottom substrates comprises an electrically insulating and thermally conductive layer 20/30 with a patterned conductive layer which provides the conductive tracks for connecting the power semiconductor devices. Thus, the insulation between the power semiconductor devices T1 to T6 and D1 to D6 and adjacent coolers C1 to C5 is achieved by the electrically insulating and thermally conductive layer 20/30. In practice, the top and bottom substrates may be metallized ceramic substrates which provide sufficient insulation and high thermal conductivity. In each of the coolers C1 to C5, the top and bottom cold plates 901, 902 and internal cooling-enhanced features 904s are integrated or welded together without the need of additional sealing. With these features, heat paths from the power semiconductor devices to the coolant within the power semiconductor apparatus 1000 has a reduced number of thermal interfaces and accordingly a reduced thermal resistance. This is in contrast to the prior technologies where the insulation between power semiconductor devices and a cooler is achieved by encapsulation resin and/or insulating plates placed between the resin packages and the adjacent coolers.

As described above in relation to Figures 6 and 7, the power and signal/control terminals 1 to 16 of the power module 100 extend from three sides of the power module 100. The three-side terminal arrangement has been maintained in the power semiconductor apparatus 1000 as shown in Figures 11 to 13. In particular, the DC power terminals of the power modules M1 to M4 are arranged at the same side (i.e., along the back XZ plane in Figure 11) of the power semiconductor apparatus 1000, thereby simplifying external connections to the battery. The AC output terminals of the power modules M1 to M4 are arranged at another side (i.e., along the right YZ plane in Figure 11) of the power semiconductor apparatus 1000, thereby simplifying external connections to the generator and traction motors. The signal/control terminals of the power modules M1 to M4 are arranged at a further side (i.e., along the front XZ plane in Figure 11) of the power semiconductor apparatus 1000. This significantly simplifies external connections to drive and control PCBs. Consequently, the three-side terminal arrangement reduces the space required to connect the terminals of the power modules M1 to M4 to the battery, power generation/delivery connectors, passive components, control/drive PCBs and the electric motors, and also reduces the parasitic inductance

and resistance values of the external connections. This is in contrast to the prior technologies where all of the power and signal/control terminals extend from a single side, or the DC power terminals and AC output terminals extend from a single side.

A fourth side (i.e., along the left YZ plane in Figure 11) of the power semiconductor apparatus 1000 is left without any terminals of the power modules M1 to M4. This arrangement facilitates the installation of the coolers C1 to C5, and allows the coolant inlets and outlets of the coolers to be arranged at the fourth side of the power modules M1 to M4.

As illustrated in Figure 17, a thermal interface material (TIM) layer TIM1 is placed between the bottom substrate of the power module M4 and an underneath neighbouring cooler C4. Another TIM layer TIM2 is placed between the top substrate of the power module M4 and an above neighbouring cooler C5. It would be understood that a TIM layer is provided at each interface of the power modules and the coolers. The TIM layers may be 0.2 to 1 mm in thickness and made of a compliant thermal interface material (e.g. graphite sheets or films) with high thermal conductivity and thermal stability.

Figure 17 further shows that two sealing rings SR1 and SR2 are placed into the cut-outs 921 and 922 of the cooler C4. The sealing rings SR1 and SR2 are for sealing the connections of the two through holes 911, 912 in the top cold plate 901 of the cooler C4 and another two through holes 941 and 942 in the bottom cold plate 902 of the neighbouring above cooler C5. The sealing is secured when the stack is pressurised by structural plates SP1, SP2 (described below) in the stacking direction. It would be understood that the sealing rings SR1 and SR2 are provided between each pair of adjacent coolers.

With further reference to Figures 11 and 17, the power semiconductor apparatus 1000 comprises a first structural plate SP1 and a second structural plate SP2, which are arranged on opposite sides of the stack in the stacking direction Z. More specifically, the first structural plate SP1 is placed under the bottom cooler C1, and a first set of compliant pads CP1 to CP8 are inserted between the first structural plate SP1 and the bottom cooler C1. The second structural plate SP2 is placed over the top cooler C5, and a second set of compliant pads CP1 to CP8 are inserted between the second structural plate SP1 and the top cooler C5. When viewed along the stacking direction Z, each set of the compliant pads have a combined area that is much smaller than (e.g., less than a third of) the area of the structural plate SP1 or SP2, and is also much smaller than (e.g., less than a third of) the area of each cooler.

The structural plates SP1, SP2 may be deemed as part of a supporting frame of the stack. Once the power semiconductor apparatus 1000 is assembled, the structural plates SP1, SP2 pressurise the stack in the stacking direction. It would be understood

that the structural plates SP1, SP2 would have sufficient mechanical strength in order to pressurise the stack without experiencing noticeable deformation in itself. In an example, the structural plates SP1 and SP2 are made of structural steel or other materials with similar mechanical properties and thermal stability, and may be 1 to 3 mm in thickness. 5 While the surfaces of the structural plates SP1 and SP2 are shown as flat in the figures, it would be understood that reinforcing features (e.g., reinforcing ribs, protrusions, and contours) may be incorporated into the surface(s) of the plates.

The power semiconductor apparatus 1000 further comprises a pressure controller for controlling the pressure applied by the structural plates SP1, SP2 to the 10 stack. With reference to Figures 11, 13 and 17, the pressure controller includes first ends N1, N2, N3, N4 which are coupled to the first structural plate SP1, and second ends S1, S2, S3, S4 which are coupled to the second structural plate SP2. In the example illustrated by Figures 11, 13 and 17, the first ends are in contact with a bottom surface of the first structural plate SP1, and the second ends are in contact with a top surface of 15 the second structural plate SP2. However, it would be appreciated that the first ends and the second ends may be coupled to the structural plates in a different manner. For example, the second ends S1-S4 may be integrally formed with the second structural plate SP2.

The pressure controller allows the distance between the first ends N1-N4 and the 20 second ends S1-S4 to be adjusted. The distance controls the amount of pressure applied by the structural plates SP1, SP2 to the stack in the stacking direction Z. In an exemplary embodiment as illustrated by Figures 11, 13 and 17, the pressure controller further comprises linkage members L1, L2, L3, L4 which extend along the stacking direction Z between the first ends N1-N4 and the second ends S1-S4, respectively; the second ends 25 S1-S4 are integrally formed or bonded to the linkage members L1-L4, respectively; and the first ends N1-N4 are rotatably coupled to respective ones of the linkage members L1-L4. For example, the linkage members L1-L4 may comprise helical threads at their surfaces while the first ends N1-N4 may comprise complementary helical threads engageable with those of the linkage members. By rotating the first ends N1-N4 around 30 the linkage members L1-L4, the distance between the first ends N1-N4 and the second ends S1-S4 is adjusted accordingly. In this particular example, a combination of the second ends S1-S4 and the linkage member L1-L4 resemble bolts, while the first ends N1-N4 resemble nuts. It would be appreciated that the pressure controller may incorporate a different mechanism for controlling the pressure applied by the structural 35 plates SP1, SP2. For example, the linkage member may surround, but not extending through, the coolers C1-C5. In general, the first ends N1-N4 are expected to have a much smaller area (e.g., less than one fifth) than the first structural plate SP1. The same

relationship applies to the second ends S1-S4 and the second structural plate SP2. In other words, it is the structural plates SP1, SP2 that apply the pressure to the stack and the first/second ends merely regulate the pressure applied. The structural plates SP1, SP2 and the pressure controller may collectively be regarded as a supporting frame of
5 the stack. The pressure controller effectively binds the structural plates SP1, SP2 together.

With the pressure controller, the pressure between the power modules M1-M4 and their neighbouring coolers C1-C5 within the stack is established by coupling the first ends N1-N4 to the linkage member L1-L4, and is controlled to reach a desired level by
10 adjusting a distance between the first ends N1-N4 and the second ends S1-S4. The pressure controller eliminates the need of the special machines/equipment required by the prior techniques to apply the pressure to the stack, and also allows the pressure applied to the stack to be easily adjusted after the power semiconductor apparatus 1000 has been assembled.

15 The linkage members L1 and L2 extend through the through holes 931, 932 of the coolers C1-C5, and thus are useful for aligning the coolers C1-C5 in the stack and preventing the coolers from rotating.

The linkage members L3 and L4 do not penetrate through any of the coolers C1-C5. Two tubes TB1 and TB2 are provided between the structural plates SP1, SP2. The
20 linkage members L3 and L4 pass the central bores of the tubes TB2, TB1, respectively. The tubes TB1, TB2 may be made of an electrically insulating material. They provide additional support to the structural plates SP1, SP2, and also insulate the linkage members L3, L4, thus reducing the risks of unintentional electrical short between the linkage members L3, L4 and the nearby terminals (i.e., the AC output terminals and the
25 signal/control terminals) of the power modules M1-M4.

The power semiconductor apparatus 1000 further comprises a binding structure for binding the coolers C1 to C5 together. The binding structure comprises a first end N5, a second end S5, and a linkage member L5 extending between the ends N5, S5. The second end S5 is integrally formed or bonded to the linkage member L5. The first end
30 N5 is rotatably coupled to the linkage member L5. For example, the linkage member L5 may comprise helical threads at its outer surface while the first end N5 may comprise complementary helical threads engageable with those of the linkage member L5. In the particular example illustrated by the figures, the second end S5 and the linkage member L5 form a bolt while the first end N5 form a nut. The ends N5, S5 are in contact with the
35 top and bottom coolers C5, C1, respectively, but do not contact the structural plates SP1, SP2. The linkage member L5 passes the through holes 933, 943 of each of the coolers C1-C5. By rotating the first end N5 with respect to the linkage member L5, additional

pressure is provided by the ends N5, S5 across the coolers C1 to C5, and is useful for enhancing the sealing of the sealing rings SR1, SR2 between adjacent coolers.

Within the two sets of compliant pads CP1 to CP8, the compliant pads CP1 to CP6 are designed with specific sizes and layout corresponding to those of the IGBT chips T1 to T6, the FRD chips D1 to D6, and the conductive shims 41 to 46 and 51 to 56 in each of the four power modules M1 to M4.

Figure 18 is the top plan view of the power semiconductor apparatus 1000 where the second ends S1 to S4, the first end N5, the second structural plate SP2, a majority of the top cooler C5 (except around the connection region 91), the TIM layer TIM2, the moulding compound 80 and the top substrate of the power module M4 are invisible. In this way, Figure 18 shows the sizes and layout of the compliant pads CP1 to CP6 in comparison with the IGBT chips T1 to T6, the FRD chips D1 to D6, and the conductive shims, 41 to 46 and 51 to 56. It can be seen that, when viewed along the stacking direction Z, the compliant pads CP1 to CP6 overlap the IGBT chips T1 to T6, the FRD chips D1 to D6 and also overlap the conductive shims, 41 to 46 and 51 to 56 bonded to the topsides of the chips. Due to the thickness of the compliant pads CP1-CP6, when the structural plates SP1, SP2 apply pressure to the stack, the compliant pads CP1-CP6 generate additional compressive stresses in the stacking direction on the joints between the chips, the conductive shims and the conductive tracks of the top and bottom substrates of the power modules M1-M4. The additional compressive stresses are useful for improving the reliability of the joints. Further, the additional compressive stresses are also useful for improving the thermal contacts between the TIM layers (TIM1, TIM2) on the one hand, and the neighbouring coolers and power modules, on the other hand. In other words, the compliant pads CP1 to CP6 ensure that the pressure applied by the structural plates SP1, SP2 is distributed to achieve intimate contact between the power modules M1 to M4, TIM layers TIM1, TIM2 and the coolers C1 to C5.

With further reference to Figures 17 and 18, it can be seen that the compliant pads CP7, CP8 are ring-shaped, and surround the linkage members L1 and L2 (and the through holes 931, 932) above the top cooler C5 and below the bottom cooler C1. The compliant pads CP7, CP8 generate additional compressive stresses around the through holes 931, 932, and thus are useful for achieving sealed connections between the coolers C1 to C5.

The two set of compliant pads CP1 to CP8 may be attached to inner surfaces of the structural plates SP1, SP2, respectively, and may be made of a mechanically highly compliant and thermally stable material (e.g. silicone rubber or other materials with similar mechanical properties and thermal stability). The thickness of the compliant pads CP1 to CP8 may be 0.2 to 2 mm.

Alternatively, the compliant pads CP1 to CP8 may obtain mechanical compliance due to its structure, and may take the form of springs (e.g., disk springs or Belleville washers). It would be understood that the compliant pads (or compliant components) CP1 to CP8 may take any other suitable forms as long as they are able to achieve force and motion transmission through elastic body deformation.

It would be understood that the power semiconductor apparatus 1000 may be modified such that less or more power modules and coolers are stacked together to construct any suitable numbers of power converters. Further, the number of coolers may be identical to the number of power modules. For example, the top cooler C5 may be omitted, and two additional spacers (not shown) which the linkage members L1 and L2 extend through may be placed on top of the cooler C4 to compensate for the height difference between the power module M4 and the cooler C4. In that case, the compliant components CP1 to CP8 may be placed on top of the conductive layer 31 of the power module M4 and the two additional spacers.

In the power module 100, each of the top and bottom substrates has electrically conductive layers provided at both sides of the substrate. It would be appreciated that one or more of the top and bottom substrates may be modified such that only one side of the substrate is provided with an electrically conductive layer. It would also be understood that the conductive shims may be modified or replaced in any suitable manner, as long as they still allow electrical connections to be made between the top and bottom substrates or between the semiconductor chips and one substrate.

Further, it would be appreciated that rather than being a single substrate, the top/bottom substrate may be split into two or more smaller substrates. In that case, the dimension of the modified power module may be slightly larger than that of the power module 100, and the interconnection between the different substrates may be added and/or modified. For example, the top substrate may be replaced by three smaller substrates which support the conductive tracks 301-303, respectively. By splitting one substrate into two or more smaller substrates, the smaller substrates are allowed to experience different degrees of deformations without causing substantial thermal stress to the power module. Therefore, the deformation of the power module as a whole tends to be more elastic and less plastic. In this way, the thermo-mechanical reliability of the power module is improved.

In the power module 100, the collector terminals of the IGBT chips T1 to T6 and the cathode terminals of the FRD chips D1 to D6 are directly attached to the conductive tracks of the bottom substrate, and the conductive shims 41-46 and 51-56 are then used to connect the emitter/anode terminals of the chips to the conductive tracks 301-303 of the top substrate. It would of course be understood that the power module 100 may be

modified such that the emitter/anode terminals of at least some of the chips are directly attached to the conductive tracks 301-303 of the top substrate, while conductive shims are used to connect the collector/cathode terminals of the chips to the bottom substrate. Further, before the top and bottom substrates are bonded to one another, some of the chips may be bonded to the bottom substrate and other chips may be bonded to the top substrates.

It would further be understood that Figures 3 to 10 merely provide one example of the physical structure of the power module 100. The shapes and layout of the terminals 1 to 16 may be modified suitably. For example, some or all of the power terminals and signal/control terminals may be bonded to the top substrate. Further, the arrangement of the power terminals 14-16 as shown in Figs. 3 to 7 may be modified such that two DC positive power terminals are placed at opposite sides of one DC negative power terminal, or that two or more DC positive power terminals and two or more DC negative power terminals are arranged in an alternating matter.

It would also be appreciated that the circuit topology of the first and/or second half-bridge switches 110, 120 may be modified to differ from that shown in Figure 2. For example, the first and second half-bridge switches 110, 120 may share the same circuit topology. Further, the first and second half-bridge switches 110, 120 may switch on at the same time interval or at different time intervals. Depending upon the specific circuit topology of the power module, the layout of the semiconductor chips and the shapes of the conductive tracks on each substrate may be modified suitably.

While the power module 100 has integrated two half-bridge switches, it would be appreciated that the power module may integrate more than two half-bridge switches.

While the power module 100 includes an NTC thermistor 130 as a temperature sensor, it would be understood that the NTC thermistor 130 may be replaced by other types of temperature sensors, or may be omitted completely.

It would be appreciated that the power modules M1 to M4 used in the power semiconductor apparatus 1000 may be different from the power module 100. For example, one or more of the power modules M1 to M4 may comprise a single half-bridge switch or a single power semiconductor chip, or may be replaced by resin molded and insulated power modules. Further, the power modules M1 to M4 may not necessarily adopt the three-side terminal arrangement. The use of the structural plates SP1, SP2, the pressure controller and the compliant components CP1 to CP8 are independent of the particular configuration of the power modules M1 to M4.

It would further be understood that the coolers C1 to C5 used in the power semiconductor apparatus 1000 may be different from those shown in the figures. For example, one or more of the coolers C1 to C5 may comprise a body made of resin, a

pair of metal plates attaching cooling-enhanced features and a pair of gaskets which seal the metal plates to the body under pressure. Further, the arrangements of the coolant inlet/outlet in each cooler and the connections between the coolers in the stacked power semiconductor modules may be modified in any suitable manner.

5 Figure 19 schematically illustrates processing steps of a method for operating a power semiconductor apparatus (e.g., the power semiconductor apparatus 1000).

At step A1, a stack of power semiconductor modules (e.g., M1 to M4) and coolers (e.g., C1 to C5) are pressurised along a stacking direction (e.g., the Z axis) with first and second structural plates (e.g., the structural plates SP1, SP2) arranged on opposite sides 10 of the stack. Each of the power semiconductor modules comprises at least one semiconductor chip and is thermally coupled to at least one of the coolers.

At step A2, a pressure applied by the first and second structural plates to the stack in the stacking direction is adjusted, by adjusting a distance between first and second ends (e.g., first ends N1 to N4 and second ends S1 to S4) of a pressure controller. 15 The first and second ends are coupled to the first and second structural plates respectively.

Figure 20 schematically illustrates processing steps of a method for assembling a power semiconductor apparatus (e.g., the power semiconductor apparatus 1000).

At step B1, a plurality of power semiconductor modules (e.g., M1 to M4) and a 20 plurality of coolers (e.g., C1 to C5) are stacked along a stacking direction (e.g., the Z axis). Each of the power semiconductor modules comprises at least one semiconductor chip and is thermally coupled to at least one of the coolers.

At step B2, first and second structural plates (e.g., the structural plates SP1, SP2) are arranged on opposite sides of the stacked coolers and power semiconductor 25 modules in the stacking direction.

At step B3, a plurality of compliant components (e.g., the compliant components CP1 to CP8) are arranged between at least one of the first and second structural plates and the stacked coolers and power semiconductor modules.

At step B4, a pressure applied by the first and second structural plates to the 30 stacked coolers and power semiconductor modules in the stacking direction is controlled, by adjusting a distance between first and second ends (e.g., first ends N1 to N4 and second ends S1 to S4) of a pressure controller. The first and second ends are coupled to the first and second structural plates respectively.

The following optional features apply to each of the methods described above:

35 Adjusting the distance between the first and second ends may comprise rotating at least one of the first and second ends around a linkage member (e.g., the linkage members L1 to L4) which extend between the first and second ends.

The second end and the linkage member may form a bolt, and the first end may form a nut.

The linkage member may extend through at least some of the plurality of coolers.

The first and/or second ends of the pressure controller may have a smaller area than the first and/or second structural plates, respectively.

The terms “having”, “containing”, “including”, “comprising” and the like are open and the terms indicate the presence of stated structures, elements or features but not preclude the presence of additional elements or features. The articles “a”, “an” and “the” are intended to include the plural as well as the singular, unless the context clearly indicates otherwise.

The skilled person will understand that in the preceding description and appended claims, positional terms such as ‘top’, ‘bottom’, ‘left’, ‘right’ etc. are made with reference to conceptual illustrations of a power module or a power semiconductor apparatus, such as those shown in the appended drawings. These terms are used for ease of reference but are not intended to be of limiting nature. These terms are therefore to be understood as referring to a power module or a power semiconductor apparatus when in an orientation as shown in the accompanying drawings.

Although the disclosure has been described in terms of preferred embodiments as set forth above, it should be understood that these embodiments are illustrative only and that the claims are not limited to those embodiments. Those skilled in the art will be able to make modifications and alternatives in view of the disclosure which are contemplated as falling within the scope of the appended claims. Each feature disclosed or illustrated in the present specification may be incorporated in the disclosure, whether alone or in any appropriate combination with any other feature disclosed or illustrated herein.

CLAIMS:

1. A power semiconductor apparatus, comprising:

a plurality of power semiconductor modules, each of which comprises at least one semiconductor chip;

a plurality of coolers stacked with the power semiconductor modules along a stacking direction, wherein each of the power semiconductor modules is thermally coupled to at least one of the coolers;

first and second structural plates arranged on opposite sides of the stacked coolers and power semiconductor modules in the stacking direction, wherein the first and second structural plates are configured to pressurise the stacked coolers and power semiconductor modules in the stacking direction;

a plurality of compliant components arranged between at least one of the first and second structural plates and the stacked coolers and power semiconductor modules; and

a pressure controller comprising first and second ends coupled to the first and second structural plates respectively, wherein a distance between the first and second ends is adjustable so as to control a pressure applied by the structural plates to the stacked coolers and power semiconductor modules in the stacking direction, wherein the pressure controller comprises a linkage member extending between the first and second ends, and the linkage member extends through at least some of the plurality of coolers.

2. A power semiconductor apparatus according to claim 1, wherein the first end is rotatably coupled to the linkage member and a rotation of the first end with respect to the linkage member is configured to adjust the distance between the first and second ends.

3. A power semiconductor apparatus according to claim 1 or 2, wherein the linkage member extends along the stacking direction.

4. A power semiconductor apparatus according to any preceding claim, wherein the second end and the linkage member form a bolt, and the first end forms a nut.

5. A power semiconductor apparatus according to any preceding claim, further comprising a tube arranged between the first and second structural plates, wherein the tube surrounds at least a part of the linkage member.

6. A power semiconductor apparatus according to any preceding claim, further comprising a plurality of the pressure controllers each arranged at a respective corner of the first and second structural plates.

5 7. A power semiconductor apparatus according to any preceding claim, wherein the first and/or second ends of the pressure controller have a smaller area than the first and/or second structural plates, respectively.

8. A power semiconductor apparatus according to any preceding claim, wherein the
10 plurality of compliant components comprises a set of compliant component(s) which overlap the at least one semiconductor chip.

9. A power semiconductor apparatus according to any preceding claim, wherein the plurality of compliant components comprises a set of compliant component(s) which at
15 least partially surround the linkage member.

10. A power semiconductor apparatus according to claim 8 or 9, wherein the compliant components are securely attached to an inner surface of the first and/or second structural plates which faces the stacked coolers and power semiconductor
20 modules.

11. A power semiconductor apparatus according to any preceding claim, wherein at least one of the coolers comprises:

a main body defined by a first cold plate and a second cold plate securely bonded
25 to one another; and

a coolant inlet and a coolant outlet, wherein the main body comprises a flow channel of coolant therein between the coolant inlet and the coolant outlet.

12. A power semiconductor apparatus according to claim 11, wherein at least one of
30 the coolers further comprises:

first and second sealing rings surrounding the coolant inlet and coolant outlet, respectively, wherein the first and second sealing rings provide a seal between the at least one of the coolers and its neighbouring cooler around the coolant inlet and the coolant outlet, and the seal is secured by the pressure applied by the structural plates.

35

13. A power semiconductor apparatus according to claim 12, wherein:

the first cold plate comprises a connection region, with the coolant inlet and outlet extending through the connection region and the second cold plate;

the connection region protrudes over the remaining of the first cold plate; and

the connection region is configured to contact a second cold plate of the neighbouring cooler via the sealing rings under the pressure applied by the structural plates.

14. A power semiconductor apparatus according to claim 13, wherein the connection region comprises recesses around the coolant inlet and outlet to hold the sealing rings.

15. A power semiconductor apparatus according to any preceding claim, further comprising thermal interface material arranged between at least one of the power semiconductor modules and its neighbouring cooler(s).

16. A power semiconductor apparatus according to any preceding claim as dependent from claim 11, wherein each of the plurality of power semiconductor modules comprises DC power terminals, AC output terminal(s) and control terminals, wherein: the DC power terminals are arranged at a first side of the respective power semiconductor module; the AC output terminal(s) are arranged at a second side of the respective power semiconductor module; the control terminals are arranged at a third side of the respective power semiconductor module; and no terminals are arranged at a fourth side of the respective power semiconductor module; and wherein the coolant input and the coolant outlet are arranged at the fourth side of the respective power semiconductor module.

17. A power semiconductor apparatus according to any preceding claim, wherein at least one of the power semiconductor modules comprises a first half-bridge switch and a second half-bridge switch.

18. A power semiconductor apparatus according to any preceding claim, wherein at least three of the power semiconductor modules each comprise a first half-bridge switch and a second half-bridge switch, and wherein: the first half-bridge switches of the at least three power semiconductor modules collectively form a generator inverter for driving a first electric motor; and the second half-bridge switches of the at least three power semiconductor modules collectively form a motor inverter for driving a second electric motor.

19. An electric vehicle comprising a power semiconductor apparatus according to any preceding claim.

20. A hybrid electric vehicle comprising a power semiconductor apparatus according to any of claims 1 to 18.

21. A method of assembling a power semiconductor apparatus, the method comprising:

stacking a plurality of power semiconductor modules and a plurality of coolers along a stacking direction, and wherein each of the power semiconductor modules comprises at least one semiconductor chip and is thermally coupled to at least one of the coolers;

arranging first and second structural plates on opposite sides of the stacked coolers and power semiconductor modules in the stacking direction;

arranging a plurality of compliant components between at least one of the first and second structural plates and the stacked coolers and power semiconductor modules; and

controlling a pressure applied by the first and second structural plates to the stacked coolers and power semiconductor modules in the stacking direction, by adjusting a distance between first and second ends of a pressure controller, wherein the first and second ends are coupled to the first and second structural plates respectively, wherein the pressure controller comprises a linkage member extending between the first and second ends, and the linkage member extends through at least some of the plurality of coolers.

22. A method of assembling a power semiconductor apparatus according to claim 21, wherein adjusting the distance between the first and second ends comprises rotating at least one of the first and second ends around the linkage member.

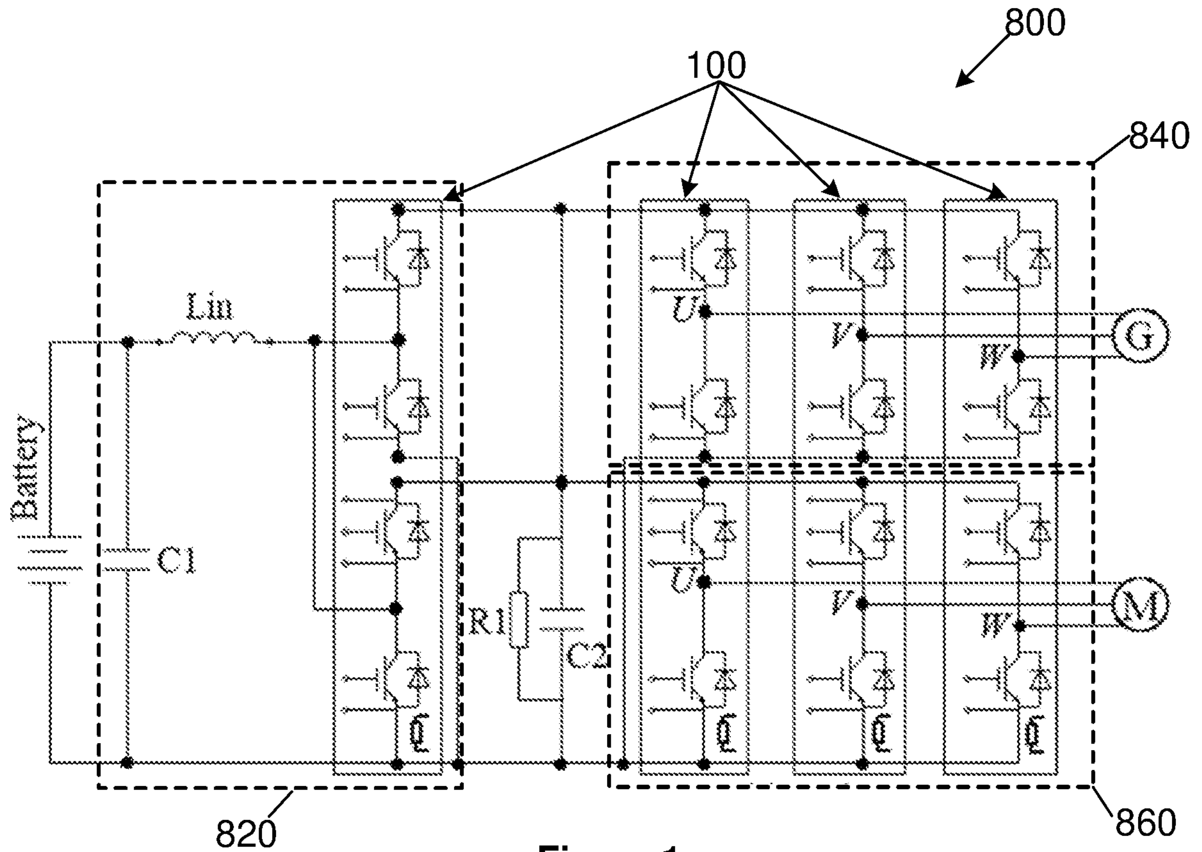

Figure 1

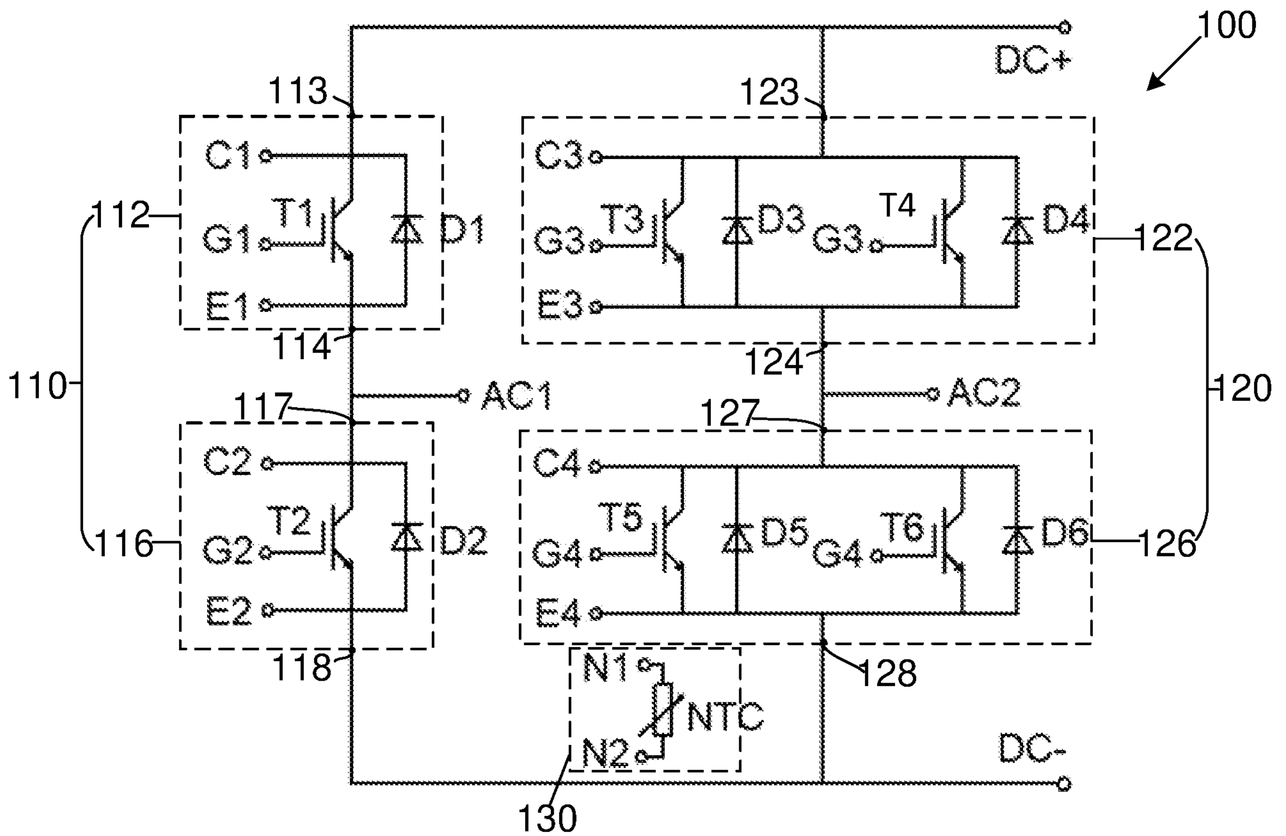

Figure 2

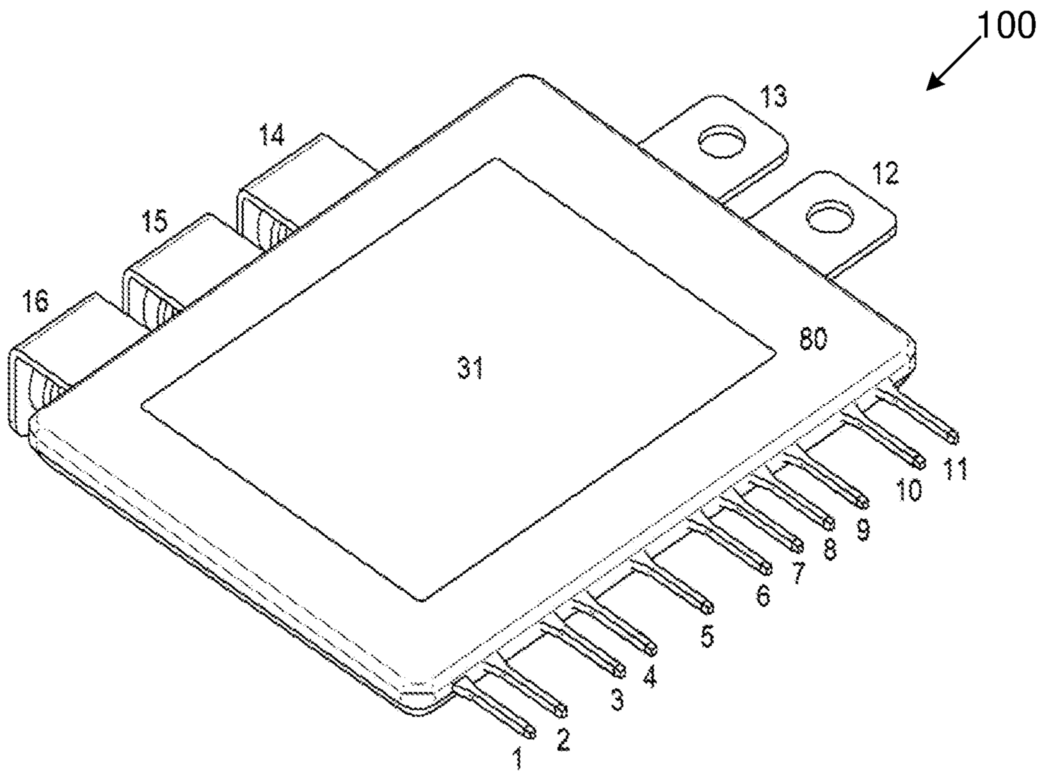

Figure 3

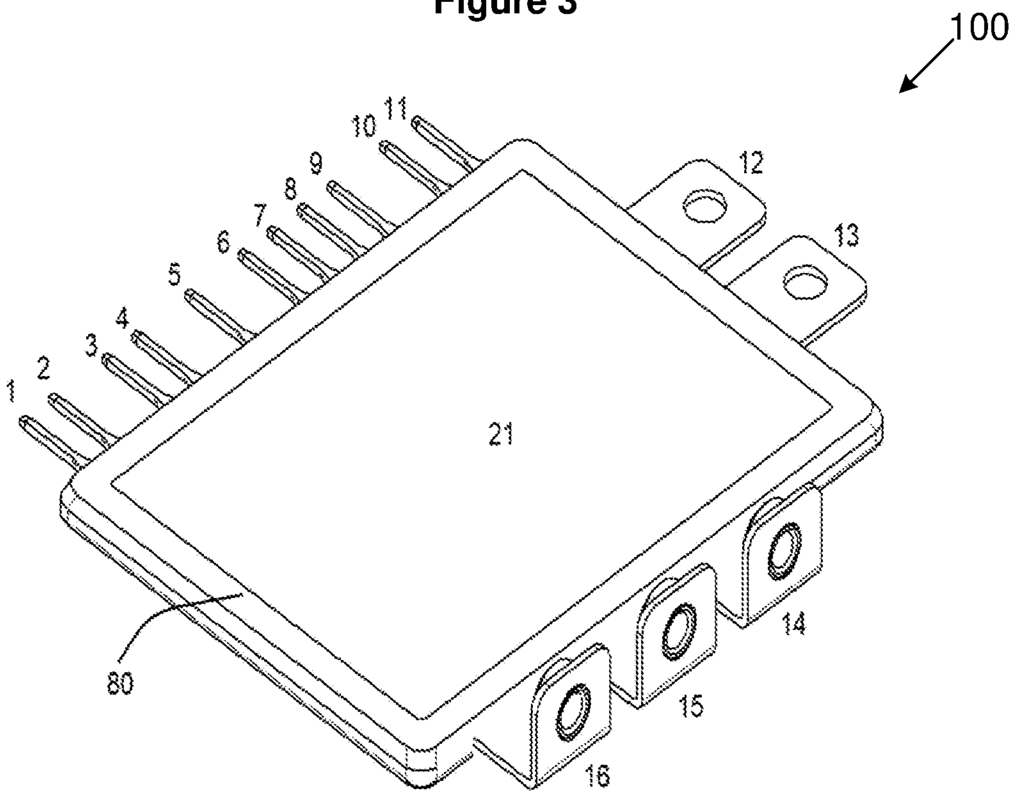

Figure 4

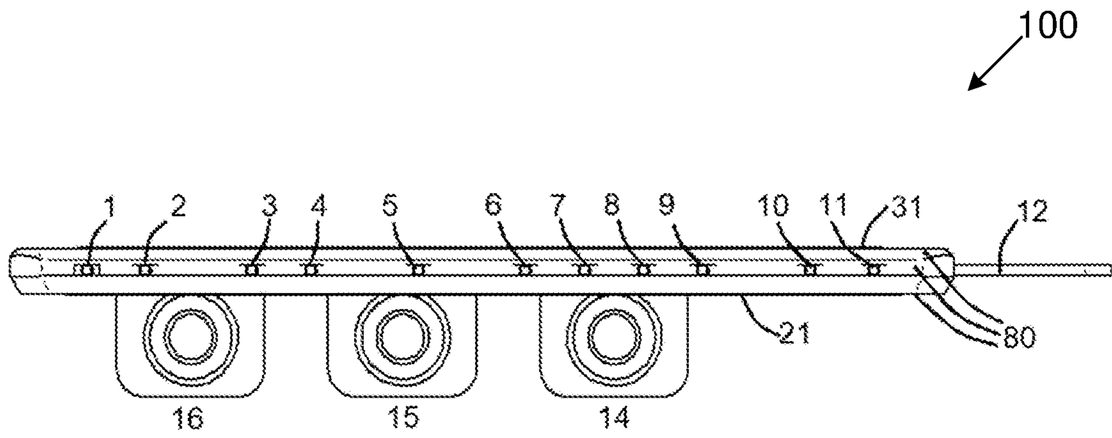

Figure 5

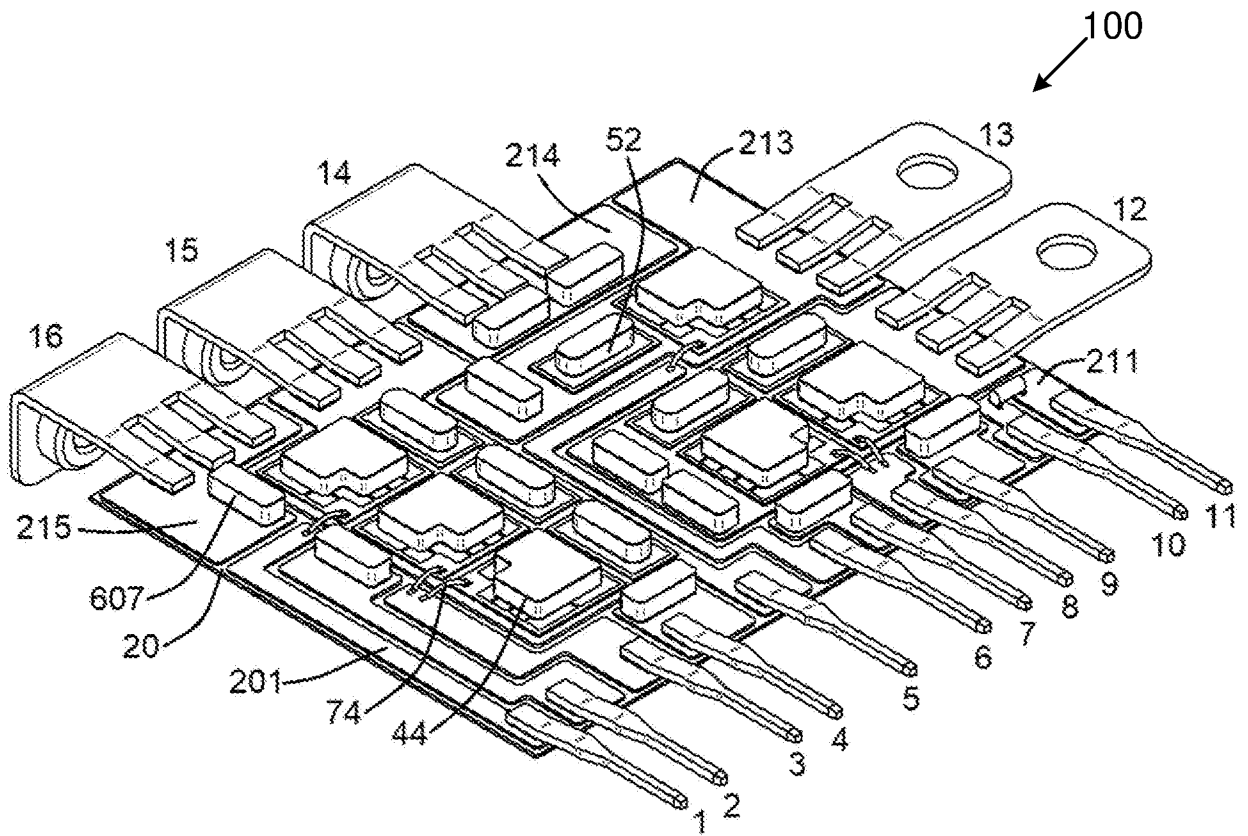

Figure 6

Figure 7

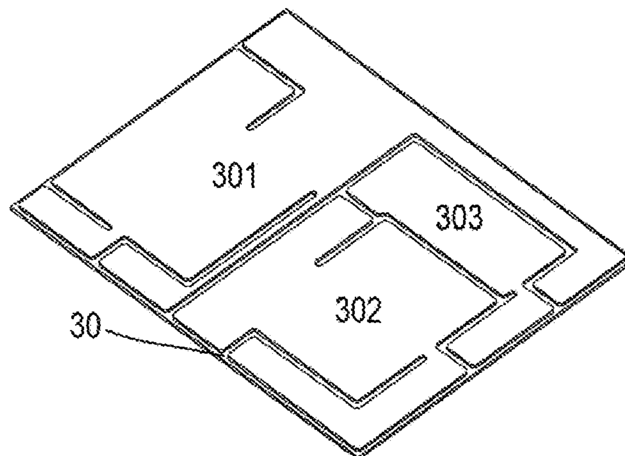

Figure 8

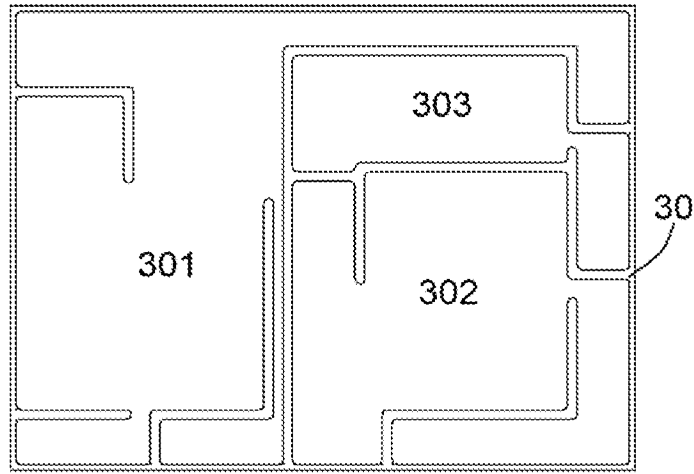

Figure 9

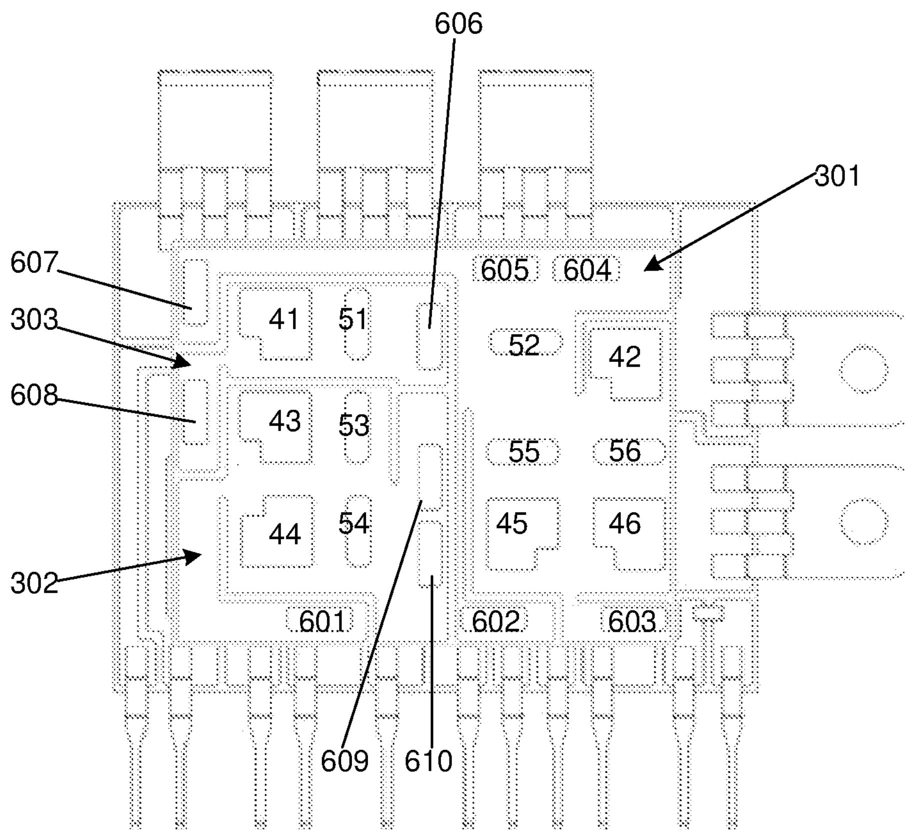

Figure 10

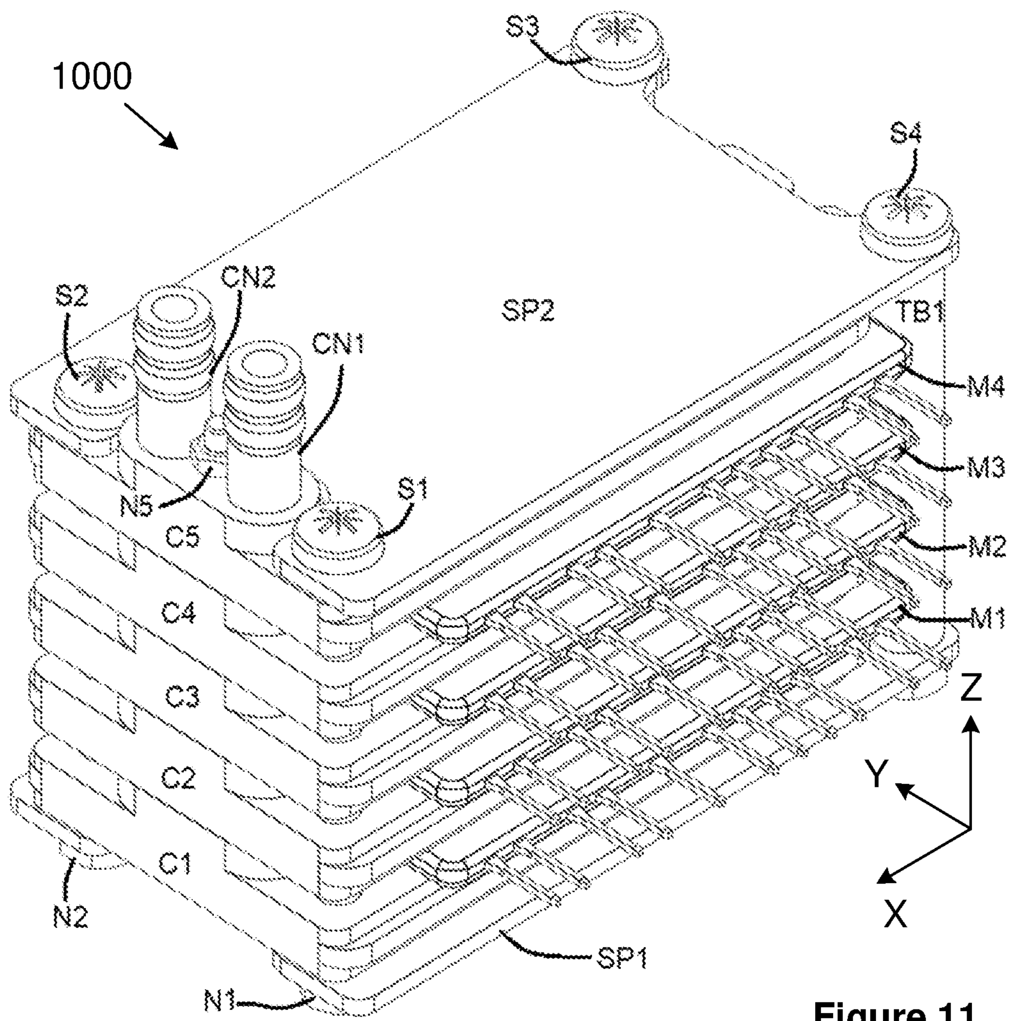

Figure 11

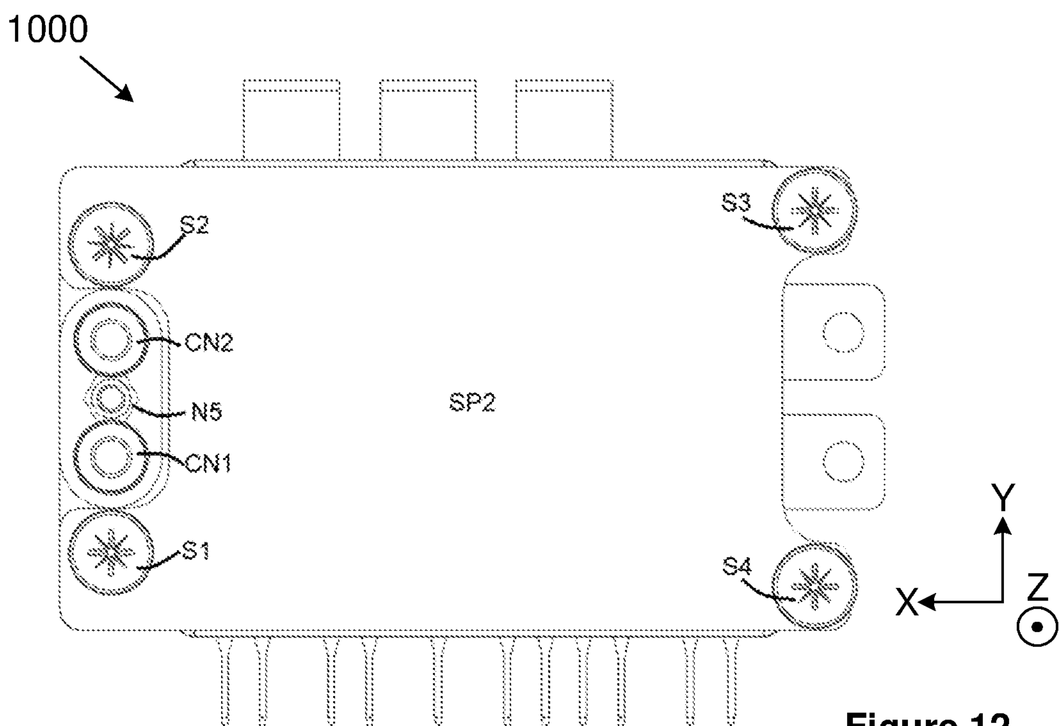

Figure 12

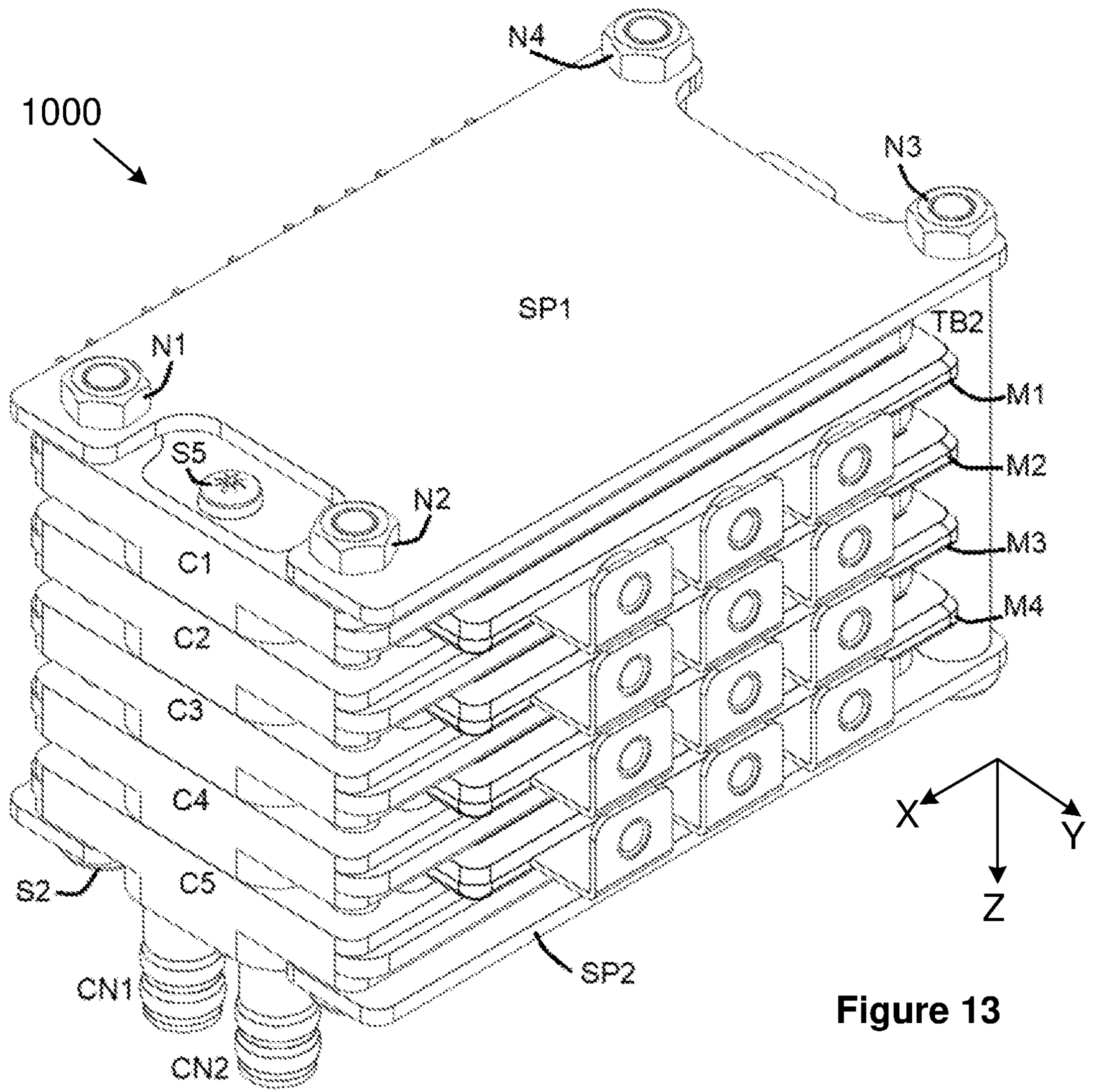

Figure 13

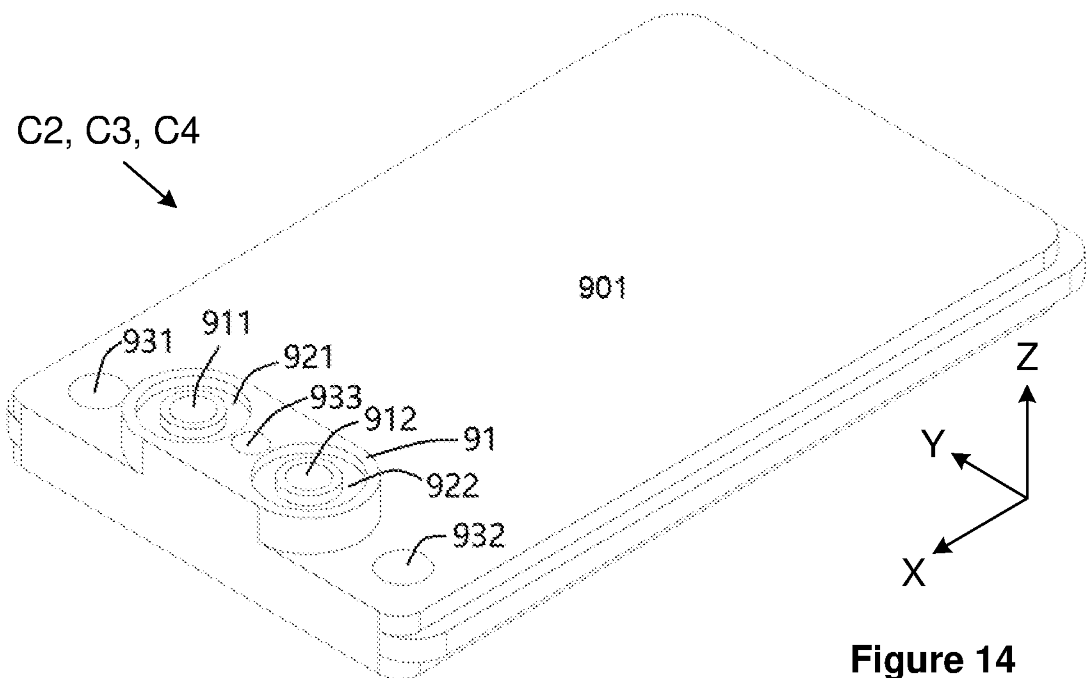

Figure 14

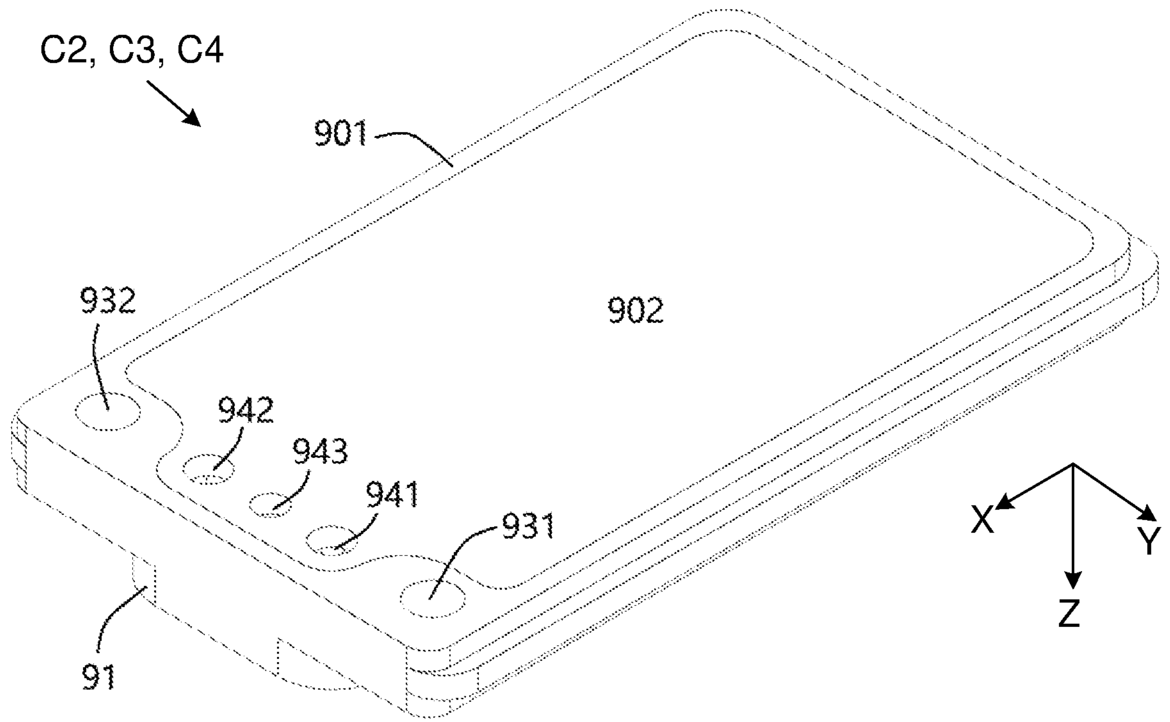

Figure 15

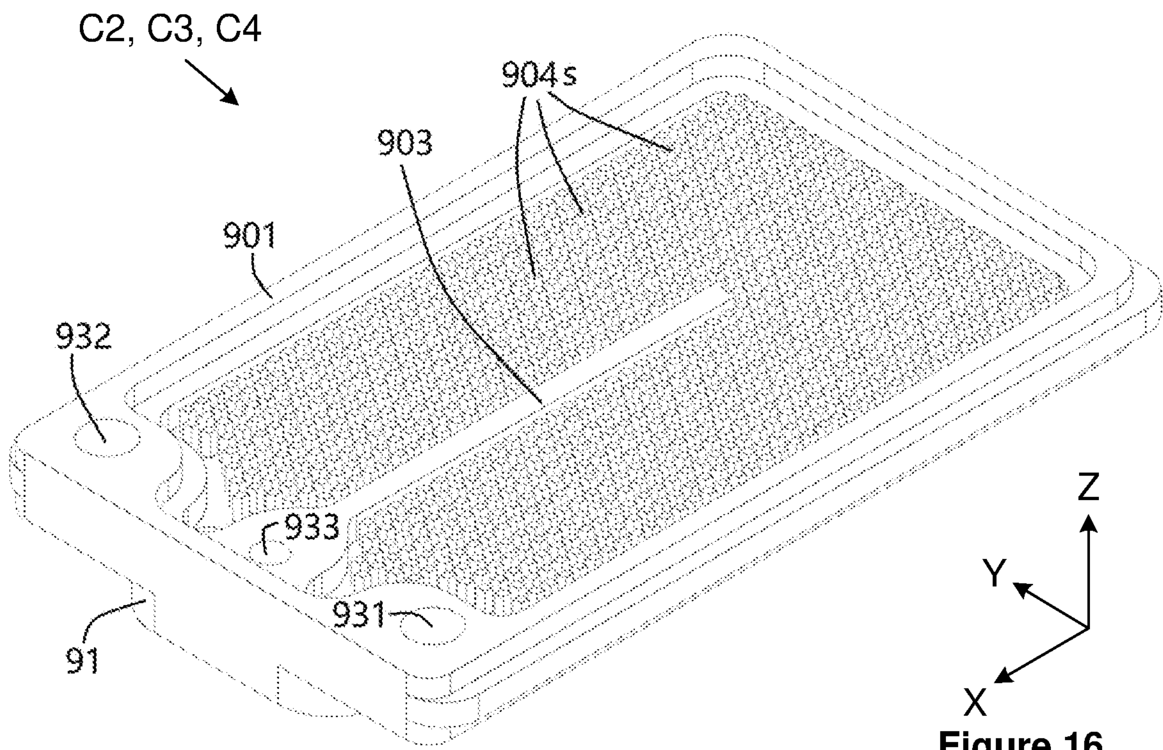

Figure 16

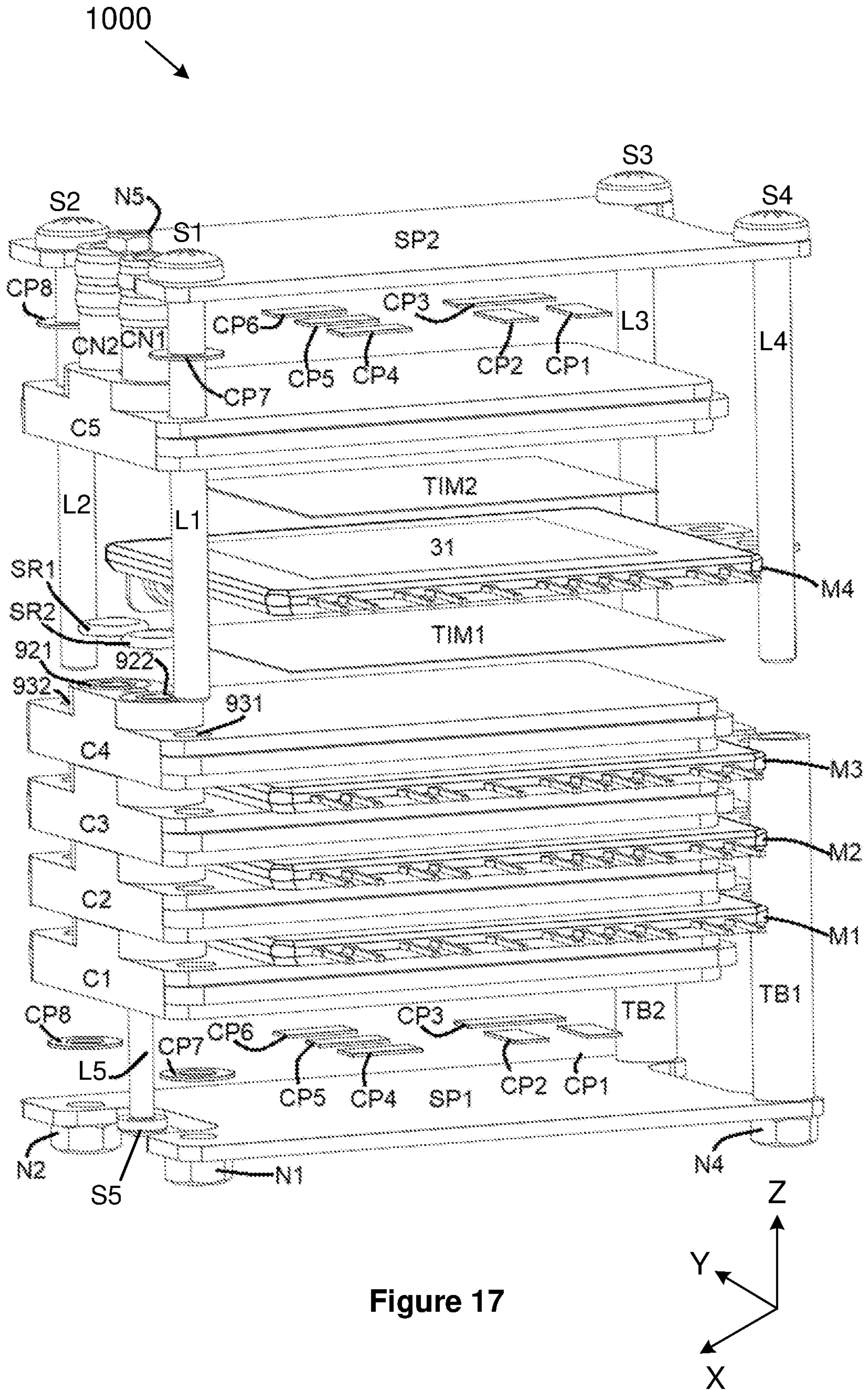

Figure 17

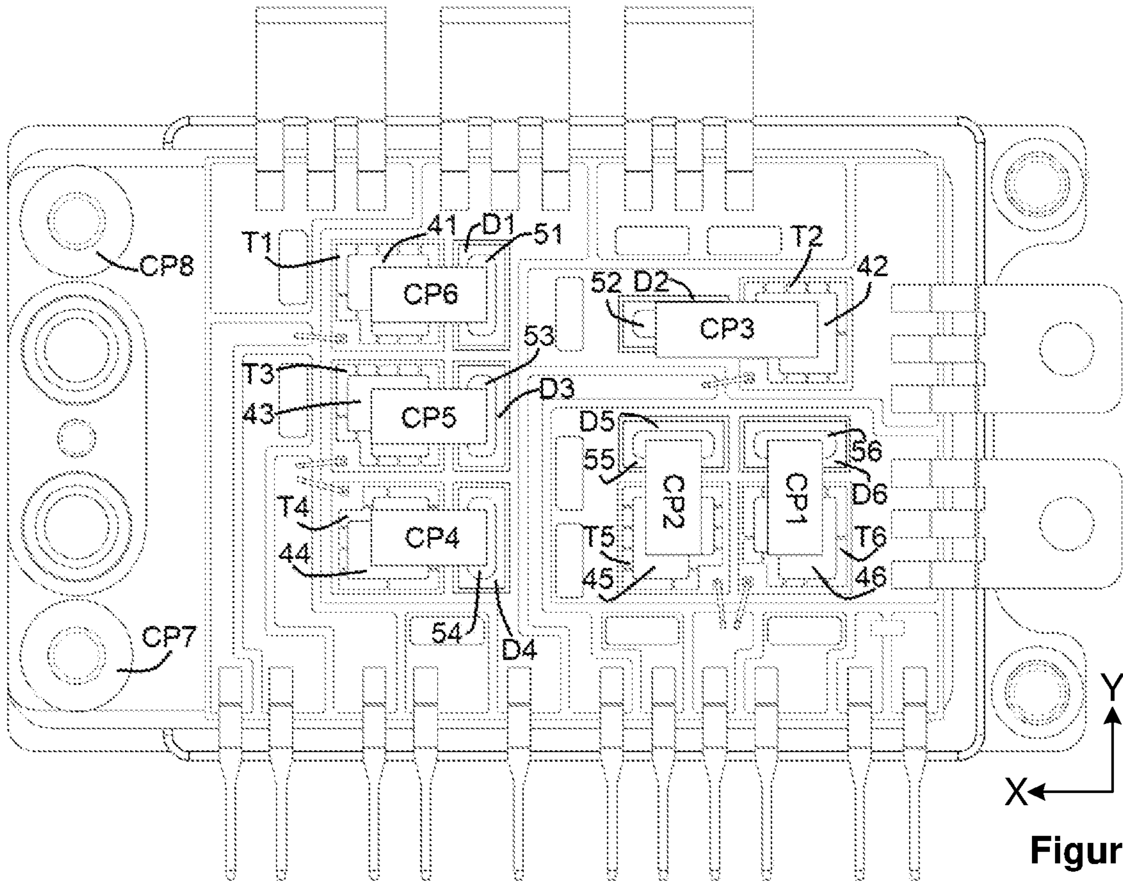

Figure 18

A1

Pressurise a stack of power semiconductor modules and coolers along a stacking direction with first and second structural plates

A2

Adjust pressure applied by adjusting a distance between first and second ends of a pressure controller

Figure 19

B1

Stack power semiconductor modules and coolers along a stacking direction

B2

Arrange first and second structural plates on opposite sides of the stack

B3

Arrange compliant components between structural plate(s) and the stack

B4

Control pressure applied by the structural plates to the stack by adjusting a distance between first and second ends of a pressure controller

Figure 20

INTERNATIONAL SEARCH REPORT

International application No
PCT/CN2022/137130

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/40 H01L23/473 H01L25/18 H02M7/00
ADD. H01L23/00 H01L25/07

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 111 970 909 A (ANHUI XENBO HEAT SINK SCIENCE&TECHNOLOGY CO LTD) 20 November 2020 (2020-11-20)	1-15, 17-22
Y	Parts of description "Background	8-10,15
A	technique", "Three beneficial effects", "In the picture", "Example 1" and "Example 2"; figures 1-6	16
X	US 2010/302733 A1 (WOODY GEORGE R [US] ET AL) 2 December 2010 (2010-12-02)	1-22
Y	paragraph [0021] - paragraph [0038]; figures 2-8	8-10,15
Y	US 2015/194367 A1 (GROSSKREUZ PAUL JEROME [US] ET AL) 9 July 2015 (2015-07-09)	8,10,15
A	paragraph [0004]; figures 1, 3B, 3C paragraph [0021] - paragraph [0039]	9

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
23 March 2023	30/03/2023

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No
PCT/CN2022/137130

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	US 2021/293495 A1 (BARAKO MICHAEL T [US] ET AL) 23 September 2021 (2021-09-23) paragraph [0018]; figures 8, 9 paragraph [0025]	8-10,15
Y	US 2009/284921 A1 (COLGAN EVAN GEORGE [US] ET AL) 19 November 2009 (2009-11-19)	8,10,15
A	paragraph [0004] - paragraph [0005]	9
A	US 10 874 037 B1 (GUPTA MAN PRAKASH [US] ET AL) 22 December 2020 (2020-12-22) page 5, line 25 - page 6, line 31; figures 2, 3	18

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