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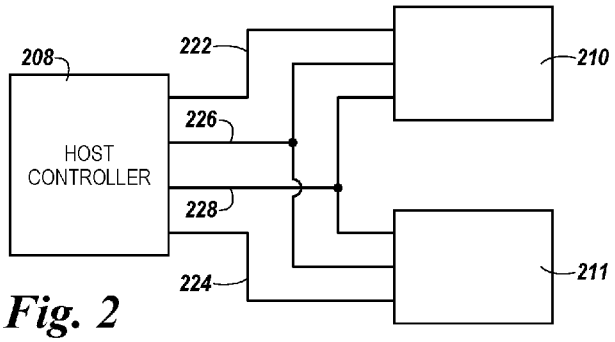

Fig. 2

(57) Abstract: The present disclosure includes apparatuses and methods related to a memory controller, such as a host memory controller. An example apparatus can include a host memory controller coupled to a first memory device and a second memory device via a channel, wherein the host memory controller is configured to send a first number of commands to the first memory device using a first device select signal, and send a second number of commands to the second memory device using a second device select signal.

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MEMORY CONTROLLER

Technical Field

[0001] The present disclosure relates generally to memory devices, and more particularly, to apparatuses and methods using a memory controller, such as a host memory controller.

Background

[0002] Memory devices are typically provided as internal, semiconductor, integrated circuits in computers or other electronic devices. There are many different types of memory including volatile and non-volatile memory. Volatile memory can require power to maintain its data and includes random-access memory (RAM), dynamic random access memory (DRAM), and synchronous dynamic random access memory (SDRAM), among others. Non-volatile memory can provide persistent data by retaining stored data when not powered and can include NAND flash memory, NOR flash memory, read only memory (ROM), Electrically Erasable Programmable ROM (EEPROM), Erasable Programmable ROM (EPROM), and resistance variable memory such as phase change random access memory (PCRAM), resistive random access memory (RRAM), and magnetoresistive random access memory (MRAM), among others.

[0003] Memory is also utilized as volatile and non-volatile data storage for a wide range of electronic applications. Non-volatile memory may be used in, for example, personal computers, portable memory sticks, digital cameras, cellular telephones, portable music players such as MP3 players, movie players, and other electronic devices. Memory cells can be arranged into arrays, with the arrays being used in memory devices.

Brief Description of the Drawings

[0004] Figure 1 is a block diagram of an apparatus in the form of a computing system including a memory system in accordance with a number of embodiments of the present disclosure.

[0005] Figure 2 is a block diagram of an apparatus in the form of a computing system including a host memory controller coupled to memory devices according to embodiments of the present disclosure.

[0006] Figure 3 is a block diagram of an apparatus in the form of a host memory controller according to embodiments of the present disclosure.

[0007] Figures 4A and 4B are timing diagrams for commands and signals sent by a host memory controller in accordance with a number of embodiments of the present disclosure.

Detailed Description

[0008] The present disclosure includes apparatuses and methods related to a memory controller, such as a host memory controller. An example apparatus can include a host memory controller coupled to a first memory device and a second memory device via a channel, wherein the host memory controller is configured to send a first number of commands to the first memory device using a first device select signal, and send a second number of commands to the second memory device using a second device select signal.

[0009] In a number of embodiments, a host including a host processor can be coupled to a number of memory devices via a channel. The number of memory devices can include a number of first memory devices, such as non-volatile memory, and a number of second memory devices, such as volatile memory. The host can select commands for execution on the first and/or second memory devices. Signals associated with commands to be executed on the first and/or second memory devices can be sent to the first and/or second memory devices on a command/address bus shared by the first and second memory devices. The first memory devices can be selected by sending a first device select signal to the first memory devices on a first device select line and then subsequent signals sent on the command/address bus will be sent to the first memory devices. The second memory devices can be selected by sending a second device select signal to the second memory devices on a second device select line and then subsequent signals sent on the command/address bus will be sent to the second memory devices. The device select signals can be used to select memory devices to account for timing parameters associated with the

memory devices and/or to account for commands that are support by particular memory devices.

[0010] In a number of embodiments, a first command can begin execution by selecting the first memory device using a first device select signal sent on a first device select line and sending signals associated with the first command to the first memory device. Timing parameters associated with a first memory device and a second memory device may allow another command to begin execution on the second memory device while the first memory device is executing the first command. While the first memory device is executing the first command, a second command can begin execution by selecting the second memory device using a second device select signal sent on a second device select line and signals associated with the second command can be sent to the second memory device. The host memory controller can send additional signals for the second command being executed on the second memory device by sending additional device select signals on the second device select line. In another embodiment, the host memory controller can select the first memory device via the first device select line and send additional signals associated with the first command being executed on the first memory device. The host memory controller can control the timing of when to send signals to the memory devices based on timing parameters associated with the memory devices using timers on the host memory controller.

[0011] In a number of embodiments, a first command can begin execution by selecting the first memory device using a first device select signal sent on a first device select line and sending signals associated with the first command to the first memory device. The signals associated with the first command can be supported by the first memory device, but may not be supported by the second memory device. The device select signals sent to the memory devices on the device select lines to select which memory devices will receive signals can be used to send commands to memory devices that support the commands being sent. A second memory device can be selected via a device select signal sent to the second memory device via a second device select line. Signals associated with a command to be executed on the second memory device can be sent to the second memory device. The signals can be supported by the second memory device, but may not be supported by the first memory

device. The host memory controller can control which memory devices will receive signals using state machines on the host memory controller.

[0012] In the following detailed description of the present disclosure, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration how a number of embodiments of the disclosure may be practiced. These embodiments are described in sufficient detail to enable those of ordinary skill in the art to practice the embodiments of this disclosure, and it is to be understood that other embodiments may be utilized and that process, electrical, and/or structural changes may be made without departing from the scope of the present disclosure. As used herein, the designators "M", "N", "S", "T", "X", "Y", and "Z" indicate that a number of the particular feature so designated can be included with a number of embodiments of the present disclosure.

[0013] As used herein, "a number of" something can refer to one or more of such things. For example, a number of memory devices can refer to one or more of memory devices. Additionally, designators such as "M", "N", "S", "T", "X", "Y", and "Z", as used herein, particularly with respect to reference numerals in the drawings, indicates that a number of the particular feature so designated can be included with a number of embodiments of the present disclosure.

[0014] The figures herein follow a numbering convention in which the first digit or digits correspond to the drawing figure number and the remaining digits identify an element or component in the drawing. Similar elements or components between different figures may be identified by the use of similar digits. For example, 108 may reference element "08" in Figure 1, and a similar element may be referenced as 308 in Figure 3. As will be appreciated, elements shown in the various embodiments herein can be added, exchanged, and/or eliminated so as to provide a number of additional embodiments of the present disclosure. In addition, the proportion and the relative scale of the elements provided in the figures are intended to illustrate various embodiments of the present disclosure and are not to be used in a limiting sense.

[0015] Figure 1 is a functional block diagram of a computing system including an apparatus in the form of a number of memory systems 104-1...104-N, in accordance with one or more embodiments of the present disclosure. As

used herein, an "apparatus" can refer to, but is not limited to, any of a variety of structures or combinations of structures, such as a circuit or circuitry, a die or dice, a module or modules, a device or devices, or a system or systems, for example. In the embodiment illustrated in Figure 1, memory systems 104-1...104-N can include a one or more memory devices, such as memory devices 110-1, . . ., 110-X, 110-Y and memory devices 111-1, . . ., 111-Z. Memory devices 110-1, . . ., 110-X, 110-Y and memory devices 111-1, . . ., 111-Z can include volatile memory and/or non-volatile memory. For example, memory devices 110-1, . . ., 110-X, 110-Y can be non-volatile RRAM memory and memory devices 111-1, . . ., 111-Z can be DRAM memory. In Figure 1, memory system 104-1 is coupled to the host via channel 112-1 can include memory devices 110-1, . . ., 110-X. In this example, each memory device 110-1, . . ., 110-X, 110-Y and 111-1, ..., 111-Z includes a controller 114. Controller 114 can receive commands from host 102 and control execution of the commands on a memory device. Memory devices 110-1, . . ., 110-X, 110-Y and 111-1, ..., 111-Z can also include memory device that do not include a controller on the memory device (e.g., onboard), such as discreet memory devices, for example.

[0016] As illustrated in Figure 1, a host 102 can be coupled to the memory systems 104-1...104-N. In a number of embodiments, each memory system 104-1...104-N can be coupled to host 102 via a channel. In Figure 1A, memory system 104-1 is coupled to host 102 via channel 112-1 and memory system 104-N is coupled to host 102 via channel 112-N. Host 102 can be a laptop computer, personal computers, digital camera, digital recording and playback device, mobile telephone, PDA, memory card reader, interface hub, among other host systems, and can include a memory access device, e.g., a processor. One of ordinary skill in the art will appreciate that "a processor" can intend one or more processors, such as a parallel processing system, a number of coprocessors, etc.

[0017] Host 102 includes a controller, e.g., host memory controllers 108-1, . . ., 108-N, to communicate with memory systems 104-1...104-N. The controller can be located on the host and/or on another portion of the memory system. The host memory controller 108 can send commands to memory devices 110-1, . . ., 110-X, 110-Y and memory devices 111-1, . . ., 111-Z via channels

112-1...112-N. The host memory controller 108 can communicate with the memory devices 110-1, . . ., 110-X, 110-Y and memory devices 111-1, . . ., 111-Z and/or the controller 114 on each of the memory devices 110-1, . . ., 110-X, 110-Y and memory devices 111-1, . . ., 111-Z to read, write, and erase data, among other operations. A physical host interface can provide an interface for passing control, address, data, and other signals between the memory systems 104-1...104-N and host 102 having compatible receptors for the physical host interface. The signals can be communicated between 102 and memory devices 110-1, . . ., 110-X, 110-Y and memory devices 111-1, . . ., 111-Z on a number of buses, such as a data bus and/or an address bus, for example, via channels 112-1...112-N.

[0018] In a number of embodiments, a host memory controller can use a first address range to address memory devices 110-1, . . ., 110-X, 110-Y and a second address range to address memory device 111-1, . . ., 111-Z. Each memory device can be accessed directly by the host processor 108, where a first address set (e.g., 0xAA..AA - 0xBB..BB) can be used to access memory devices 110-1, . . ., 110-X, 110-Y and a second address set (e.g., 0xCC..CC - 0xDD..DD) can be used to access memory devices 111-1, . . ., 111-Z, for example.

[0019] In a number of embodiments, memory devices 110-1, . . ., 110-Y can be the main memory for memory system 104-N and memory devices 111-1, . . ., 111-Z can be cache for memory system 104-N. The host processor 108 can access memory devices 110-1, . . .,, 110-Y using an address set (e.g., 0xAA..AA - 0xDD..DD) and the host processor 108 can include tag information for data in the cache, memory devices 111-1, . . ., 111-Z, to locate and/or store data in the cache. The tag information for the cache can also be stored in other memory devices, such as memory devices 110-1, . . ., 110-X and/or 111-1, . . ., 111-Z.

[0020] In a number of embodiments, a first portion of memory devices 110-1, . . ., 110-Y can be access using a first address set (e.g., 0xAA..AA - 0xBB..BB) and a first portion of memory devices 111-1, . . ., 111-Z can be accessed using a second address set (e.g., 0xCC..CC - 0xDD..DD), for example. In a number of embodiments, a second portion of memory devices 110-1, . . ., 110-Y can be accessed using a third address set (e.g., 0xEE..EE - 0xFF..FF) and a second portion of memory devices 111-1, . . ., 111-Z can be cache for the second portion of memory devices memory devices 110-1, . . ., 110-X, 110-Y.

[0021] In a number of embodiments, the host memory controller 108 can control execution of commands by giving priority to commands that are to be executed on particular memory devices 110-1, . . ., 110-X, 110-Y and 111-1, . . ., 111-Z based on the type of memory device. The host memory controller 108 can give priority to commands based on the address set of the commands, where commands with addresses in the first address set associated with particular memory device may be given priority over commands with addresses in the a second address set associated with a different memory device. The priority assigned to the commands can be changed based on a number of commands in a command queue and types of commands in a command queue. The priority assignments can be programmed as the memory devices are being started and they are not changed until the memory devices are shut down and started again. Also, the priority assignments can be changed while the memory device are being operated based on the number and types of commands that the host is sending to the memory devices. In a number of embodiments, priority assignments can be modified based on the applications that are being serviced by the host memory controller.

[0022] Memory controllers, such as host memory controller 108 and/or controller 114 on a memory device, can include control circuitry, e.g., hardware, firmware, and/or software. In one or more embodiments, the host memory controller 108 and/or controller 114 on a memory device can be an application specific integrated circuit (ASIC) coupled to a printed circuit board including a physical interface.

[0023] Memory devices 110-1, . . ., 110-X, 110-Y and memory devices 111-1, . . ., 111-Z can provide main memory for the memory system or could be used as additional memory or storage throughout the memory system. Each memory device 110-1, . . ., 110-X, 110-Y and memory device 111-1, . . ., 111-Z can include one or more arrays of memory cells, e.g., non-volatile memory cells. The arrays can be flash arrays with a NAND architecture, for example. Embodiments are not limited to a particular type of memory device. For instance, the memory device can include RAM, ROM, DRAM, SDRAM, PCRAM, RRAM, and flash memory, among others.

[0024] The embodiment of Figure 1 can include additional circuitry that is not illustrated so as not to obscure embodiments of the present disclosure. For

example, the memory systems 104-1... 104-N can include address circuitry to latch address signals provided over I/O connections through I/O circuitry. Address signals can be received and decoded by a row decoder and a column decoder to access the memory devices 110-1, . . ., 110-X, 110-Y and memory devices 111-1, . . ., 111-Z. It will be appreciated by those skilled in the art that the number of address input connections can depend on the density and architecture of the memory devices 110-1, . . ., 110-X, 110-Y and memory devices 111-1, . . ., 111-Z. In a number of embodiments, memory devices 110-1, . . ., 110-X, 110-Y can have storage densities that are different than the storage density of memory devices 111-1, . . ., 111-Z. Also, memory devices 110-1, . . ., 110-X, 110-Y can use a different number of address signals than memory devices 111-1, . . ., 111-Z.

[0025] Figure 2 is a block diagram of an apparatus in the form of a computing system including a host memory controller coupled to memory devices according to embodiments of the present disclosure. In Figure 2, host memory controller 208 is coupled to a first memory device 210 via data bus 226, command/address bus 228, and a first device select line 222. Host memory controller 208 is coupled to a second memory device 211 via data bus 226, command/address bus 228, and a second device select line 224. Host memory controller can select memory device 210 by sending a device select signal to memory device 210 via device select line 222. Host memory controller can select memory device 211 by sending a device select signal to memory device 211 via device select line 224

[0026] Figure 3 is a block diagram of an apparatus in the form of a host memory controller according to embodiments of the present disclosure. In Figure 3, host memory controller 308 includes host port 332, which can be coupled to a host processor. Host port 332 can receive commands from a host processor and place them in command queue 338. Commands from command queue 338 can be sent to memory devices via channel control 340. Channel control 340 can include state machines 342-1, . . ., 342-T. Commands can be selected for execution on a set of the state machines 342-1, . . ., 342-T. Particular sets of state machines 342-1, . . ., 342-T can be associated with particular memory devices. For example, a first set of state machines 342-1, . . ., 342-T can be used to execute commands on a first memory device (e.g., memory

device 110-1 in Figure 1) and a second set of state machines 342-1, . . ., 342-T can be used to execute commands on a second memory device (e.g., memory device 111-1 in Figure 1).

[0027] The commands can be sent from state machines 342-1, . . ., 342-T to the memory devices via arbiter 344 and physical interface 346 of the host memory controller 308. Physical interface 346 can include timers 348-1, . . . , 348-S. Particular sets of timers 348-1, . . . , 348-S can be associated with particular memory devices. For example, a first set of timers 348-1, . . . , 348-S can be used to control the timing of commands on a first memory device (e.g., memory device 110-1 in Figure 1) and a second set of timers 348-1, . . . , 348-S can be used to control the timing of commands on a second memory device (e.g., memory device 111-1 in Figure 1). The first memory device may have different timing parameters than the second memory device, therefore timers 348-1, . . . , 348-S can be configured to include a number of timing parameters that control the timing of commands on a different memory devices. The commands from the host memory controller 308 can be sent to memory devices via data bus 326 and/or command/address bus 328. Data associated with the commands can be stored in write data buffer 334 on the controller and sent from the host to memory devices via data bus 326. Also, data associated with the commands can be received at the host from memory devices via data bus 326 and stored in read data buffer 336.

[0028] Figures 4A and 4B are timing diagrams for commands and signals sent by a host memory controller in accordance with a number of embodiments of the present disclosure. In Figure 4A, a host memory controller can send signals to a first memory device (e.g., memory device 110-1 in Figure 1) and/or a second memory device (e.g., memory device 111-1 in Figure 1) based on the timing parameters associated with memory devices. Device select signals can be sent to a first memory device via device select line 424, along with activate commands 454-1 and 454-2. The device select signals sent can indicate that activate commands 454-1 and 454-2 are for the first memory device(s) coupled to the host via device select line 424. The timing parameters associated with the performing commands on the first device can include an activate to read time (t_1) 450 that allows for another command to be activated and/or executed on the second memory device during activate to read time 450.

[0029] The host memory controller can start execution of a command on a second memory device by sending device select signals to a second memory device via device select line 422, along with activate commands 458-1 and 458-2. The execution of the command on the second memory device can occur right after the activate commands 454-1 and 454-2 or after a period of time, as indicated by deselect signal 456. Activate to read time (t_2) 452 for the second memory device is such that the second memory device will be ready to continue execution of the command before the first memory device will be ready to continue execution of its command, therefore device select signals can be sent to the second memory device along with device command signal 460 and address signal 462 on command bus 426 for the second memory device command. The execution of the command on the second memory device can continue right after the activate commands 458-1 and 458-2 or after a period of time, as indicated by deselect signal 456.

[0030] During the time where activate commands 458-1 and 458-2, command signal 460, and address signal 462 were sent to the second memory device, the first memory device is nearing the end of activate to read time (t_1) 450. The host memory controller can continue execution of a command on the first memory device by sending device select signals can be sent to the first memory device along with command signal 464 and address signal 466 to the first memory device on command bus 426. The execution of the command on the first memory device can continue right after device command signal 460 and address signal 462 or after a period of time, as indicated by deselect signal 456.

[0031] In Figure 4B, a host memory controller can send signals to a first memory device (e.g., memory device 110-1 in Figure 1) and/or a second memory device (e.g., memory device 111-1 in Figure 1) based on the type of commands that the memory devices supported by the memory devices. For example, a first memory device may not support a command that is supported by a second memory device. The device select signals sent to the memory devices via device select lines can be used to select the device that will receive commands supported by the selected memory device.

[0032] In Figure 4B, device select signals can be sent to a first memory device via device select line 422, along with activate commands 458-1 and 458-2. The device select signals sent can indicate that activate commands 458-1 and

458-2 are for the first memory device(s) coupled to the host via device select line 422. The first memory device can be configured to support activate commands 458-1 and 458-2.

[0033] The host memory controller can start execution of a command on a second memory device by sending device select signals to a second memory device via device select line 424, along with activate commands 454-1,454-2, and 454-3. The execution of the command on the second memory device can continue right after activate signals 458-1 and 458-2 or after a period of time, as indicated by deselect signal 456. The command being executed on the second memory device may include activate commands 454-1,454-2, and 454-3, which might not be supported by the first memory device. The device select signals sent to the second memory device via select line 424 can select the second device for receiving activate commands 454-1,454-2, and 454-3, which are supported by the second memory device.

[0034] The command selected for execution by the host on the first memory device can continue after sending activate commands 454-1,454-2, and 454-3 to the second memory device. The host memory controller can continue execution of the command on the first memory device by sending device select signals to the first memory device via device select line 422 to select the first memory device for receiving command signal 460 and address signal 462 via command bus 426. The execution of the command on the first memory device can continue right after activate signals 458-1, 458-2 and 458-3 or after a period of time, as indicated by deselect signal 456.

[0035] Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art will appreciate that an arrangement calculated to achieve the same results can be substituted for the specific embodiments shown. This disclosure is intended to cover adaptations or variations of various embodiments of the present disclosure. It is to be understood that the above description has been made in an illustrative fashion, and not a restrictive one. Combination of the above embodiments, and other embodiments not specifically described herein will be apparent to those of skill in the art upon reviewing the above description. The scope of the various embodiments of the present disclosure includes other applications in which the above structures and methods are used. Therefore, the scope of various

embodiments of the present disclosure should be determined with reference to the appended claims, along with the full range of equivalents to which such claims are entitled.

[0036] In the foregoing Detailed Description, various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the disclosed embodiments of the present disclosure have to use more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

What is claimed is:

1. An apparatus, comprising:

a host memory controller coupled to a first memory device and a second memory device via a channel, wherein the host memory controller is configured to:

send a first number of commands to the first memory device using a first device select signal; and

send a second number of commands to the second memory device using a second device select signal.

2. The apparatus of claim 1, wherein the channel includes data lines and command lines that couple the host memory controller to the first memory device and the second memory device.

3. The apparatus of claim 1, wherein the channel includes a first device select line that couples the host memory controller to the first memory device and wherein the channel includes a second device select line that couples the host memory controller to the second memory device.

4. The apparatus of any one of claims 1-3, wherein the first number of commands are sent to the first memory device on commands lines shared by the first memory device and the second memory device in response the host memory controller sending the first device select signal.

5. The apparatus of any one of claims 1-3, wherein the second number of commands are sent to the second memory device on commands lines shared by the first memory device and the second memory device in response the host memory controller sending the second device select signal based on timing parameters associated with the second memory device.

6. An apparatus, comprising:

a first memory device;

a second memory device; and

a host memory controller coupled to the first memory device and the second memory device via a channel, wherein the host memory controller is configured to:

send a first command to the first memory device; and

send a second command to the second memory device prior to sending another command to the first memory device due to timing parameters associated with the second memory device.

7. The apparatus of claim 6, wherein the second memory device is activated and ready to receive the second command prior to the first memory device being activated.

8. The apparatus of any one of claims 6-7, wherein the host memory controller is configured to send a third command to the first memory device after sending the second command to the second memory device and in response to the first memory device being activated and ready to receive the third command.

9. The apparatus of any one of claims 6-7, wherein the first command is selected for execution on the first memory device by a state machine on the host memory controller based on an address associated with the first command.

10. The apparatus of any one of claims 6-7, wherein the first command and the second command are sent using a number of timing registers on the host memory controller.

11. An apparatus, comprising:

a first memory device;

a second memory device; and

a host memory controller coupled to the first memory device and the second memory device via a channel, wherein the controller is configured to:

select an operation for execution on the first memory device based on the operation including a particular type of command; and

send a first command associated with the operation to the first memory device.

12. The apparatus of claim 11, wherein the first command is send to the first memory device using a first select signal in response to a state machine selecting the first memory device for executing of the operation.

13. The apparatus of any one of claims 11-12, wherein the first command is sent to the first memory device along with other commands associated with the operation based on timing parameters associated with the first memory device and timing parameters associated with the second memory device.

14. The apparatus of claim 11, wherein the first memory device is mapped to a first range of addresses by the host memory controller and the second memory device is mapped to a second ranged of addresses by the host memory controller.

15. The apparatus of claim 11, wherein the first memory device is mapped to a range of addresses by the host memory controller and the second memory device acts as cache for the first memory device.

16. A method, comprising:

selecting a first memory device to execute a first operation by sending a first device select signal to the first memory device;

sending a first number of commands associated with the first operation to the first memory device in response to sending the first device select signal.

17. The method of claim 16, further including selecting a second memory device to execute a second operation by sending a second device select signal to the second memory device.

18. The method of claim 17, further including sending a second number of commands associated with the second operation to the second memory device based on timing parameters of the first memory device.

19. The method of claim 17, further including sending a second number of commands associated with the second operation to the second first memory

device prior to the first number of commands being executed by the first memory device.

20. The method of claim 16, wherein sending the first number of commands associated with the first operation to the first memory device includes sending a portion of the first number of commands that are not executable by the second memory device.

21. A method, comprising:

sending a first activate command from a host memory controller to a first memory device using on a first timer on the host memory controller associated with the first memory device; and

sending a second activate command and a first access command from the host memory controller to a second memory device prior to sending another command to the first memory device using on a second timer on the host memory controller associated with the second memory device.

22. The method of claim 21, including sending the first activate command to the first memory device based on priority given to commands to be executed on the first memory device.

23. The method of claim 21, including sending the first activate command to the first memory device based on the second memory device receiving a particular number of prior commands consecutively.

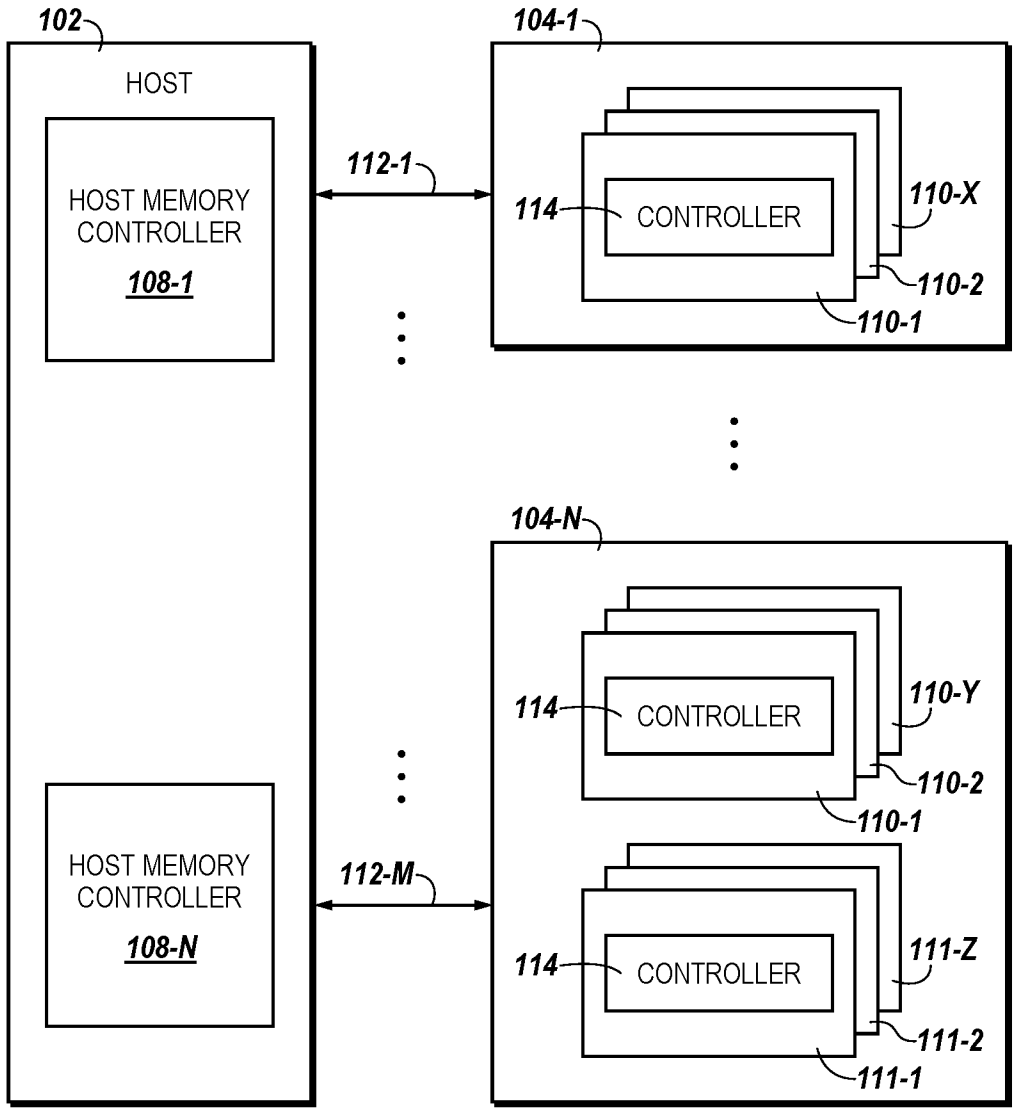
102
HOST
HOST MEMORY CONTROLLER
108-1
HOST MEMORY CONTROLLER
108-N
112-1
112-M
104-1
114
CONTROLLER
110-X
110-2
110-1
104-N
114
CONTROLLER
110-Y
110-2
110-1
114
CONTROLLER
111-Z
111-2
111-1

Fig. 1

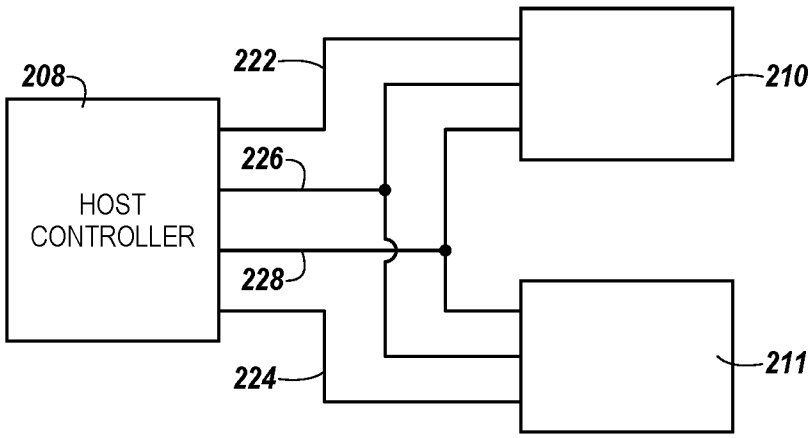
208
HOST CONTROLLER
222
226
228
224
210
211

Fig. 2

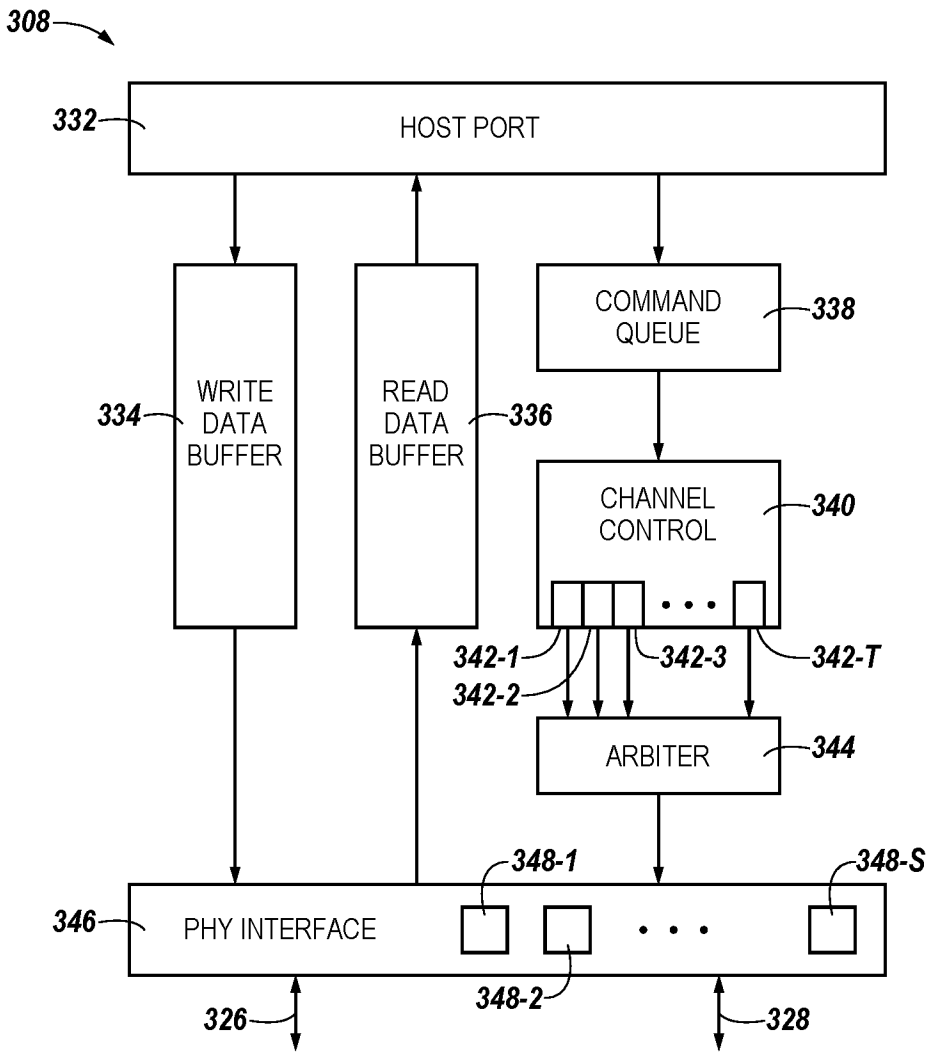
308
332
HOST PORT
334
WRITE DATA BUFFER
336
READ DATA BUFFER
COMMAND QUEUE
338
CHANNEL CONTROL
340
342-1
342-2
342-3
342-T
ARBITER
344
346
PHY INTERFACE
348-1
348-2
348-S
326
328

Fig. 3

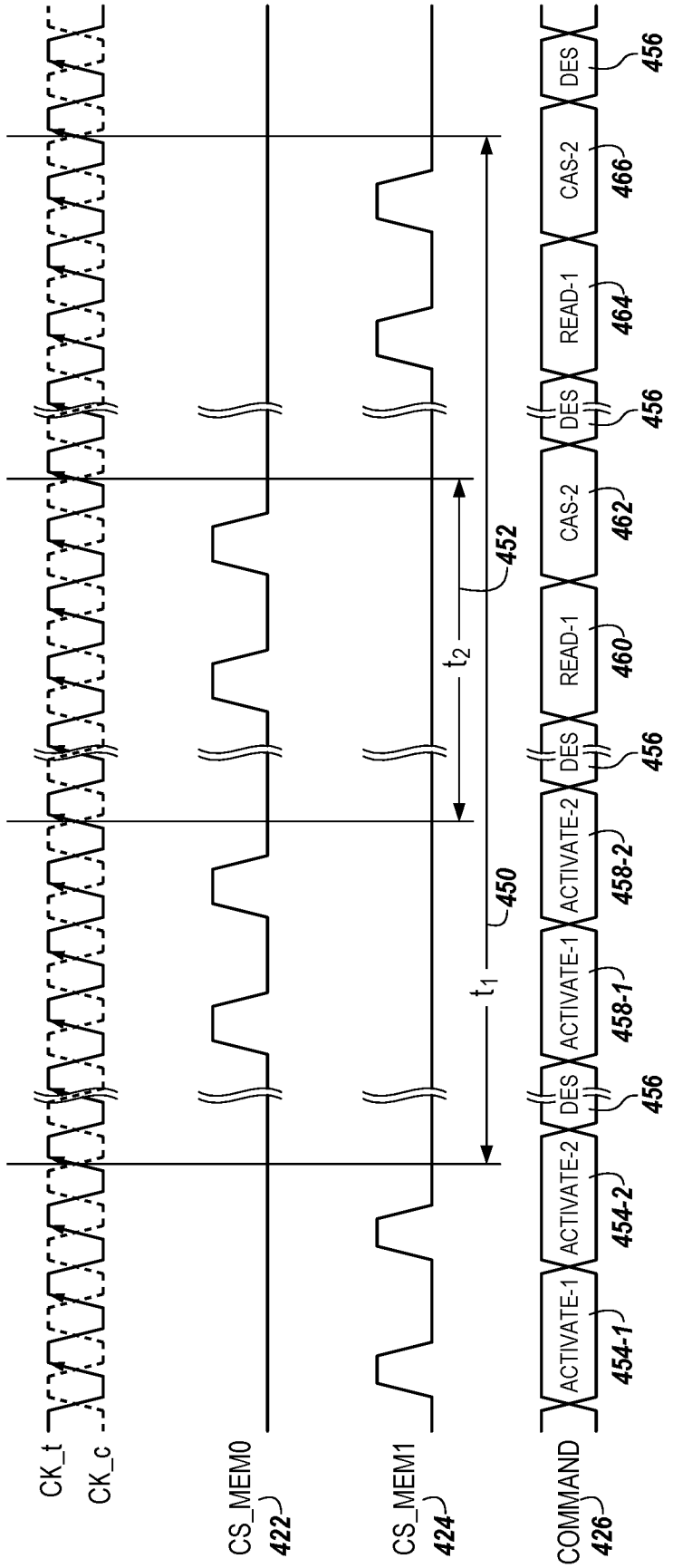
CK_t
CK_c
CS_MEM0
422
CS_MEM1
424
COMMAND
426
ACTIVATE-1
454-1
ACTIVATE-2
454-2
DES
456
ACTIVATE-1
458-1
ACTIVATE-2
458-2
DES
456
READ-1
460
CAS-2
462
DES
456
READ-1
464
CAS-2
466
DES
456
t_1
450
t_2
452

Fig. 4A

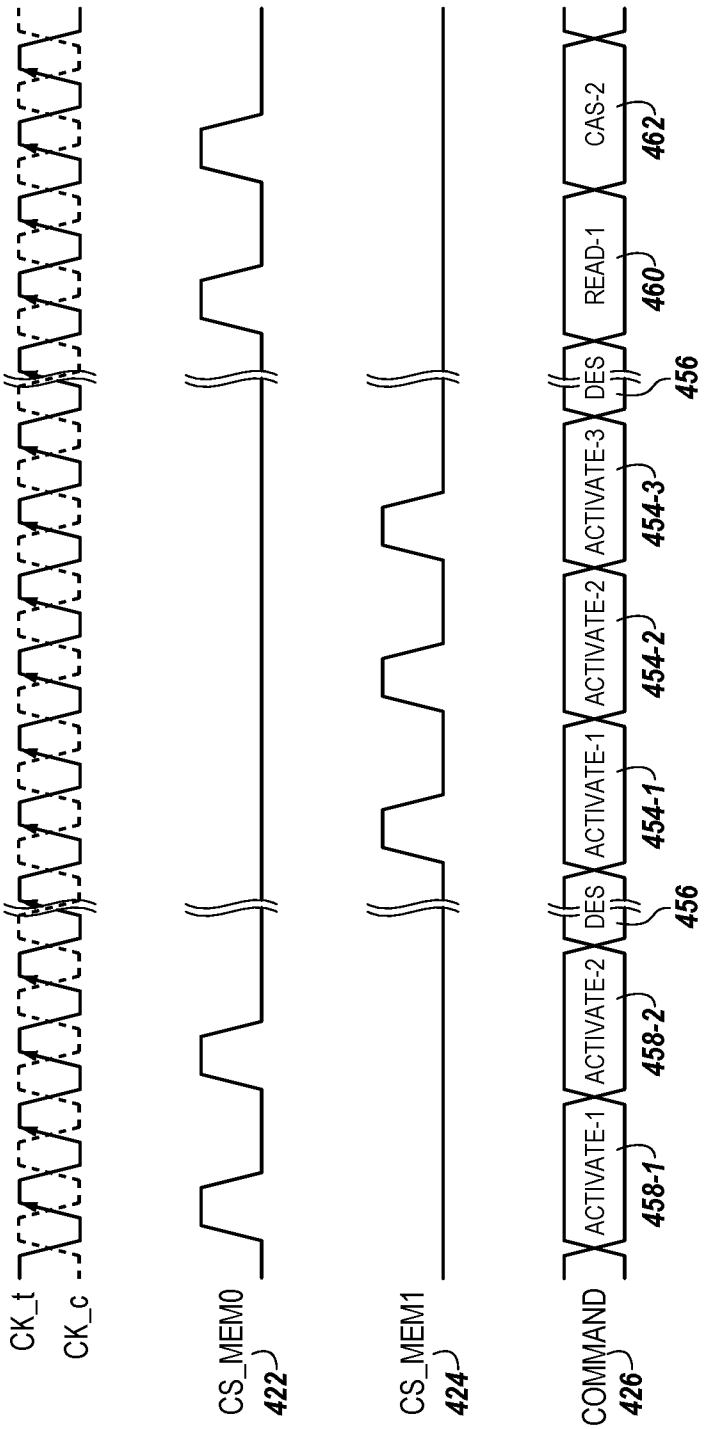
CK_t
CK_c
CS_MEM0
422
CS_MEM1
424
COMMAND
426
ACTIVATE-1
458-1
ACTIVATE-2
458-2
DES
456
ACTIVATE-1
454-1
ACTIVATE-2
454-2
ACTIVATE-3
454-3
DES
456
READ-1
460
CAS-2
462

Fig. 4B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/036988

A. CLASSIFICATION OF SUBJECT MATTER

G06F 13/16(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 13/16; G06F 012/00; G06F 1/12; G06F 13/00; G06F 17/00; G06F 19/00; G11C 7/22

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: controller, second memory, time parameter, channel, select, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005-0144375 A1 (KULJIT S. BAINS et al.) 30 June 2005 See paragraphs [0015], [0020], [0036]; claims 1-2, 9; and figures 4a, 6.	1-4,11-12,14-17,20
Y		5-10,13,18-19,21-23
Y	US 2006-0217865 A1 (RICHARD SANDERS) 28 September 2006 See paragraphs [0014], [0016], [0024]-[0025]; and figures 1-2.	5-10,13,18-19,21-23
A	US 2013-0124904 A1 (DAVID T. WANG et al.) 16 May 2013 See paragraphs [0029]-[0054]; claim 2; and figures 2A-4B.	1-23
A	US 2014-0286107 A1 (TORU ISHIKAWA) 25 September 2014 See paragraphs [0056]-[0073]; claim 1; and figures 5-11.	1-23
A	US 2002-0184461 A1 (JOHN F. ZUMKEHR) 05 December 2002 See paragraphs [0040]-[0055]; claim 1; and figures 6-12.	1-23

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01 October 2018 (01.10.2018)	**01 October 2018 (01.10.2018)**

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