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More et al.

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(45) **Date of Patent: Jul. 18, 2023**

(54) **SEMICONDUCTOR DEVICES HAVING MERGED SOURCE/DRAIN FEATURES AND METHODS OF FABRICATION THEREOF**

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(73) Assignee: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**, Hsinchu (TW)

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(51) **Int. Cl.**

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H01L 27/088	(2006.01)
H01L 29/06	(2006.01)
B82Y 10/00	(2011.01)
H01L 29/08	(2006.01)
H01L 29/423	(2006.01)
H01L 29/66	(2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ***H01L 21/823425*** (2013.01); ***H01L 21/823412*** (2013.01); ***H01L 21/823431*** (2013.01); ***H01L 27/088*** (2013.01); ***H01L 27/0886*** (2013.01)

(58) **Field of Classification Search**

CPC H01L 21/823425; H01L 21/823418; H01L 21/823814; H01L 21/823412; H01L 29/0673; H01L 29/66439; H01L 29/775; H01L 29/78696; H01L 21/823431; H01L 27/088; H01L 27/0886; H01L 29/0847; H01L 29/42392; H01L 27/0924; H01L 21/823821; H01L 29/0653; H01L 29/06; H01L 29/0684; H01L 29/0843; H01L 29/0856; H01L 29/0865; H01L 29/0869; H01L 29/0873; H01L 29/0882; H01L 29/0886; H01L 29/66553; H01L 29/6656; H01L 29/7848; H01L 29/66545; H01L 29/66606; H01L 29/66871; H01L 21/823468; H01L 21/823864; B82Y 10/00

See application file for complete search history.

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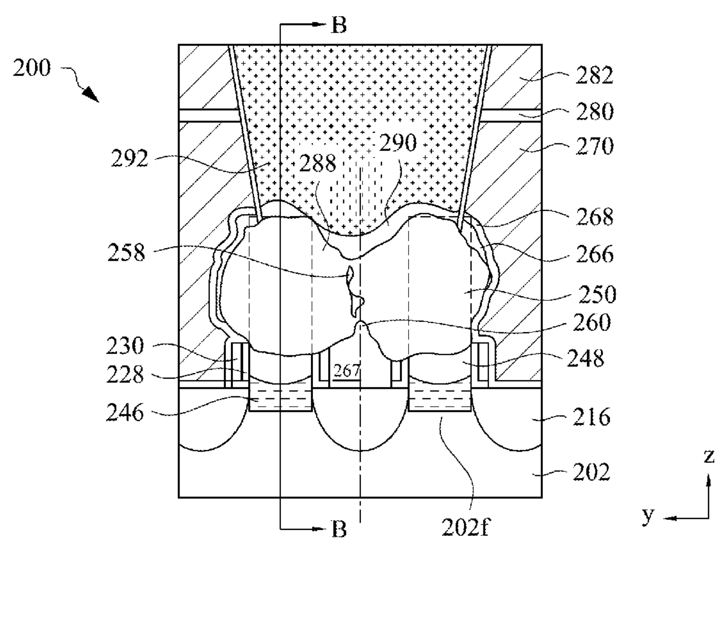
Primary Examiner — Sonya McCall-Shepard
(74) *Attorney, Agent, or Firm* — NZ Carr Law Office

(57) **ABSTRACT**

Embodiments of the present disclosure provide methods for forming merged source/drain features from two or more fin structures. The merged source/drain features according to the present disclosure have a merged portion with an increased height percentage over the overall height of the source/drain feature. The increase height percentage provides an increased landing range for source/drain contact features, therefore, reducing the connection resistance between the source/drain feature and the source/drain contact features. In some embodiments, the emerged source/drain features include one or more voids formed within the merged portion.

20 Claims, 30 Drawing Sheets



(51) **Int. Cl.**

H01L 29/775	(2006.01)
H01L 29/786	(2006.01)
H01L 27/092	(2006.01)
H01L 21/8238	(2006.01)

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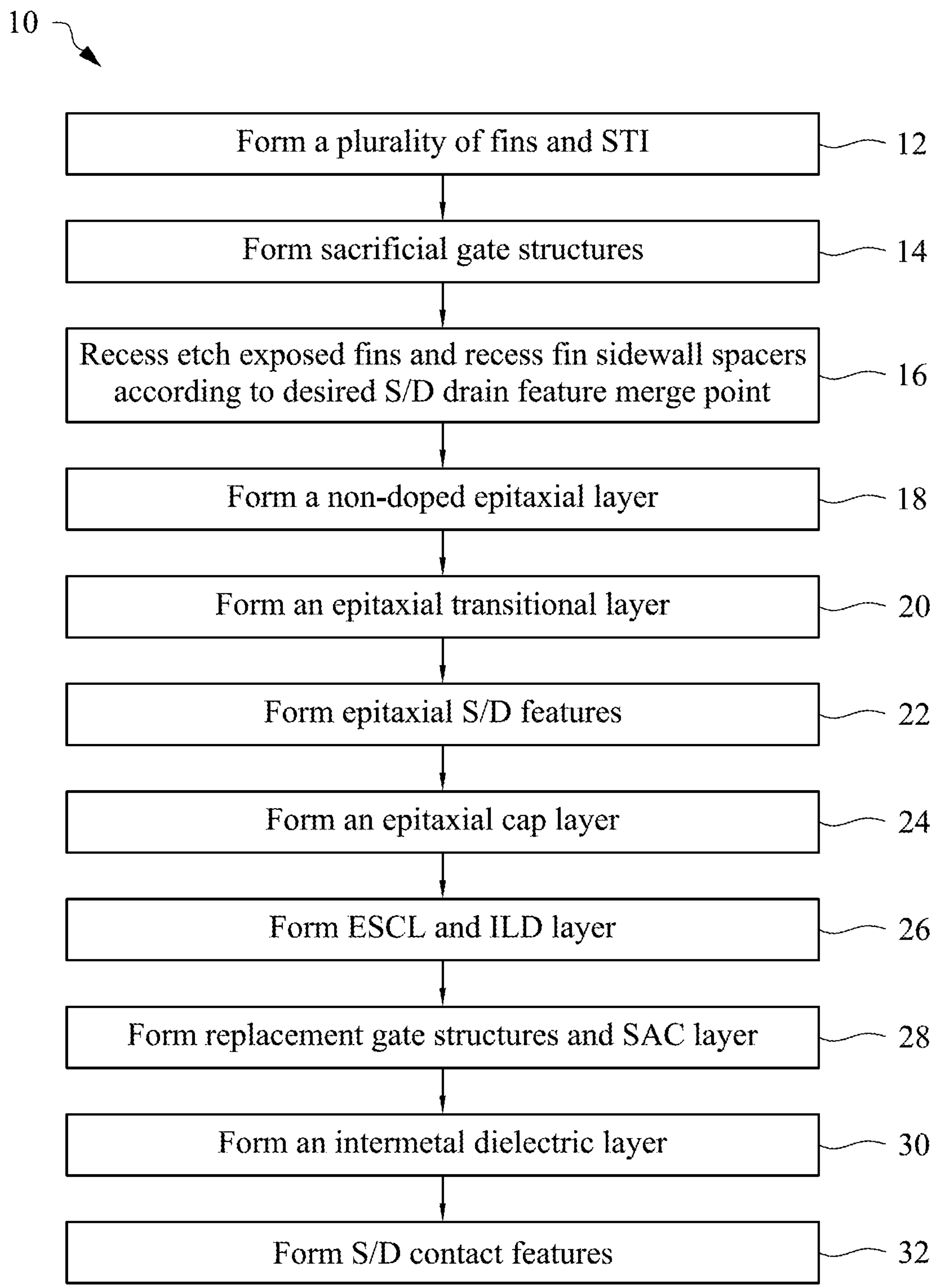
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Form a plurality of fins and STI
12
Form sacrificial gate structures
14
Recess etch exposed fins and recess fin sidewall spacers according to desired S/D drain feature merge point
16
Form a non-doped epitaxial layer
18
Form an epitaxial transitional layer
20
Form epitaxial S/D features
22
Form an epitaxial cap layer
24
Form ESCL and ILD layer
26
Form replacement gate structures and SAC layer
28
Form an intermetal dielectric layer
30
Form S/D contact features
32

Fig. 1A

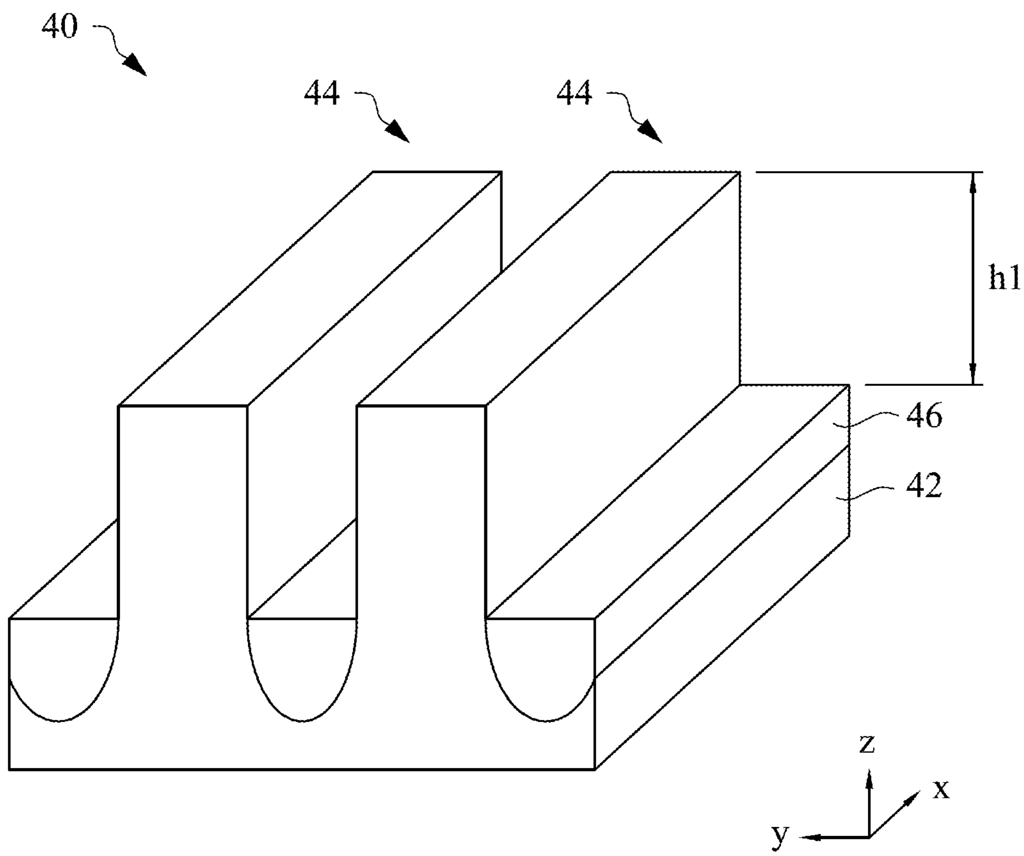
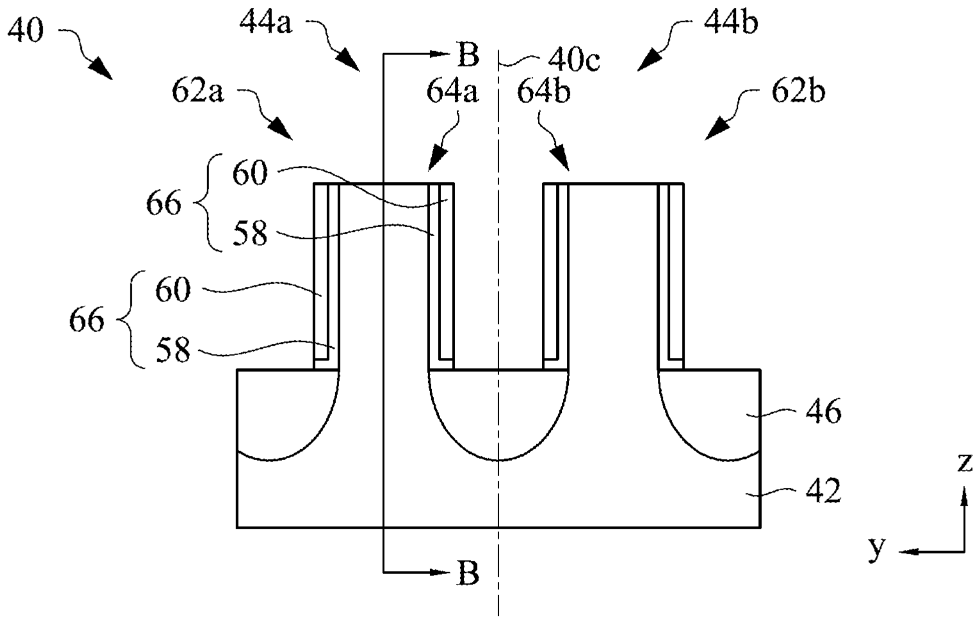


Fig. 1B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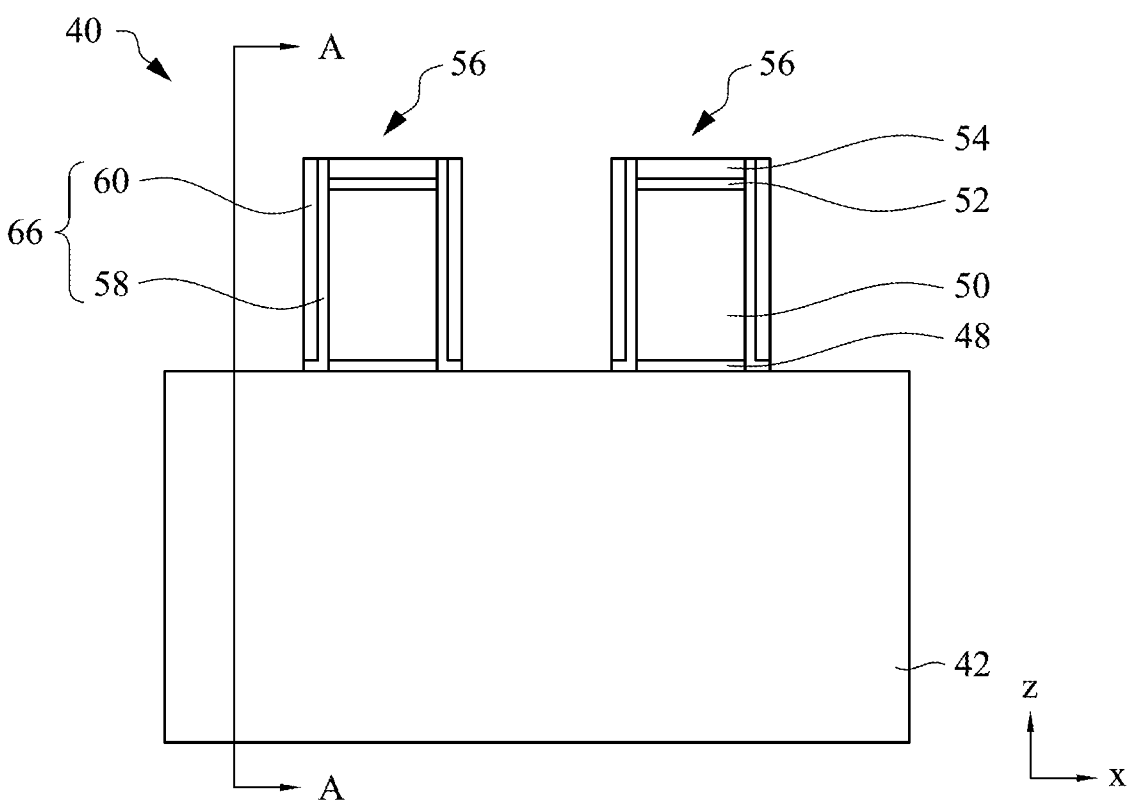
44a
44b
B
40c
62a
64a
64b
62b
60
66
58
60
66
58
46
42
z
y
B

Fig. 1C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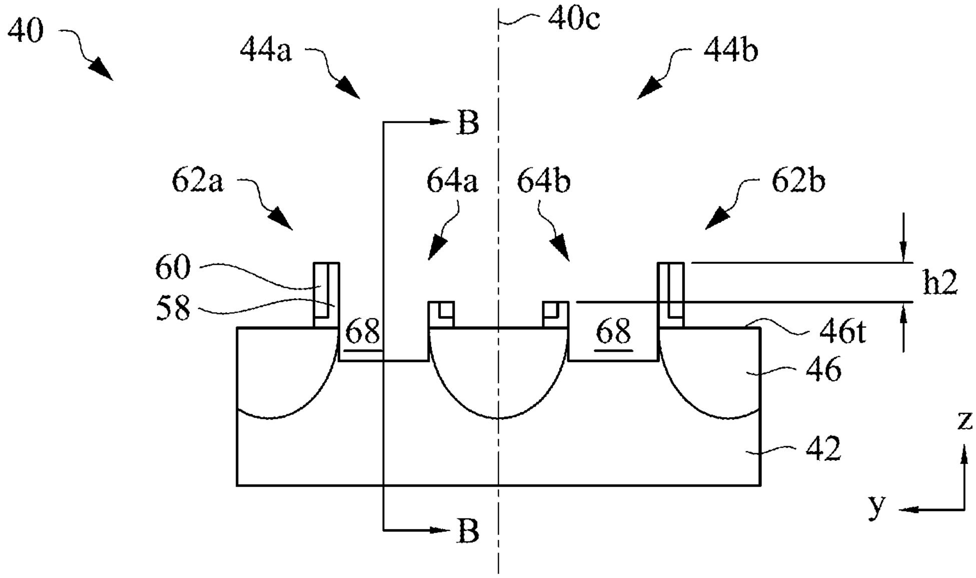
A
56
56
54
60
52
66
58
50
48
42
z
x
A

Fig. 1D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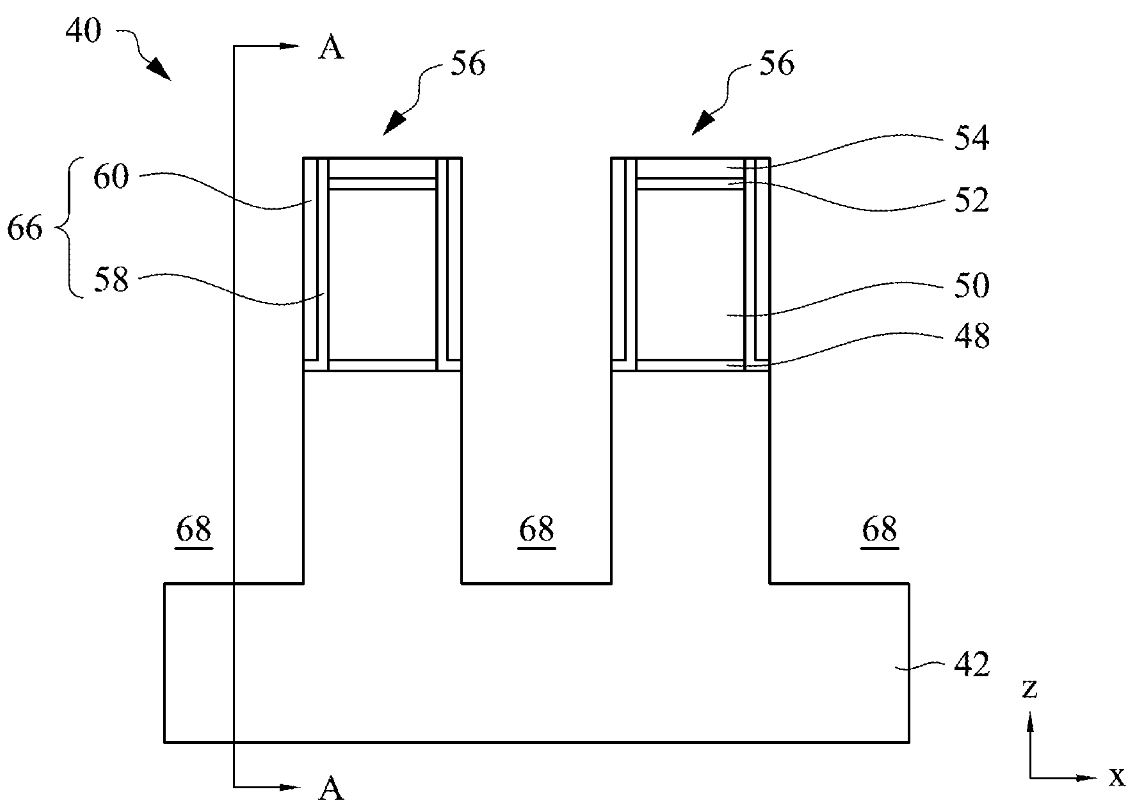
44a
40c
44b
B
62a
64a
64b
62b
60
58
68
68
h2
46t
46
42
z
y
B

Fig. 1E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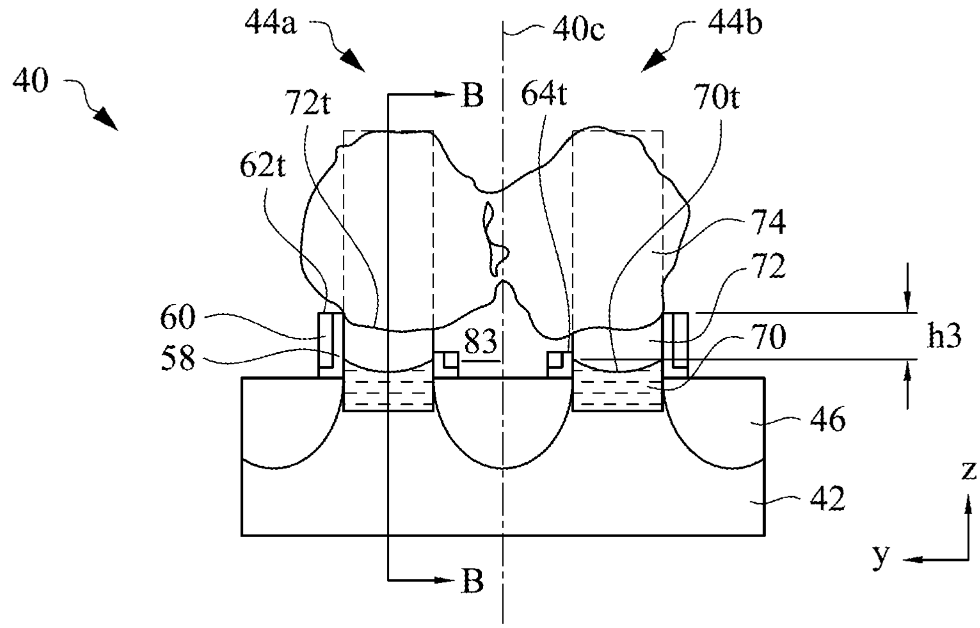
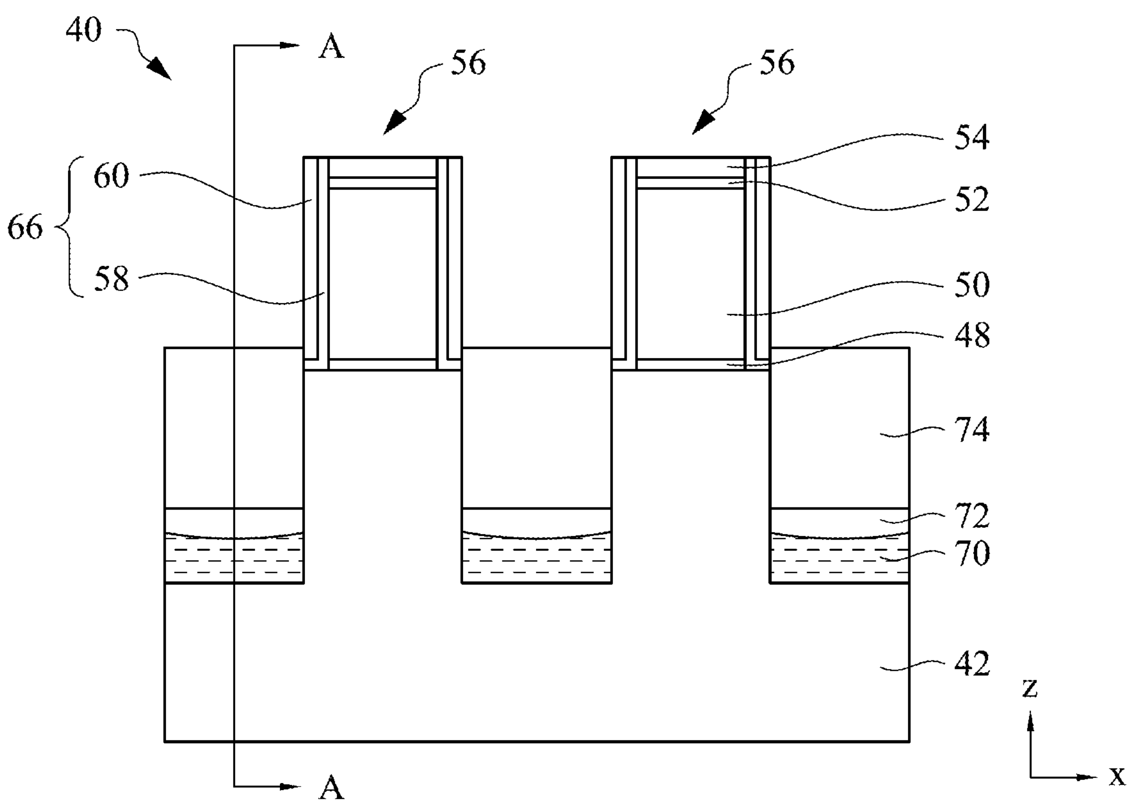
A
56
56
54
60
52
66
58
50
48
68
68
68
42
z
x
A

Fig. 1F



44a
40c
44b
40
72t
B
64t
70t
62t
74
72
60
83
h3
70
58
46
z
42
y
B

Fig. 1G



40
A
56
56
54
60
52
66
58
50
48
74
72
70
42
z
x
A

Fig. 1H

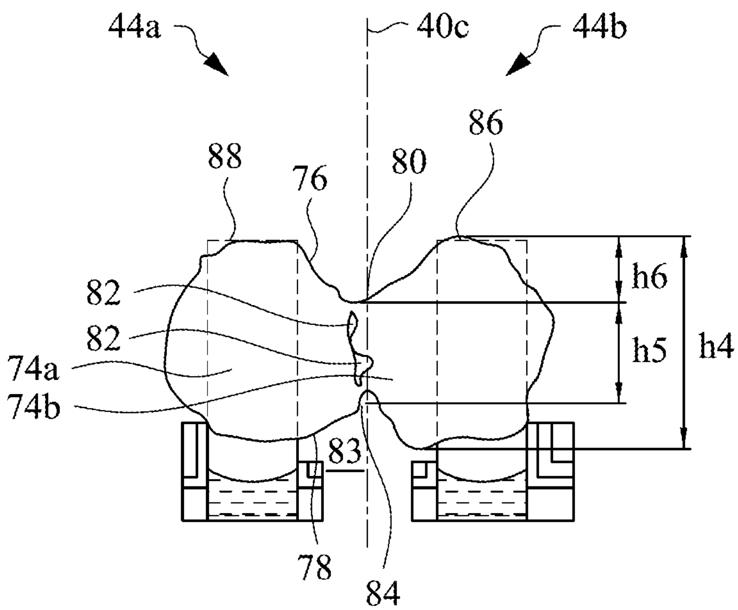


Fig. 1I

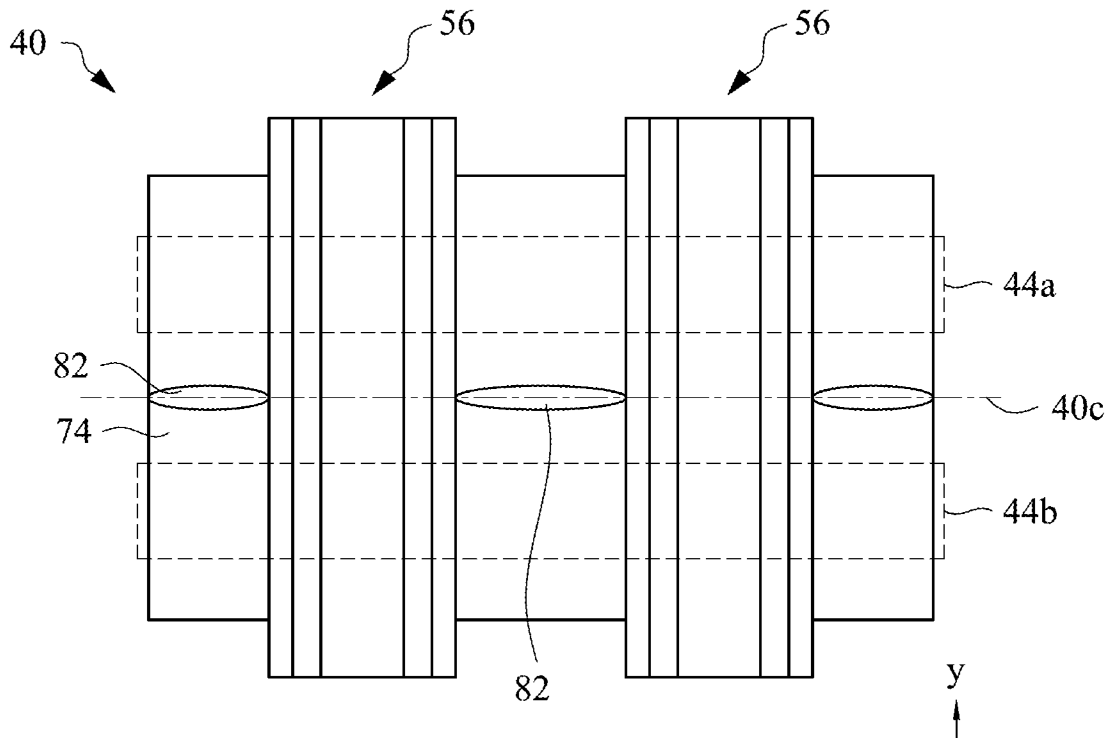
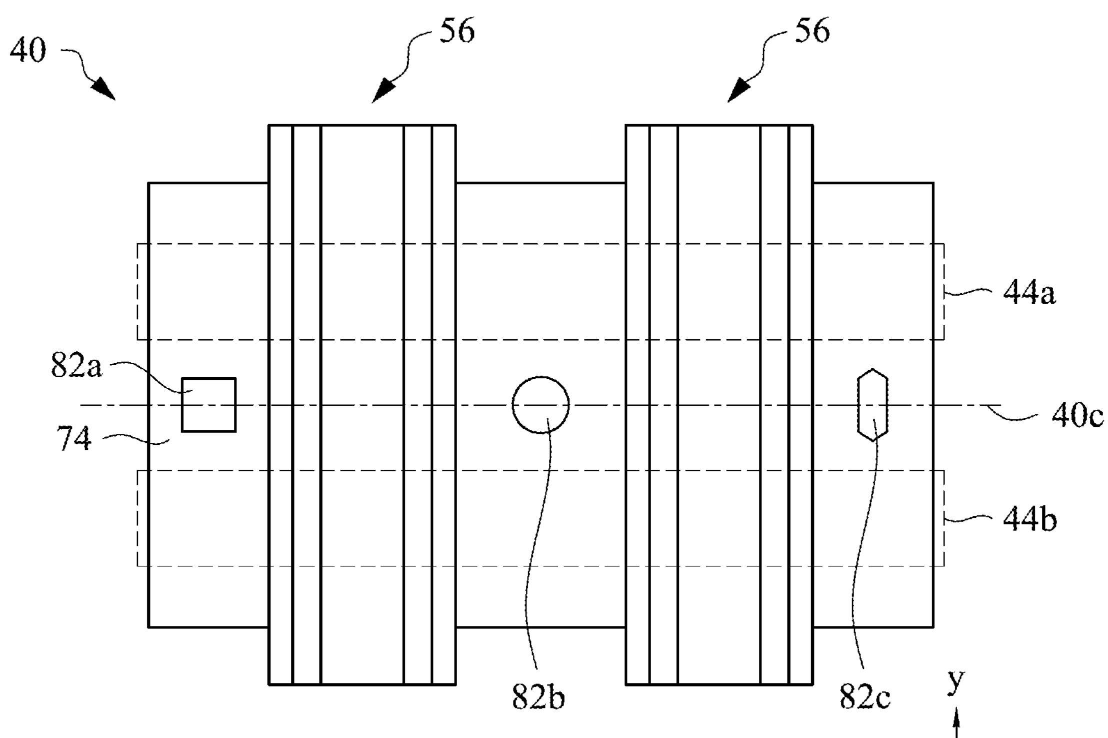

40
56
56
44a
82
74
40c
44b
82
y
x

Fig. 1J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56
56
44a
82a
74
40c
44b
82b
82c
y
x

Fig. 1K

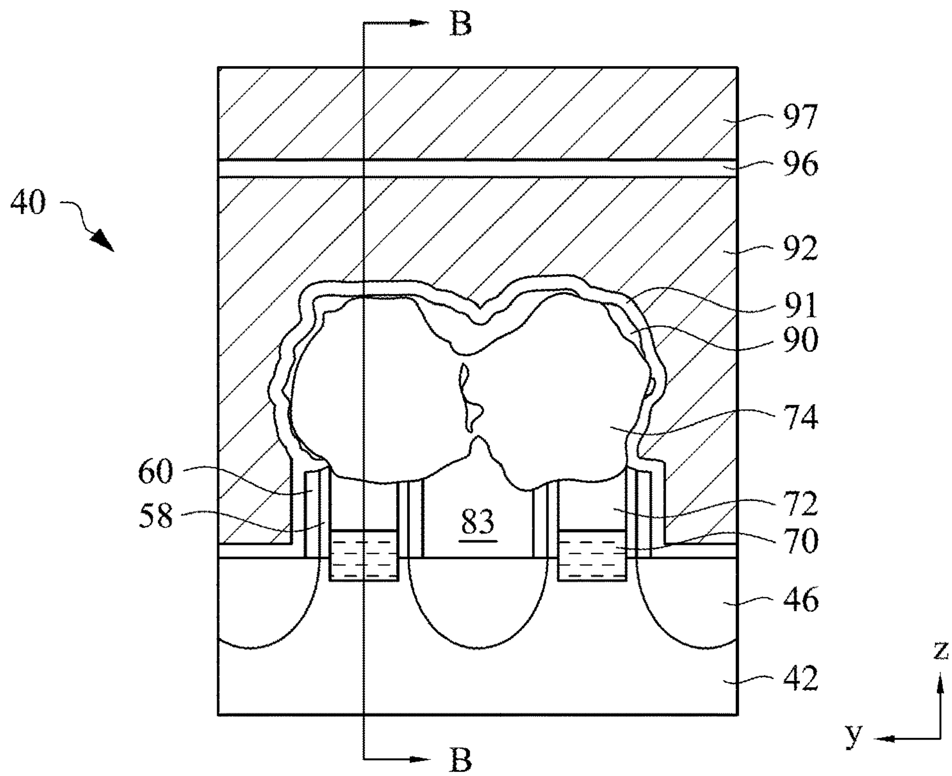

B
97
96
40
92
91
90
74
60
58
83
72
70
46
42
z
y
B

Fig. 1L

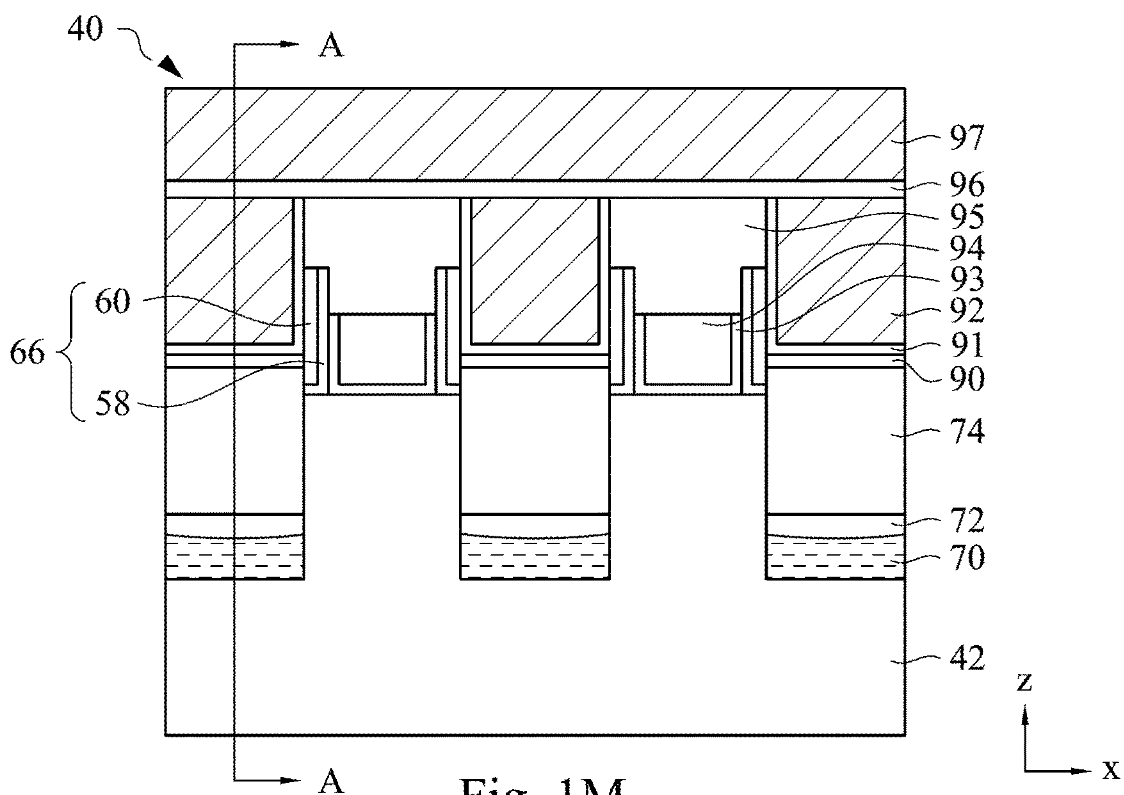
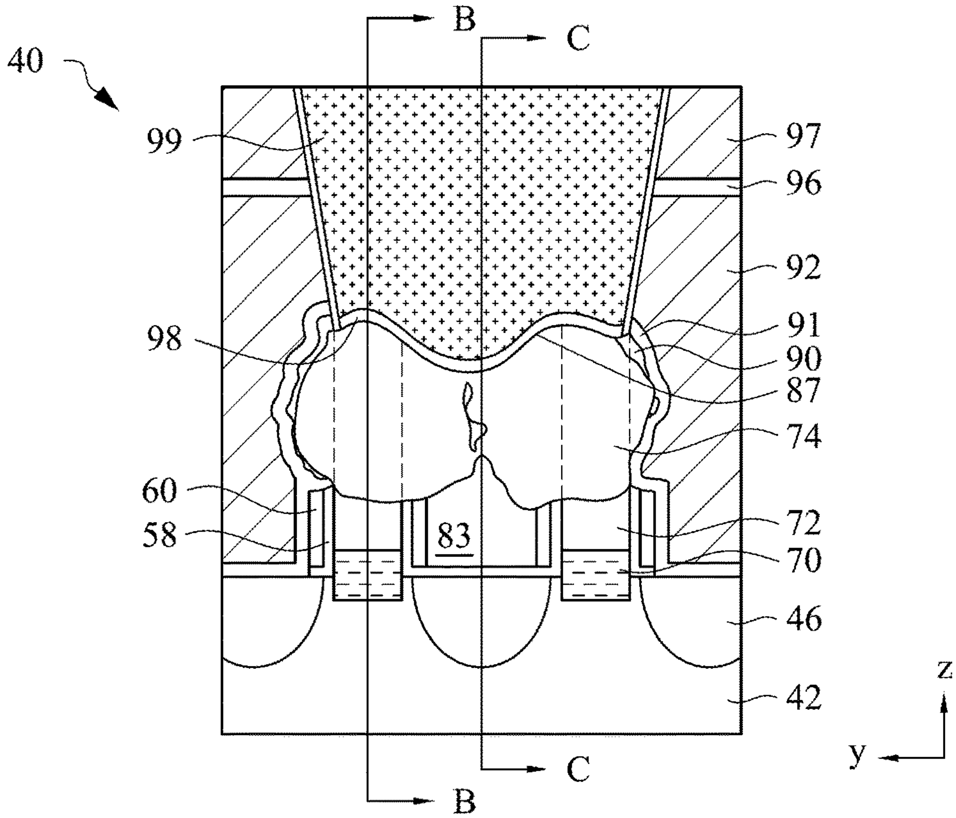
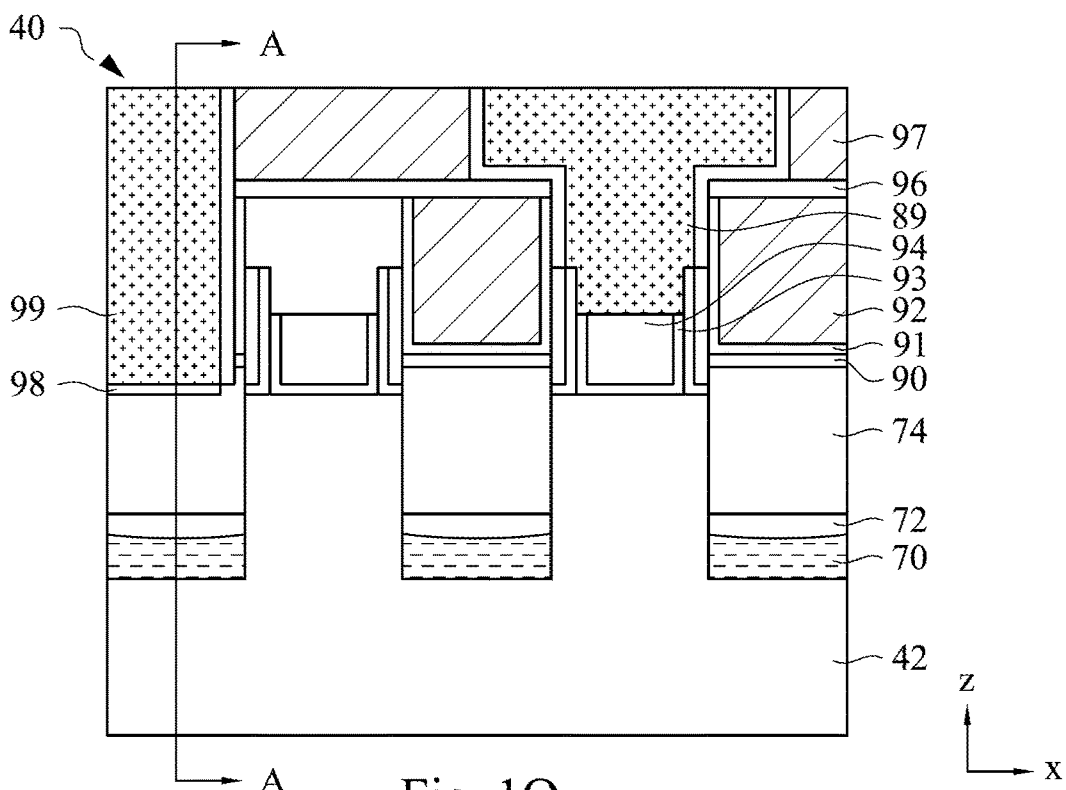

40
A
97
96
95
94
93
60
92
66
91
90
58
74
72
70
42
z
x
A

Fig. 1M



B
C
40
99
97
96
92
98
91
90
87
74
60
58
83
72
70
46
42
z
y
C
B

Fig. 1N



40
A
97
96
89
94
93
92
91
90
99
98
74
72
70
42
z
x
A

Fig. 1O

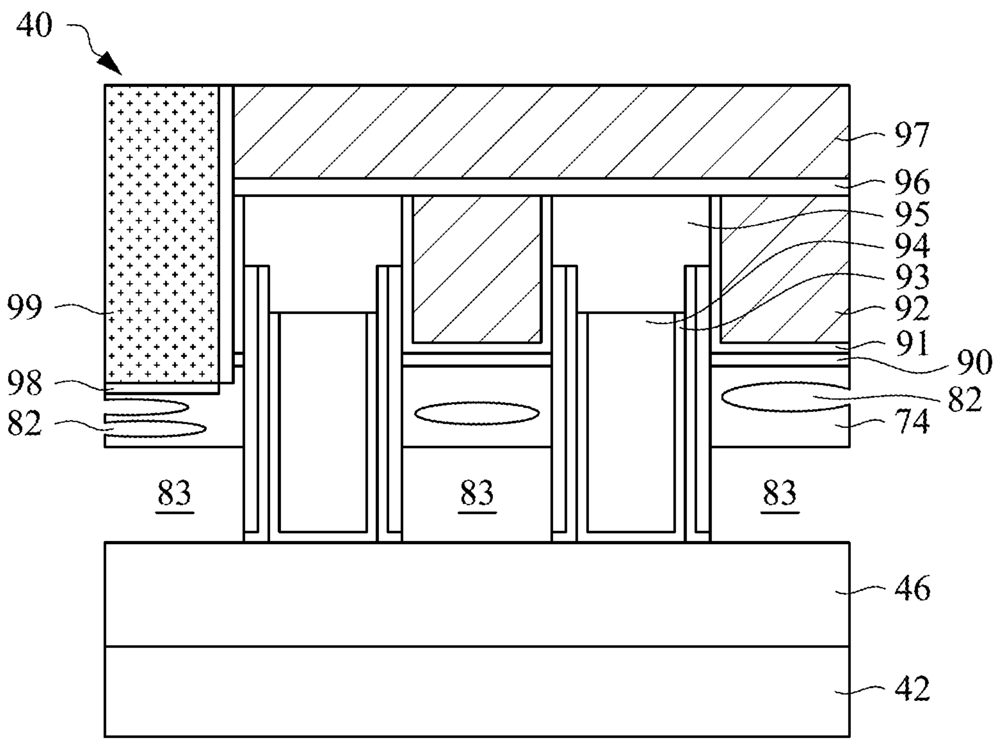


Fig. 1P

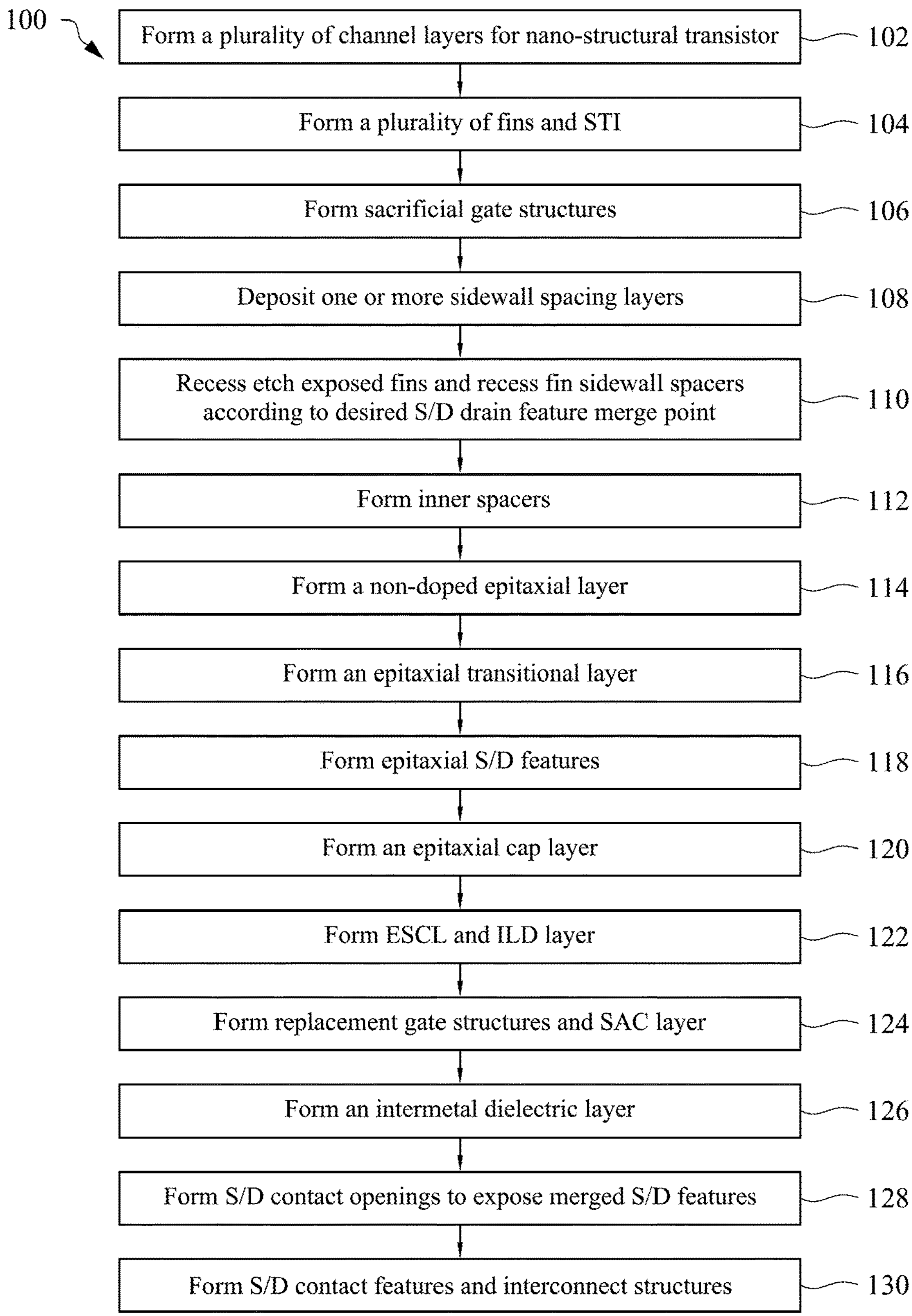

100
Form a plurality of channel layers for nano-structural transistor
102
Form a plurality of fins and STI
104
Form sacrificial gate structures
106
Deposit one or more sidewall spacing layers
108
Recess etch exposed fins and recess fin sidewall spacers according to desired S/D drain feature merge point
110
Form inner spacers
112
Form a non-doped epitaxial layer
114
Form an epitaxial transitional layer
116
Form epitaxial S/D features
118
Form an epitaxial cap layer
120
Form ESCL and ILD layer
122
Form replacement gate structures and SAC layer
124
Form an intermetal dielectric layer
126
Form S/D contact openings to expose merged S/D features
128
Form S/D contact features and interconnect structures
130

Fig. 2

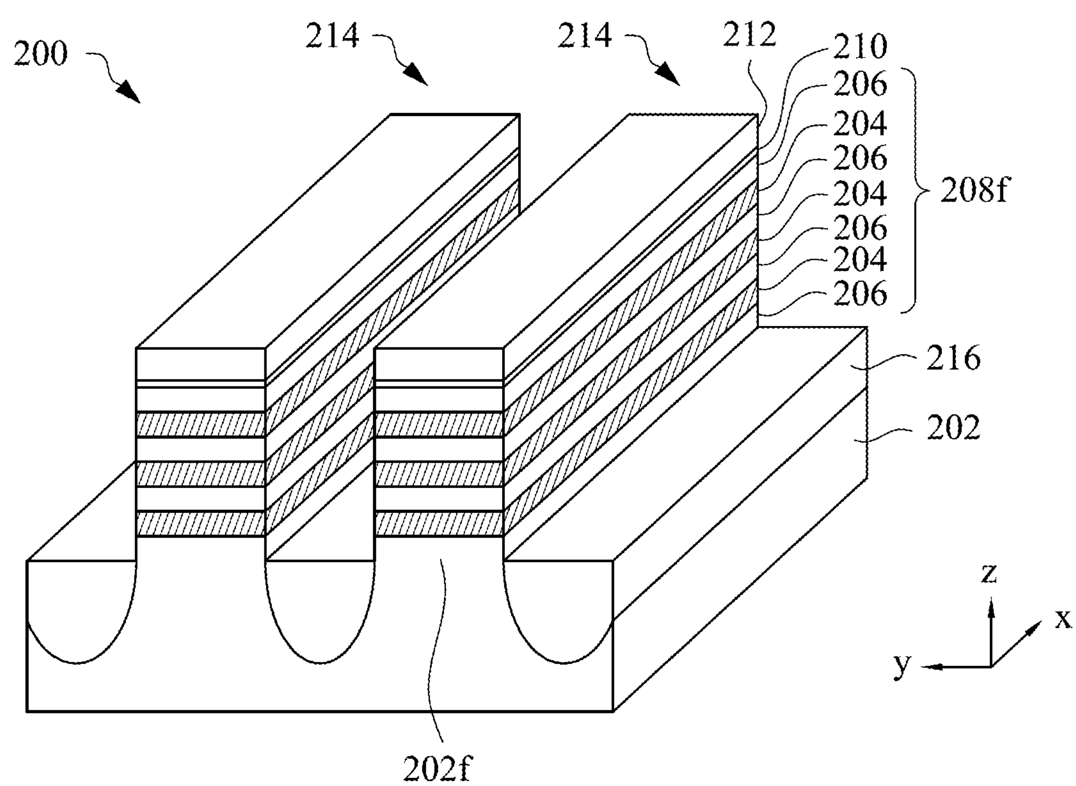

200
214
214
212
210
206
204
206
204
206
204
206
208f
216
202
202f
z
x
y

Fig. 3

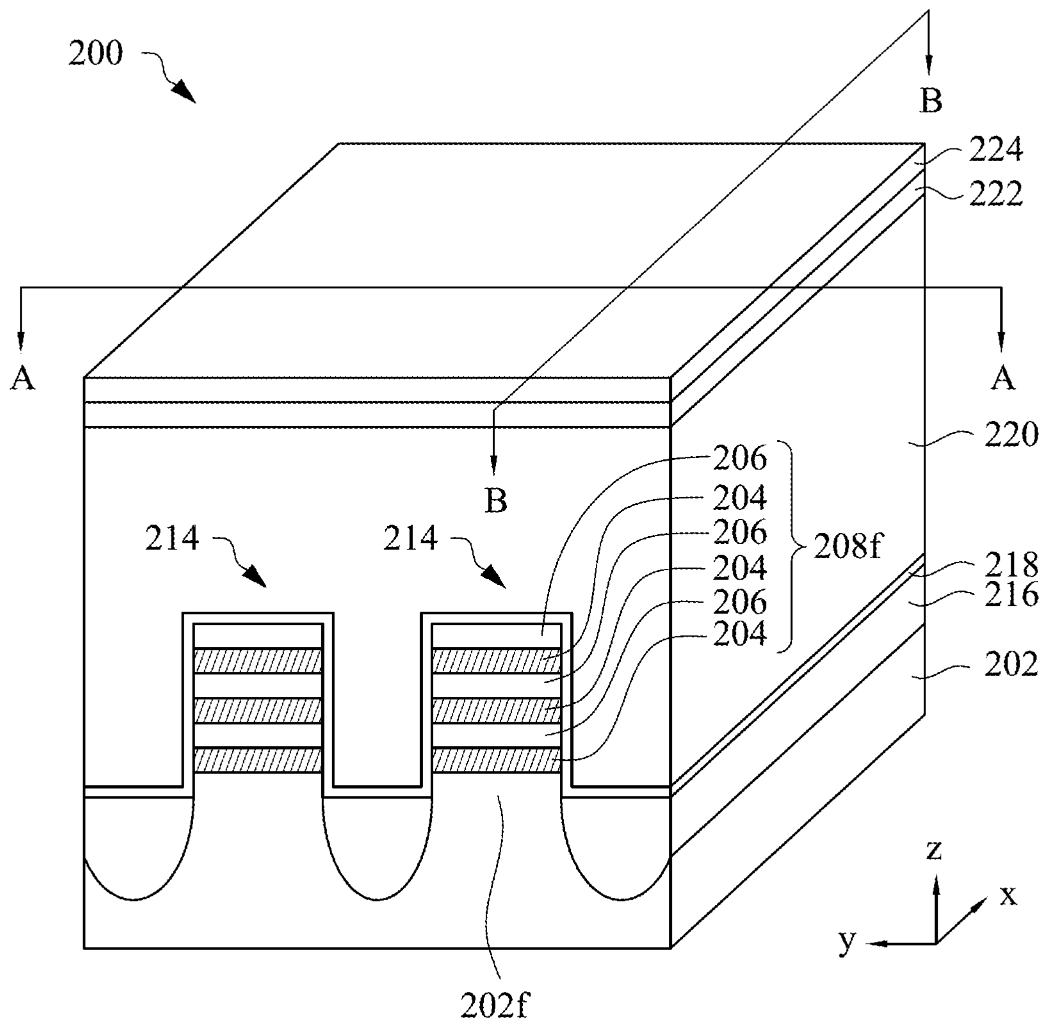

200
B
224
222
A
A
220
206
204
206
204
206
204
208f
B
214
214
218
216
202
z
x
y
202f

Fig. 4

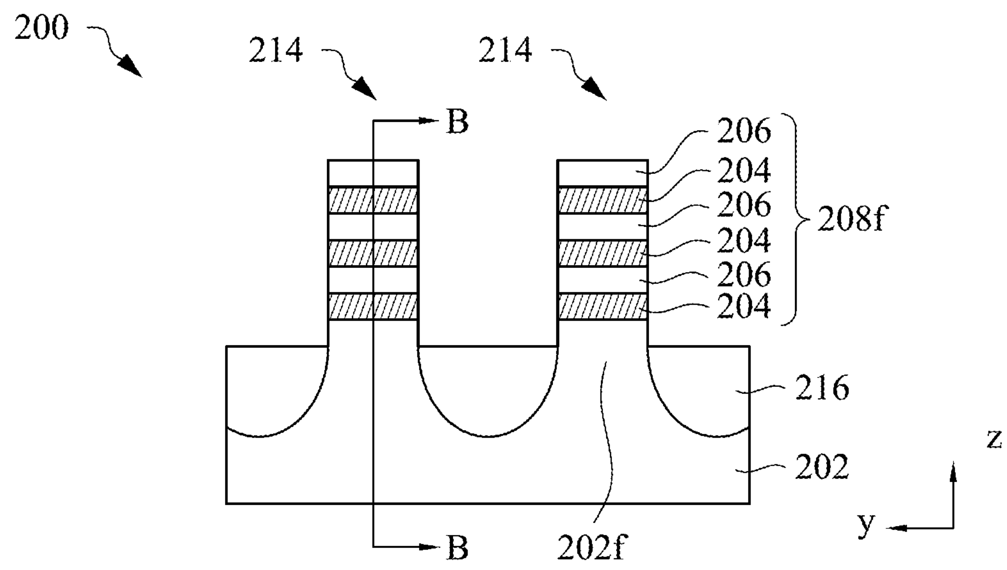

200
214
214
B
206
204
206
204
206
204
208f
216
202
z
y
B
202f

Fig. 5A

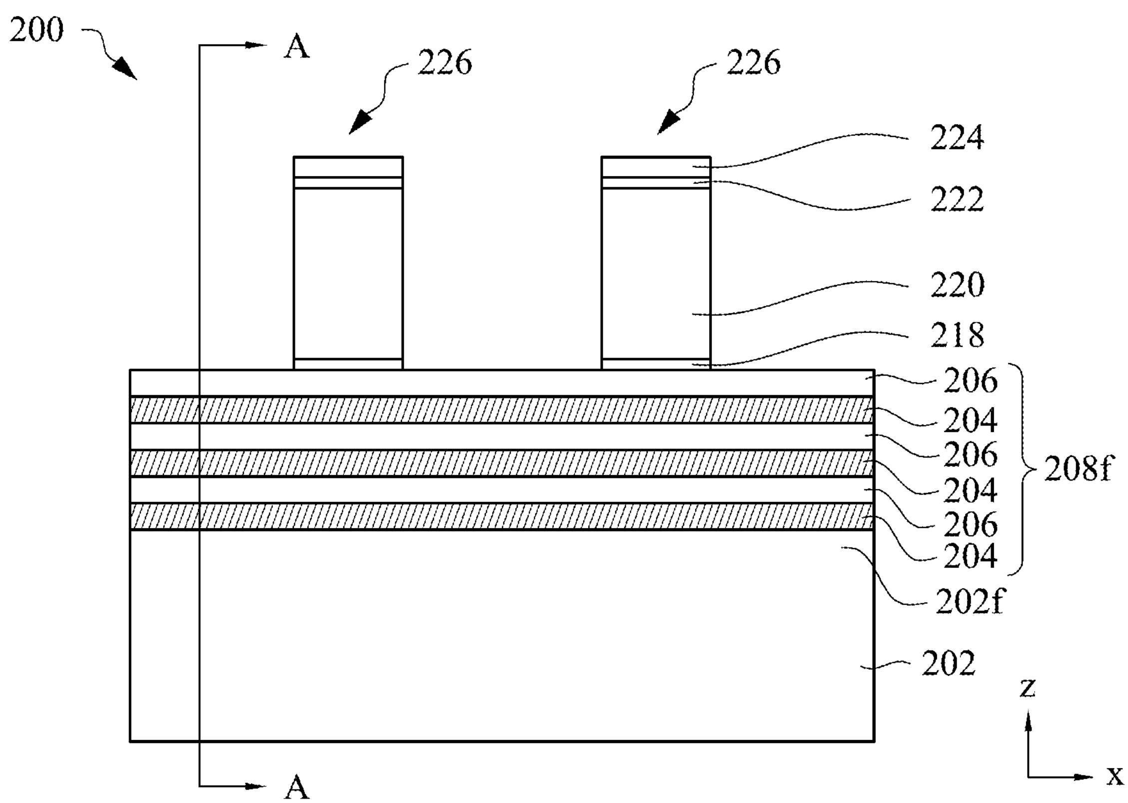

200
A
226
226
224
222
220
218
206
204
206
204
206
204
208f
202f
202
z
x
A

Fig. 5B

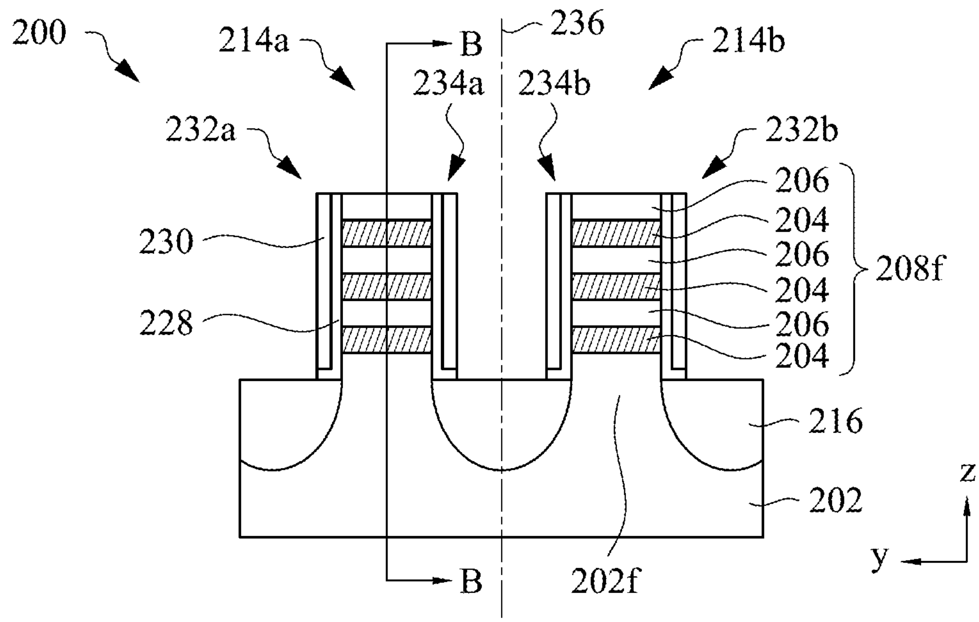
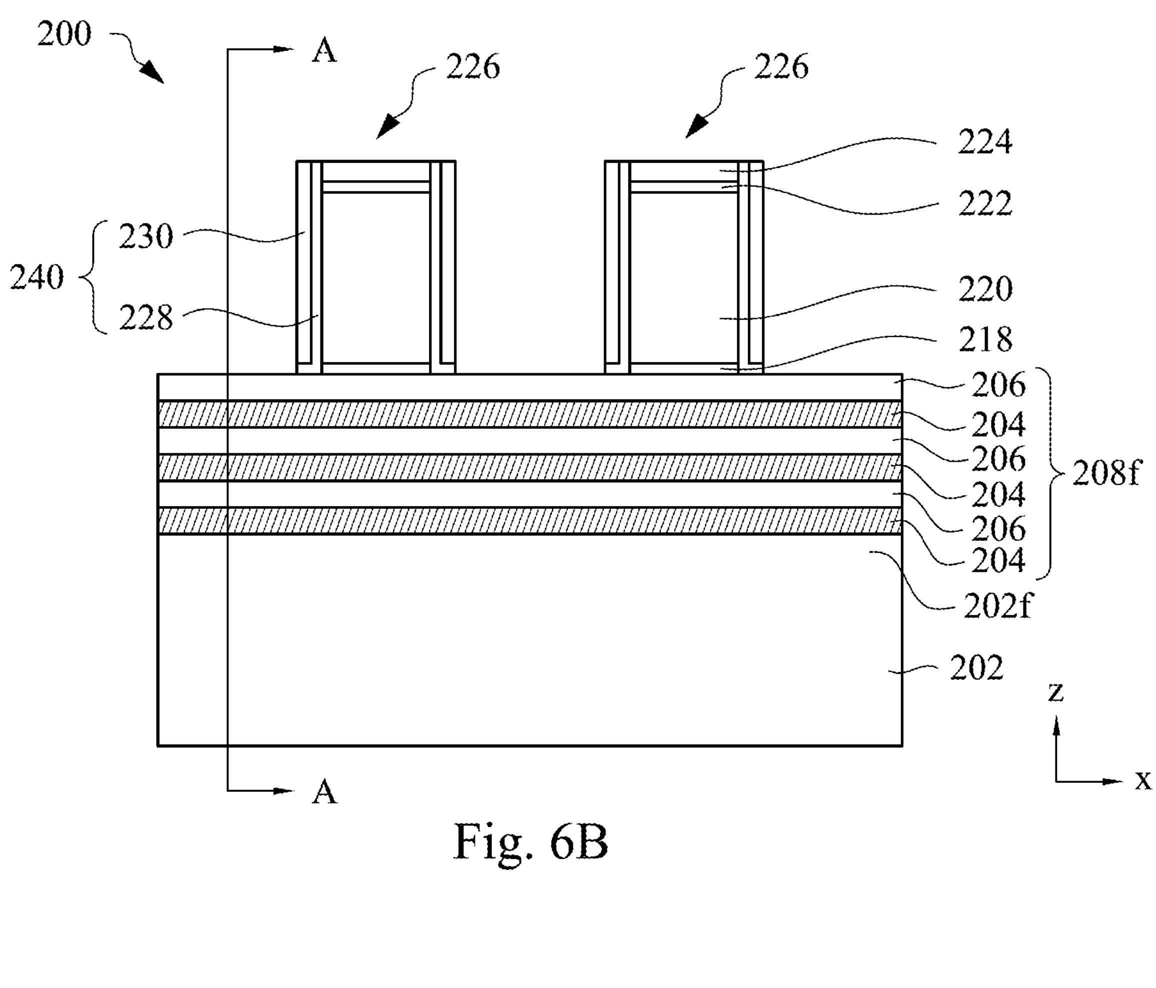

200
214a
B
236
214b
234a
234b
232a
232b
206
204
206
204
206
204
208f
230
228
216
202
202f
B
z
y

Fig. 6A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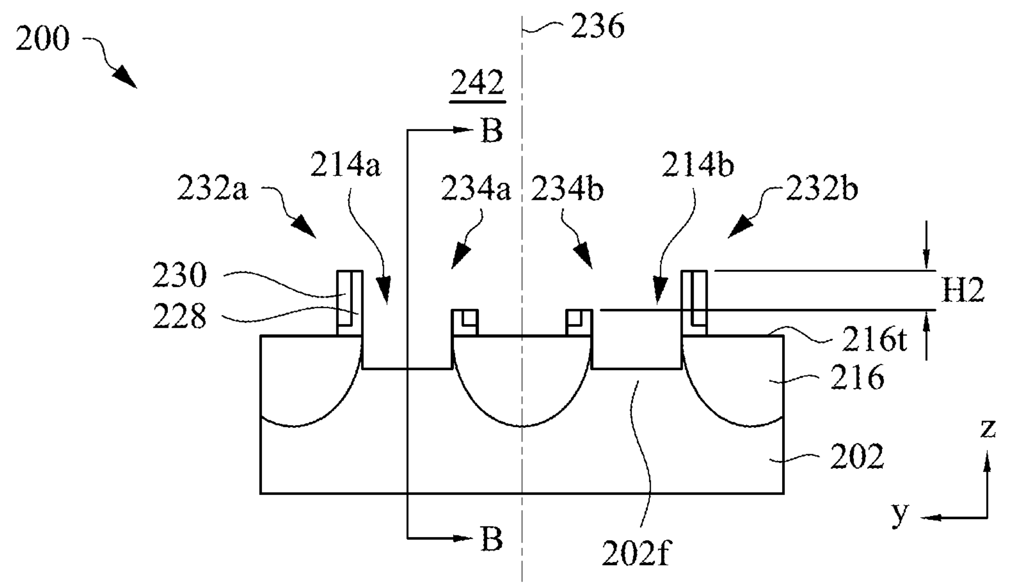
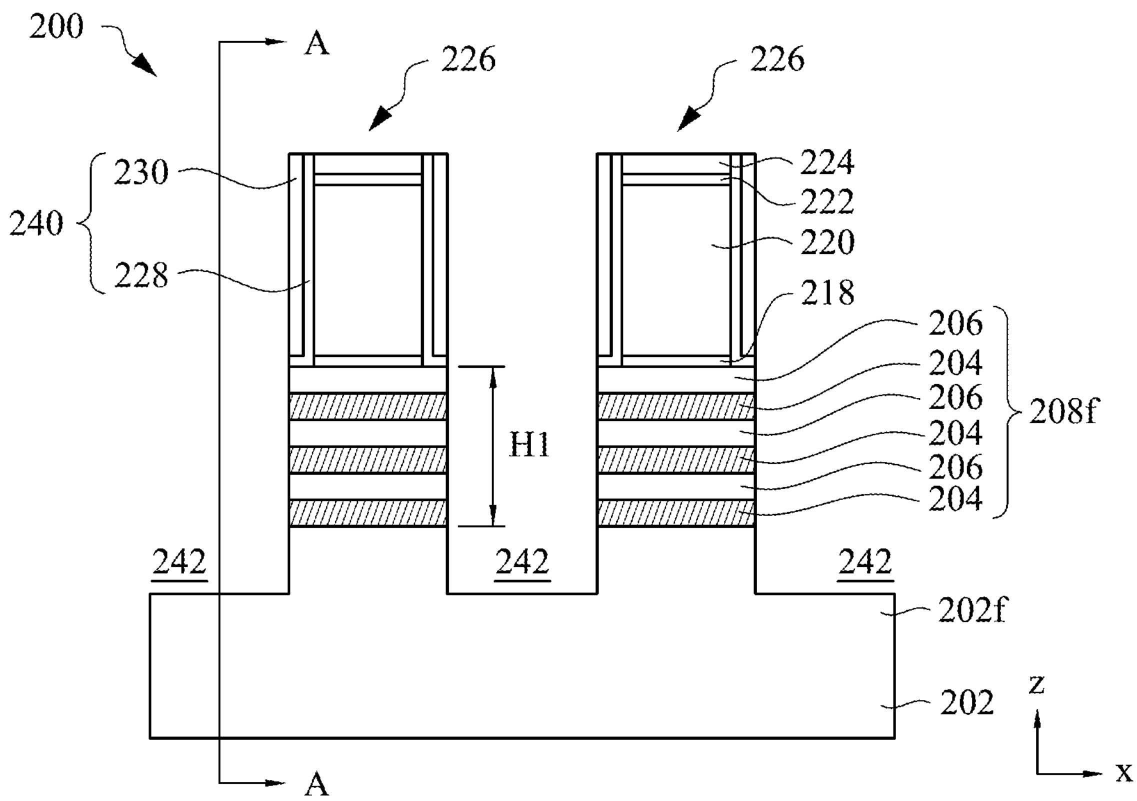
A
226
226
224
222
230
240
228
220
218
206
204
206
204
206
204
208f
202f
202
z
x
A

Fig. 6B



200
236
242
B
214a
214b
232a
234a
234b
232b
230
228
H2
216t
216
202
z
y
B
202f

Fig. 7A



200
A
226
226
230
224
222
240
220
228
218
206
204
206
208f
H1
204
206
204
242
242
242
202f
202
z
x
A

Fig. 7B

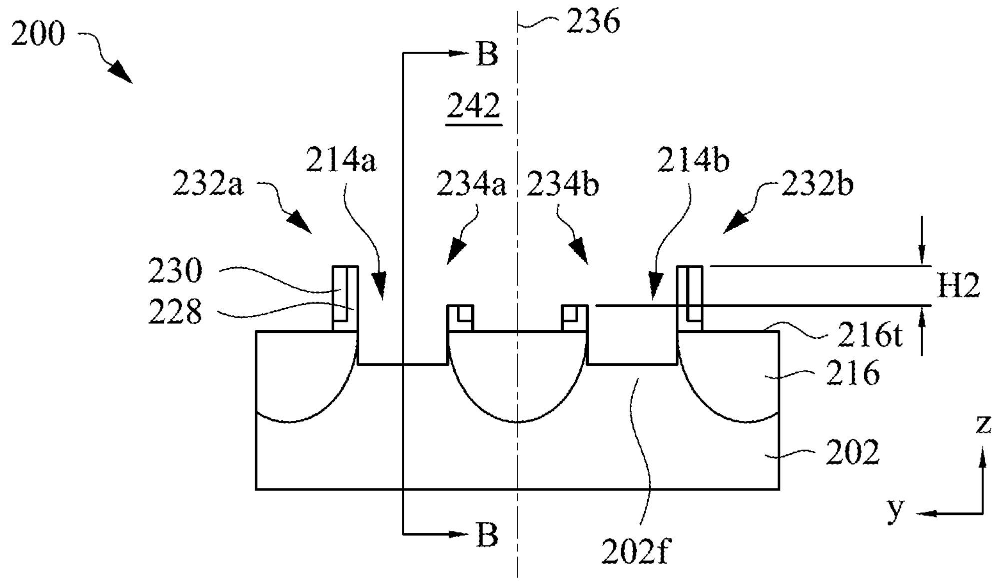

200
236
B
242
214a
214b
232a
234a
234b
232b
230
228
H2
216t
216
202
z
y
B
202f

Fig. 8A

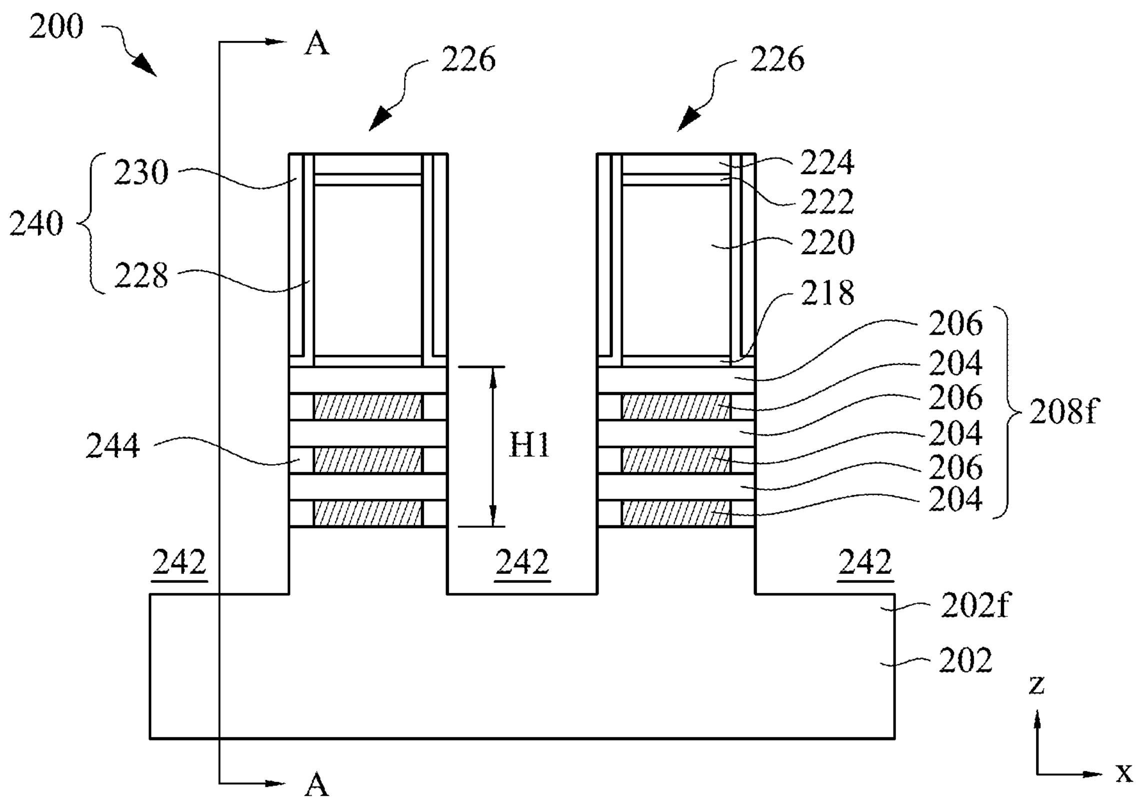
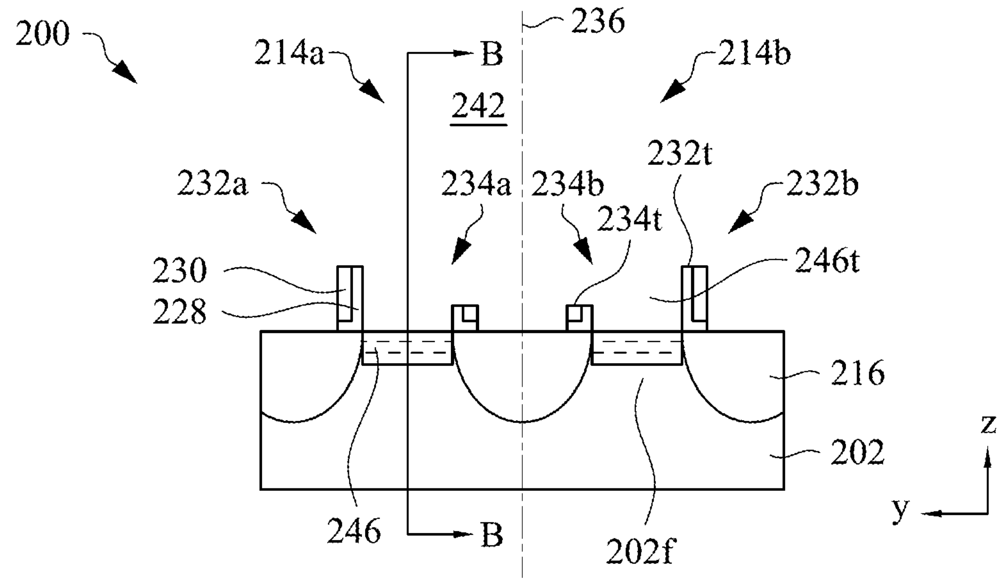

200
A
226
226
230
224
222
240
220
228
218
206
204
206
208f
244
H1
204
206
204
242
242
242
202f
202
z
x
A

Fig. 8B


200
214a
B
236
242
214b
232a
234a
234b
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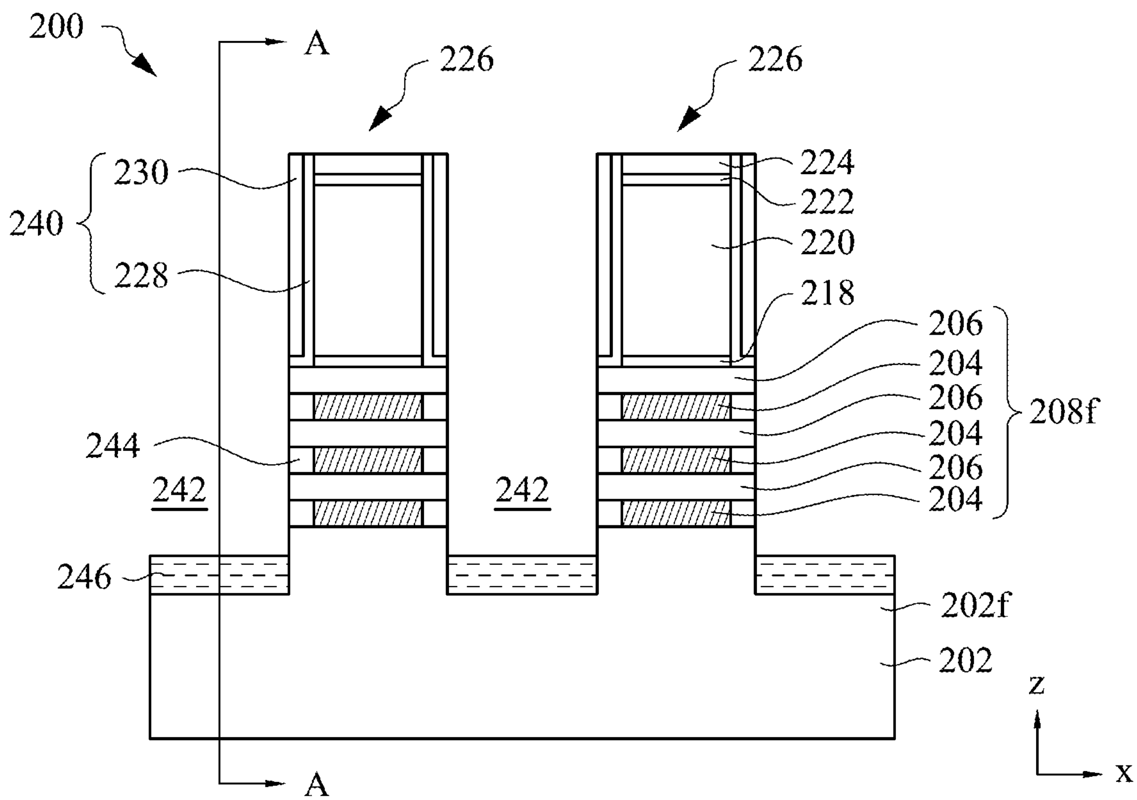
232b
234t
246t
230
228
216
202
z
y
246
B
202f

Fig. 9A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A
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226
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222
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208f
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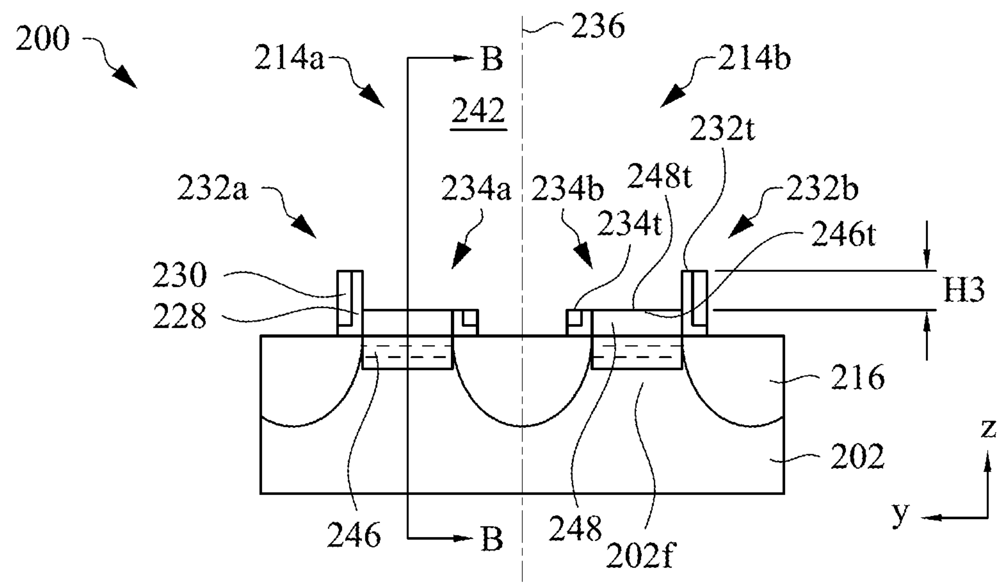
242
242
204
246
202f
202
z
x
A

Fig. 9B



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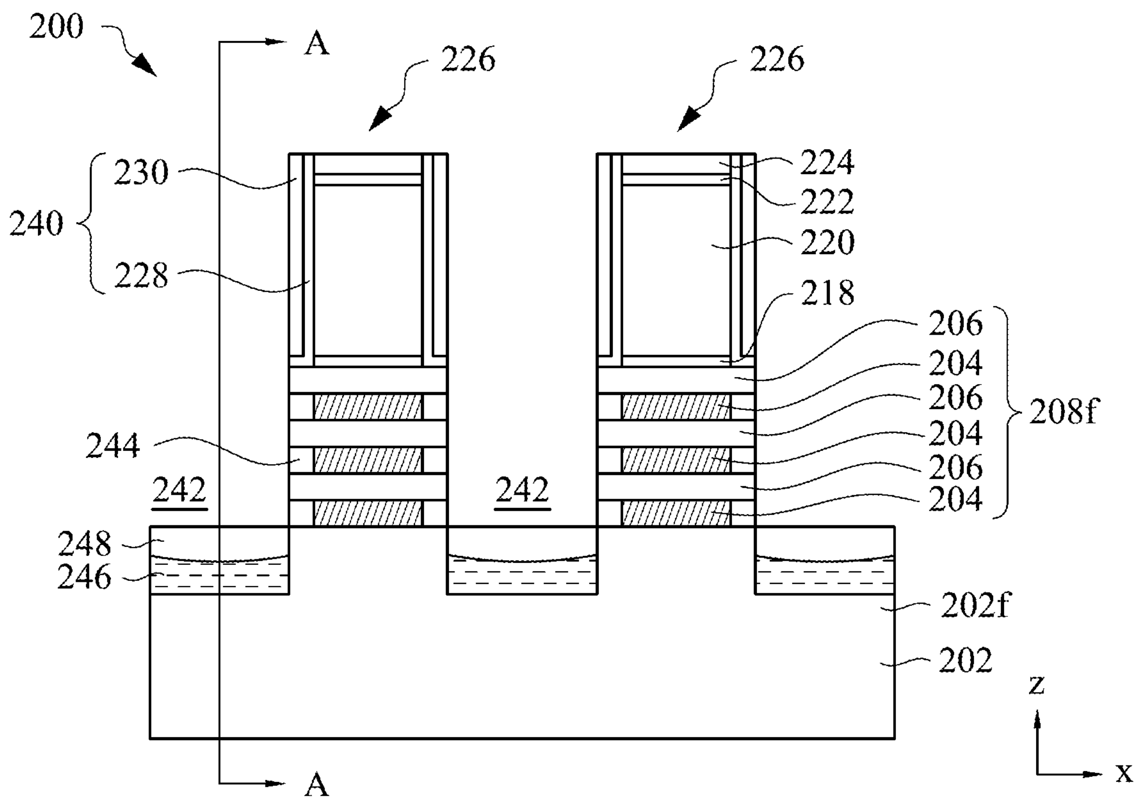

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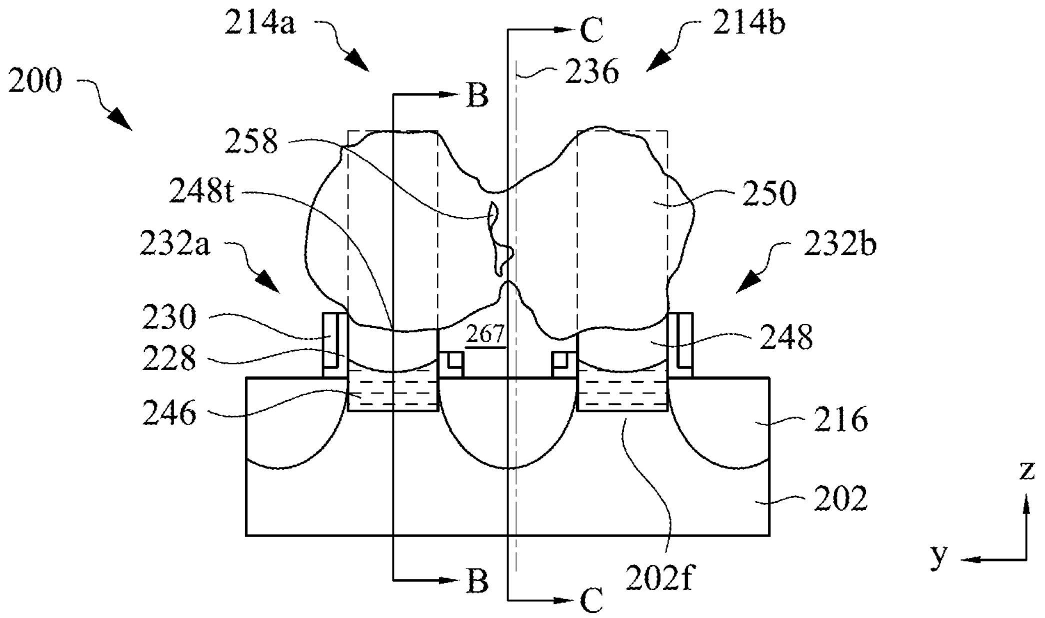


Fig. 11A

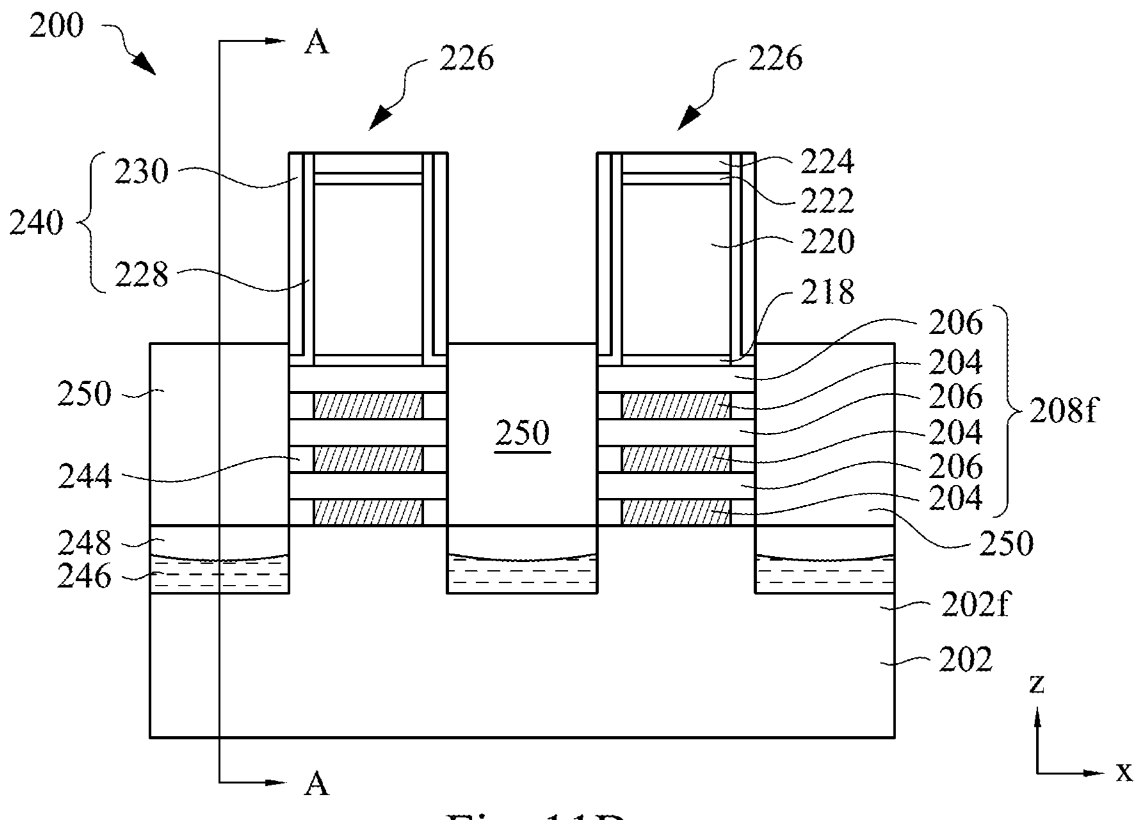


Fig. 11B

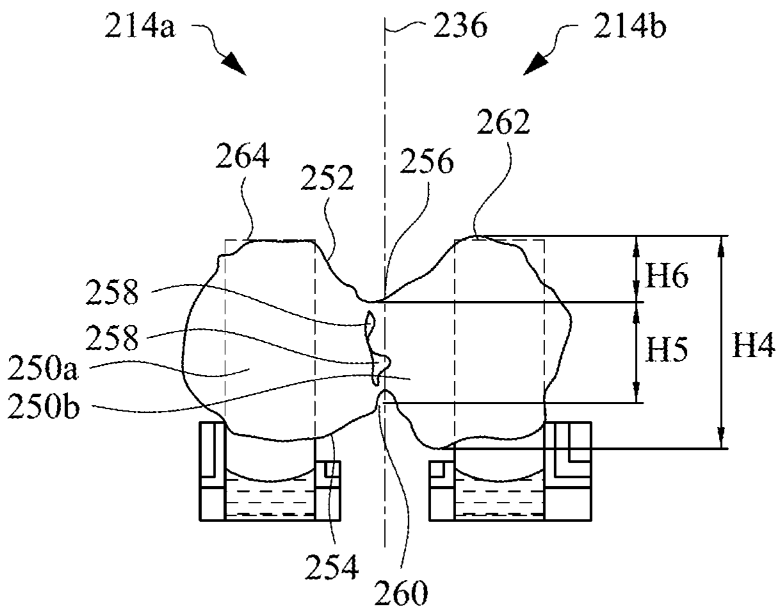


Fig. 11C

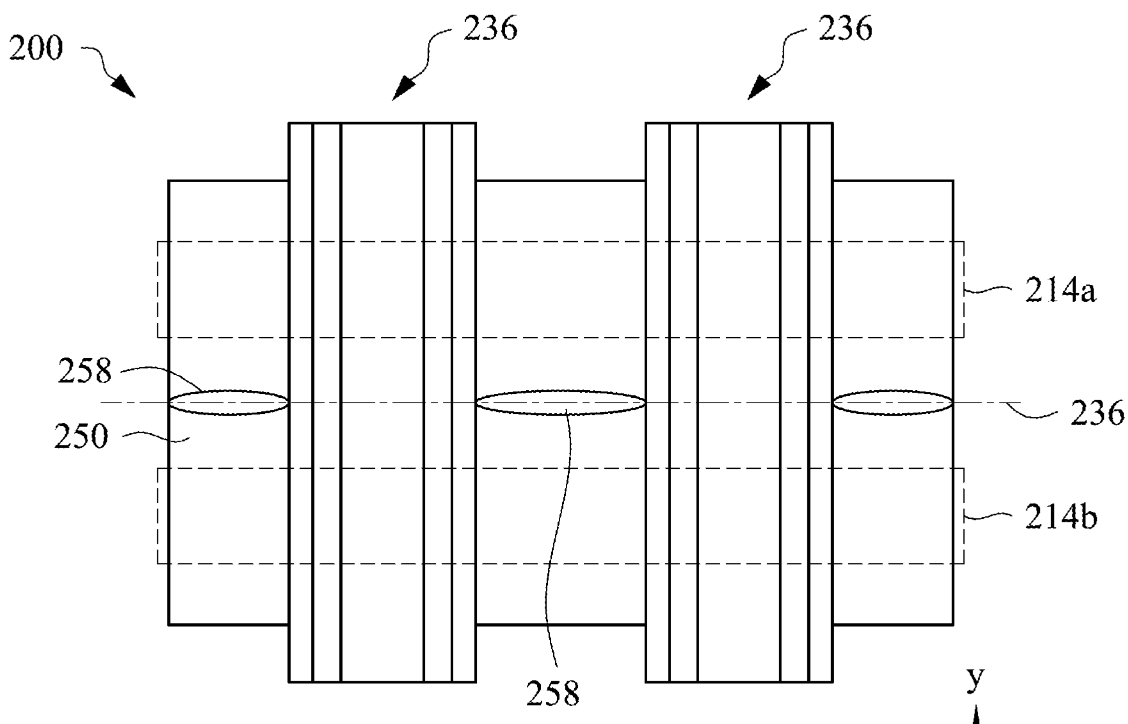


Fig. 11D

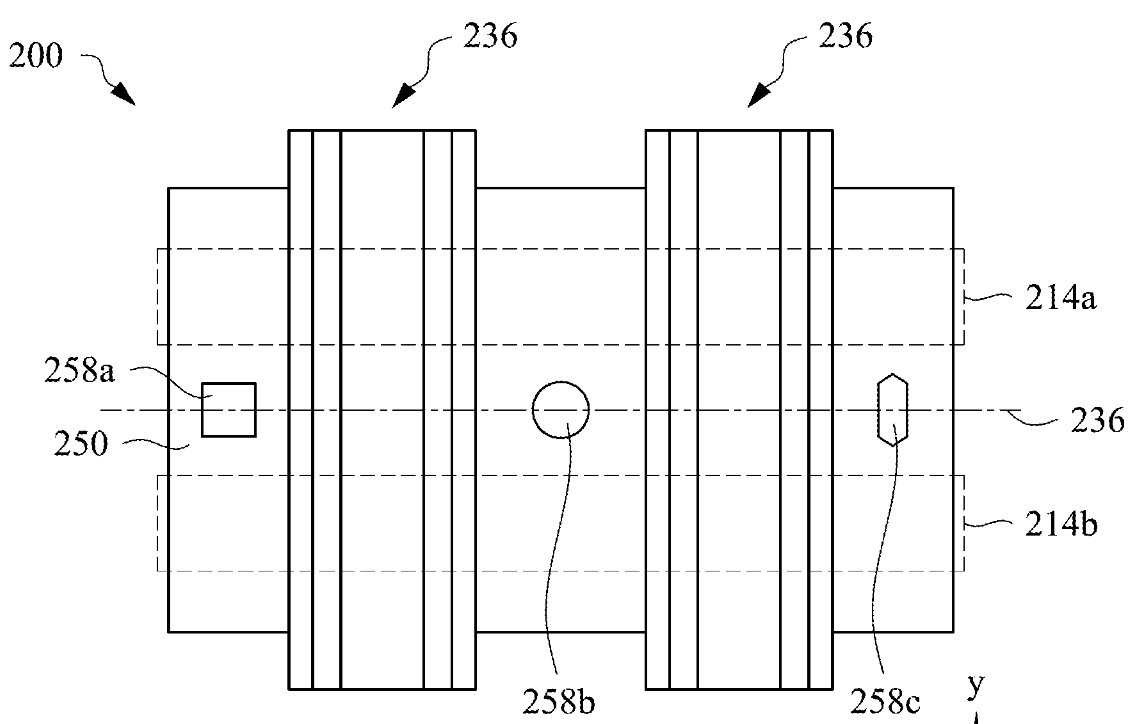


Fig. 11E

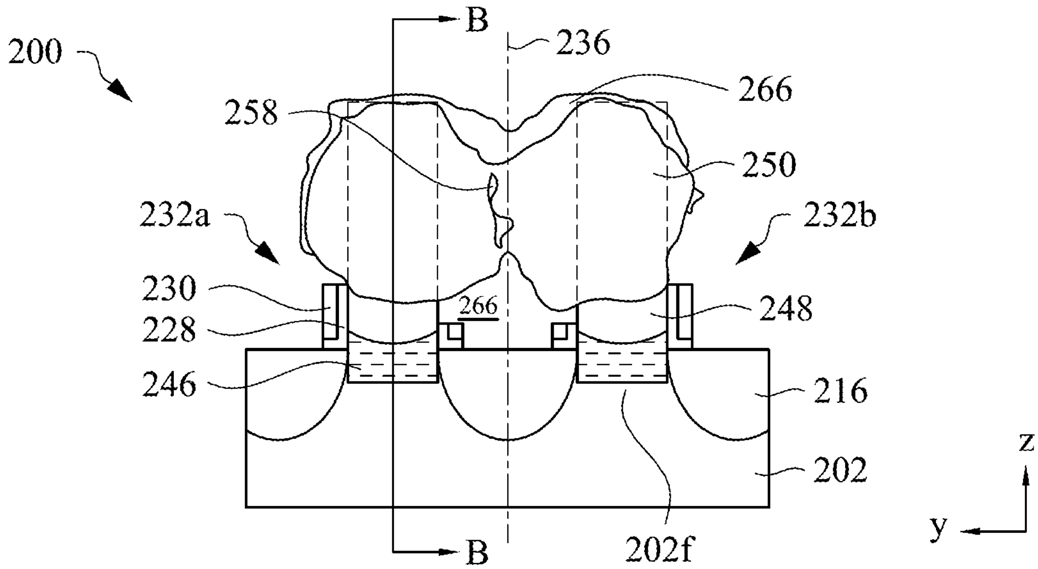
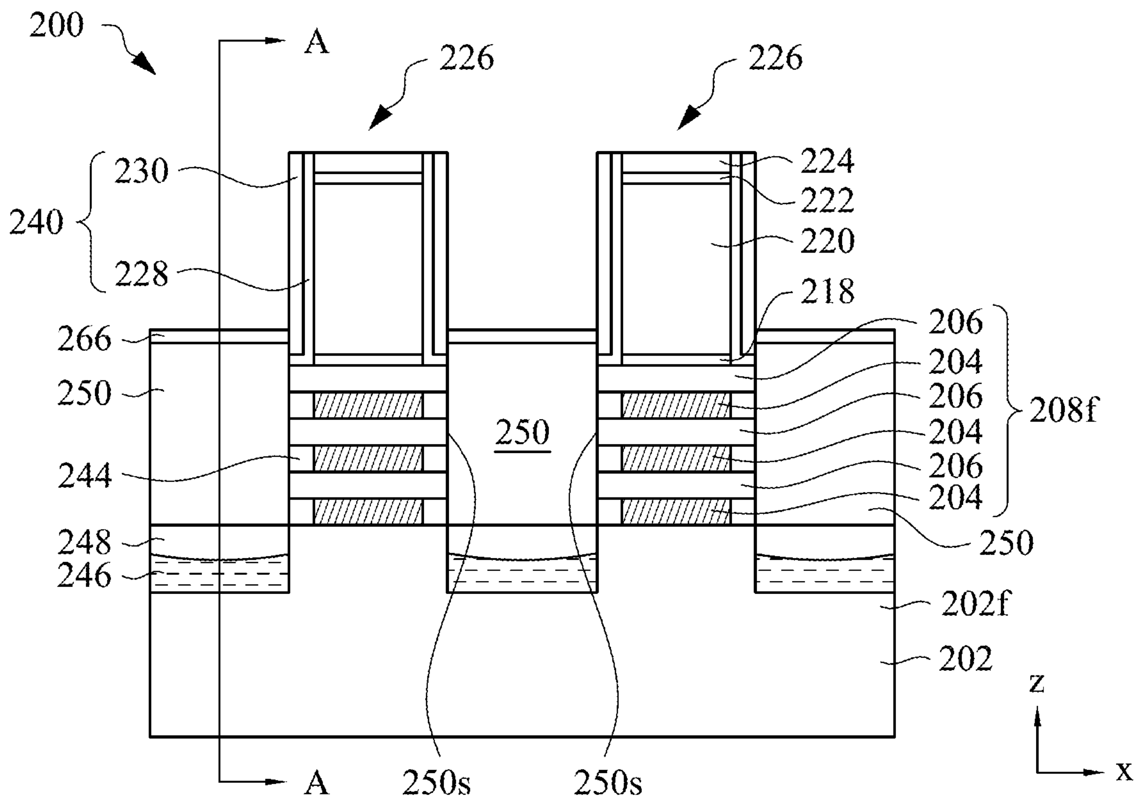


Fig. 12A



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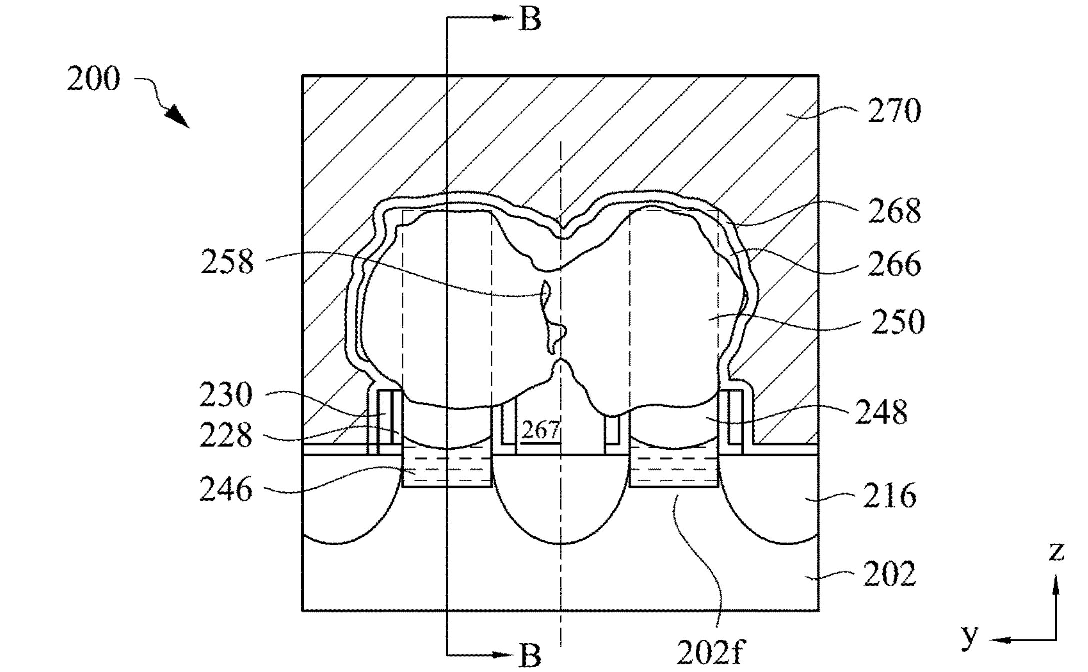

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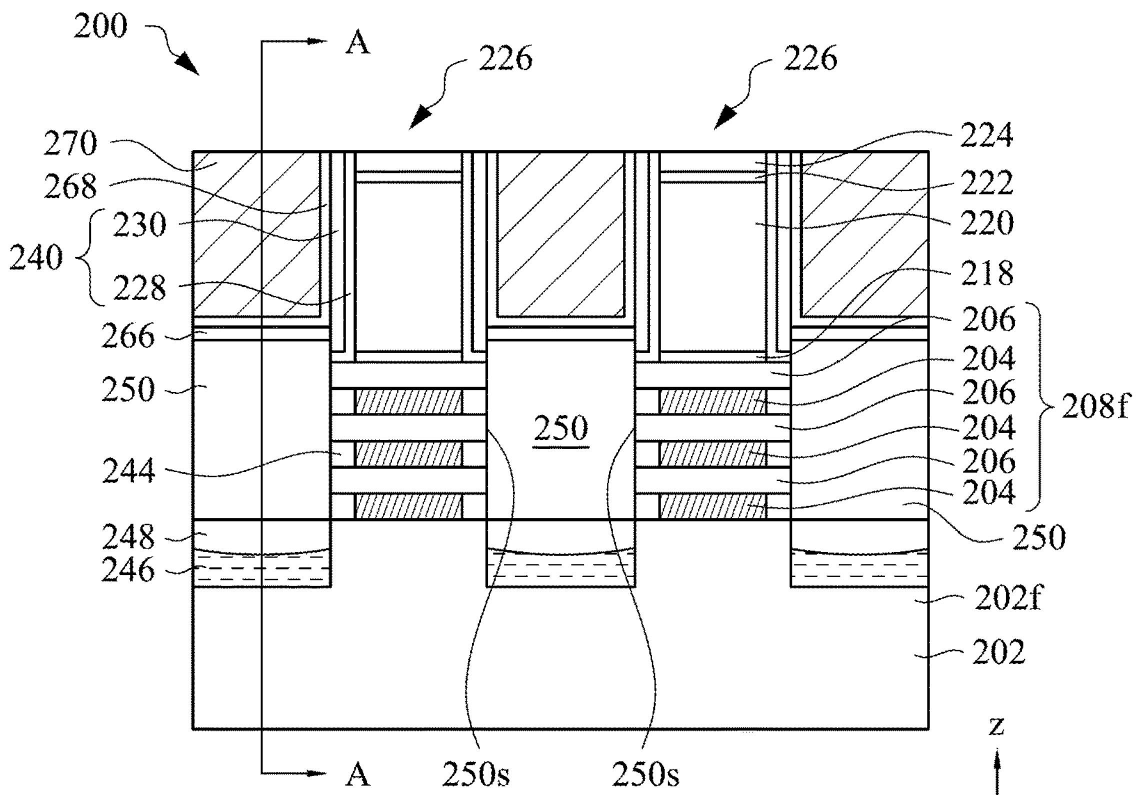

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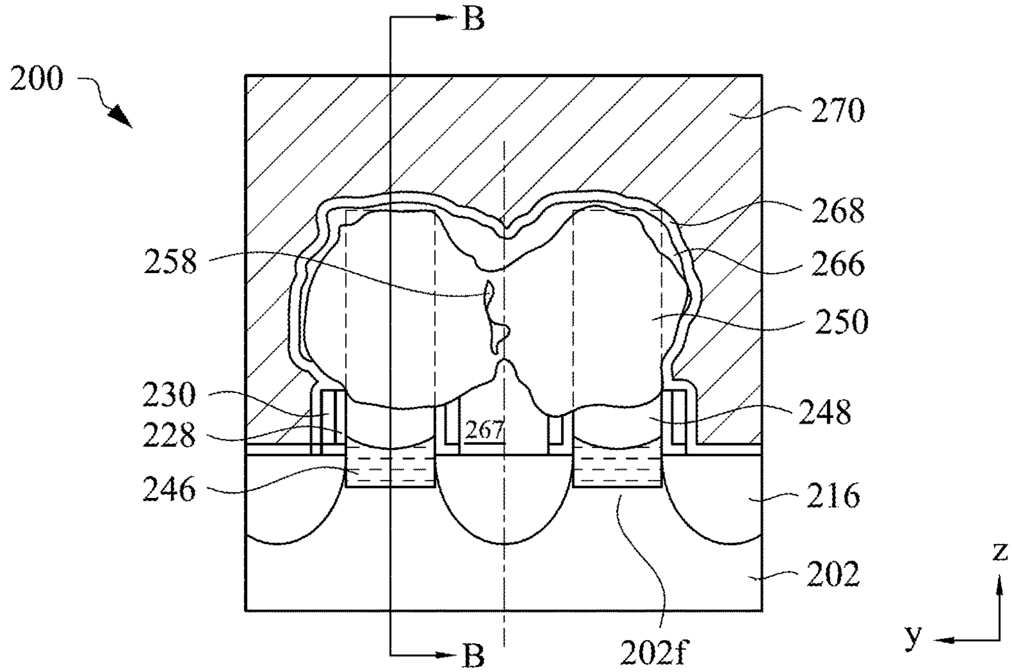

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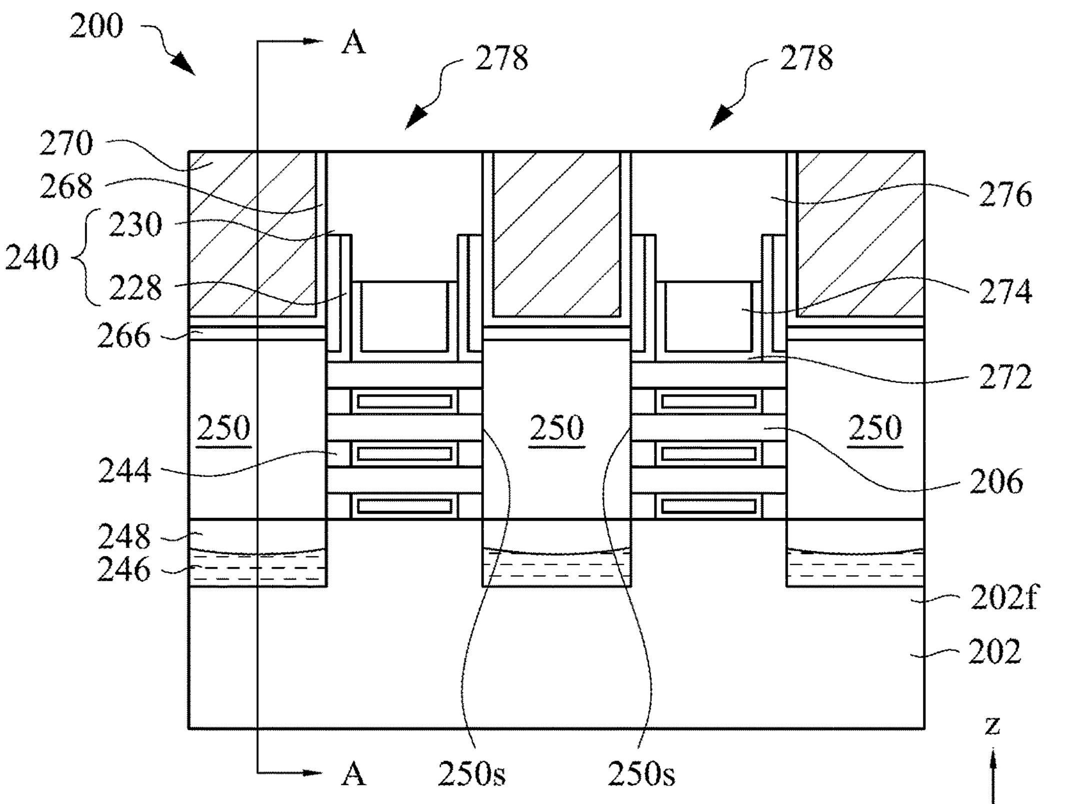

Fig. 14B

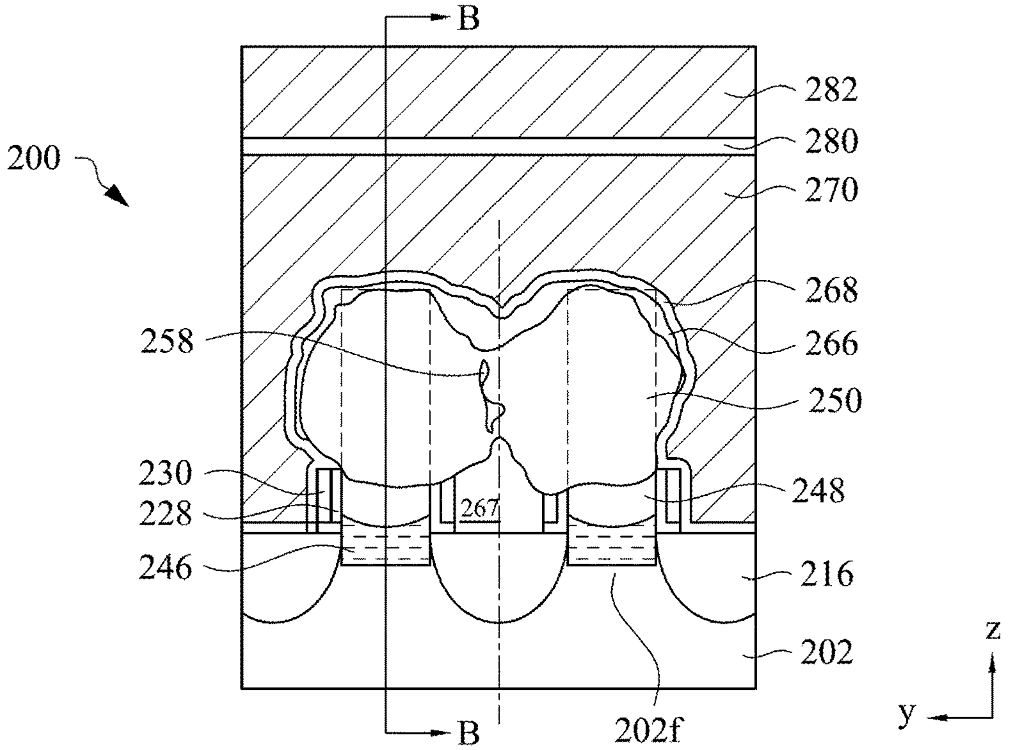

Fig. 15A

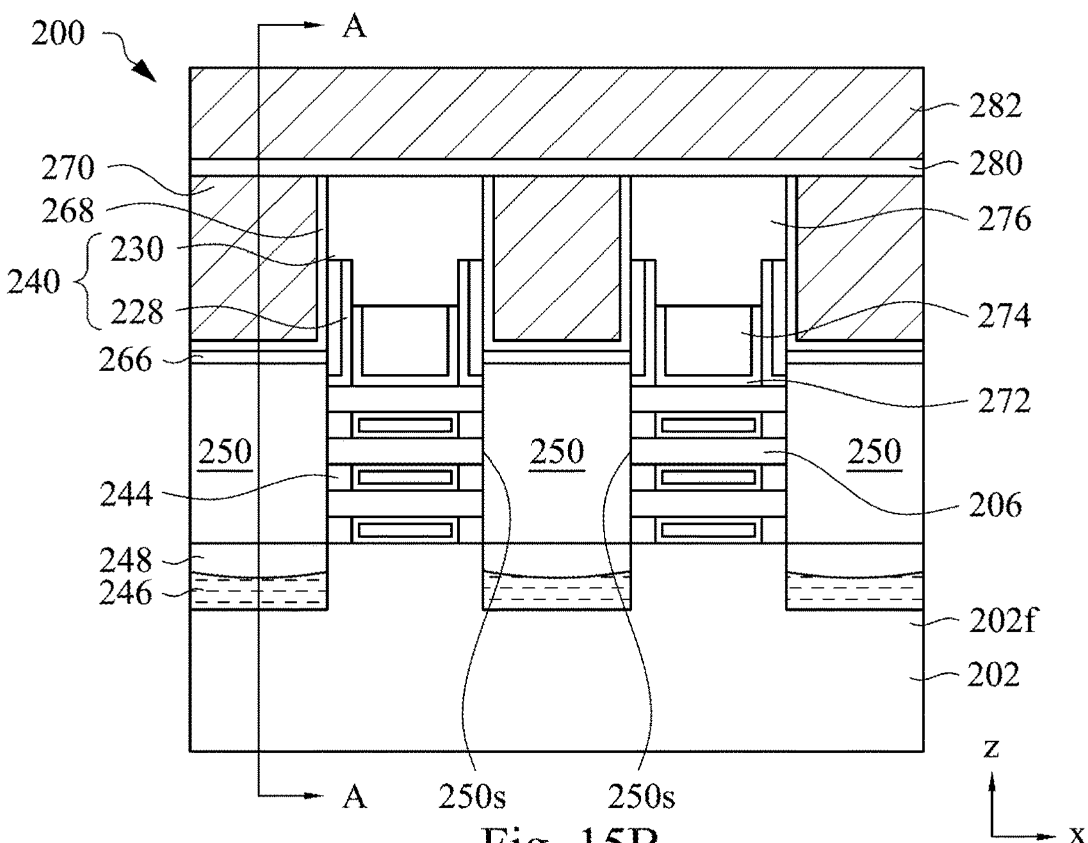

Fig. 15B

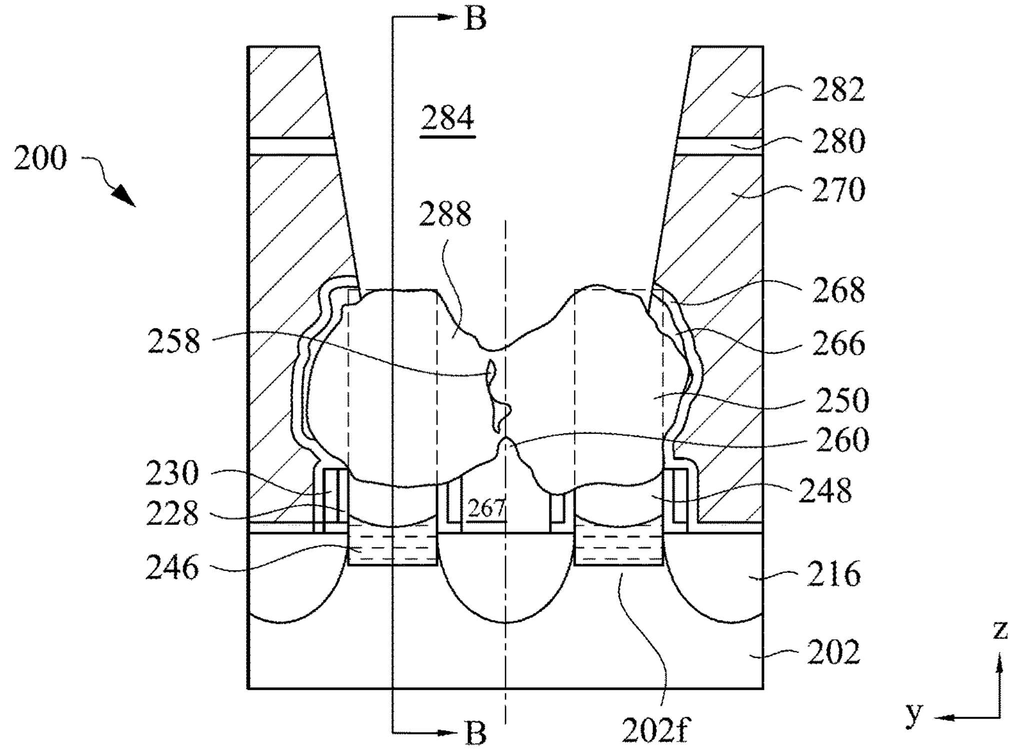

Fig. 16A

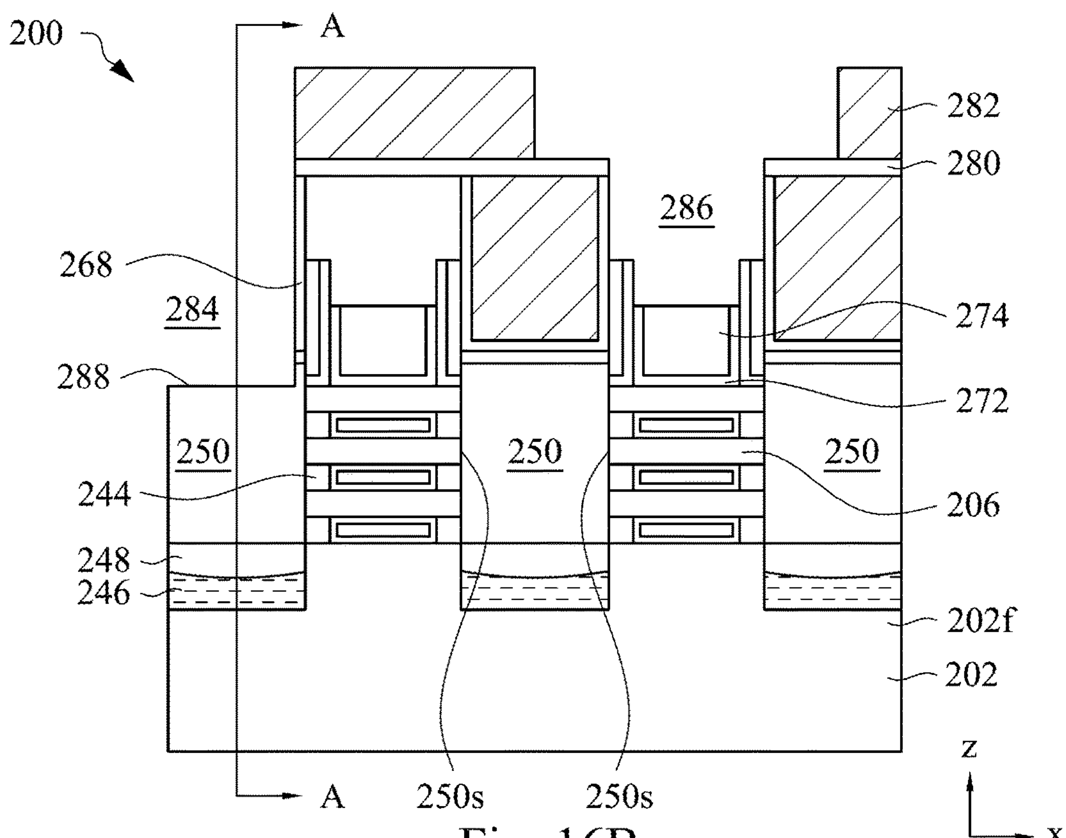

Fig. 16B

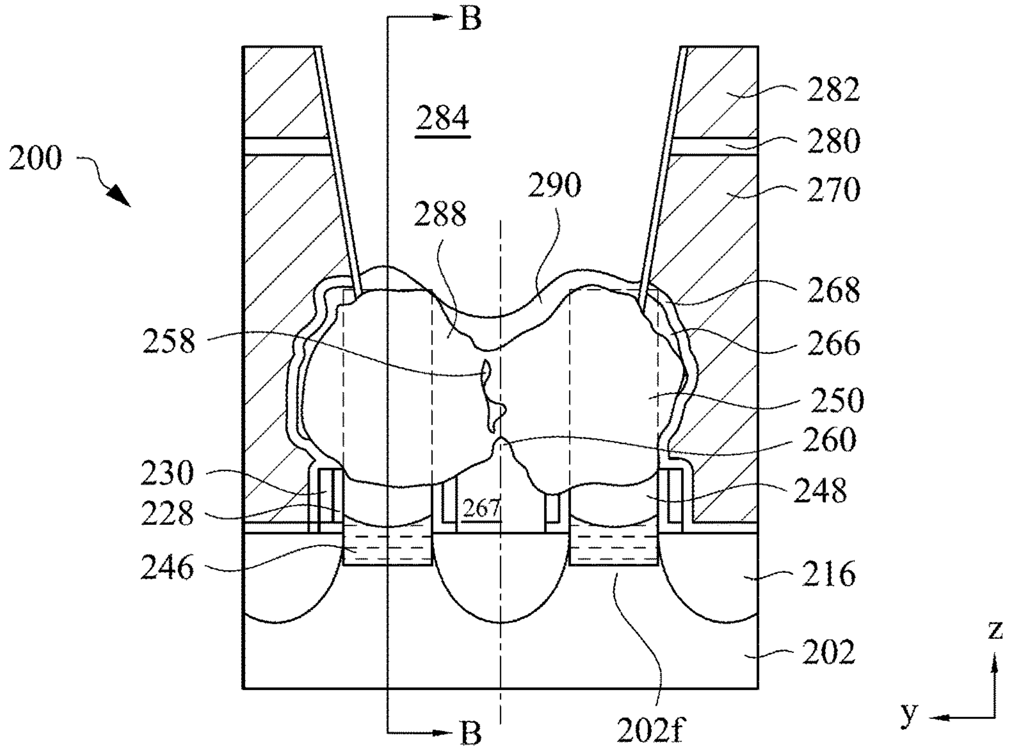

Fig. 17A

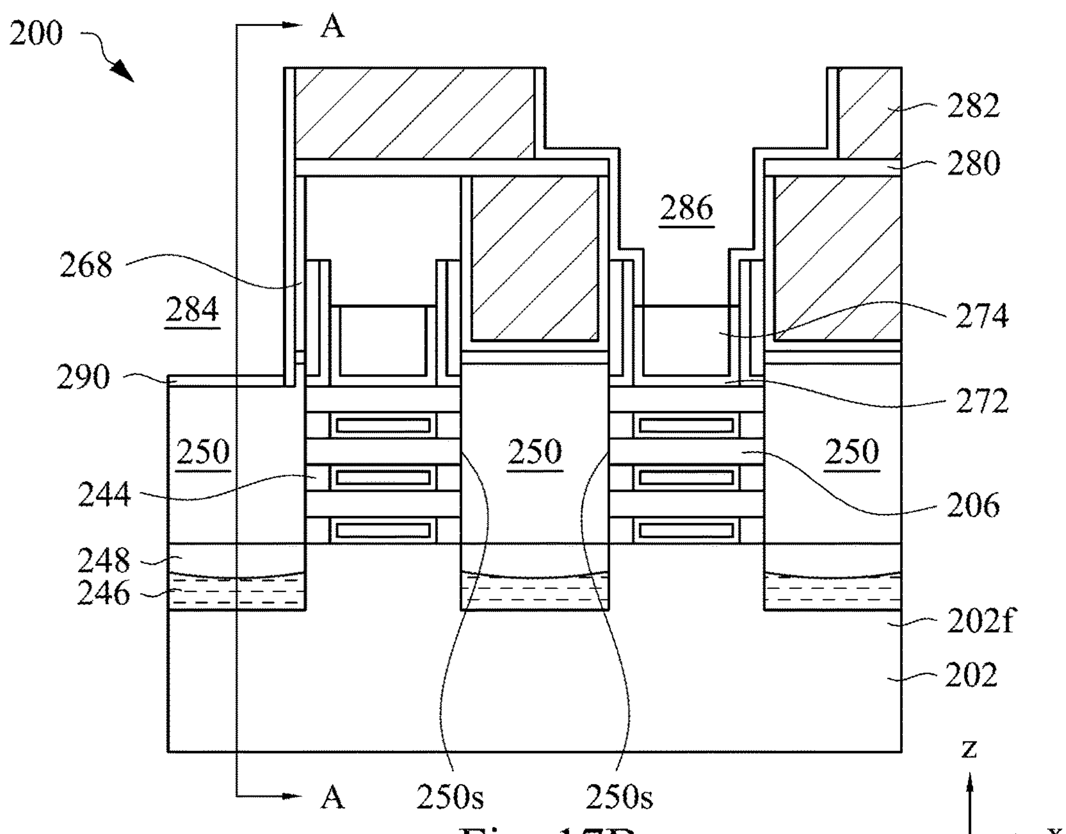

Fig. 17B

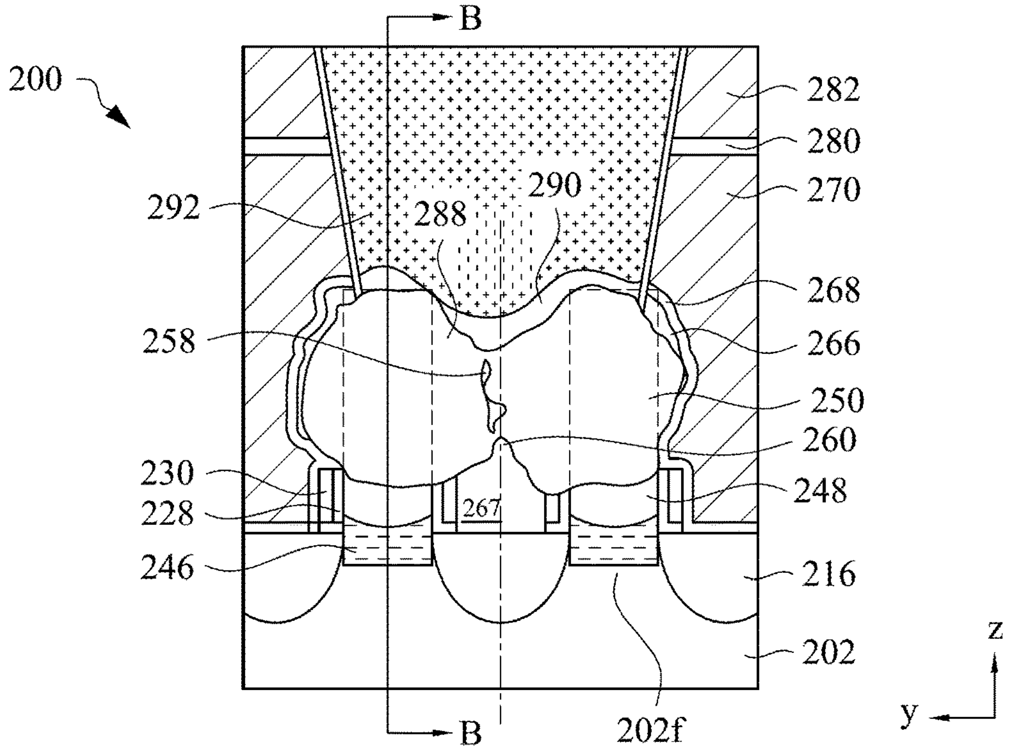

Fig. 18A

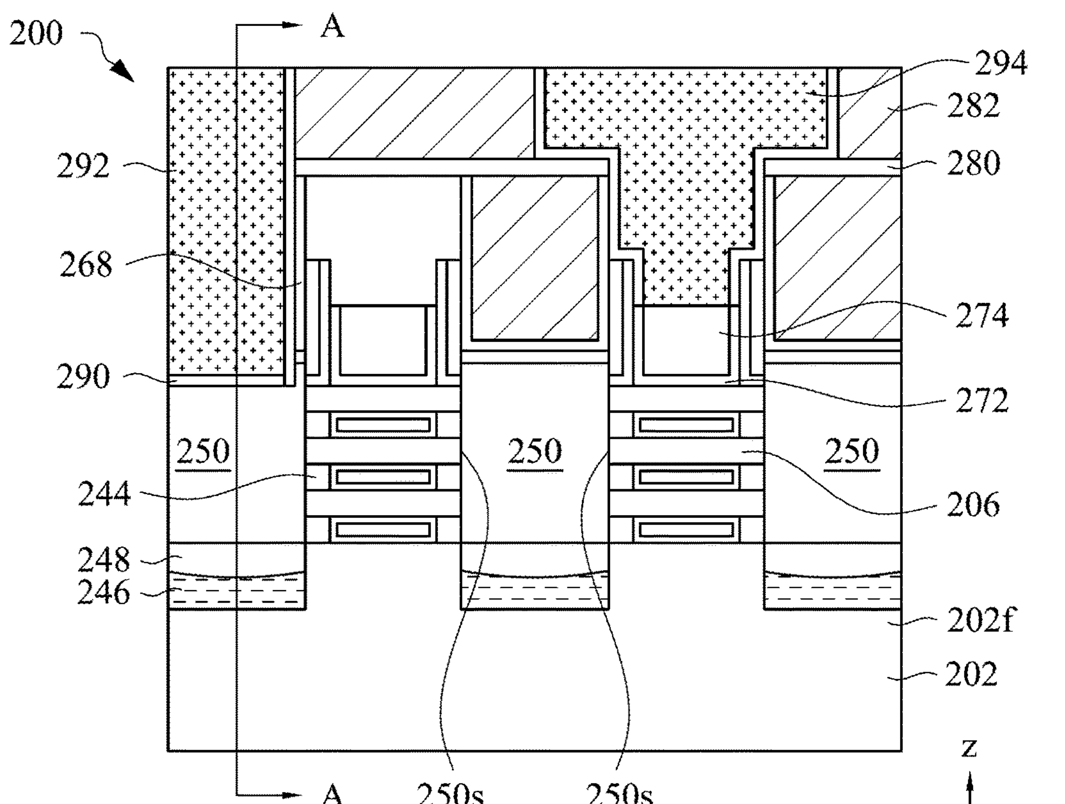

Fig. 18B

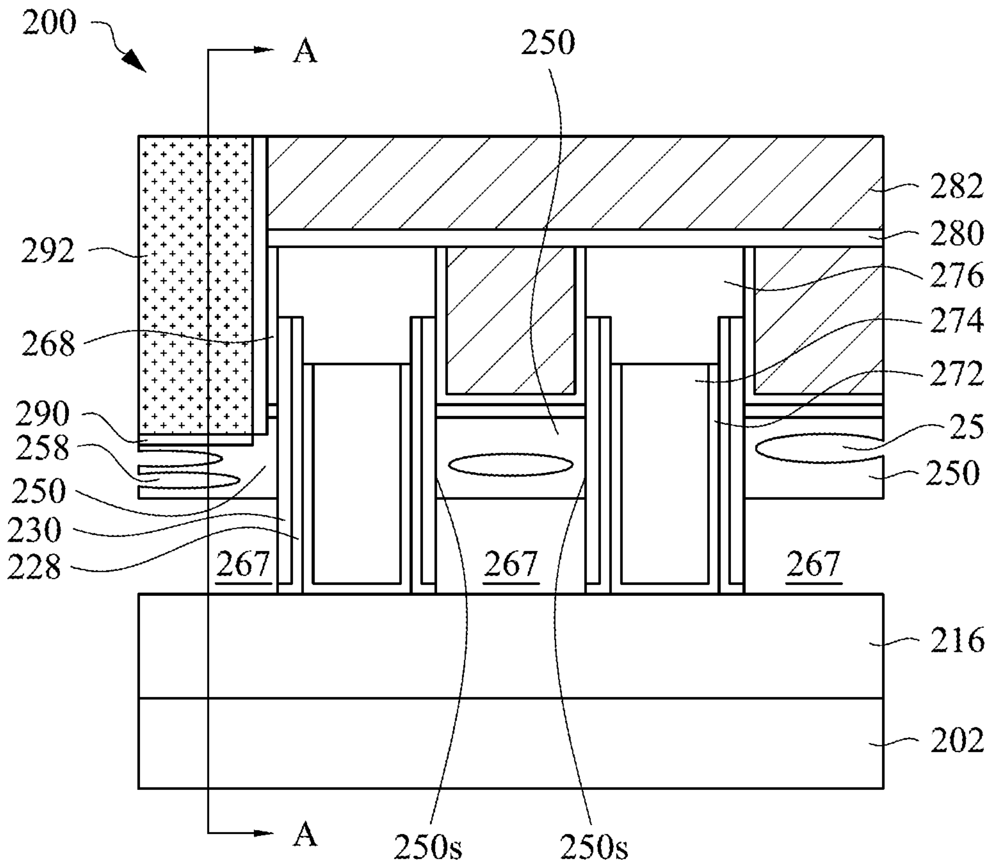
200
A
250
282
280
292
276
274
268
272
290
258
258
250
250
230
228
267
267
267
216
202
A
250s
250s

Fig. 18C

SEMICONDUCTOR DEVICES HAVING MERGED SOURCE/DRAIN FEATURES AND METHODS OF FABRICATION THEREOF

BACKGROUND

The semiconductor integrated circuit (IC) industry has experienced exponential growth. Technological advances in IC materials and design have produced generations of ICs where each generation has smaller and more complex circuits than the previous generation. In the course of IC evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased. This scaling down process generally provides benefits by increasing production efficiency and lowering associated costs. Such scaling down has also increased the complexity of processing and manufacturing ICs.

Therefore, there is a need to improve processing and manufacturing ICs.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1**A is a flow chart of a method for manufacturing of a semiconductor device according to embodiments of the present disclosure.

FIGS. **1**B-**1**P schematically illustrate various stages of manufacturing a semiconductor device according to embodiments of the present disclosure.

FIG. **2** is a flow chart of a method for manufacturing of a semiconductor device according to embodiments of the present disclosure.

FIGS. **3** to **4**, **5**A-**5**B, **6**A-**6**B, **7**A-**7**B, **8**A-**8**B, **9**A-**9**B, **10**A-**10**B, **11**A-**11**E, **12**A-**12**B, **13**A-**13**B, **14**A-**14**B, **15**A-**15**B, **16**A-**16**B, **17**A-**17**B, and **18**A-**18**C schematically illustrate various stages of manufacturing a semiconductor device according to embodiments of the present disclosure.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “over,” “top,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 64 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

The foregoing broadly outlines some aspects of embodiments described in this disclosure. While some embodiments described herein are described in the context of nanostructure FETs (e.g. nanowire transistor, nanosheet transistor, gate all around transistor, etc.), implementations of some aspects of the present disclosure may be used in other processes and/or in other devices, such as planar FETs, Fin-FETs, and other suitable devices. A person having ordinary skill in the art will readily understand other modifications that may be made are contemplated within the scope of this disclosure. In addition, although method embodiments may be described in a particular order, various other method embodiments may be performed in any logical order and may include fewer or more steps than what is described herein. In the present disclosure, a source/drain refers to a source and/or a drain. A source and a drain are interchangeably used.

The nanostructure transistor may be patterned by any suitable method. For example, the structures may be patterned using one or more photolithography processes, including double-patterning or multi-patterning processes. Generally, double-patterning or multi-patterning processes combine photolithography and self-aligned processes, allowing patterns to be created that have, for example, pitches smaller than what is otherwise obtainable using a single, direct photolithography process. For example, in one embodiment, a sacrificial layer is formed over a substrate and patterned using a photolithography process. Spacers are formed alongside the patterned sacrificial layer using a self-aligned process. The sacrificial layer is then removed, and the remaining spacers may then be used to pattern the GAA structure.

Embodiments of the present disclosure provide methods for forming merged source/drain features from two or more fin structures. The merged source/drain features according to the present disclosure have a merged portion with an increased height percentage over the overall height of the source/drain feature. The increased height percentage provides an increased landing range for source/drain contact features, therefore, reducing the connection resistance between the source/drain feature and the source/drain contact features. In some embodiments, the emerged source/drain features include one or more voids formed within the merged portion.

FIG. **1**A is a flow chart of a method **10** for manufacturing of a semiconductor device according to embodiments of the present disclosure. FIGS. **1**B-**1**P schematically illustrate various stages of manufacturing a semiconductor device **40** according to embodiments of the present disclosure. Particularly, the semiconductor device **40** may be manufactured according to the method **10** of FIG. **1**A.

At operation **12** of the method **10**, fin structures **44** are formed on a substrate **42**, and an isolation layer **46** is formed in trenches between the fin structures **44**, as shown in **1**B. FIG. **1**B is a schematic side view of the semiconductor device **40** according to the present disclosure. The substrate **42** may include a single crystalline semiconductor material such as, but not limited to Si, Ge, SiGe, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, and InP. The substrate **42** may include various doping configurations depending on circuit design. For example, the substrate **42** may include one or more p-doped regions and one or more n-doped regions. In some embodiments, the substrate **42** is a silicon (**100**) substrate. The fin structures **44** are then formed using one or more patterning and etching processes. The isolation layer **46** is formed in the trenches between the fin structures **44** by a suitable deposition followed by an etch back process. The bottom profile of the isolation layer **46** is shown to be curved as an example. Depending on pitch and/or height of the fin structures **44**, a bottom profile of the isolation layer **46** may vary, for example curved, substantially flat, or other shapes. The isolation layer **46** may be formed by a high-density plasma chemical vapor deposition (HDP-CVD), a flowable CVD (FCVD), or other suitable deposition process. In some embodiments, the isolation layer **46** may include silicon oxide, silicon nitride, silicon oxynitride, fluorine-doped silicate glass (FSG), a low-k dielectric, or combinations thereof. In some embodiments, the isolation layer **46** is formed to cover the fin structures **44** by a suitable deposition process to fill the trenches between the fin structures **44**, a planarization process may be performed to expose the fin structures **44**, and then recess etched using a suitable anisotropic etching process to expose a portion of the fin structures **44**, as shown in FIG. **1**B. In some embodiments, the fin structures **44** have a height h**1** over the isolation layer **46**. The height h**1** may vary according to circuit design. In some embodiments, the height h**1** is in a range between about 20 nm to about 100 nm.

At operation **14**, sacrificial gate structures **56**, gate sidewall spacers **66**, and fin sidewall spacers **62**, **62***a*, **62***b*, **64**, **64***a*, **64***b* are formed as shown in FIGS. **1**C and **1**D. FIG. **1**C is a sectional view of the semiconductor device **40** along the line A-A in FIG. **1**D. FIG. **1**D is a sectional view of the semiconductor device **40** along the line B-B in FIG. **1**C.

A sacrificial gate dielectric layer **48** is conformally formed over the substrate **42**. The sacrificial gate dielectric layer **48** is formed over the fin structures **44** and the isolation layer **46**. The sacrificial gate dielectric layer **48** may include silicon oxide, silicon nitride, a combination thereof, or the like. The sacrificial gate dielectric layer **48** may be deposited or thermally grown according to acceptable techniques, such as thermal CVD, CVD, ALD, and other suitable methods.

A sacrificial gate electrode layer **50** is deposited on the sacrificial gate dielectric layer **48** and then planarized, such as by a CMP process. The sacrificial gate electrode layer **50** includes silicon such as polycrystalline silicon, amorphous silicon, poly-crystalline silicon-germanium (poly-SiGe), or the like. In some embodiments, the sacrificial gate electrode layer **50** is subjected to a planarization operation. The sacrificial gate electrode layer **50** may be deposited using CVD, including LPCVD and PECVD, PVD, ALD, or other suitable process. In some embodiments, a pad layer **52**, and a mask layer **54** are sequentially deposited over the sacrificial gate electrode layer **50**. The pad layer **52** may include silicon nitride. The mask layer **54** may include silicon oxide. A patterning operation is performed on the mask layer **54**, the pad layer **52**, the sacrificial gate electrode layer **50**, and the sacrificial gate dielectric layer **48** to form the sacrificial gate structures **56** using one or more etching processes, such as one or more plasma etching processes or one or more wet etching processes. In some embodiments, the mask layer **54** and pad layer **52** are first patterned using a patterning process. The sacrificial gate electrode layer **50** is then patterned using the patterned mask layer **54** and pad layer **52** as an etching mask. In some embodiments, the sacrificial gate electrode layer **50** may be etched by an anisotropic etching, such as a reactive ion etching (RIE) process. The anisotropic etching has a greater etching rate along the Z direction than etching rates along the X and Y directions. During the etching of the sacrificial gate electrode layer **50**, the sacrificial gate dielectric layer **48** on the fin structures **44** may act as an etch stop to prevent the etchant from removing the fin structures **44**.

In some embodiments, after patterning the sacrificial gate electrode layer **50**, any exposed residual sacrificial gate dielectric layer **48** is removed by a suitable etch process. In some embodiments, the residual sacrificial gate dielectric layer **48** can be etched by tuning one or more parameters, such as etchant, etching temperature, etching solution concentration, etching pressure, source power, radio frequency (RF) bias voltage, etchant flow rate, of the etch process for etching the sacrificial gate electrode layer **50**.

The sacrificial gate structure **56** covers a portion of the fin structures **44**. The portion of the fin structures **44** covered by the sacrificial gate structures **56** eventually form a channel region.

In some embodiments, a spacer layer **58** and a spacer layer **60** may be formed over exposed surfaces of the semiconductor device **40**. The spacer layer **58** and the spacer layer **60** may be formed by ALD or CVD, or any other suitable method. The spacer layer **58** may include an oxide material, such as silicon oxide, and the spacer layer **60** may include a nitride material, such as silicon nitride. Alternatively, the spacer layer **60** includes another suitable dielectric material, such as silicon oxide, silicon oxynitride, or combinations thereof. The spacer layer **58** may also comprise another suitable dielectric material. The spacer layer **58** and spacer layer **60** are formed by a suitable process. For example, the spacer layer **58** and spacer layer **60** are formed by blanket deposition sequentially. In some embodiments, an anisotropic etching may be performed to remove the spacer layer **58** and spacer layer **60** from horizontal surfaces, such that the spacer layer **58** and spacer layer **60** are positioned on sidewalls of the sacrificial gate structures **56**. As shown in FIG. **1**D, the gate sidewall spacers **66** formed on sidewall of the sacrificial gate structures **56**. In this example, the gate sidewall spacers **66** include spacer layer **58** and the spacer layer **60**. The gate sidewall spacers **66** may have other suitable arrangements and/or compositions.

The fin sidewall spacers **62** are formed from the spacer layer **58** and spacer layer **60** and may remain on exposed sidewalls of the fin structures **44**. In FIG. **1**C, the fin structures **44** are denoted as fin structure **44***a*, **44***b* respectively. The fin structures **44***a*, **44***b* are neighboring fin structures. In some embodiments, the fin structures **44***a*, **44***b* are substantially symmetrical to a central line **40***c*. In other words, the fin structures **44***a*, **44***b* may be disposed on opposite sides of the central line **40***c* and at substantially equal distances from the central line **40***c*. The As shown in FIG. **1**C, fin sidewall spacers **62***a*, **64***a* are formed on sidewalls of the fin structure **44***a*, and fin sidewall spacers **62***b*, **64***b* are formed on sidewalls of the fin structure **44***b*. The fin sidewall spacers **62***a*, **62***b*, collectively **62**, are formed on outer sidewalls of the fin structures **44***a*, **44***b* and the fin sidewall spacers **64***a*, **64***b*, collectively **64**, are formed on inner sidewalls of the fin structures **44***a*, **44***b*. In this example, the fin side wall spacers **62***a*, **64***a*, **62***b*, **64***b* include the spacer layer **58** and the spacer layer **60**. The fin side wall spacers **62***a*, **64***a*, **62***b*, **64***b* may have other suitable arrangements and/or compositions.

In operation **16**, the fin structures **44** in source/drain region, or regions not covered by the sacrificial gate structures **46**, are recess etched, as shown in FIGS. **1**E and **1**F. FIG. **1**E is a sectional view of the semiconductor device **40** along the line A-A in FIG. **1**F. FIG. **1**F is a sectional view of the semiconductor device **40** along the line B-B in FIG. **1**E. The fin sidewall spacers **62**, **64** are also at least partially recessed. In some embodiments, suitable dry etching and/or wet etching may be used to remove the semiconductor material in the fin structure **44**. In some embodiments, the fin structures **44***a*, **44***b* are recessed to a level below the isolation layer **46**, as shown in FIG. **1**E. As shown in FIG. **1**F, source/drain recesses **68** are formed on both sides of the sacrificial gate structures **56**.

In some embodiments, the fin sidewall spacers **64***a*, **62***a*, **62***b*, **64***b* are partially recessed as shown in FIG. **1**E. In some embodiments, the fin sidewall spacers **64***a*, **62***a*, **62***b*, **64***b* may be recessed during recess etch of the fin structures **44**. In other embodiments, the fin sidewall spacers **64***a*, **62***a*, **62***b*, **64***b* may be removed using a separate process. In some embodiments, heights of the fin sidewall spacers **64***a*, **62***a*, **62***b*, **64***b* may be controlled to achieve desired shape of the source/drain features to be formed from the fin structures **44**. For example, the heights of the fin sidewall spacers **64***a*, **62***a*, **62***b*, **64***b*, along the z-direction, from a top surface **46***t* of the isolation layer **46** may be controlled to define critical dimension and/or shape of the source/drain features to be formed. In some embodiments, the heights of the fin sidewall spacers **64***a*, **62***a*, **62***b*, **64***b* may be set to control location of the merge point of the two source/drain features formed from the neighboring fin structures **44***a*, **44***b*. For example, the heights of the fin sidewall spacers **64***a*, **62***a*, **62***b*, **64***b* are used control the level of merge point along the z-direction.

Various factors may be considered when selecting heights of the fin sidewall spacers **64***a*, **62***a*, **62***b*, **64***b* to achieve desired shape of the source/drain features to be formed, for example, the pitch of the fin structures **44***a*, **44***b*, i.e. the distance between the fin structures **44***a*, **44***b* along the y-axis, the width of the fin structures **44***a*, **44***b* along the Y-axis, the height h**1** of the fin structures **44** over the top surface **46***t* of the isolation layer **46**, and other relevant geometry and/or material properties of the fin structures **44***a*, **44***b* and source/drain structures to be formed.

In some embodiments, the fin sidewall spacers **64***a*, **62***a*, **62***b*, **64***b* may have the same heights. In other embodiments, the fin sidewall spacers **62***a*, **64***a* may have different heights as shown in FIG. **1**C. Similarly, the fin sidewall spacers **62***b*, **64***b* may also have different heights. In some embodiments, the fin sidewall spacers **64***a*, **64***b* are higher than the fin sidewall spacers **62***a*, **62***b*. In other embodiments, the fin sidewall spacers **64***a*, **64***b* are shorter than the fin sidewall spacers **62***a*, **62***b*. In some embodiments, heights of the fin sidewall spacers **64***a*, **62***a*, **62***b*, **64***b* maybe symmetrical to the central line **40***c*. For example, the fin sidewall spacers **64***a*, **64***b* may have substantially the same height and the fin sidewall spacers **62***a*, **62***b* may have substantially the same height. In some embodiments, the fin sidewall spacers **62***a*, **62***b* and the fin sidewall spacers **64***a*, **64***b* may have a height difference h**2**. The dimension of h**2** may vary according to the dimension of the semiconductor device **40**. In some embodiment, h**2** may be in a range between 5 nm and about 30 nm. In other embodiments, a ratio of h**2** over h**1** may be in a range between 0.05 and about 0.5.

At operation **18**, an undoped epitaxial layer **70** is formed in the source/drain recess **68**, as shown in FIGS. **1**G and **1**H. FIG. **1**G is a sectional view of the semiconductor device **40** along the line A-A in FIG. **1**H. FIG. **1**H is a sectional view of the semiconductor device **40** along the line B-B in FIG. **1**G.

In some embodiments, a pre-clean process may be performed to remove any undesirable silicon oxide that is formed as a result of the oxidation of the exposed surfaces of the source/drain recesses **68**. In some embodiments, the pre-clean process may be performed using inductively coupled plasma of a cleaning agent. In some embodiment, the cleaning agent includes Ar, NF_3, and NH_3. The pre-cleaning process may be performed in a temperature range between about 25° C. and about 74° C. for a time period between 80 seconds and about 400 seconds. Alternatively, the pre-cleaning process may be performed using an HF-based gas or a SiCoNi based gas.

In some embodiments, the undoped epitaxial layer **70** may be an epitaxial silicon layer. The undoped epitaxial layer **70** may be formed by any suitable method, such as by CVD, CVD epitaxy, molecular beam epitaxy (MBE), or any suitable deposition technique.

In some embodiments, the undoped epitaxial layer **70** may be formed to refill the fin structure **44** between the fin sidewall spacers **62***a*, **64***a* and between the fin sidewall spacers **62***b*, **64***b*. The undoped epitaxial layer **70** may be formed to a level between below the top surface **46***t* of the isolation layer **46** and below the fin sidewall spacers **64***a*/**64***b*. For example, the undoped epitaxial layer **70** may level with the top surface **46***t* of the isolation layer **46**. As shown in FIG. **1**G, a top surface **70***t* of the undoped epitaxial layer **70** is substantially level with a top surface **64***t* of the fin sidewall spacers **64***a*, **64***b*.

At operation **20**, an epitaxial transitional layer **72** is formed over the undoped epitaxial layer **70**, as shown in FIGS. **1**G and **1**H. The epitaxial transitional layer **72** is formed over the undoped epitaxial layer **70**. The epitaxial transitional layer **72** may be formed by any suitable method, such as by CVD, CVD epitaxy, molecular beam epitaxy (MBE), or any suitable deposition technique. The epitaxial transitional layer **72** can serve to gradually change the lattice constant from that of the undoped epitaxial layer **70** to that of the source/drain features to be formed. In some embodiments, the epitaxial transitional layer **72** may be a semiconductor material with a lattice structure similar to the semiconductor material configured to function as a source/drain feature for a n-type device. In some embodiments, the epitaxial transitional layer **72** may be a semiconductor material includes n-type dopants at a dopant concentration lower than a dopant concentration used in a source/drain feature. The epitaxial transitional layer **72** may include one or more layers of Si, SiAs, SiP, SiC and SiCP. The epitaxial transitional layer **72** also include n-type dopants, such as phosphorus (P), arsenic (As), etc. In some embodiments, the epitaxial transitional layer **72** may be a Si layer includes arsenic dopants. In some embodiments, the epitaxial transitional layer **72** includes a dopant concentration in a range between about 15E19 atoms/cm^3 and about 5E20 atoms/cm^3.

The epitaxial transitional layer **72** may have a thickness h**3** in a range between about 3 nm and about 15 nm. If the thickness of the epitaxial transitional layer **72** is below 3 nm, the epitaxial transitional layer **72** may not be thick enough to function as lattice transitional layer between the undoped epitaxial layer **70** and the source/drain features to be formed. If the thickness of epitaxial transitional layer **72** is greater than 15 nm, the epitaxial transitional layer **72** may be in contact with the semiconductor channel layers **206** and affect the device function and without obvious additional advantages for crystalline structural transition. In some embodiments, the top surface **72***t* of the epitaxial transitional layer **72** may be substantially level with a top surface of the higher one of the fin sidewall spacers **62***a*/**62***b* and **64***a*/**64***b*. As shown in FIG. **1**G, the top surface **72***t* of the epitaxial transitional layer **72** is substantially level with a top surface **62***t* of the fin sidewall spacers **62***a*, **62***b*. In some embodiments, the height difference between the fin sidewall spacers **62***a*/**62***b* and **64***a*/**64***b* and the epitaxial transitional layer **72** may result in the top surface **72***t* that is lob sided towards the central line **40***c*, enabling formation of merged source/drain features to be formed.

In some embodiments, the epitaxial transitional layer **72** may be grown in an epitaxial chamber by a suitable process. For example, the epitaxial transitional layer **72** is formed by a selective etching growth process, in which a thin film is deposited by introducing a reactant gas including deposition agent and etchant together. In some embodiments, an optional etching process may be performed to achieve desired shape and/or thickness of the epitaxial layer being formed. The epitaxial deposition may be performed at a temperature in a range between about 600° C. and 700° C., under a pressure in a range between about 100 and 600 Torr, and performed for a time duration in a range between about 100 seconds and 400 seconds, by using a Si containing gas such as $SiCl_2H_2$, SiH_4, or Si_2H_6, such as AsH_3, and PH_3, HCl, and a carrier gas, such as Hz. In some embodiments, the reactant gas may include $SiCl_2H_2$ at a flow rate in a range between 200 sccm and 600 sccm, AsH_3 at a flow rate in a range between 100 sccm and 300 sccm, HCl at a flow rate in a range between 50 sccm and 200 sccm, and Hz at a flow rate in a range between 2000 sccm and 8000 sccm. In some embodiments, an optional etch process may be performed at a temperature in a range between about 650° C. and 750° C., under a pressure in a range between about 100 and 500 Torr, and performed for a time duration in a range between about 10 seconds and 80 seconds, by using an etchant, such as HCl. In some embodiments, the etchant may include HCl at a flow rate in a range between 300 sccm and 1000 sccm.

At operation **22**, epitaxial source/drain features **74** are formed over the epitaxial transitional layer **72**, as shown in FIGS. **1**G, **1**H, and **1**I. FIG. **1**I is a partial enlarged view of FIG. **1**G showing the epitaxial source/drain features **74**. The epitaxial source/drain features **74** are formed over the epitaxial transitional layer **72**. The epitaxial source/drain features **74** may be formed by any suitable method, such as by CVD, CVD epitaxy, molecular beam epitaxy (MBE), or any suitable deposition technique. The epitaxial source/drain features **74** may include one or more layers of Si, SiP, SiC and SiCP. The epitaxial source/drain features **74** also include n-type dopants, such as phosphorus (P), arsenic (As), etc. In some embodiments, the epitaxial source/drain features **74** may be a Si layer including phosphorus dopants. The dopant concentration in the epitaxial source/drain features **74** is higher than that of the epitaxial transitional layer **72**. In some embodiments, the epitaxial source/drain features **74** include a dopant concentration of between about 1E20 atoms/cm^3 and about 5E21 atoms/cm^3.

The epitaxial source/drain features **74** may have a height h**4**, shown in FIG. **1**I, in a range between about 30 nm and about 70 nm or a thickness enough for side surfaces of the epitaxial features **74** to cover all of the fin structures **44** in the z-direction.

In some embodiments, the epitaxial source/drain features **74** may be grown in an epitaxial chamber by a suitable process. For example, the epitaxial source/drain features **74** are formed by a selective etching growth process, in which a thin film is deposited by introducing a reactant gas including deposition agent and etchant together. In some embodiments, an optional etching process may be performed to achieve desired shape and/or thickness of the epitaxial layer being formed. The epitaxial deposition may be performed at a temperature in a range between about 600° C. and 700° C., under a pressure in a range between about 100 and 600 Torr, and performed for a time duration in a range between about 50 seconds and 300 seconds, by using a Si containing gas such as SiH_4, Si_2H_6, and $SiCl_2H_2$, a dopant gas, such as PH_3, and AsH_3, and HCl, and a carrier gas, such as Hz. In some embodiments, the reactant gas may include SiH_4 at a flow rate in a range between 200 sccm and 500 sccm, PH_3 at a flow rate in a range between 100 sccm and 500 sccm, HCl at a flow rate in a range between 50 sccm and 100 sccm, and H_2 at a flow rate in a range between 2000 sccm and 4000 sccm. In some embodiments, an optional etch process following the epitaxial deposition may be performed at a temperature in a range between about 600° C. and 700° C., under a pressure in a range between about 100 and 500 Torr, and performed for a time duration in a range between about 10 seconds and 80 seconds, by using an etchant, including HCl and SiH_4. In some embodiments, the etchant may include HCl at a flow rate in a range between 500 sccm and 1000 sccm, and SiH_4 at a flow rate in a range between 100 sccm and 300 sccm. The etchant may include a carrier gas, such as Hz.

Because of the epitaxial process parameters at operation **22** and the height selection of the fin sidewall spacers **62***a*, **64***a*, **64***b*, **62***b*, the epitaxial source/drain features **74** grown from the fin structures **44***a* and **44***b* merged along the central line **40***c*. As shown in FIG. **1**I, the epitaxial source/drain feature **74***a* grown from the fin structure **44***a* and the epitaxial source/drain feature **74***b* grown from the fin structure **44***b* merge together to form one epitaxial source/drain feature **74**. The merged epitaxial source/drain feature **74** may have a top surface **76** and a bottom surface **78** opposing the top surface **76**. The sidewalls connect the top surface **76** and the bottom surface **78**. The epitaxial source/drain features **74***a*, **74***b* merge substantially along the central line **40***c*. The epitaxial source/drain features **74***a*, **74***b* are merged from a lower merge point **84** on the bottom surface **78** and an upper merge point **80** on the top surface **76**. The lower merge point **84** and the top merge point **80** are at different vertical levels along the z-direction. A merge length in the z-direction from the lower merge point **84** to the upper merge point **80** is denoted by h**5**. In some embodiments, a ratio of the merge length h**5** and the height h**4** is in a range between about 65% and about 80%. The merge height h**5** is about 50% to 70% of the non-merge height, or the height above the upper merge point **80** and below the lower merge point **84**.

In some embodiments, the shapes of the epitaxial source/drain features **74***a*, **74***b* are tuned such that the epitaxial source/drain features **74***a*, **74***b* are "just" merge to allow the epitaxial source/drain features **74***a*, **74***b* substantially retain the natural shapes from epitaxial growth without merging. The "just" merge arrangement allows the epitaxial source/drain features **74***a*, **74***b* to merge yet substantially maintain "natural" or "unmerged" source/drain feature volume.

As shown in FIG. **1**I, the top surface **76** may be a wavy surface having peak points **86**, **88** defining a valley therebetween. The upper merge point **80** coincides with the valley point between the peak points **86**, **88**. A wavy height h**6** is defined by a distance from the valley point to the peak points

86, 88. In some embodiments, a ratio of the wavy height h6 over the total height h4 is in a range between about 5% and about 35%.

In some embodiments, one or more voids 82 are formed along the merge line or the central line 40c as the "just" merge arrangement. The one or more voids 82 may be filled with air or gas, such as hydrogen, helium, or other suitable gas. In some embodiments, the voids 82 may have a shape of circular, elliptical, parabolic, or triangular in the z-y plane. In some embodiments, the voids 82 may have a radius in a range between about 0.5 nm and about 3 nm. In some embodiments, the void 82 may be located along the central line 40c about 3 nm to 7 nm below the upper merge point 80. The merging of the epitaxial source/drain features 74a, 74b also result a void 83 between the bottom surface 78 and the isolation layer 46. The void 83 may be filled with air or gas, such as hydrogen, helium, or other suitable gas

FIGS. 1J and 1K are schematic layout views of the semiconductor device 40 showing various positions and shapes of the voids 82 in the merged epitaxial source/drain features 74. As shown in FIG. 1J, the voids 82 may extend along the x-direction across the merged epitaxial source/drain features 74. Alternatively, the voids 82 may be located in a central portion of the epitaxial source/drain features 74. As shown in FIG. 1K, voids 82a, 82b, 82c of various cross-sectional shapes in the x-y plane are located within the epitaxial source/drain features 74. Particularly, a void with a triangle shaped cross section in the y-z plane (shown in FIG. 1G) may have a square or rectangular shaped cross section in the x-y plane as shown in the void 82a in FIG. 1K. A void with a cone or hyperbolic shaped cross section in the y-z plane (shown in FIG. 1G) may have an oval or circular shaped cross section in the x-y plane as shown in the void 82b in FIG. 1K. A void with an oval or elliptical shaped cross section in the y-z plane (shown in FIG. 1G) may have a hexagonal shaped cross section in the x-y plane as shown in the void 82c in FIG. 1K.

At operation 24, an epitaxial cap layer 90 is formed over the epitaxial source/drain features 74, as shown in FIGS. 1L and 1M. FIG. 1L is a sectional view of the semiconductor device 40 along the line A-A in FIG. 1M. FIG. 1M is a sectional view of the semiconductor device 40 along the line B-B in FIG. 1L.

The epitaxial cap layer 90 is formed on the exposed surfaces of the epitaxial source/drain features 74. The epitaxial cap layer 90 may be formed by any suitable method, such as by CVD, CVD epitaxy, molecular beam epitaxy (MBE), or any suitable deposition technique. The epitaxial cap layer 90 may include one or more layers of Si, SiP, SiC and SiCP. The epitaxial cap layer 90 also include n-type dopants, such as phosphorus (P), arsenic (As), etc. In some embodiments, the epitaxial cap layer 90 may be a Si layer including phosphorus dopants. In some embodiments, the epitaxial cap layer 90 includes a dopant concentration of between about 1E21 atoms/cm^3 and about 2E21 atoms/cm^3.

The epitaxial cap layer 90 may have a thickness along the z-direction in a range between about 3 nm and about 10 nm. The epitaxial cap layer 90 maintains a wavy shape over the top surface 76 of the merged epitaxial source/drain feature 74.

In some embodiments, the epitaxial cap layer 90 may be grown in an epitaxial chamber by a suitable process. For example, the epitaxial cap layer 90 is formed by a selective etching growth process, in which a thin film is deposited by introducing a reactant gas including deposition agent and etchant together. In some embodiments, an optional etching process may be performed to achieve desired shape and/or thickness of the epitaxial layer being formed. The epitaxial deposition may be performed at a temperature in a range between about 650° C. and 750° C., under a pressure in a range between about 100 and 600 Torr, and performed for a time duration in a range between about 20 seconds and 100 seconds, by using a Si containing gas such as SiH_4, Si_2H_6, and $SiCl_2H_2$, a dopant gas, such as PH_3, and AsH_3, and HCl, and a carrier gas, such as Hz. In some embodiments, the reactant gas may include $SiCl_2H_2$ at a flow rate in a range between 200 sccm and 500 sccm, PH_3 at a flow rate in a range between 20 sccm and 80 sccm, HCl at a flow rate in a range between 50 sccm and 100 sccm, and Hz at a flow rate in a range between 2000 sccm and 6000 sccm. In some embodiments, an optional etch process following the epitaxial deposition may be performed at a temperature in a range between about 700° C. and 780° C., under a pressure in a range between about 5 and 50 Torr, and performed for a time duration in a range between about 10 seconds and 80 seconds, by using an etchant, including HCl and GeH_4. In some embodiments, the etchant may include HCl at a flow rate in a range between 1000 sccm and 2000 sccm, and GeH_4 at a flow rate in a range between 100 sccm and 400 sccm. The etchant may include a carrier gas, such as Hz.

In some embodiments, the epitaxial deposition at operations 18, 20, 22, and 24 may be performed in the same epitaxial deposition chamber.

At operation 26, a contact etch stop layer (CESL) 91 and an interlayer dielectric (ILD) layer 92 are formed over the semiconductor device 40, as shown in FIGS. 1L and 1M. The CESL 91 is conformally formed over exposed surfaces of the semiconductor device 40. The CESL 91 is formed on the epitaxial cap layer 90, the gate sidewall spacers 66, the fin sidewall spacers 62a, 62b, and the isolation layer 46 if exposed. The CESL 91 may include SiN, SiON, SiCN or any other suitable material, and may be formed by CVD, PVD, or ALD.

The interlayer dielectric (ILD) layer 92 is formed over the CESL 91. The materials for the ILD layer 92 include compounds comprising Si, O, C, and/or H, such as silicon oxide, SiCOH and SiOC. Organic materials, such as polymers, may be used for the ILD layer 92. In some embodiments, the ILD layer 92 may be formed by flowable CVD (FCVD). The ILD layer 92 protects the epitaxial source/drain features 74 during the removal of the sacrificial gate structures 56.

At operation 28, replacement gate structures are formed, as shown in FIGS. 1L and 1M. The sacrificial gate dielectric layer 48 and sacrificial gate electrode layer 50 are removed by one or more suitable process, such as dry etch, wet etch, or a combination thereof, to expose the fin structures 44. In some embodiments, a wet etchant such as a tetramethylammonium hydroxide (TMAH) solution is used. The replacement gate structure may include a gate dielectric layer 93, and a gate electrode layer 94. Optionally, the replacement gate structure may include a self-aligned contact (SAC) layer 95.

The gate dielectric layer 93 may be conformally deposited on exposed surfaces in the gate cavities. The gate dielectric layer 93 may have different composition and dimensions for N-type devices and P-type devices and are formed separately using patterned mask layers and different deposition recipes. The gate dielectric layer 93 may include one or more layers of a dielectric material, such as silicon oxide, silicon nitride, or high-k dielectric material, other suitable dielectric material, and/or combinations thereof. Examples of high-k dielectric material include HfO_2, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, zirconium oxide, aluminum oxide, titanium oxide, hafnium dioxide-alumina (HfO_2—Al_2O_3) alloy, other suitable high-k dielectric materials, and/or combinations thereof. The gate dielectric layer **93** may be formed by CVD, ALD or any suitable method.

The gate electrode layer **94** is then formed on the gate dielectric layer **93** to fill the gate cavities. The gate electrode layer **94** may include one or more layers of conductive material, such as polysilicon, aluminum, copper, titanium, tantalum, tungsten, cobalt, molybdenum, tantalum nitride, nickel silicide, cobalt silicide, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, metal alloys, other suitable materials, and/or combinations thereof. In some embodiments, the gate electrode layer **94** may be formed by CVD, ALD, electroplating, or other suitable method. After the formation of the gate electrode layer **94**, a planarization process, such as a CMP process, is performed to remove excess deposition of the gate electrode material and expose the top surface of the ILD layer **92**.

In some embodiments, a metal gate etching back (MGEB) process is performed to form the self-aligned contact (SAC) layer **95**. One or more etching processes are performed to remove portions of the gate dielectric layer **93** and the gate electrode layer **94** to form trenches in the region above the remaining gate electrode layer **94**. The MGEB process may be a plasma etching process employing one or more etchants such as chlorine-containing gas, a bromine-containing gas, and/or a fluorine-containing gas. The etching process allows the gate dielectric layer **93** and the gate electrode layer **94** to be selectively etched from the ILD layer **92** and the CESL **91**.

In the MGEB process, the gate dielectric layer **93** and gate electrode layer **94** are etched back to a level lower than a top surface of high-k dielectric features formed on hybrid fins (not shown) parallel to the fin structures **44**. In some embodiments, the gate sidewall spacers **66** are also etched back to a level be lower than the CESL **91** and higher than the gate electrode layer **94**.

In some embodiments, a metal gate liner, not shown, may be first deposited on exposed surfaces in the trenches above the gate electrode layer **94** prior to depositing the SAC layer **95**. The metal gate liner and the SAC layer **95** may be formed by a suitable deposition process, such as CVD, PVD, or ALD. The metal gate liner may function as a diffusion barrier for the gate electrode layer **94**. The metal gate liner may be a dielectric layer including but not limited to SiO, SiN, SiC, SiCN, SiOC, SiON, SiOCN, ZrO, ZrN, or a combination thereof. The SAC layer **95** may be any dielectric layer that can be used as an etch stop layer during subsequent trench and via patterning for metal contacts. In some embodiments, the SAC layer **95** may a high-k dielectric layer. The SAC layer **95** may be a dielectric layer including but not limited to SiO, HfSi, SiOC, AlO, ZrSi, AlON, ZrO, HfO, TiO, ZrAlO, ZnO, TaO, LaO, YO, TaCN, SiN, SiOCN, Si, SiOCN, ZrN, SiCN, or any combinations thereof.

After filling the trenches with the SAC layer **95**, a planarization process, such as a CMP process, is performed to remove excess deposition of the SAC layer **95** and metal gate liner to expose the top surface of the ILD layer **92**.

At operation **30**, an etch stop layer **96** and an interlayer dielectric (ILD) layer **97** are formed over the semiconductor device **40**, as shown in FIGS. **1**L and **1**M. In some embodiments, the etch stop layer **96** may be conformally formed over the semiconductor device **40** by a blanket deposition. The etch stop layer **96** may include SiN, SiON, SiCN or any other suitable material, and may be formed by CVD, PVD, or ALD. The ILD layer **97** is formed over the etch stop layer **96**. The materials for the ILD layer **97** may include compounds comprising Si, O, C, and/or H, such as silicon oxide, SiCOH and SiOC. Organic materials, such as polymers, may be used for the ILD layer **97**. In some embodiments, the ILD layer **97** may be formed by flowable CVD (FCVD).

At operation **32**, source/drain contact features **99** and gate contact features **89** are formed as shown in FIGS. **1**N, **1**O, and **1**P. FIG. **1**N is a sectional view of the semiconductor device **40** along the line A-A in FIG. **1**O. FIG. **1**O is a sectional view of the semiconductor device **40** along the line B-B in FIG. **1**N. FIG. **1**P is a sectional view of the semiconductor device **40** along the line C-C in FIG. **1**N.

Contact holes for the source/drain contact features **99** and gate contact features **89** are formed by one or more patterning and suitable etching processes. Contact holes for the gate contact features **89** may be formed by one or more patterning and suitable etching process to remove the ILD layer **97**, the etch stop layer **96**, and the SAC layer **95**.

Contact holes for source/drain contact features **99** may be formed by one or more patterning and etch processes to remove the ILD layer **97**, the etch stop layer **96**, the ILD layer **92**, and the CESL layer **91** to expose a contact surface **87** on the epitaxial source/drain features **74**. In some embodiments, at least a portion of the epitaxial cap layer **90** is removed to expose the epitaxial source/drain feature **74** below. In some embodiments, a portion of the epitaxial source/drain feature **74** is removed so that the contact surface **87** lands at below the upper merge point **80** (shown in FIG. **1**I) to land within the merged portion of the epitaxial source/drain features **74***a*, **74***b*. Particularly, the source/drain contact holes may be formed to have the contact surface **87** located at a level between the upper merge point **80** and the lower merge point **84** to land the contact surface **87** within the merged portion of the epitaxial source/drain feature **74**. Landing the source/drain contact hole in the merged portion of the epitaxial source/drain feature **74** increases total exposed areas of the merged epitaxial source/drain feature **74**, thus, increasing contact areas and reducing contact resistance. As discussed in FIG. **1**I, the merged epitaxial source/drain features **74** according to the present disclosure has increased merged portion along the z-direction, thus providing an increased landing window for the source/drain contact holes.

After formation of the source/drain contact holes, a silicide layer **98** is selectively formed over an exposed surface of the epitaxial source/drain features **74** exposed by the source/drain contact holes. In some embodiments, the silicide layer **98** is formed on the contact surface **87**. In some embodiments, the silicide layer **98** includes one or more of WSi, CoSi, NiSi, TiSi, MoSi, and TaSi.

The source/drain contact features **99** and gate contact features **89** are then formed by filling a conductive material in the source/drain contact holes and gate contact holes. In some embodiments, the conductive material layer for the gate contact may be formed by CVD, PVD, plating, ALD, or other suitable technique. In some embodiments, the conductive material for the source/drain contact features **99** and the gate contact features **89** includes TiN, TaN, Ta, Ti, Hf, Zr, Ni, W, Co, Cu, Ag, Al, Zn, Ca, Au, Mg, Mo, Cr, or the like. Subsequently, a CMP process is performed to remove a portion of the conductive material layer above a top surface of the ILD layer **97**. As shown in FIG. **1**N, the source/drain contact feature **99** contacts the epitaxial source/drain feature **74** at the merged portion, thus, with increased contact area. As shown in FIG. **1**P, the source/drain contact feature **99** may be formed over the voids **82**.

The semiconductor device **40** discussed above includes FinFET structures. Embodiments of the present disclosure may be used in any suitable structures. FIGS. **2-4**, **5**A-**5**B, **6**A-**6**B, **7**A-**7**B, **8**A-**8**B, **9**A-**9**B, **10**A-**10**B, **11**A-**11**E, **12**A-**12**B, **13**A-**13**B, **14**A-**14**B, **15**A-**15**B, **16**A-**16**B, **17**A-**17**B, and **18**A-**18**C include methods and schematic views of manufacturing a semiconductor device including GAA structures.

FIG. **2** is a flow chart of a method **100** for manufacturing of a semiconductor device according to embodiments of the present disclosure. FIGS. **3-4**, **5**A-**5**B, **6**A-**6**B, **7**A-**7**B, **8**A-**8**B, **9**A-**9**B, **10**A-B, **11**A-**11**E, **12**A-**12**B, **13**A-**13**B, **14**A-**14**B, **15**A-**15**B, **16**A-**16**B, **17**A-**17**B, and **18**A-**18**C schematically illustrate various stages of manufacturing a semiconductor device **200** according to embodiments of the present disclosure. Particularly, the semiconductor device **200** may be manufactured according to the method **100** of FIG. **2**. FIGS. **3-4** are schematic side views of various stages of the semiconductor device **200** during fabrication.

At operation **102** of the method **100**, a plurality of channel layers and a plurality of semiconductor layers for multi-channel transistors, such as nanostructure transistors, are formed. A substrate **202** is provided to form the semiconductor device **200** thereon. The substrate **202** may include a single crystalline semiconductor material such as, but not limited to Si, Ge, SiGe, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, and InP. The substrate **202** may include various doping configurations depending on circuit design. For example, the substrate **202** may one or more p-doped regions and one or more n-doped regions. In some embodiments, the substrate **202** is a silicon (**100**) substrate.

In the example of FIG. **3**, only a portion of the substrate **202** where a N-type device is to be formed is shown. It should be noted that the substrate **202** includes other portions where other devices, such as p-type devices, resistors, capacitors, and other suitable devices in an IC are to be formed.

At operation **102**, a semiconductor stack **208** including alternating semiconductor layers **204** and semiconductor channel layers **206** are formed on the substrate **202**. The semiconductor layers **204** and semiconductor channel layers **206** have different compositions. In some embodiments, the semiconductor layer **204** and the semiconductor channel layer **206** have different oxidation rates and/or different etch selectivity. In later fabrication stages, portions of the semiconductor channel layers **206** form nanostructure channels in a multi-gate device. Three semiconductor layers **204** and three semiconductor channel layers **206** are alternately arranged as illustrated in FIG. **3** as an example. More or less semiconductor layers **204** and semiconductor channel layers **206** may be included depending on the desired number of channels in the semiconductor device to be formed. In some embodiments, the number of semiconductor layers **204** and the semiconductor channel layers **206** is between 1 and 10.

When n-type devices are to be formed over the substrate **202**, the semiconductor layer **204** may include silicon germanium (SiGe) and the semiconductor channel layer **206** may include silicon. The semiconductor layer **204** may be a SiGe layer including more than 25% Ge in molar ratio. For example, the semiconductor layer **204** may be a SiGe layer including Ge in a molar ratio in a range between 25% and 50%. In some embodiments, the semiconductor channel layer **206** may be a Ge layer. The semiconductor channel layer **206** may include n-type dopants, such as phosphorus (P), arsenic (As), etc.

The semiconductor layers **204** and the semiconductor channel layers **206** may be formed by a molecular beam epitaxy (MBE) process, a metal organic chemical vapor deposition (MOCVD) process, and/or other suitable epitaxial growth processes.

A pad layer **210** and a mask layer **212** may be formed over the semiconductor stack **208** for fin formation. The pad layer **210** may be a thin film including silicon oxide formed, for example, using a thermal oxidation process. In some embodiments, the mask layer **212** is formed of silicon nitride, for example, using low-pressure chemical vapor deposition (LPCVD). The pad layer **210** may act as an adhesion layer between the semiconductor stack **208** and the mask layer **212**. The pad layer **210** may also act as an etch stop layer for etching the mask layer **212**.

At operation **104**, fin structures **214** are formed and an isolation layer **216** is formed in the trenches between the fin structures **214**, as shown in FIG. **3**. The fin structures **214** may be formed by depositing and patterning a photoresist layer (not shown) over the mask layer **212**. The patterned photoresist layer may be used to pattern the mask layer **212**. The fin structures **214** are then formed using one or more etching processes using the patterned mask layer **212** as an etching mask. The fin structures **214** may be formed by the etching through the semiconductor stack **208** and a portion of the substrate **202**. As shown in FIG. **3**, each fin structure **214** may include a nanostructure portion **208*f*** and a well portion **202*f*** formed in the substrate **202**.

The isolation layer **216** is formed in the trenches between the fin structures **214** by a suitable deposition followed by an etch back process. In some embodiments, a semiconductor liner (not shown) may be formed over exposed portions of the fin structures **214** and the mask layers (not shown) over the fin structures **214** prior to deposition and etching back of the isolation layer **216**. The isolation layer **216** may be formed by a high-density plasma chemical vapor deposition (HDP-CVD), a flowable CVD (FCVD), or other suitable deposition process. In some embodiments, the isolation layer **216** may include silicon oxide, silicon nitride, silicon oxynitride, fluorine-doped silicate glass (FSG), a low-k dielectric, combinations thereof. In some embodiments, the isolation layer **216** is formed to cover the fin structures **214** by a suitable deposition process to fill the trenches between the fin structures **214**, a planarization process may be performed to expose the topmost semiconductor channel layer **206** and then recess etched using a suitable anisotropic etching process to expose the nanostructure portion **208*f*** of the fin structures **214**, as shown in FIG. **3**.

At operation **106**, sacrificial gate structures **226** are formed as shown in FIG. **4** and FIGS. **5**A-**5**B. FIG. **5**A is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **5**B. FIG. **5**B is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **5**A.

As shown in FIG. **4**, a sacrificial gate dielectric layer **218** is conformally formed over the substrate **202**. The sacrificial gate dielectric layer **218** is formed over the fin structures **214** and the isolation layer **216**. The sacrificial gate dielectric layer **218** may include silicon oxide, silicon nitride, a combination thereof, or the like. The sacrificial gate dielectric layer **218** may be deposited or thermally grown according to acceptable techniques, such as thermal CVD, CVD, ALD, and other suitable methods.

A sacrificial gate electrode layer **220** is deposited on the sacrificial gate dielectric layer **218** and then planarized, such as by a CMP process. The sacrificial gate electrode layer **220** includes silicon such as polycrystalline silicon, amorphous silicon, poly-crystalline silicon-germanium (poly-SiGe), or the like. In some embodiments, the sacrificial gate electrode layer **220** is subjected to a planarization operation. The sacrificial gate electrode layer **220** may be deposited using CVD, including LPCVD and PECVD, PVD, ALD, or other suitable process.

In some embodiments, a pad layer **222**, and a mask layer **224** are sequentially deposited over the sacrificial gate electrode layer **220**. The pad layer **222** may include silicon nitride. The mask layer **224** may include silicon oxide. A patterning operation is performed on the mask layer **224**, the pad layer **222**, the sacrificial gate electrode layer **220**, and the sacrificial gate dielectric layer **218** to form the sacrificial gate structures **226** using one or more etching processes, such as one or more plasma etching processes or one or more wet etching processes. In some embodiments, the mask layer **224** and pad layer **222** are first patterned using a patterning process. The sacrificial gate electrode layer **220** is then patterned using the patterned mask layer **224** and pad layer **222** as an etching mask. In some embodiments, the sacrificial gate electrode layer **220** may be etched by an anisotropic etching, such as a reactive ion etching (RIE) process. The anisotropic etching has a greater etching rate along the Z direction than etching rates along the X and Y directions. During the etching of the sacrificial gate electrode layer **220**, the sacrificial gate dielectric layer **218** on the fin structures **214** may act as an etch stop to prevent the etchant from removing the fin structures **214**.

In some embodiments, after patterning the sacrificial gate electrode layer **220**, any exposed residual sacrificial gate dielectric layer **218** is removed by a suitable etch process. In some embodiments, the residual sacrificial gate dielectric layer **218** can be etched by tuning one or more parameters, such as etchant, etching temperature, etching solution concentration, etching pressure, source power, radio frequency (RF) bias voltage, etchant flow rate, of the etch process for etching the sacrificial gate electrode layer **220**.

The sacrificial gate structure **226** covers a portion of the fin structures **214**. The portion of the fin structures **214** covered by the sacrificial gate structures **226** eventually form a channel region, including one or more channels in a FET device, such as a Fin-FET with a single channel in a fin structure, a nanostructure FET, a GAA FET, or the like.

In operation **108**, one or more sidewall spacer layers are deposited over the exposed surfaces of the semiconductor device **200** and sidewall spacers are formed, as shown in FIGS. **6**A-**6**B. FIG. **6**A is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **6**B. FIG. **6**B is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **6**A.

In FIGS. **6**A-**6**B, a spacer layer **228** and a spacer layer **230** may be formed over exposed surfaces of the semiconductor device **200**. The spacer layer **228** and the spacer layer **230** may be formed by ALD or CVD, or any other suitable method. The spacer layer **228** may include an oxide material, such as silicon oxide, and the spacer layer **230** may include a nitride material, such as silicon nitride. Alternatively, the spacer layer **230** includes another suitable dielectric material, such as silicon oxide, silicon oxynitride, or combinations thereof. The spacer layer **228** may also comprise another suitable dielectric material.

The spacer layer **228** and spacer layer **230** are formed by a suitable process. For example, the spacer layer **228** and spacer layer **230** are formed by blanket deposition sequentially. In some embodiments, an anisotropic etching may be performed to remove the spacer layer **228** and spacer layer **230** from horizontal surfaces, such that the spacer layer **228** and spacer layer **230** are positioned on sidewalls of the sacrificial gate structures **226**. As shown in FIG. **6**B, gate sidewall spacers **240** formed on sidewall of the sacrificial gate structures **226**. In this example, the gate sidewall spacers **240** include spacer layer **228** and the spacer layer **230**. The gate sidewall spacers **240** may have other suitable arrangements and/or compositions.

In some embodiments, the spacer layer **228** and spacer layer **230** may remain on exposed sidewalls of the fin structures **214** forming fin sidewall spacers. In FIG. **6**A, the fin structures **214** are denoted as fin structure **214***a*, **214***b* respectively. The fin structures **214***a*, **214***b* are neighboring fin structures. In some embodiments, the fin structures **214***a*, **214***b* are substantially symmetrical to a central line **236**. In other words, the fin structures **214***a*, **214***b* may be disposed on opposite sides of the central line **236** and at substantially equal distances from the central line **236**. The as shown in FIG. **6**A, fin sidewall spacers **232***a*, **234***a* are formed on sidewalls of the fin structure **214***a*, and fin sidewall spacers **232***b*, **234***b* are formed on sidewalls of the fin structure **214***b*. The fin sidewall spacers **232***a*, **232***b* are formed on outer sidewalls of the fin structures **214***a*, **214***b* and the fin sidewall spacers **234***a*, **234***b* are formed on inner sidewalls of the fin structures **214***a*, **214***b*. In this example, the fin side wall spacers **232***a*, **234***a*, **232***b*, **234***b* include the spacer layer **228** and the spacer layer **230**. The fin side wall spacers **232***a*, **234***a*, **232***b*, **234***b* may have other suitable arrangements and/or compositions.

In operation **110**, the fin structures **214** in source/drain region, or regions not covered by the sacrificial gate structures **234**, **234***a*, **234***b*, are recess etched, as shown in FIGS. **7**A-**7**B. FIG. **7**A is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **7**B. FIG. **7**B is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **7**A. The spacer layer **228** and the spacer layer **230** are also at least partially recessed. In some embodiments, suitable dry etching and/or wet etching may be used to remove the semiconductor channel layers **206**, the semiconductor layers **204**, together or separately. In some embodiments, the nanostructure portion **208***f* of the fin structure **214***a*, **214***b* are completely removed exposing the well portion **202***f* of the fin structures **214***a*, **214***b*. In some embodiment, a portion of the well portion **202***f* is also recessed during operation **110**. For example, the well portion **202***f* may be recessed to a level below a top surface **216***t* of the isolation layer **216**. As shown in FIG. **7**B, source/drain recesses **242** are formed on both sides of the sacrificial gate structures **226**.

In some embodiments, the fin sidewall spacers **234***a*, **232***a*, **232***b*, **234***b* are partially recessed as shown in FIG. **7**A. In some embodiments, the fin sidewall spacers **234***a*, **232***a*, **232***b*, **234***b* may be recessed during recess etch of the fin structures **214**. In other embodiments, the fin sidewall spacers **234***a*, **232***a*, **232***b*, **234***b* may be removed using a separate process. In some embodiments, heights of the fin sidewall spacers **234***a*, **232***a*, **232***b*, **234***b* may be controlled to achieve desired shape of the source/drain features to be formed from the fin structures **214**. For example, the heights of the fin sidewall spacers **234***a*, **232***a*, **232***b*, **234***b*, along the z-direction, from a top surface **216***t* of the isolation layer **216** may be controlled to define critical dimension and/or shape of the source/drain features to be formed. In some embodiments, the heights of the fin sidewall spacers **234***a*, **232***a*, **232***b*, **234***b* may be set to control location of the merge point the two source/drain features formed from the neighboring fin structures **214***a*, **214***b*. For example, the heights of the fin sidewall spacers **234***a*, **232***a*, **232***b*, **234***b* are used control the level of merge point along the z-direction.

Various factors may be considered when selecting heights of the fin sidewall spacers **234***a*, **232***a*, **232***b*, **234***b* to achieve desired shape of the source/drain features to be formed, for example, the pitch of the fin structures **214***a*, **214***b*, i.e. the distance between the fin structures **214***a*, **214***b* along the Y-axis, the width of the fin structures **214***a*, **214***b* along the Y-axis, the total height H**1** of the semiconductor stack **208**, and other relevant geometry and/or material properties of the fin structures **214***a*, **214***b* and source/drain structures to be formed.

In some embodiments, the fin sidewall spacers **234***a*, **232***a*, **232***b*, **234***b* may have the same heights. In other embodiments, the fin sidewall spacers **232***a*, **234***a* may have different heights as shown in FIG. **7**A. Similarly, the fin sidewall spacers **232***b*, **234***b* may also have different heights. In some embodiments, the fin sidewall spacers **234***a*, **234***b* are higher than the fin sidewall spacers **232***a*, **232***b*. In other embodiments, the fin sidewall spacers **234***a*, **234***b* are shorter than the fin sidewall spacers **232***a*, **232***b*. In some embodiments, heights of the fin sidewall spacers **234***a*, **232***a*, **232***b*, **234***b* maybe symmetrical to the central line **236**. For example, the fin sidewall spacers **234***a*, **234***b* may have substantially the same height and the fin sidewall spacers **232***a*, **232***b* may have substantially the same height. In some embodiments, the fin sidewall spacers **232***a*, **232***b* and the fin sidewall spacers **234***a*, **234***b* may have a height difference H**2**. The dimension of H**2** may vary according to the dimension of the semiconductor device **200**. In some embodiment, H**2** may be in a range between 5 nm and about 30 nm. In other embodiments, a ratio of H**2** over H**1** may be in a range between 0.05 and about 0.5.

In operation **112**, the semiconductor layers **204** under the gate sidewall spacers **240** are recessed etched and inner spacers **244** are formed therein, as shown in FIGS. **8**A-**8**B. FIG. **8**A is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **8**B. FIG. **8**B is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **8**A.

The semiconductor layers **204** under the gate sidewall spacers **240** are selectively etched along the horizontal direction, or x-direction, to form inner spacer cavities between the semiconductor channel layers **206**. In some embodiments, the semiconductor layer **204** can be selectively etched by using a wet etchant such as, but not limited to, ammonium hydroxide (NH_4OH), tetramethylammonium hydroxide (TMAH), ethylenediamine pyrocatechol (EDP), or potassium hydroxide (KOH) solutions.

The inner spacers **244** are formed in the inner spacer cavities by conformally deposit and then partially remove an insulating layer. The insulating layer can be formed by ALD or any other suitable method. The subsequent etch process removes most of the insulating layer except inside the cavities, resulting in the inner spacers **244**. In some embodiments, the insulating material of the inner spacers **244** is a silicon nitride-based material, such as SiN, SiON, SiOCN or SiCN and combinations thereof.

At operation **114**, an undoped epitaxial layer **246** is formed from the well portion **202***f* of the fin structure **214** between the fin sidewall spacers **232***a* and **234***a*, and between the fin sidewall spacers **232***b* and **234***b*, as shown in FIGS. **9**A-**9**B. FIG. **9**A is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **9**B. FIG. **9**B is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **9**A.

In some embodiments, a pre-clean process may be performed to remove any undesirable silicon oxide that is formed as a result of the oxidation of the exposed surfaces the source/drain recesses **242**. In some embodiments, the pre-clean process may be performed using inductively coupled plasma of a cleaning agent. In some embodiment, the cleaning agent includes Ar, NF_3, and NH_3. The pre-cleaning process may be performed in a temperature range between about 25° C. and about 250° C. for a time period between 80 seconds and about 400 seconds. Alternatively, the pre-cleaning process may be performed using an HF-based gas or a SiCoNi based gas.

In some embodiments, the undoped epitaxial layer **246** may be an epitaxial silicon layer. The undoped epitaxial layer may be formed by any suitable method, such as by CVD, CVD epitaxy, molecular beam epitaxy (MBE), or any suitable deposition technique.

In some embodiments, the undoped epitaxial layer **246** may be formed to refill the fin structure **214** between the fin sidewall spacers **232***a*, **234***a* and between the fin sidewall spacers **232***b*, **234***b*. The undoped epitaxial layer **246** may be formed to a level between below the top surface **216***t* of the isolation layer **216** and below the fin sidewall spacers **234***a*/**234***b*. For example, the undoped epitaxial layer **246** may level with the top surface **216***t* of the isolation layer **216** or a bottom of the semiconductor channel layer **206**. As shown in FIG. **9**A, a top surface **246***t* of the undoped epitaxial layer **246** is substantially level with a top surface **234***t* of the fin sidewall spacers **234***a*, **234***b*.

At operation **116**, an epitaxial transitional layer **248** is formed over the undoped epitaxial layer **246**, as shown in FIGS. **10**A-**10**B. FIG. **10**A is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **10**B. FIG. **10**B is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **10**A.

The epitaxial transitional layer **248** is formed over the undoped epitaxial layer **246**. The epitaxial transitional layer **248** may be formed by any suitable method, such as by CVD, CVD epitaxy, molecular beam epitaxy (MBE), or any suitable deposition technique. The epitaxial transitional layer **248** can serve to gradually change the lattice constant from that of the undoped epitaxial layer **246** to that of the source/drain features to be formed. In some embodiments, the epitaxial transitional layer **248** may be a semiconductor material with a lattice structure similar to the semiconductor material configured to function as a source/drain feature for a n-type device. In some embodiments, the epitaxial transitional layer **248** may be a semiconductor material includes n-type dopants at a dopant concentration lower than a dopant concentration used in a source/drain feature. The epitaxial transitional layer **248** may include one or more layers of Si, SiAs, SiP, SiC and SiCP. The epitaxial transitional layer **248** also include n-type dopants, such as phosphorus (P), arsenic (As), etc. In some embodiments, the epitaxial transitional layer **248** may be a Si layer includes arsenic dopants. In some embodiments, the epitaxial transitional layer **248** includes a dopant concentration in a range between about 15E19 atoms/cm^3 and about 5E20 atoms/cm^3.

The epitaxial transitional layer **248** may have a thickness H**3** in a range between about 3 nm and about 15 nm. If the thickness of the epitaxial transitional layer **248** is below 3 nm, the epitaxial transitional layer **248** may not be thick enough to function as lattice transitional layer between the undoped epitaxial layer **246** and the source/drain features to be formed. If the thickness of epitaxial transitional layer **248** is greater than 15 nm, the epitaxial transitional layer **248** may be in contact with the semiconductor channel layers **206** and affect the device function and without obvious additional advantages for crystalline structural transition. In some embodiments, a top surface **248***t* of the epitaxial transitional layer **248** is below the semiconductor channel layers **206** of the semiconductor stack **208**. In some embodiments, the top surface **248***t* of the epitaxial transitional layer **248** may be substantially level with a top surface of the higher one of the fin sidewall spacers **232***a*/**232***b* and **234***a*/**234***b*. As shown in FIG. **10**A, the top surface **248***t* of the epitaxial transitional layer **248** is substantially level with a top surface **232***t* of the fin sidewall spacers **232***a*, **232***b*. In some embodiments, the height difference between the fin sidewall spacers **232***a*/**232***b* and **234***a*/**234***b*, the epitaxial transitional layer **248** may result in the top surface **248***t* that is lob sided towards the central line **236**, enabling formation of merged source/drain features to be formed.

In some embodiments, the epitaxial transitional layer **248** may be grown in an epitaxial chamber by a suitable process. For example, the epitaxial transitional layer **248** is formed by a selective etching growth process, as described with the operation **20** in the method **10**.

At operation **118**, epitaxial source/drain features **250** are formed over the epitaxial transitional layer **248**, as shown in FIGS. **11**A-**11**B. FIG. **11**A is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **11**B. FIG. **11**B is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **11**A. FIG. **11**C is a partial enlarged view of FIG. **11**A showing the epitaxial source/drain features **250**.

The epitaxial source/drain features **250** are formed over the epitaxial transitional layer **248**. The epitaxial source/drain features **250** may be formed by any suitable method, such as by CVD, CVD epitaxy, molecular beam epitaxy (MBE), or any suitable deposition technique. The epitaxial source/drain features **250** may include one or more layers of Si, SiP, SiC and SiCP. The epitaxial source/drain features **250** also include n-type dopants, such as phosphorus (P), arsenic (As), etc. In some embodiments, the epitaxial source/drain features **250** may be a Si layer including phosphorus dopants. The dopant concentration in the epitaxial source/drain features **250** is higher than that of the epitaxial transitional layer **248**. In some embodiments, the epitaxial source/drain features **250** include a dopant concentration of between about 1E20 atoms/cm^3 and about 5E21 atoms/cm^3.

The epitaxial source/drain features **250** may have a height H**4** in a range between about 30 nm and about 70 nm or a thickness enough for side surfaces **250***s* of the epitaxial features **250** to cover all of the semiconductor channel layers **206** in the semiconductor stack **208**. In some embodiments, a top surface **248***t* of the epitaxial transitional layer **248** is below the semiconductor channel layers **206** of the semiconductor stack **208**.

In some embodiments, the epitaxial source/drain features **250** may be grown in an epitaxial chamber by a suitable process. For example, the epitaxial source/drain features **250** are formed by a selective etching growth process, as described with the operation **22** in the method **10**.

Because of the epitaxial process parameters at operation **118** and the height selection of the fin sidewall spacers **232***a*, **234***a*, **234***b*, **232***b*, the epitaxial source/drain features **250** grown from the fin structures **214***a* and **214***b* merged along the central line **236**. As shown in FIG. **11**C, the epitaxial source/drain feature **250***a* grown from the fin structure **214***a* and the epitaxial source/drain feature **250***b* grown from the fin structure **214***b* merge together to form one epitaxial source/drain feature **250**. The merged epitaxial source/drain feature **250** may have a top surface **252** and a bottom surface **254** opposing the top surface **252**. The sidewalls **250***s* connect the top surface **252** and the bottom surface **254**. The epitaxial source/drain features **250***a*, **250***b* merge substantially along the central line **236**. The epitaxial source/drain features **250***a*, **250***b* are merged from a lower merge point **260** on the bottom surface **254** and an upper merge point **256** on the top surface **252**. The lower merge point **260** and the top merge point **256** are at different vertical levels along the Z-direction. A merge length in the z-direction from the lower merge point **260** to the upper merge point **256** is denoted by H**5**. In some embodiments, a ratio of the merge length H**5** and the height H4 is in a range between about 65% and about 80%. The merge height H5 is about 50% to 70% of the non-merge height, or the height above the upper merge point **256** and below the lower merge point **260**.

In some embodiments, the shapes of the epitaxial source/drain features **250***a*, **250***b* are tuned such that the epitaxial source/drain features **250***a*, **250***b* are "just" merge to allow the epitaxial source/drain features **250***a*, **250***b* substantially retain the natural shapes from epitaxial growth without merging. The "just" merge arrangement allows the epitaxial source/drain features **250***a*, **250***b* to merge yet substantially maintain "natural" or "unmerged" source/drain feature volume.

As shown in FIG. **11**C, the top surface **252** may be a wavy surface having peak points **262**, **264** defining a valley therebetween. The upper merge point **256** coincides with the valley point between the peak points **262**, **264**. A wavy height H**6** is defined by a distance from the valley point to the peak points **262**, **264**. In some embodiments, a ratio of the wavy height H**6** over the total height H**4** is in a range between about 5% and about 35%.

In some embodiments, one or more voids **258** are formed along the merge line or the central line **236** as the "just" merge arrangement. The one or more voids **258** may be filled with air or gas, such as hydrogen, helium, or other suitable gas. In some embodiments, the voids **258** may have a shape of circular, elliptical, parabolic, or triangular in the z-y plane. In some embodiments, the voids **258** may have a radius in a range between about 0.5 nm and about 3 nm. In some embodiments, the void **258** may be located along the central line **236** about 3 nm to 7 nm below the upper merge point **256**. The merging of the epitaxial source/drain features **250***a*, **250***b* also result a void **267** between the bottom surface **254** and the isolation layer **216**. The void **267** may be filled with air or gas, such as hydrogen, helium, or other suitable gas

FIGS. **11**D and **11**E are schematic layout views of the semiconductor device **200** showing various positions and shapes of the voids **258** in the merged epitaxial source/drain features **250**. As shown in FIG. **11**D, the voids **258** may extend along the x-direction across the merged epitaxial source/drain features **250**. Alternatively, the voids **258** may be located in a central portion of the epitaxial source/drain features **250**. As shown in FIG. **11**E, voids **258***a*, **258***b*, **258***c* of various cross-sectional shapes in the x-y plane are located within the epitaxial source/drain features **250**. Particularly, a void with a triangle shaped cross section in the y-z plane (shown in FIG. **11**A) may have a square or rectangular shaped cross section in the x-y plane as shown in the void **258***a* in FIG. **11**E. A void with a cone or hyperbolic shaped cross section in the y-z plane (shown in FIG. **11**A) may have an oval or circular shaped cross section in the x-y plane as shown in the void **258***b* in FIG. **11**E. A void with an oval or elliptical shaped cross section in the y-z plane (shown in FIG. **11**A) may have a hexagonal shaped cross section in the x-y plane as shown in the void **258***c* in FIG. **11**E.

At operation **120**, an epitaxial cap layer **266** is formed over the epitaxial source/drain features **250**, as shown in

FIGS. **12A-12B**. FIG. **12A** is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **12B**. FIG. **12B** is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **12A**.

The epitaxial cap layer **266** is formed on the exposed surfaces of the epitaxial source/drain features **250**. The epitaxial cap layer **266** may be formed by any suitable method, such as by CVD, CVD epitaxy, molecular beam epitaxy (MBE), or any suitable deposition technique. The epitaxial cap layer **266** may include one or more layers of Si, SiP, SiC and SiCP. The epitaxial cap layer **266** also include n-type dopants, such as phosphorus (P), arsenic (As), etc. In some embodiments, the epitaxial cap layer **266** may be a Si layer including phosphorus dopants. In some embodiments, the epitaxial cap layer **266** includes a dopant concentration of between about 1E21 atoms/cm^3 and about 2E21 atoms/cm^3.

The epitaxial cap layer **266** may have a thickness along the z-direction in a range between about 3 nm and about 10 nm. The epitaxial cap layer **266** maintains a wavy shape over the top surface **252** of the merged epitaxial source/drain feature **250**.

In some embodiments, the epitaxial cap layer **266** may be grown in an epitaxial chamber by a suitable process. For example, the epitaxial cap layer **266** is formed by a selective etching growth process as described with the operation **24** in the method **10**.

In some embodiments, the epitaxial deposition at operations **114**, **116**, **118**, and **120** may be performed in the same epitaxial deposition chamber.

At operation **122**, a contact etch stop layer (CESL) **268** and an interlayer dielectric (ILD) layer **270** are formed over the semiconductor device **200**, as shown in FIGS. **13A-13B**. FIG. **13A** is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **13B**. FIG. **13B** is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **13A**.

The CESL **268** is conformally formed over exposed surfaces of the semiconductor device **200**. The CESL **268** is formed on the epitaxial cap layer **266**, the gate sidewall spacers **240**, the fin sidewall spacers **232*a***, **232*b***, and the isolation layer **216** if exposed. The CESL **268** may include SiN, SiON, SiCN or any other suitable material, and may be formed by CVD, PVD, or ALD.

The interlayer dielectric (ILD) layer **270** is formed over the CESL **268**. The materials for the ILD layer **270** include compounds comprising Si, O, C, and/or H, such as silicon oxide, SiCOH and SiOC. Organic materials, such as polymers, may be used for the ILD layer **270**. In some embodiments, the ILD layer **270** may be formed by flowable CVD (FCVD). The ILD layer **270** protects the epitaxial source/drain features **250** during the removal of the sacrificial gate structures **226**.

At operation **124**, replacement gate structures **278** are formed, as shown in FIGS. **14A-14B**. FIG. **14A** is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **14B**. FIG. **14B** is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **14A**.

The sacrificial gate dielectric layer **218** and sacrificial gate electrode layer **220** are removed by one or more suitable process, such as dry etch, wet etch, or a combination thereof, to expose the semiconductor stack **208** underneath the sacrificial gate structures **226**. In some embodiments, a wet etchant such as a tetramethylammonium hydroxide (TMAH) solution is used.

The semiconductor layers **204** are then removed by one or more suitable etching process to expose the semiconductor channel layers **206** and form gate cavities around the semiconductor channel layers **206**.

The replacement gate structures **278** are formed around the semiconductor channel layers **206**, as shown in FIG. **14B**. In some embodiments, the replacement gate structure **278** includes a gate dielectric layer **272** and a gate electrode layer **274**. Optionally, the replacement gate structure **278** may include a self-aligned contact (SAC) layer **276**.

The gate dielectric layer **272** may be conformally deposited on exposed surfaces in the gate cavities. The gate dielectric layer **272** may have different composition and dimensions for N-type devices and P-type devices and are formed separately using patterned mask layers and different deposition recipes. The gate dielectric layer **272** may include one or more layers of a dielectric material, such as silicon oxide, silicon nitride, or high-k dielectric material, other suitable dielectric material, and/or combinations thereof. Examples of high-k dielectric material include HfO_2, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, zirconium oxide, aluminum oxide, titanium oxide, hafnium dioxide-alumina (HfO_2—Al_2O_3) alloy, other suitable high-k dielectric materials, and/or combinations thereof. The gate dielectric layer **272** may be formed by CVD, ALD or any suitable method.

The gate electrode layer **274** is then formed on the gate dielectric layer **272** to fill the gate cavities. The gate electrode layer **274** may include one or more layers of conductive material, such as polysilicon, aluminum, copper, titanium, tantalum, tungsten, cobalt, molybdenum, tantalum nitride, nickel silicide, cobalt silicide, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, metal alloys, other suitable materials, and/or combinations thereof. In some embodiments, the gate electrode layer **274** may be formed by CVD, ALD, electro-plating, or other suitable method. After the formation of the gate electrode layer **274**, a planarization process, such as a CMP process, is performed to remove excess deposition of the gate electrode material and expose the top surface of the ILD layer **270**.

In some embodiments, a metal gate etching back (MGEB) process is performed to form the self-aligned contact (SAC) layer **276**. One or more etching processes are performed to remove portions of the gate dielectric layer **272** and the gate electrode layer **274** to form trenches in the region above the remaining gate electrode layer **274**. The MGEB process may be a plasma etching process employing one or more etchants such as chlorine-containing gas, a bromine-containing gas, and/or a fluorine-containing gas. The etching process allows the gate dielectric layer **272** and the gate electrode layer **274** to be selectively etched from the ILD layer **270** and the CESL **268**.

In the MGEB process, the gate dielectric layer **272** and gate electrode layer **274** are etched back to a level lower than a top surface of high-k dielectric features formed on hybrid fins (not shown) parallel to the fin structures **214**. In some embodiments, the gate sidewall spacers **240** are also etched back to a level be lower than the CESL **268** and higher than the gate electrode layer **274**.

In some embodiments, a metal gate liner, not shown, may be first deposited on exposed surfaces in the trenches above the gate electrode layer **274** prior to depositing the SAC layer **276**. The metal gate liner and the SAC layer **276** may be formed by a suitable deposition process, such as CVD, PVD, or ALD. The metal gate liner may function as a diffusion barrier for the gate electrode layer **274**. The metal gate liner may be a dielectric layer including but not limited to SiO, SiN, SiC, SiCN, SiOC, SiON, SiOCN, ZrO, ZrN, or a combination thereof. The SAC layer **276** may be any dielectric layer that can be used as an etch stop layer during subsequent trench and via patterning for metal contacts. In some embodiments, the SAC layer **276** may a high-k dielectric layer. The SAC layer **276** may a dielectric layer including but not limited to SiO, HfSi, SiOC, AlO, ZrSi, AlON, ZrO, HfO, TiO, ZrAlO, ZnO, TaO, LaO, YO, TaCN, SiN, SiOCN, Si, SiOCN, ZrN, SiCN, or any combinations thereof.

After filling the trenches with the SAC layer **276**, a planarization process, such as a CMP process, is performed to remove excess deposition of the SAC layer **276** and metal gate liner to expose the top surface of the ILD layer **270**.

At operation **126**, an etch stop layer **280** and an interlayer dielectric (ILD) layer **282** are formed over the semiconductor device **200**, as shown in FIGS. **15A-15B**. FIG. **15A** is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **15B**. FIG. **15B** is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **15A**.

In some embodiments, the etch stop layer **280** may be conformally formed over the semiconductor device **200** by a blanket deposition. The etch stop layer **280** may include SiN, SiON, SiCN or any other suitable material, and may be formed by CVD, PVD, or ALD.

The ILD layer **282** is formed over the etch stop layer **280**. The materials for the ILD layer **282** may include compounds comprising Si, O, C, and/or H, such as silicon oxide, SiCOH and SiOC. Organic materials, such as polymers, may be used for the ILD layer **282**. In some embodiments, the ILD layer **282** may be formed by flowable CVD (FCVD).

At operation **128**, source/drain contact holes **284** and gate contact holes **286** are formed, as shown in FIGS. **16A-16B**. FIG. **16A** is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **16B**. FIG. **16B** is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **16A**.

The source/drain contact holes **284** may be formed by one or more patterning and etch processes to remove the ILD layer **282**, the etch stop layer **280**, the ILD layer **270**, and the CESL layer **268** to expose the epitaxial source/drain features **250**. In some embodiments, at least a portion of the epitaxial cap layer **266** is removed to expose the epitaxial source/drain feature **250** below.

In some embodiments, a portion of the epitaxial source/drain feature **250** is removed so that the contact surface **288** lands at below the upper merge point **256** (shown in FIG. **11C**) to land within the merged portion of the epitaxial source/drain features **250***a*, **250***b*. Particularly, the source/drain contact holes **284** may be formed to have the contact surface **288** located at a level between the upper merge point **256** and above the lower merge point **260** to land the contact surface **288** within the merged portion of the epitaxial source/drain feature **250**. Landing the source/drain contact hole **284** in the merged portion of the epitaxial source/drain feature **250** increases total exposed areas of the merged epitaxial source/drain feature **250**, thus, increasing contact areas and reducing contact resistance. As discussed in FIG. **11C**, the merged epitaxial source/drain features **250** according to the present disclosure has increased merged portion along the z-direction, thus providing an increased landing window for the source/drain contact holes **284**.

The gate contact holes **286** may be formed by one or more patterning and suitable etching process to remove the ILD layer **282**, the etch stop layer **280**, and the SAC layer **276**.

In operation **130**, source/drain contact features **292** and gate contact features **294** are formed as shown in FIGS. **17A-17B**, and FIGS. **18A-18C**. FIG. **17A** is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **17B**. FIG. **17B** is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **17A**. FIG. **18A** is a sectional view of the semiconductor device **200** along the line A-A in FIG. **4** and FIG. **18B**. FIG. **18B** is a sectional view of the semiconductor device **200** along the line B-B in FIG. **4** and FIG. **18A**. FIG. **18C** is a sectional view of the semiconductor device **200** along the line C-C in FIG. **18A**.

After formation of the source/drain contact holes **284**, a silicide layer **290** is selectively formed over an exposed surface of the epitaxial source/drain features **250** exposed by the source/drain contact holes **284**. In some embodiments, the silicide layer **290** is formed on the contact surface **288**. In some embodiments, the silicide layer **290** includes one or more of WSi, CoSi, NiSi, TiSi, MoSi, and TaSi.

The source/drain contact features **292** and gate contact features **294** are then formed by filling a conductive material in the source/drain contact holes **284** and gate contact holes **286**. In some embodiments, the conductive material layer for the gate contact may be formed by CVD, PVD, plating, ALD, or other suitable technique. In some embodiments, the conductive material for the source/drain contact features **292** and the gate contact features **294** includes TiN, TaN, Ta, Ti, Hf, Zr, Ni, W, Co, Cu, Ag, Al, Zn, Ca, Au, Mg, Mo, Cr, or the like. Subsequently, a CMP process is performed to remove a portion of the conductive material layer above a top surface of the ILD layer **282**. As shown in FIG. **18A**, the source/drain contact feature **292** contacts the epitaxial source/drain feature **250** at the merged portion, thus, with increased contact area. As shown in FIG. **18C**, the source/drain contact feature **292** may be formed over the voids **258**.

Even though source/drain structures in the example above are formed from two fin structures, embodiments of the present disclosure may be extended to forming merged source/drain features from two or more fin structures. It should be noted that the semiconductor device **200** may include other type of devices, such as the p-type devices, and various operations may be performed before, after, in between the operations of the method **100** to fabricate the other type of devices.

Various embodiments or examples described herein offer multiple advantages over the state-of-art technology. Embodiments of the present disclosure provide an epitaxial source/drain feature with one or more voids formed therein. The voids result from barely merging two epitaxial source/drain features grown from two fins. By barely merging two epitaxial source/drain features, the result source/drain feature benefit from the merging without obvious reduction of total volume of the epitaxial feature. Merging two epitaxial source/drain features provides an increased contact surface between the source/drain feature and source/drain contact, thus, reducing the source/drain contact resistance.

Some embodiments of the present disclosure provide a semiconductor device. The semiconductor device includes, a first fin, a second fin, a first epitaxial source/drain feature extending from the first fin, and a second epitaxial source/drain feature extending from the second fin, wherein the first and second epitaxial source/drain features are merged at a first level and at a second level, and a void is defined by the first and second epitaxial features at a third level between the first level and the second level.

Some embodiments of the present disclosure provide a semiconductor device. The semiconductor device includes a source/drain feature including a top surface, a bottom surface opposite the top surface, and a side surface connecting the top surface and bottom surface, wherein a first void is formed between the top surface and the bottom surface, and one or more semiconductor channels in contact with the side surface of the source/drain feature.

Some embodiments of the present disclosure provide a method for forming a semiconductor device. The method includes forming a first fin and a second fin adjacent the first fin, forming a sacrificial gate structure across the first and second fins, recess etching the first and second fins exposed by the sacrificial gate structure, and forming first and second epitaxial source/drain features from the first and second fins respectively, wherein the first and second epitaxial source/drain features are merged at a first level and at a second level, and a void is formed between the first and second levels.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

The invention claimed is:

1. A method for manufacturing a semiconductor device, comprising:

forming a first fin and a second fin adjacent the first fin;

forming a sacrificial gate structure across the first and second fins;

recess etching the first and second fins exposed by the sacrificial gate structure; and

forming first and second epitaxial source/drain features from the first and second fins respectively, wherein the first and second epitaxial source/drain features are merged at a first level and at a second level, and a void is formed between the first and second levels.

2. The method of claim **1**, further comprising:

forming fin sidewall spacers on sidewalls of the first and second fins; and

recess etching the fin sidewall spacers to selected heights to enable the first and second epitaxial source/drain features to merge, and the first fin and second fin are recessed below the fin sidewall spacers.

3. The method of claim **2**, further comprising:

growing an epitaxial transitional layer over the first fin and the second fin to cover the fin sidewall spacers, wherein the first and second epitaxial source/drain features are formed from the epitaxial transitional layer on the first fin and second fin respectively.

4. The method of claim **3**, wherein the epitaxial transitional layer includes SiAs.

5. The method of claim **3**, further comprising:

growing an undoped epitaxial layer on the first fin and the second fin prior to growing the epitaxial transitional layer.

6. The method of claim **3**, further comprising:

forming an epitaxial cap layer over the first and second epitaxial source/drain features.

7. The method of claim **6**, further comprising:

forming a source/drain contact hole by etching back the epitaxial cap layer and the first and second epitaxial source/drain features to a level below the first level.

8. A method, comprising:

forming a first fin and a second fin parallel to the first fin on a substrate;

forming an isolation layer on the substrate, wherein the first and second fins extend over the isolation layer;

forming a sacrificial gate structure across the first and second fins and the isolation layer;

forming a sidewall spacer layer on sidewalls of the first and second fins;

recess etching the first and second fins exposed by the sacrificial gate structure;

forming first and second epitaxial source/drain features from the first and second fins respectively, wherein the first and second epitaxial source/drain features are merged between a first level and at a second level;

depositing an epitaxial cap layer over the first and second epitaxial source/drain features;

depositing a CESL (contact etch stop layer) over the epitaxial cap layer;

forming an ILD (inter layer dielectric) layer over the CESL;

forming a contact opening through the ILD layer, the CESL layer, and the epitaxial cap layer to expose the first and second epitaxial source/drain features; and

forming a source/drain contact feature in the contact opening.

9. The method of claim **8**, further comprising:

forming a first epitaxial transitional layer between the first fin and the first epitaxial source/drain feature, a second epitaxial transitional layer between the second fin and the second epitaxial source/drain feature.

10. The method of claim **9**, wherein recess etching the first and second fins comprises etching the sidewall spacer layer so that first and second fin sidewall spacers remaining on opposing sides of the first fin, and third and fourth fin sidewall spacers remaining on opposing sides of the second fin, the first epitaxial transitional layer is formed between the first and second fin sidewall spacers, and the second epitaxial transitional layer is formed between the third and fourth fin sidewall spacers.

11. The method of claim **10**, wherein the merged first and second epitaxial source/drain features have a wavy top surface above the first level.

12. The method of claim **11**, wherein depositing the epitaxial cap layer comprises performing a selective etching growth process by introducing a reactant gas including deposition agent and etchant together.

13. The method of claim **12**, wherein the source/drain contact feature is in connection with the first and second epitaxial source/drain features through a contact surface, and the contact surface is at a level below the first level.

14. The method of claim **12**, further comprising:

forming a first undoped epitaxial layer between the first fin and first epitaxial transitional layer, and a second undoped epitaxial layer between the second fin and second epitaxial transitional layer.

15. A method, comprising:

forming a first semiconductor fin and a second semiconductor fin;

forming a sacrificial gate structure across the first and second semiconductor fins;

forming a sidewall spacer layer on sidewalls of the first and second semiconductor fins;

recess etching the first and second semiconductor fins exposed by the sacrificial gate structure;

forming an epitaxial source/drain feature from the first and second fins, wherein the epitaxial source/drain feature includes a top surface, a bottom surface opposite the top surface, and a side surface connecting the top surface and bottom surface, a first void is formed between the top surface and the bottom surface;

depositing a CESL (contact etch stop layer) over the epitaxial source/drain feature;

forming an ILD (inter layer dielectric) layer over the CESL;

forming a contact opening through the ILD layer and the CESL layer to expose the epitaxial source/drain feature; and

forming a source/drain contact feature in the contact opening;

wherein each of the first and second semiconductor fin comprises two or more channel layers and two or more sacrificial semiconductor layers alternately arranged with the two more channel layers.

16. The method of claim **15**, wherein a second void is defined between the first and second semiconductor fins and exposed to the bottom surface of the source/drain feature.

17. The method of claim **16**, wherein forming the epitaxial source/drain feature comprises:

forming a first epitaxial material, wherein the first epitaxial material includes the first void formed therein and defines a portion of the bottom surface; and

forming a second epitaxial material in contact with the first epitaxial material, wherein the second epitaxial material defines at least a portion of the top surface.

18. The method of claim **17**, further comprising:

forming a third epitaxial material between the first epitaxial material and the first semiconductor fin.

19. The method of claim **15**, wherein the top surface of the source/drain feature is a wavy surface having a valley point between a first peak and a second peak, and the first void is substantially aligned with the valley point.

20. The method of claim **19**, wherein a wavy height is measured from the first peak to the valley point, a total height is measured from the first peak to the bottom surface, and a ratio of the wavy height over the total height is in a range between about 5% and about 35%.

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