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(54) **MEMORY DEVICE HAVING 2-TRANSISTOR VERTICAL MEMORY CELL AND WRAPPED DATA LINE STRUCTURE**

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(21) Appl. No.: **18/623,956**

(22) Filed: **Apr. 1, 2024**

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(60) Continuation of application No. 18/126,679, filed on Mar. 27, 2023, now Pat. No. 11,950,426, which is a division of application No. 17/514,979, filed on Oct. 29, 2021, now Pat. No. 11,616,073.

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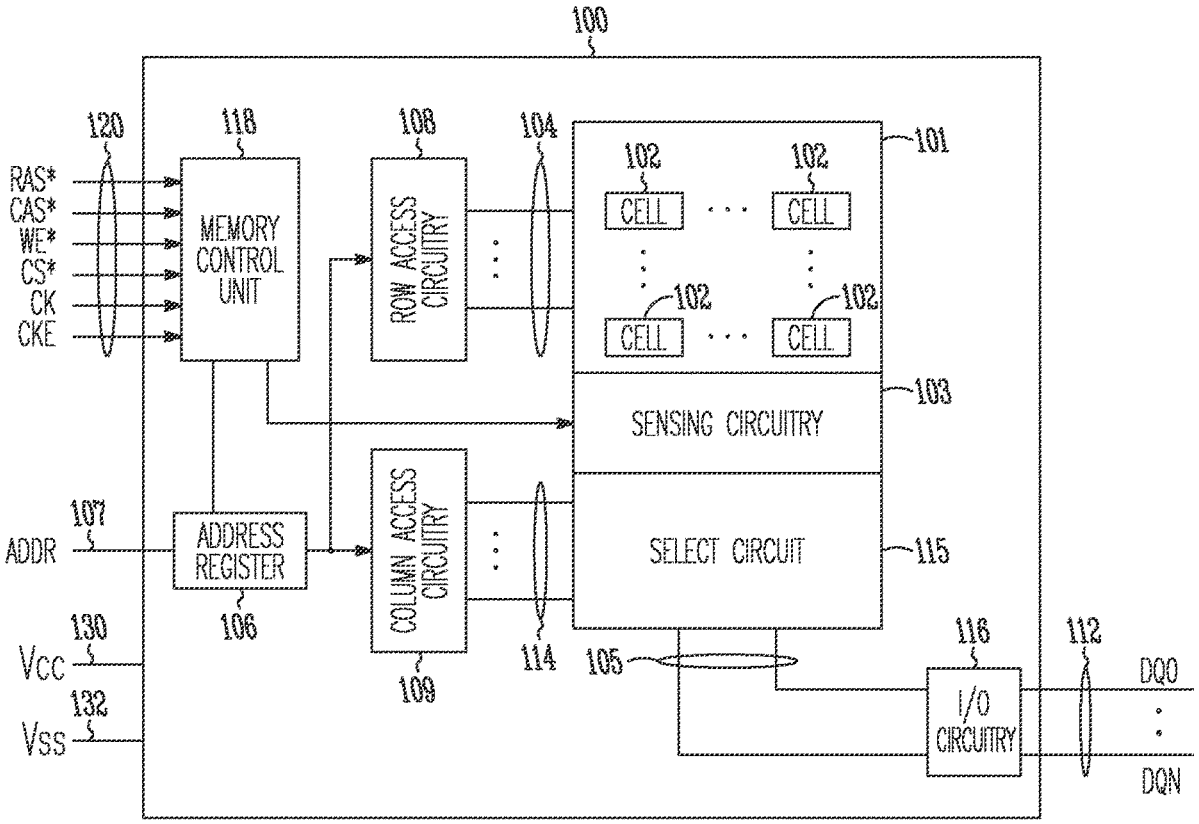
H01L 29/423 (2006.01)

(52) **U.S. Cl.**
CPC ***H10B 43/50*** (2023.02); ***H01L 29/1062*** (2013.01); ***H01L 29/42396*** (2013.01)

(57) **ABSTRACT**

Some embodiments include apparatuses and methods forming the apparatuses. One of the apparatuses includes a first transistor including a first channel region, and a charge storage structure separated from the first channel region; a second transistor including a second channel region formed over the charge storage structure; and a data line formed over and contacting the first channel region and the second channel region, the data line including a portion adjacent the first channel region and separated from the first channel region by a dielectric material.



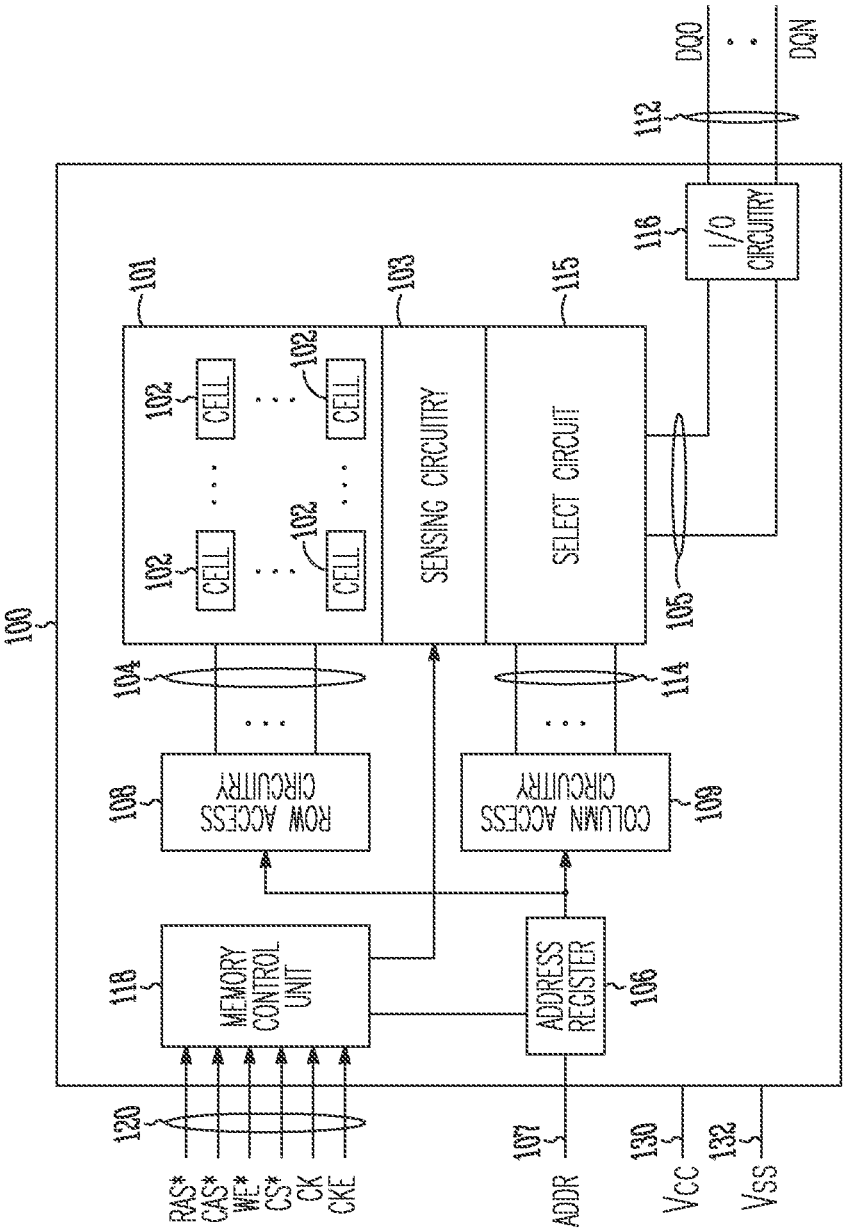

100
101
102
CELL
103
SENSING CIRCUITRY
115
SELECT CIRCUIT
105
104
114
108
ROW ACCESS CIRCUITRY
109
COLUMN ACCESS CIRCUITRY
118
MEMORY CONTROL UNIT
106
ADDRESS REGISTER
116
I/O CIRCUITRY
112
DQ0
DQN
120
RAS*
CAS*
WE*
CS*
CK
CKE
107
ADDR
130
VCC
132
VSS

FIG. 1

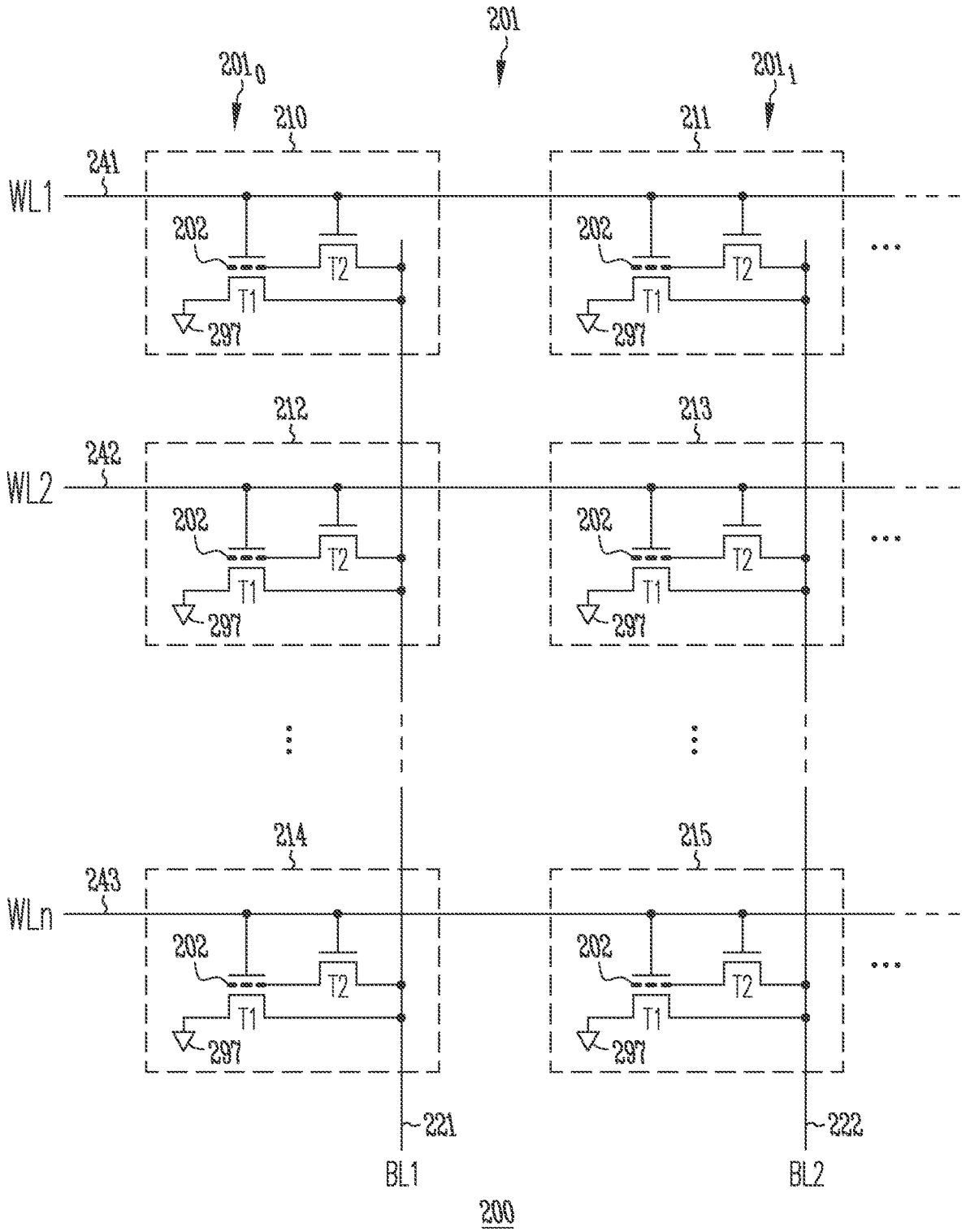

201
201 0
201 1
210
211
212
213
214
215
241
242
243
WL1
WL2
WLn
202
T1
T2
297
221
222
BL1
BL2
200

FIG.2

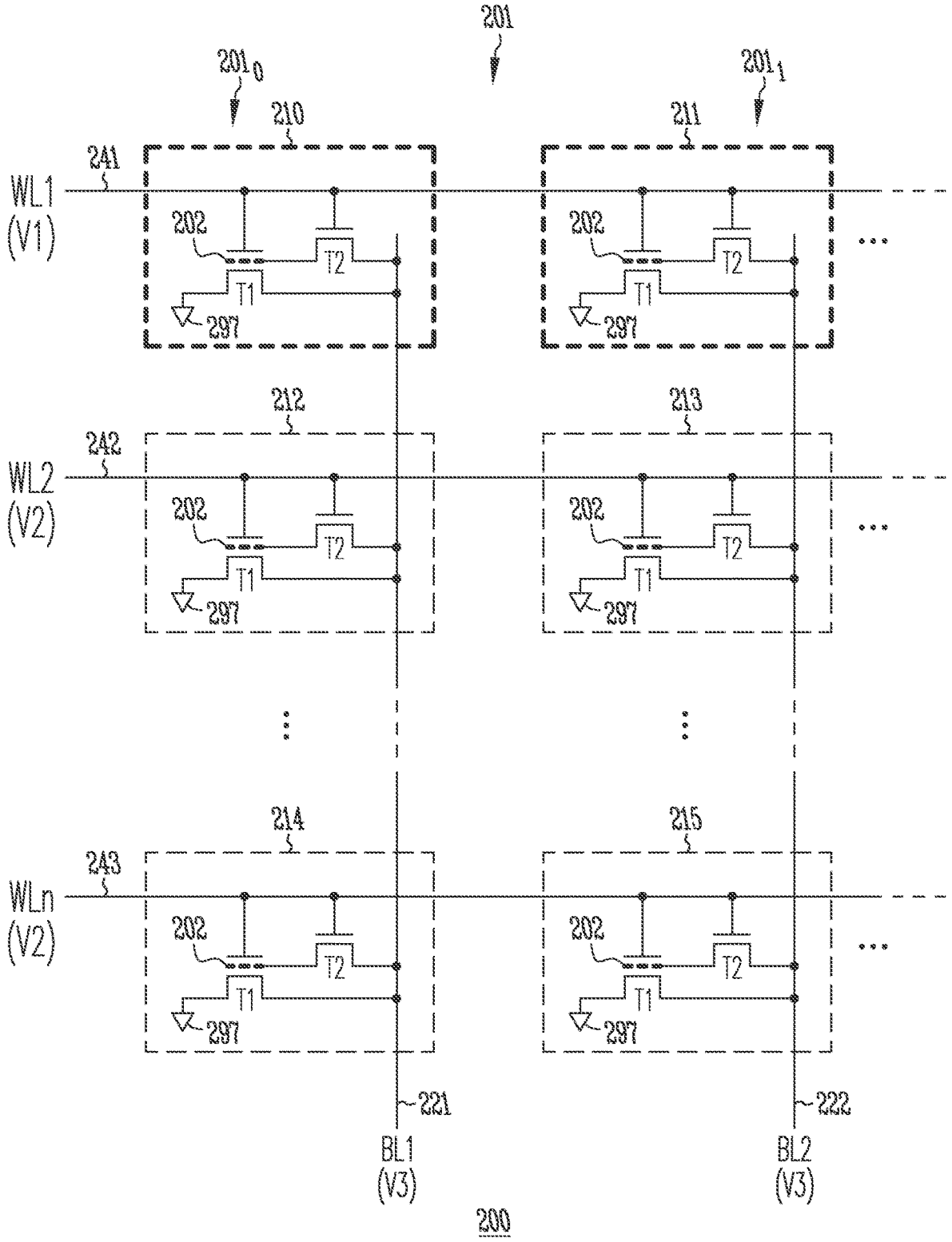

201
201 0
201 1
210
211
212
213
214
215
241
242
243
WL1
(V1)
WL2
(V2)
WLn
(V2)
202
T1
T2
297
221
222
BL1
(V3)
BL2
(V3)
200

FIG. 3

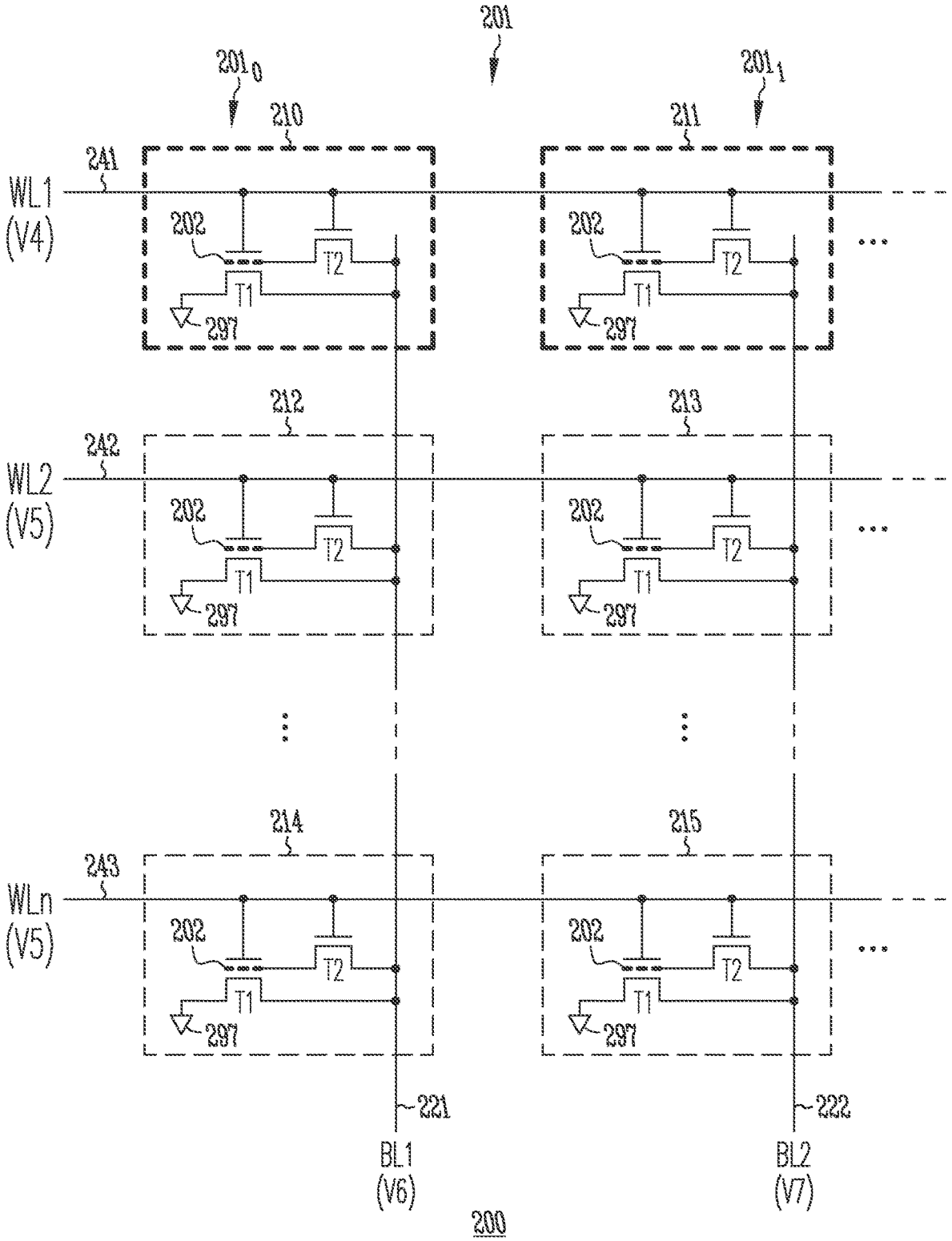

201
201 0
201 1
210
211
212
213
214
215
241
242
243
WL1
(V4)
WL2
(V5)
WLn
(V5)
202
T1
T2
297
221
222
BL1
(V6)
BL2
(V7)
200

FIG. 4

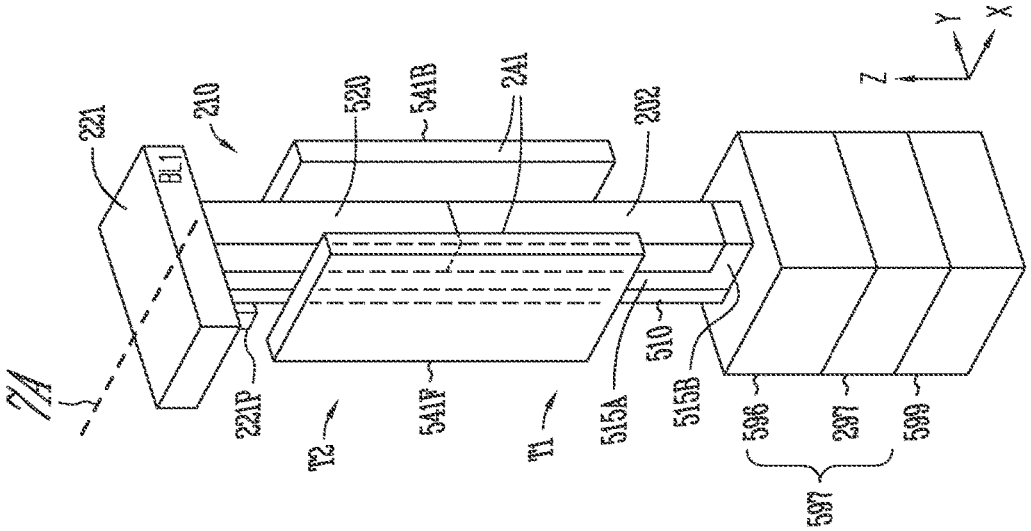

7A
221
BL1
210
520
541B
241
202
Z
Y
X
221P
T2
541F
T1
515A
510
515B
596
597
599
597
200

FIG. 6

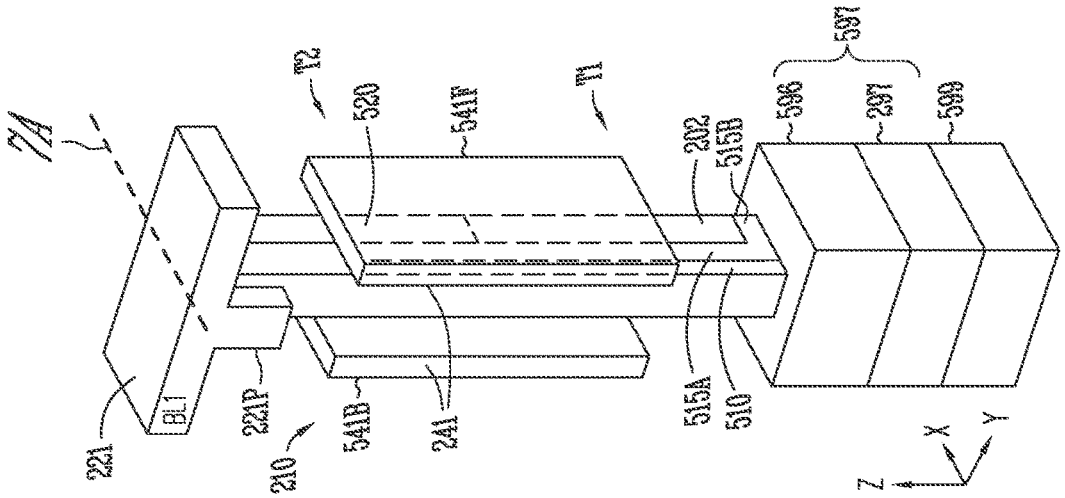

7A
T2
520
541F
T1
202
515B
596
597
599
597
221
BL1
221P
210
541B
241
515A
510
Z
X
Y
200

FIG. 5

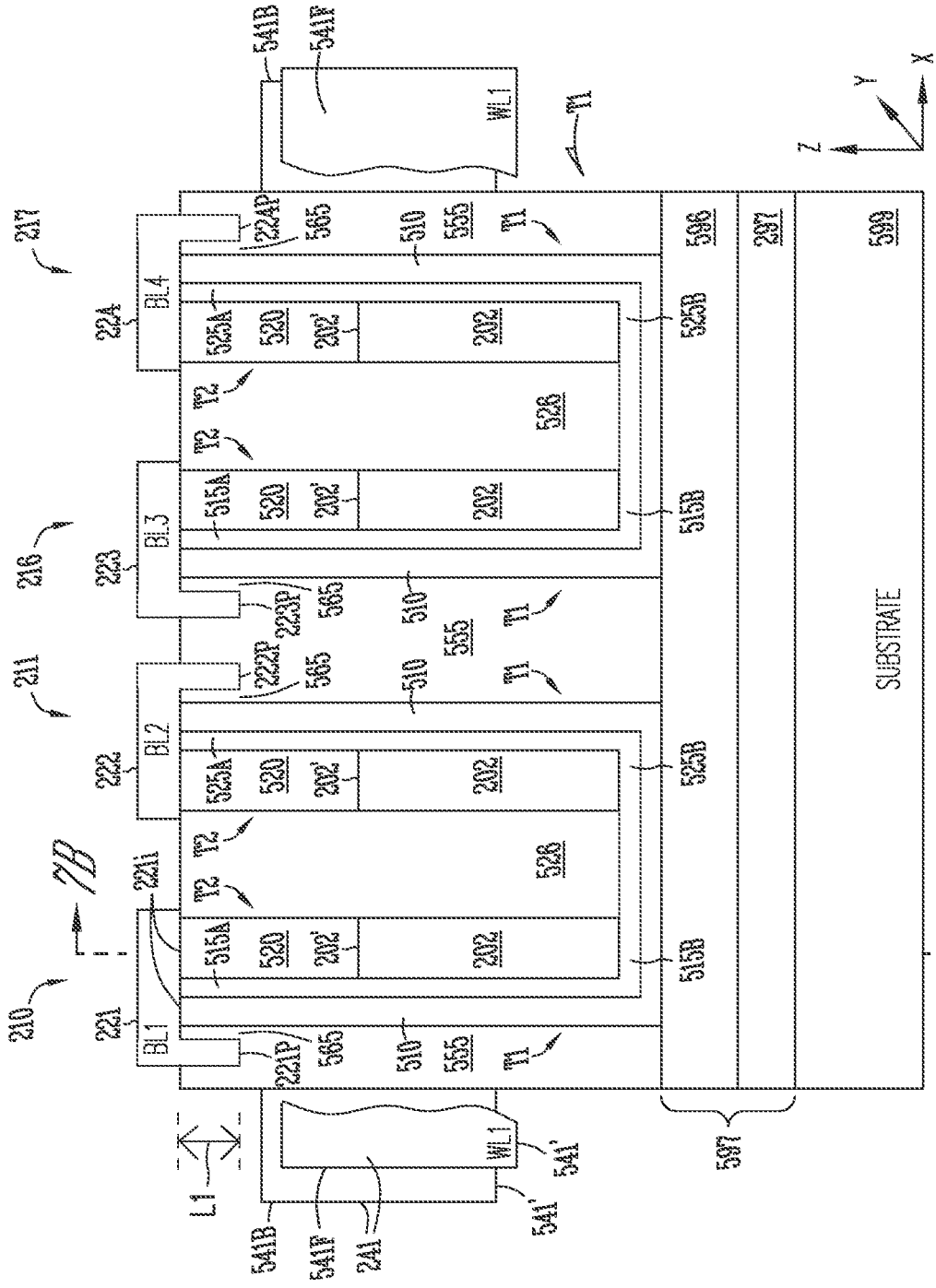

541B
541F
WL1
T1
Z
Y
X
217
224P
565
510
555
T1
596
207
599
224
BL4
525A
520
202'
202
525B
T2
T2
526
216
223
BL3
515A
520
202'
202
515B
223P
565
510
555
T1
211
222P
565
510
555
T1
222
BL2
525A
520
202'
202
525B
7B
221i
T2
T2
526
7B
210
221
BL1
515A
520
202'
202
515B
221P
565
510
555
T1
SUBSTRATE
200
L1
WL1
541'
597
541B
541F
241
541'

FIG. 7A

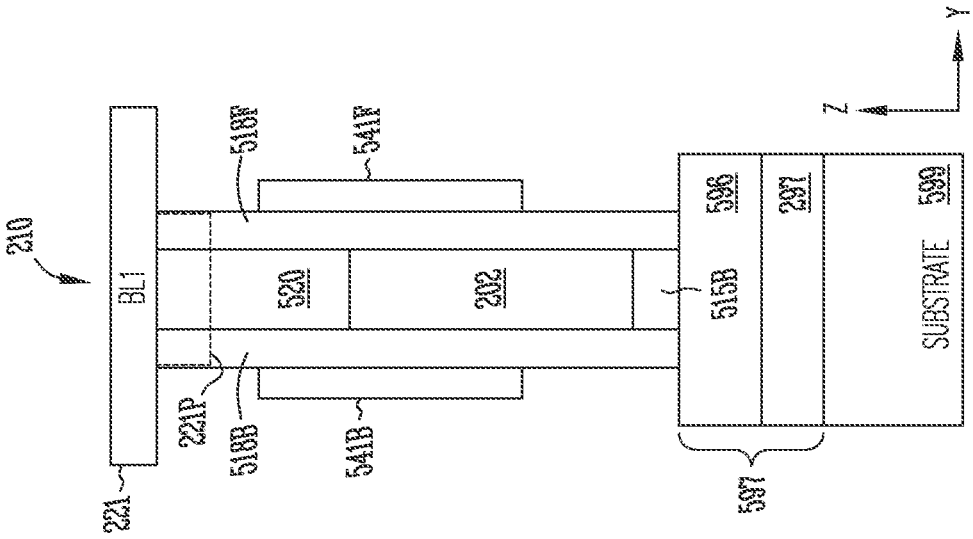

210
BL1
221
221P
518F
518B
520
541F
541B
202
515B
596
597
597
599
SUBSTRATE
Z
Y
200

FIG. 7B

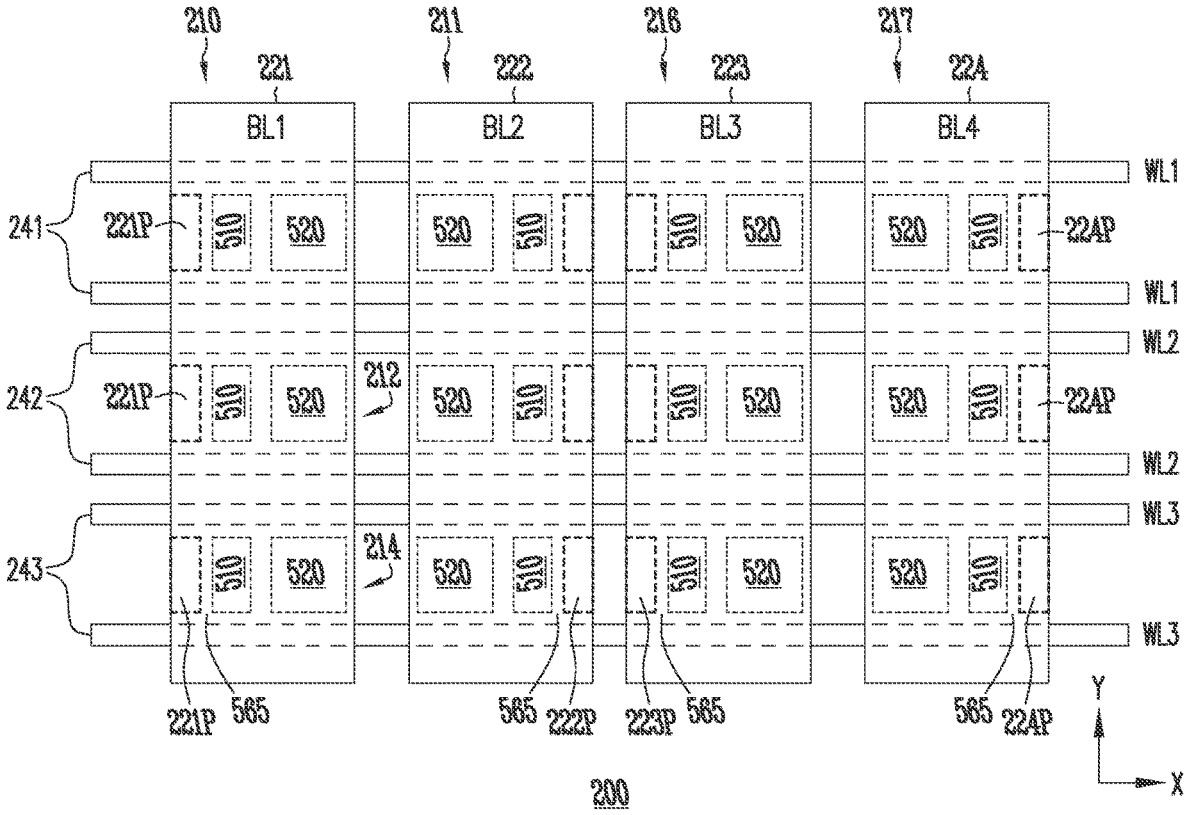

210
211
216
217
221
222
223
22A
BL1
BL2
BL3
BL4
WL1
WL1
WL2
WL2
WL3
WL3
241
242
243
221P
22AP
510
520
212
214
565
222P
223P
Y
X
200

FIG. 7C

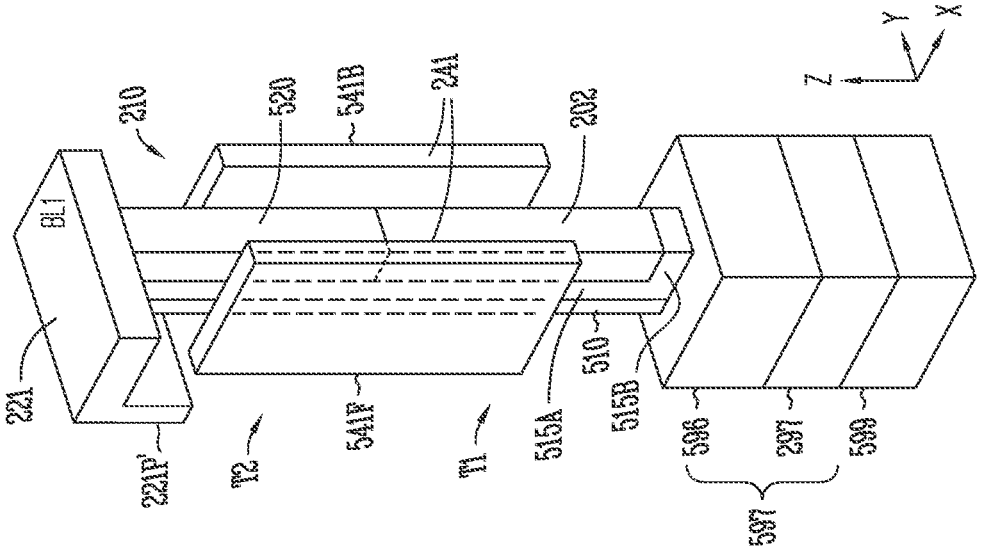

210
BL1
221
221P'
T2
520
541F
541B
241
T1
202
515A
510
515B
596
597
598
597
800
Z
Y
X

FIG. 8B

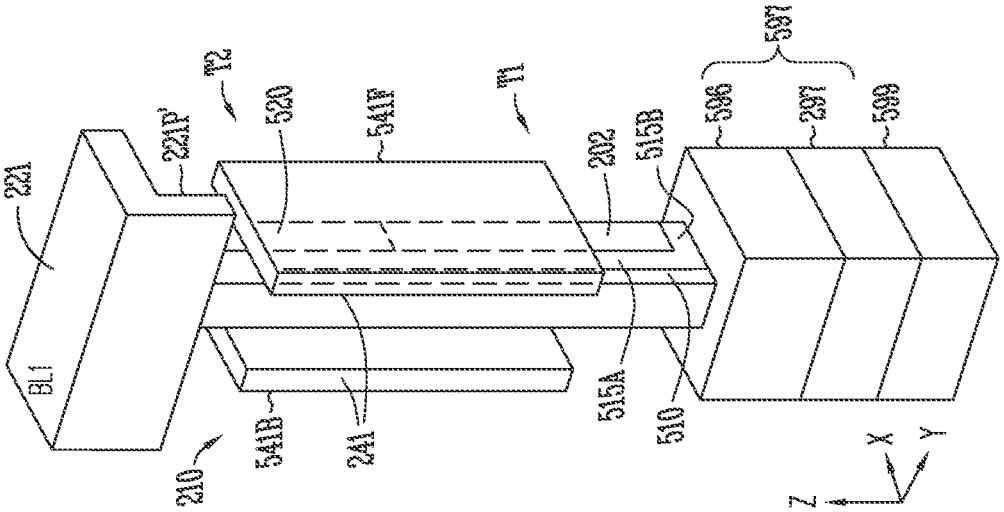

221
BL1
210
221P'
T2
520
541F
541B
241
T1
202
515A
515B
510
596
597
598
597
800
Z
X
Y

FIG. 8A

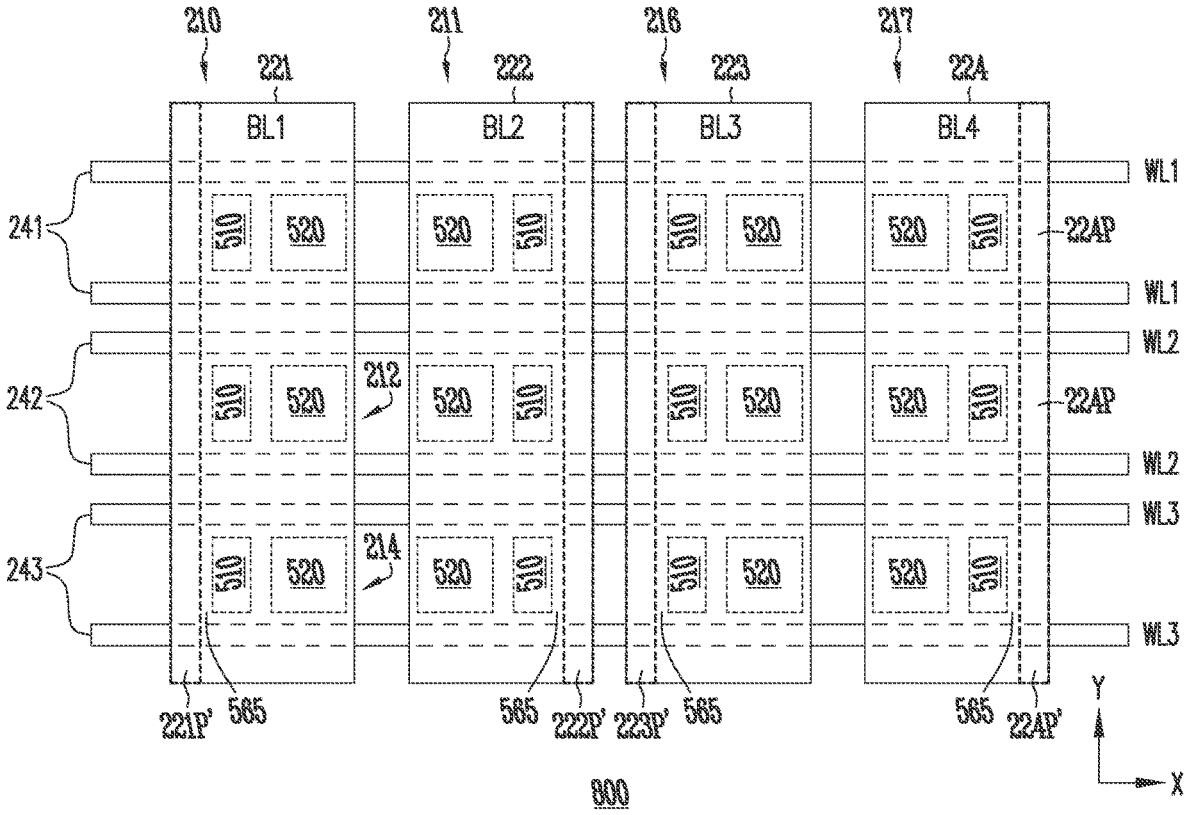

210
211
216
217
221
222
223
22A
BL1
BL2
BL3
BL4
WL1
WL1
WL2
WL2
WL3
WL3
241
242
243
510
520
212
214
22AP
221P'
565
222P'
223P'
22AP'
Y
X
800

FIG. 8C

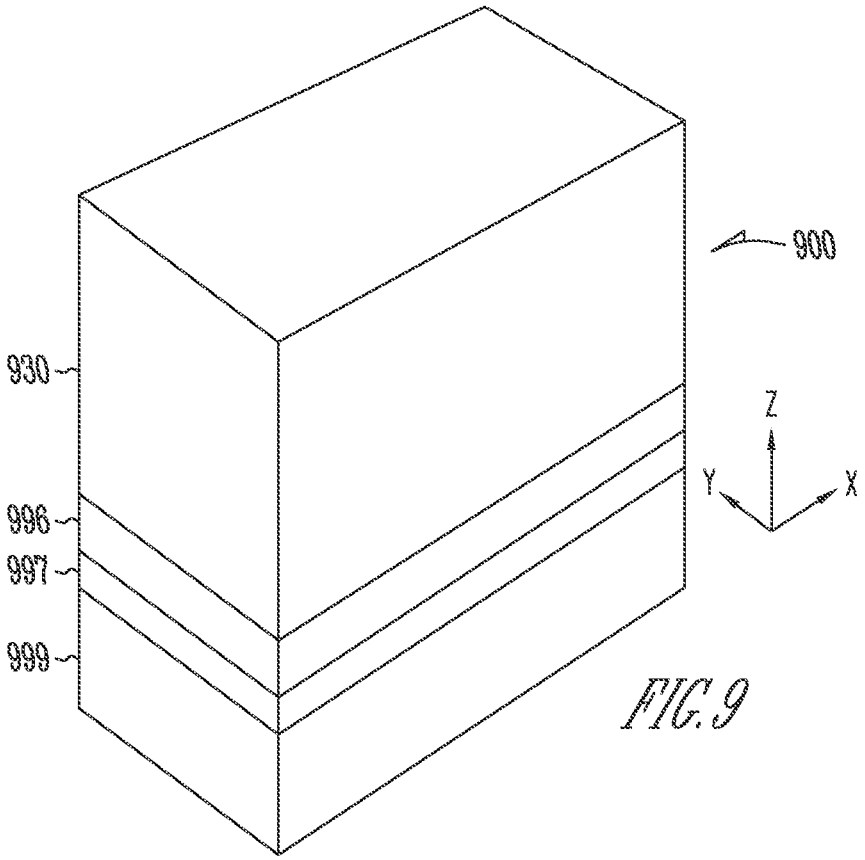

900
930
996
997
999
Z
Y
X

FIG. 9

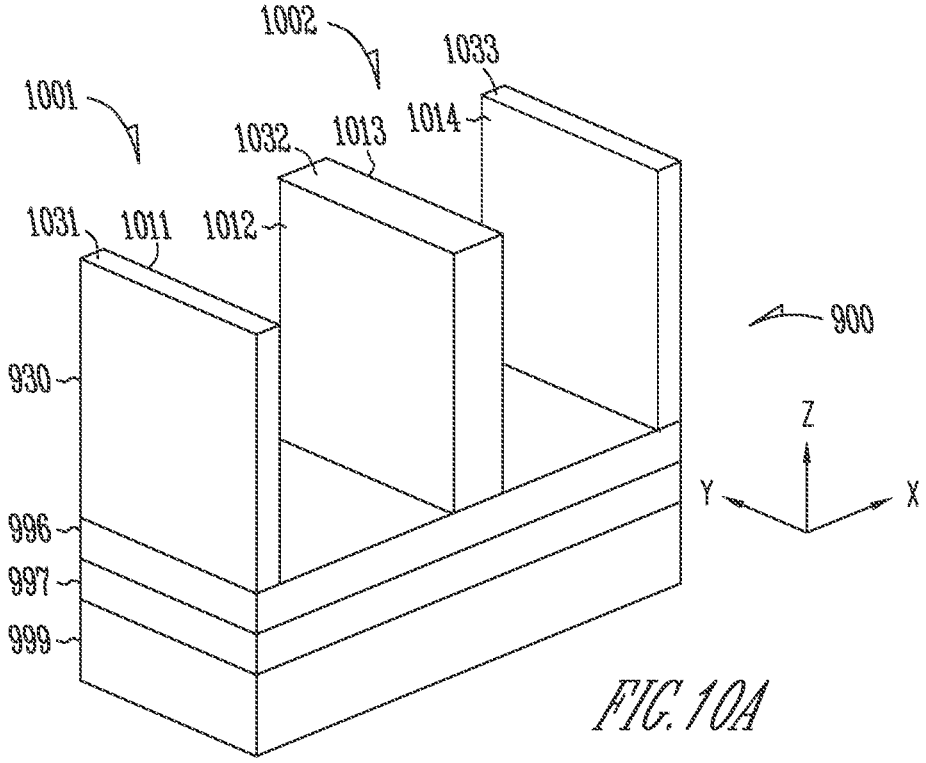

1002
1033
1001
1014
1032
1013
1031
1011
1012
900
930
Z
Y
X
996
997
999

FIG. 10A

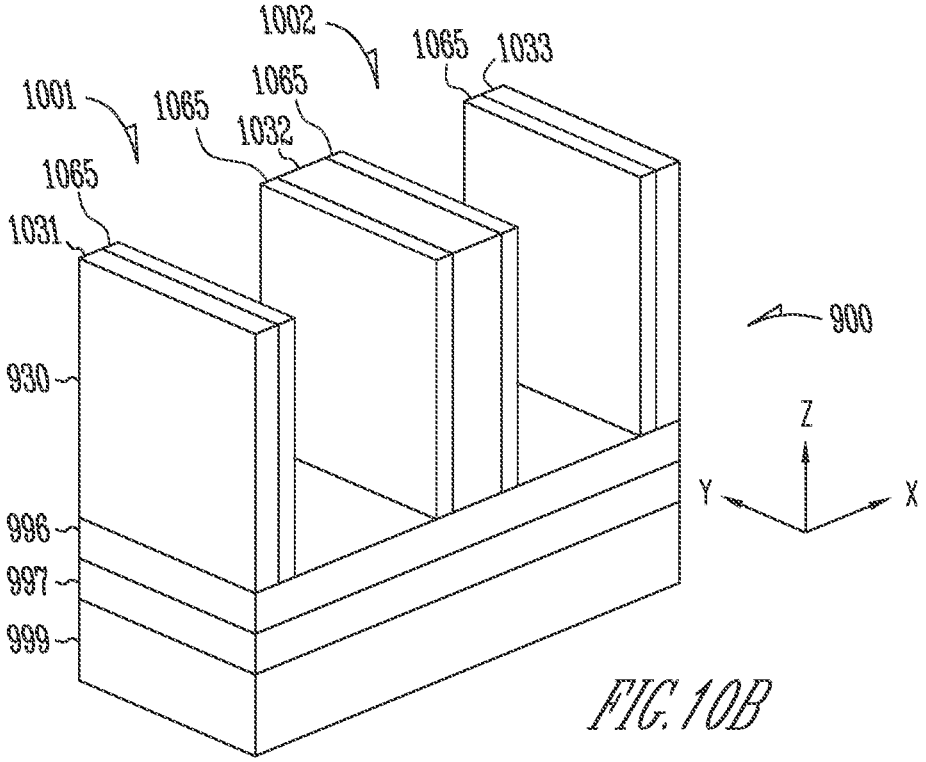


FIG. 10B

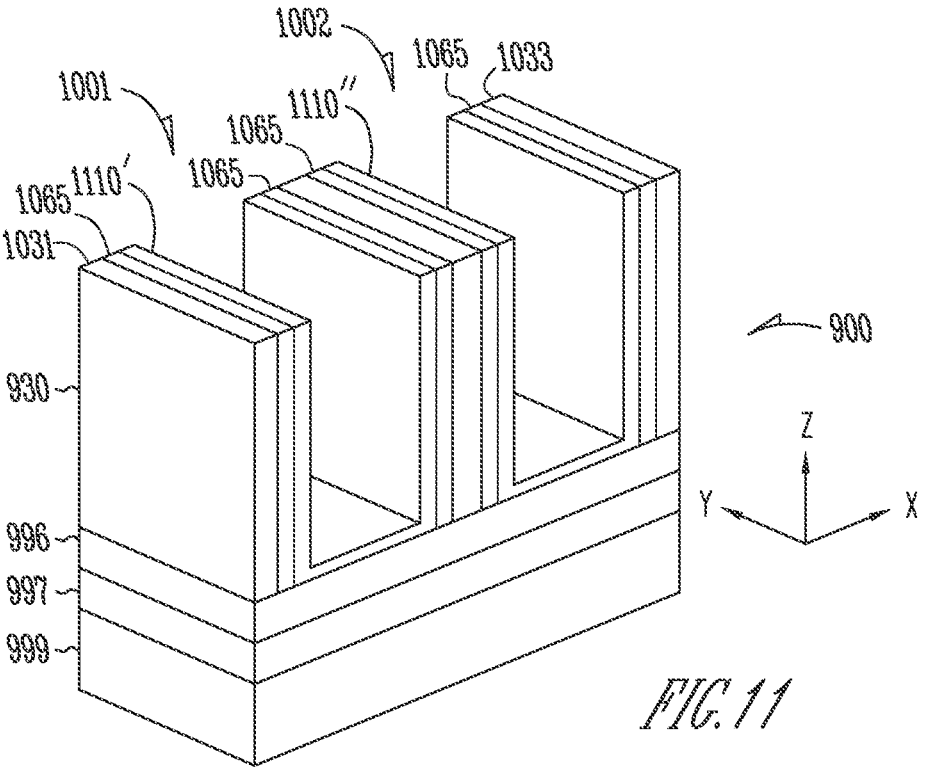


FIG. 11

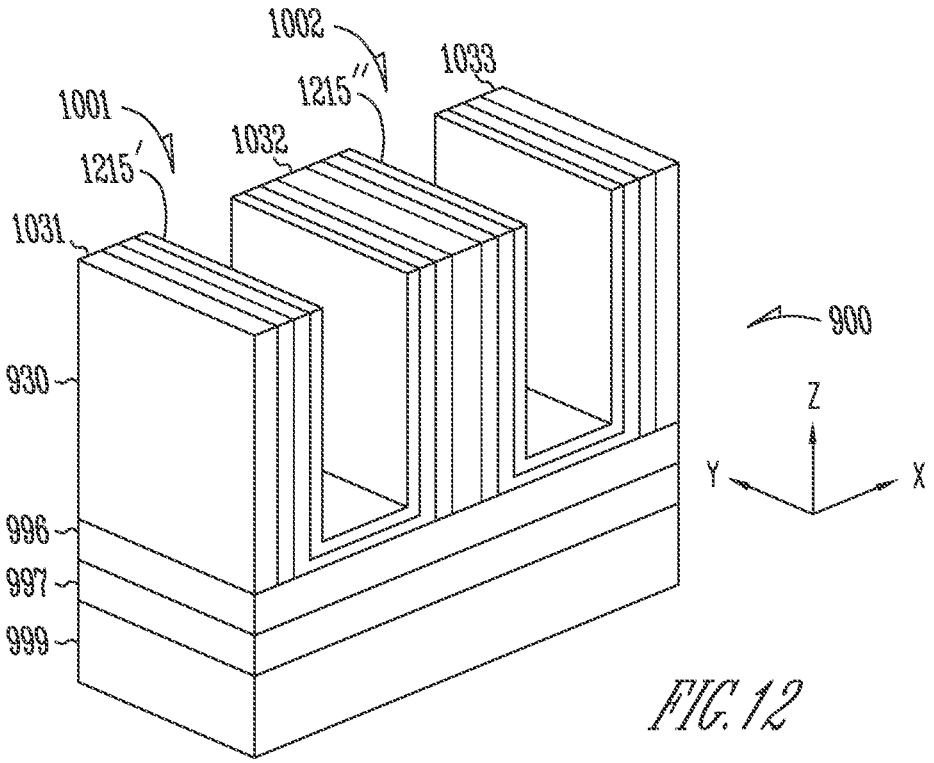

1002
1033
1215''
1001
1032
1215'
1031
900
930
Z
Y
X
996
997
999

FIG. 12

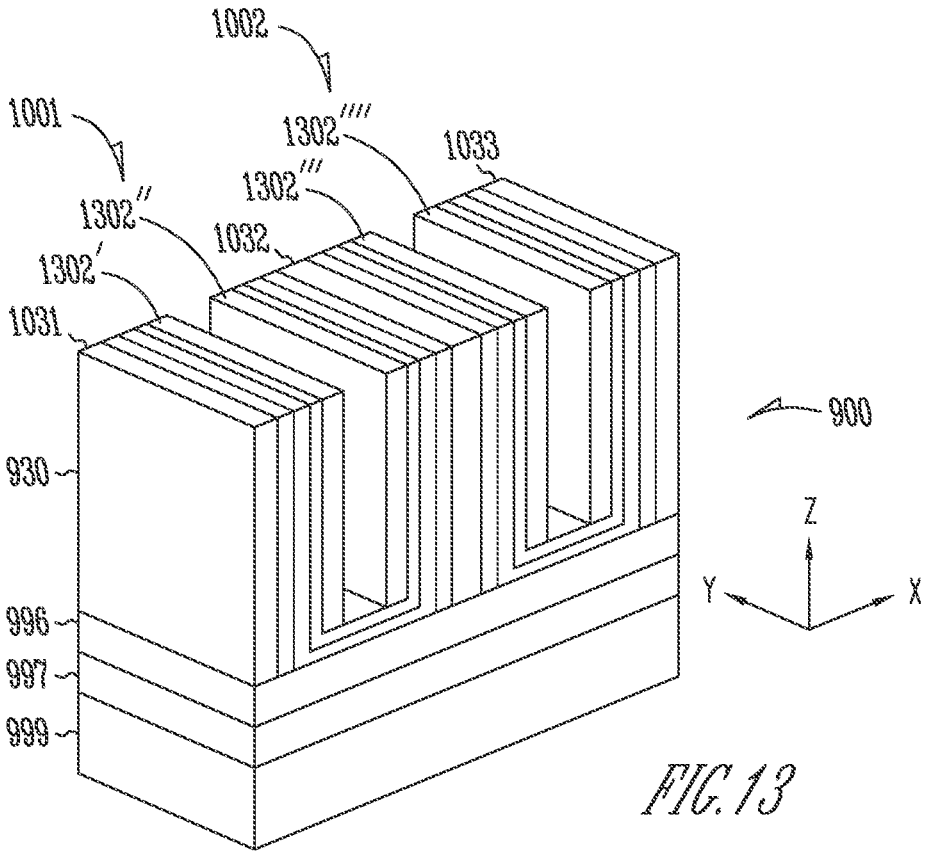

1002
1001
1302''''
1033
1302'''
1302''
1032
1302'
1031
900
930
Z
Y
X
996
997
999

FIG. 13

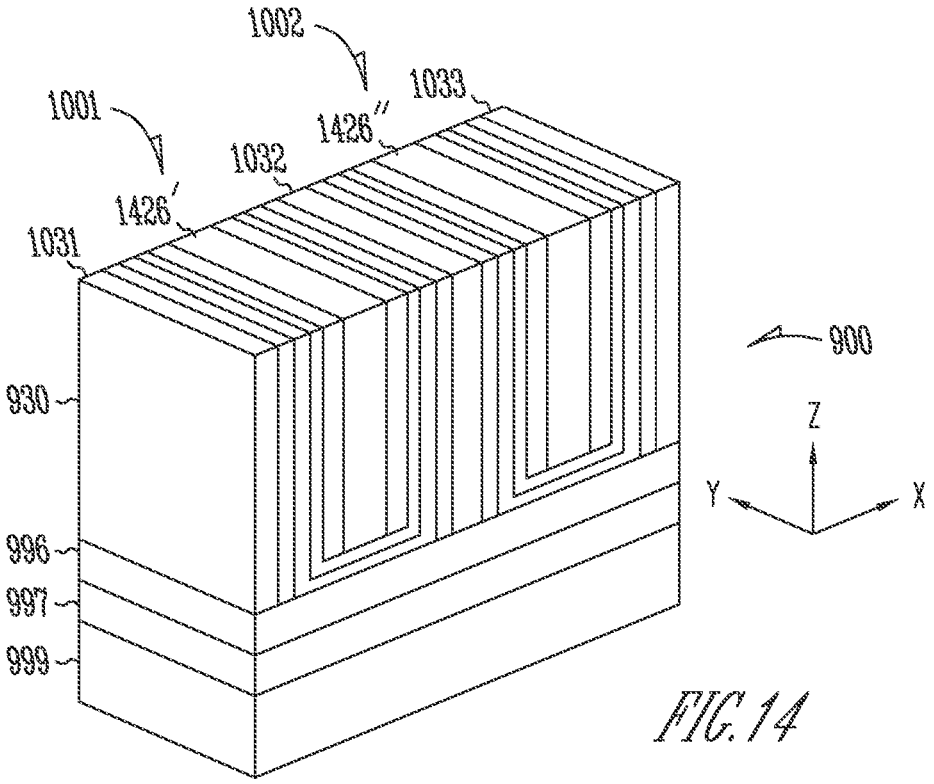

1002
1001
1033
1426″
1032
1426′
1031
900
930
Z
Y
X
996
997
999

FIG. 14

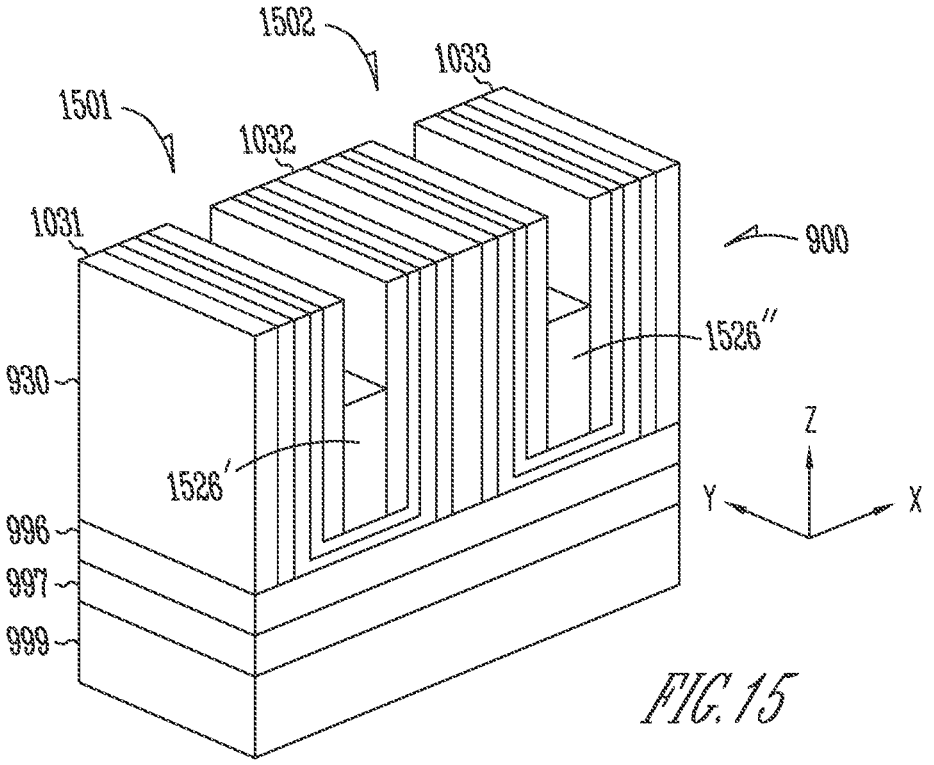

1502
1033
1501
1032
1031
900
1526″
930
Z
1526′
Y
X
996
997
999

FIG. 15

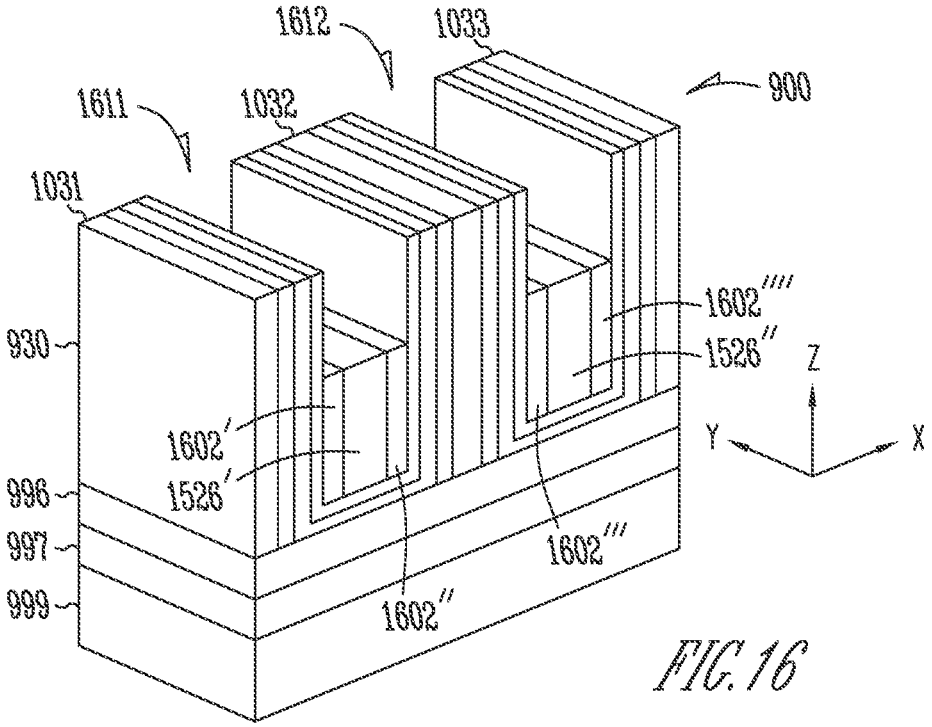

1612
1033
900
1611
1032
1031
1602''''
930
1526''
Z
1602'
Y
X
1526'
996
997
1602'''
999
1602''

FIG. 16

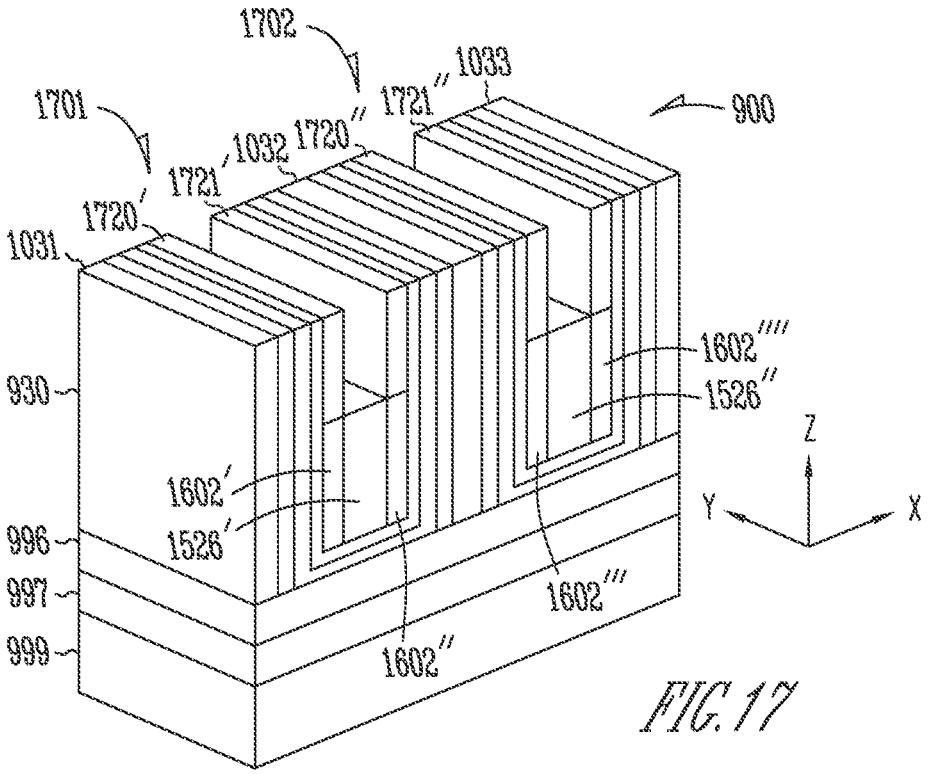

1702
1033
1721''
900
1701
1720''
1032
1721'
1720'
1031
1602''''
930
1526''
Z
1602'
Y
X
1526'
996
997
1602'''
999
1602''

FIG. 17

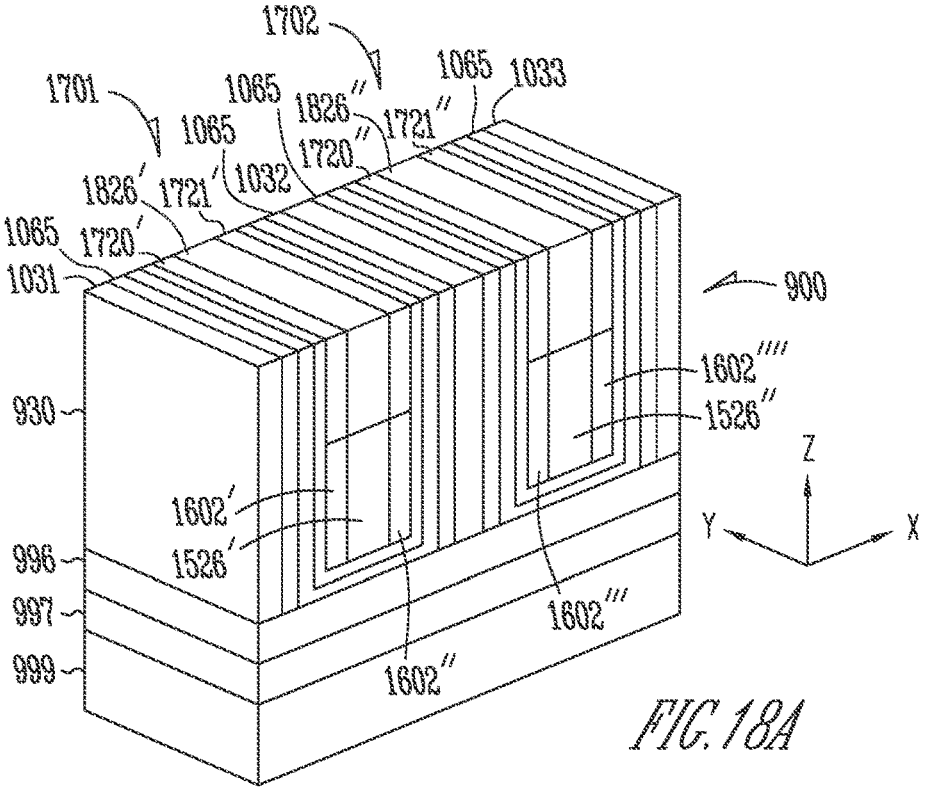


FIG. 18A

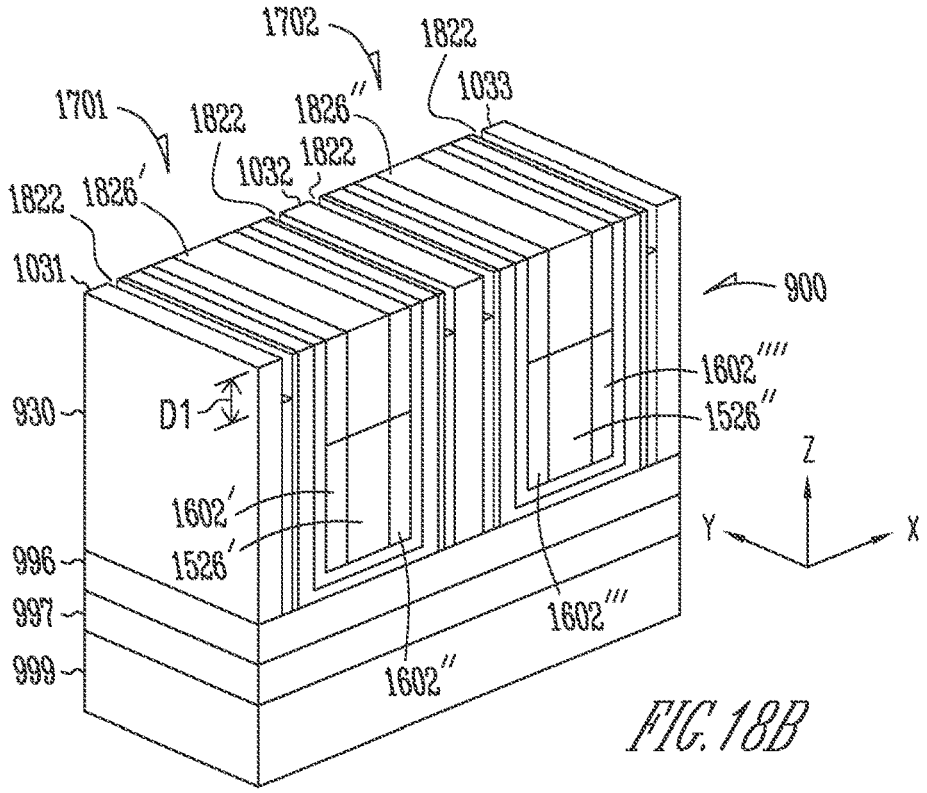


FIG. 18B

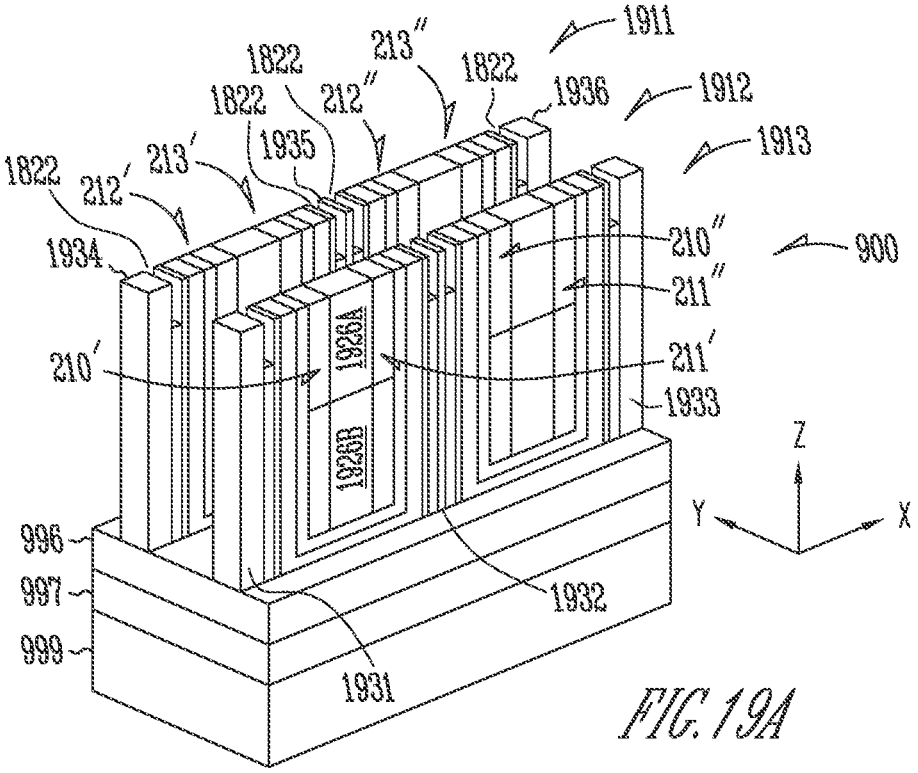

1911
1822
213″
1822
1822
212″
1936
1912
1935
1913
1822
213′
212′
1934
210″
900
211″
1926A
210′
211′
1933
1926B
Z
Y
X
996
997
1932
999
1931

FIG. 19A

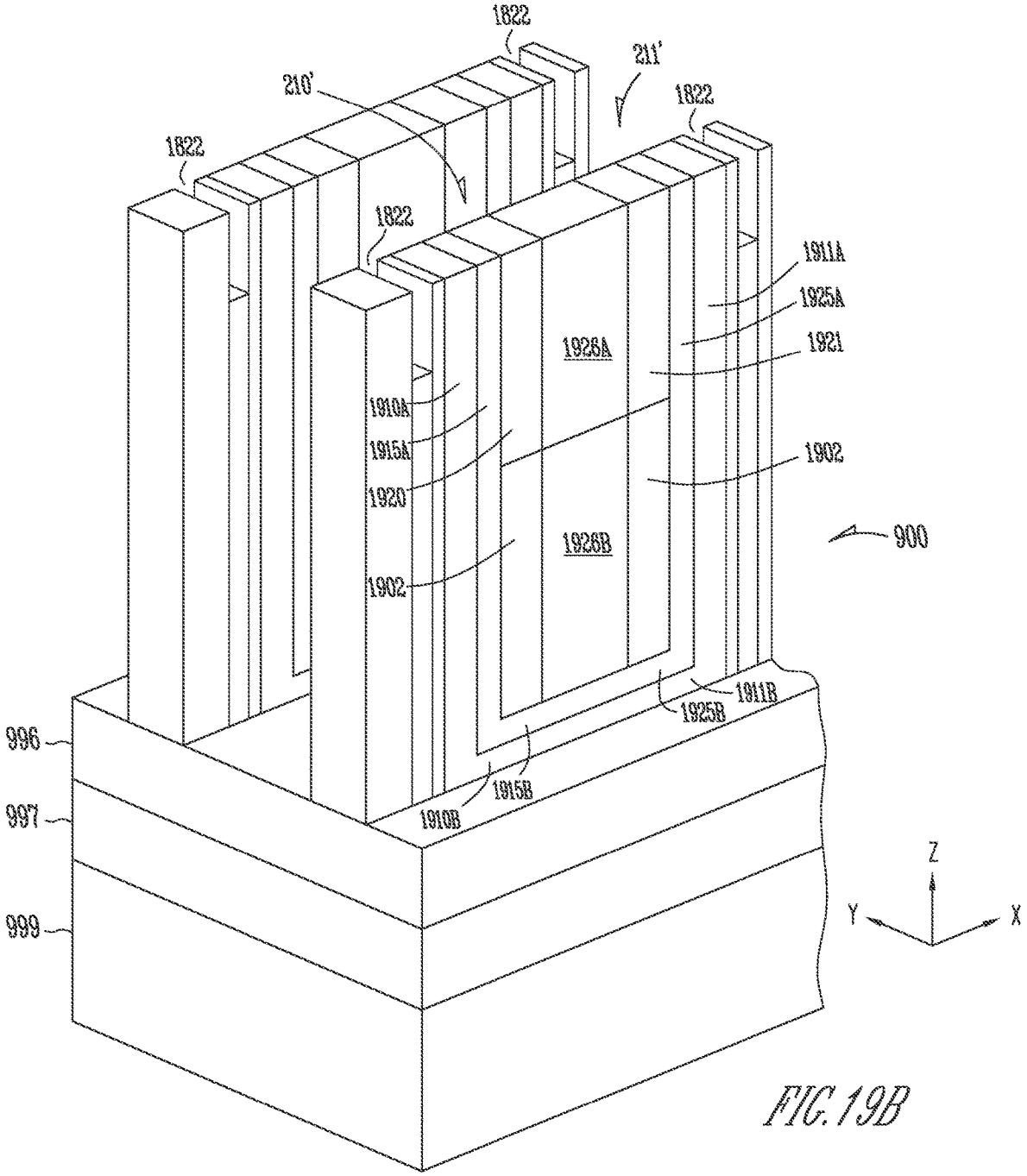

1822
211'
210'
1822
1822
1822
1911A
1925A
1921
1926A
1910A
1915A
1920
1902
1926B
1902
900
1911B
1925B
996
997
999
1915B
1910B
Z
Y
X

FIG. 19B

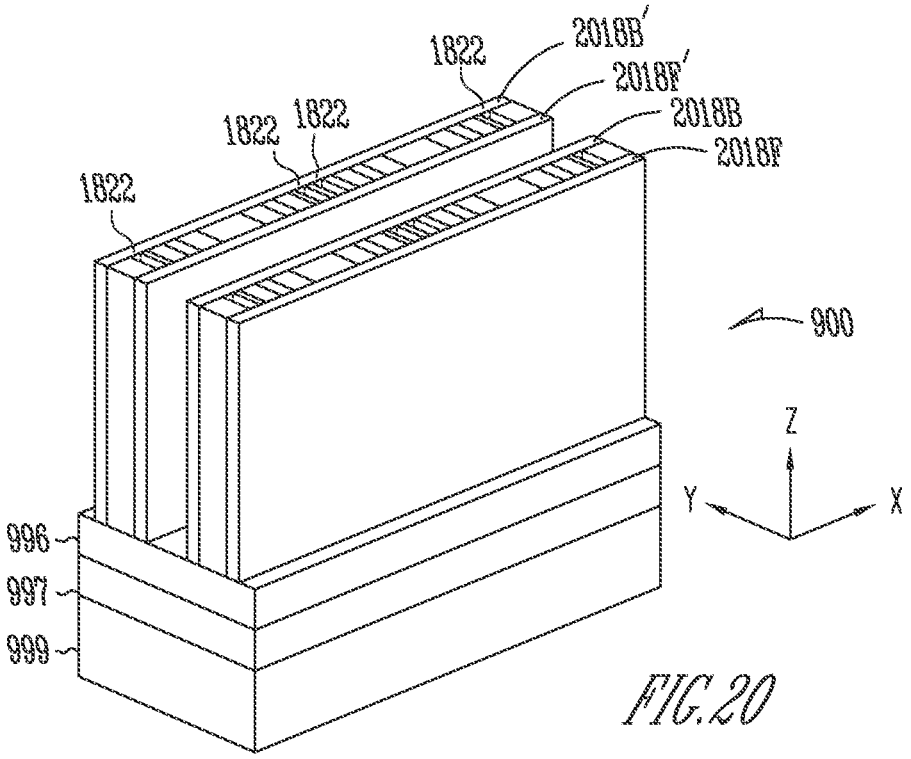

1822
2018B'
2018F'
2018B
2018F
1822
1822
1822
900
Z
Y
X
996
997
999

FIG.20

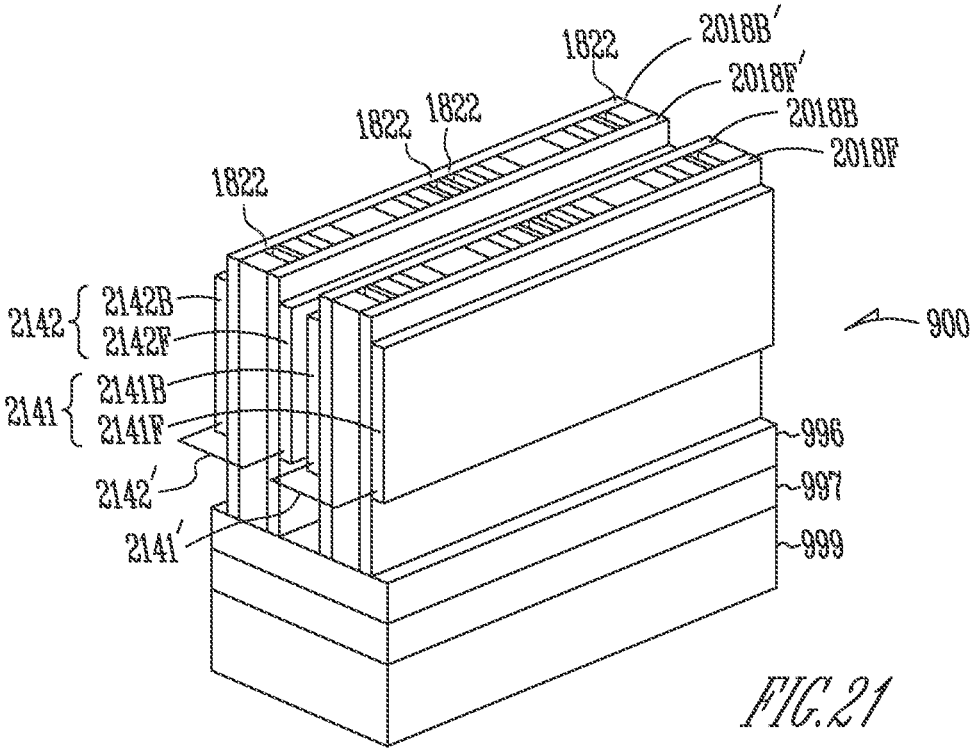

1822
2018B'
2018F'
2018B
2018F
1822
1822
1822
2142
2142B
2142F
2141
2141B
2141F
2142'
2141'
900
996
997
999

FIG.21

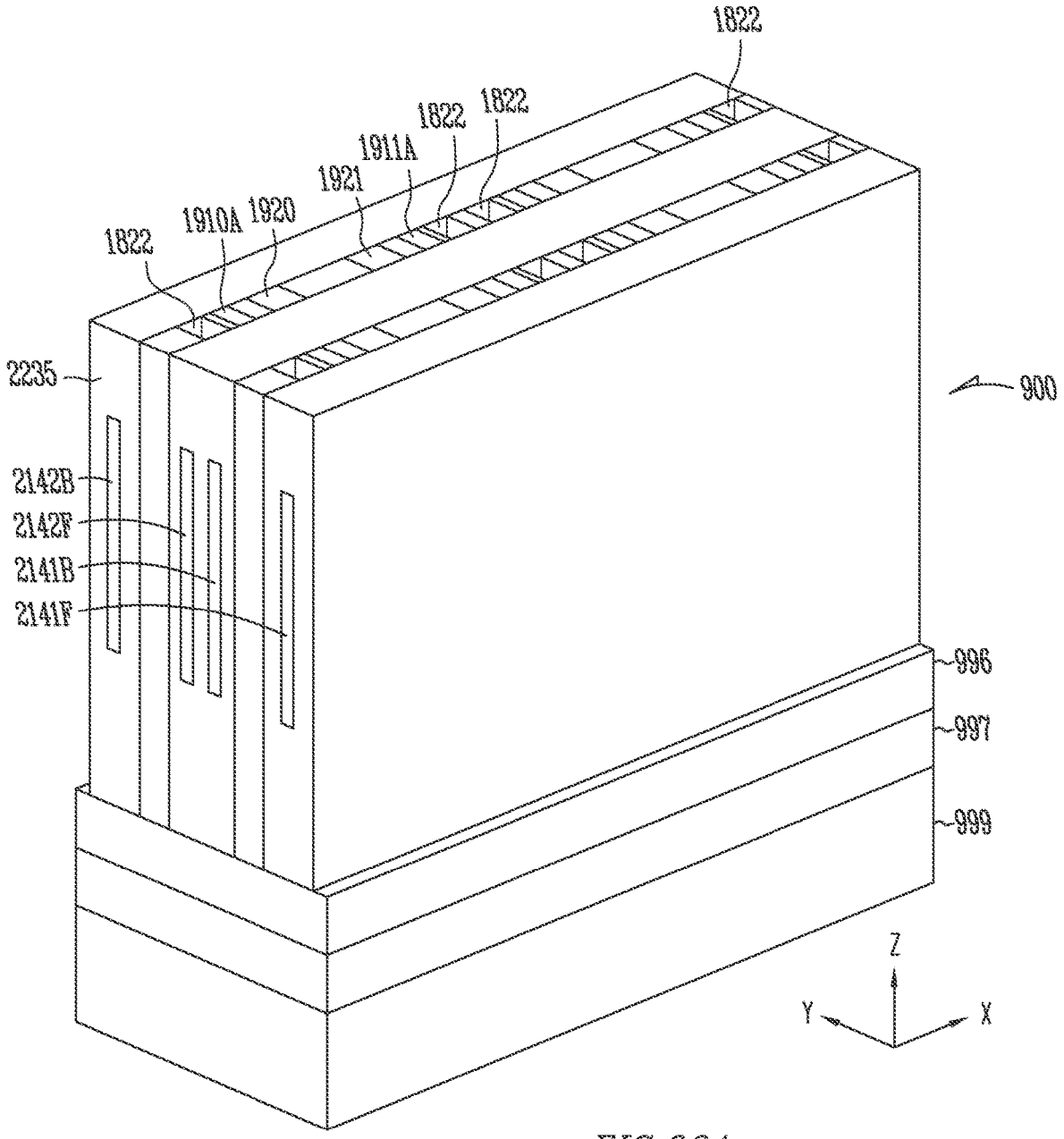

1822
1822
1822
1911A
1921
1920
1910A
1822
2235
900
2142B
2142F
2141B
2141F
996
997
999
Z
Y
X

FIG.22A

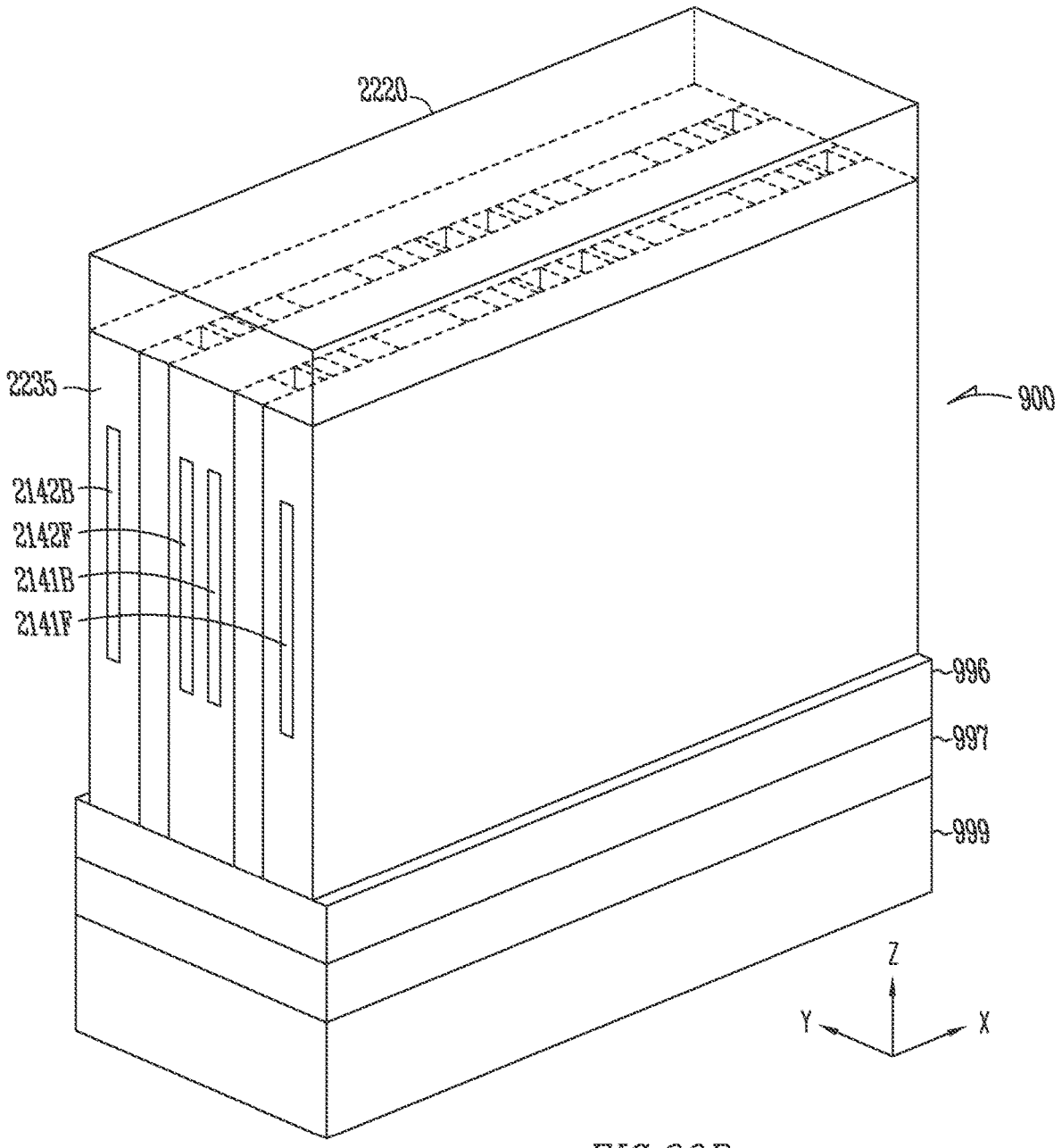


FIG.22B

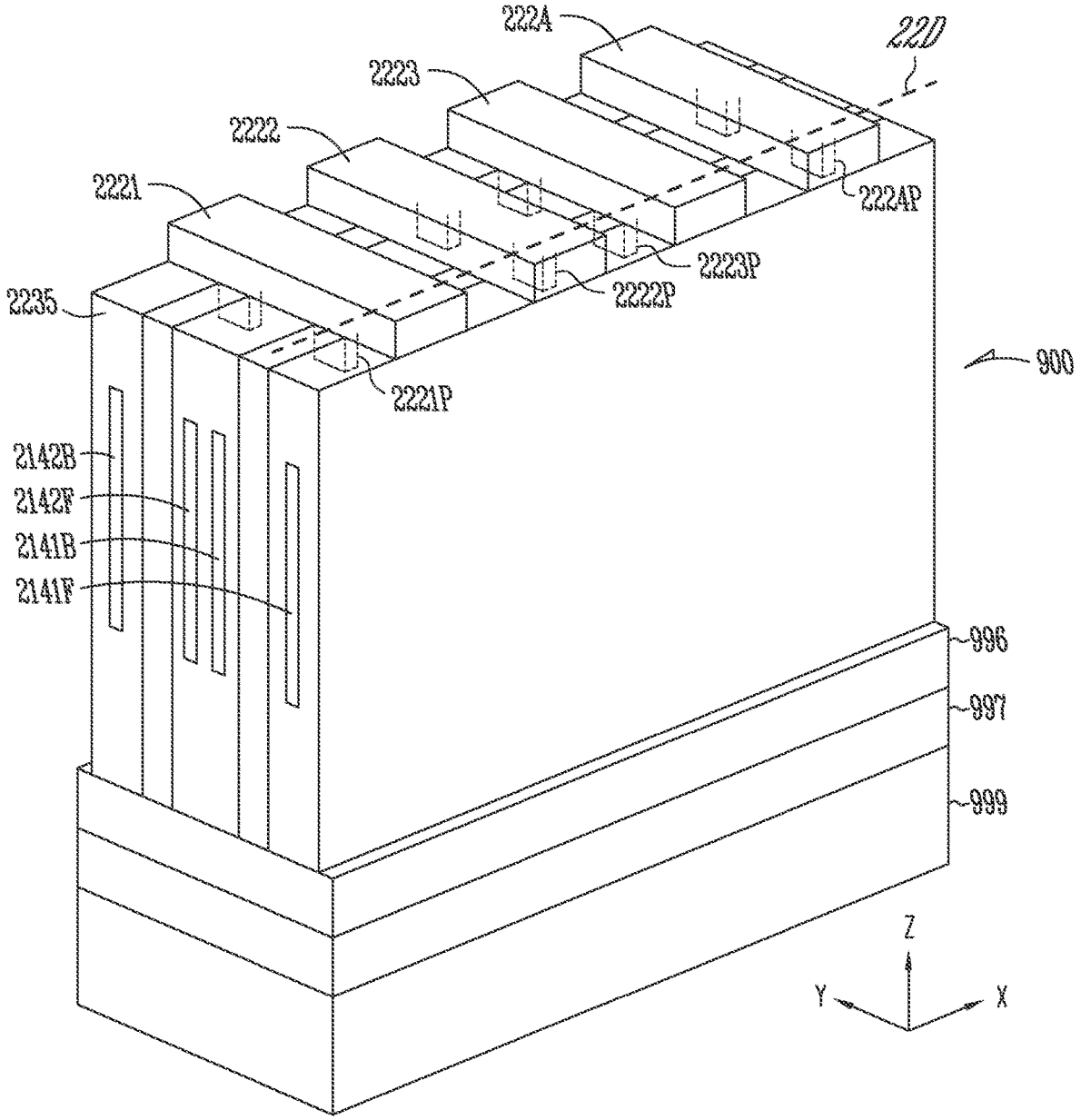

222A
22D
2223
2222
2221
222AP
2223P
2222P
2235
2221P
900
2142B
2142F
2141B
2141F
996
997
999
Z
Y
X

FIG.22C

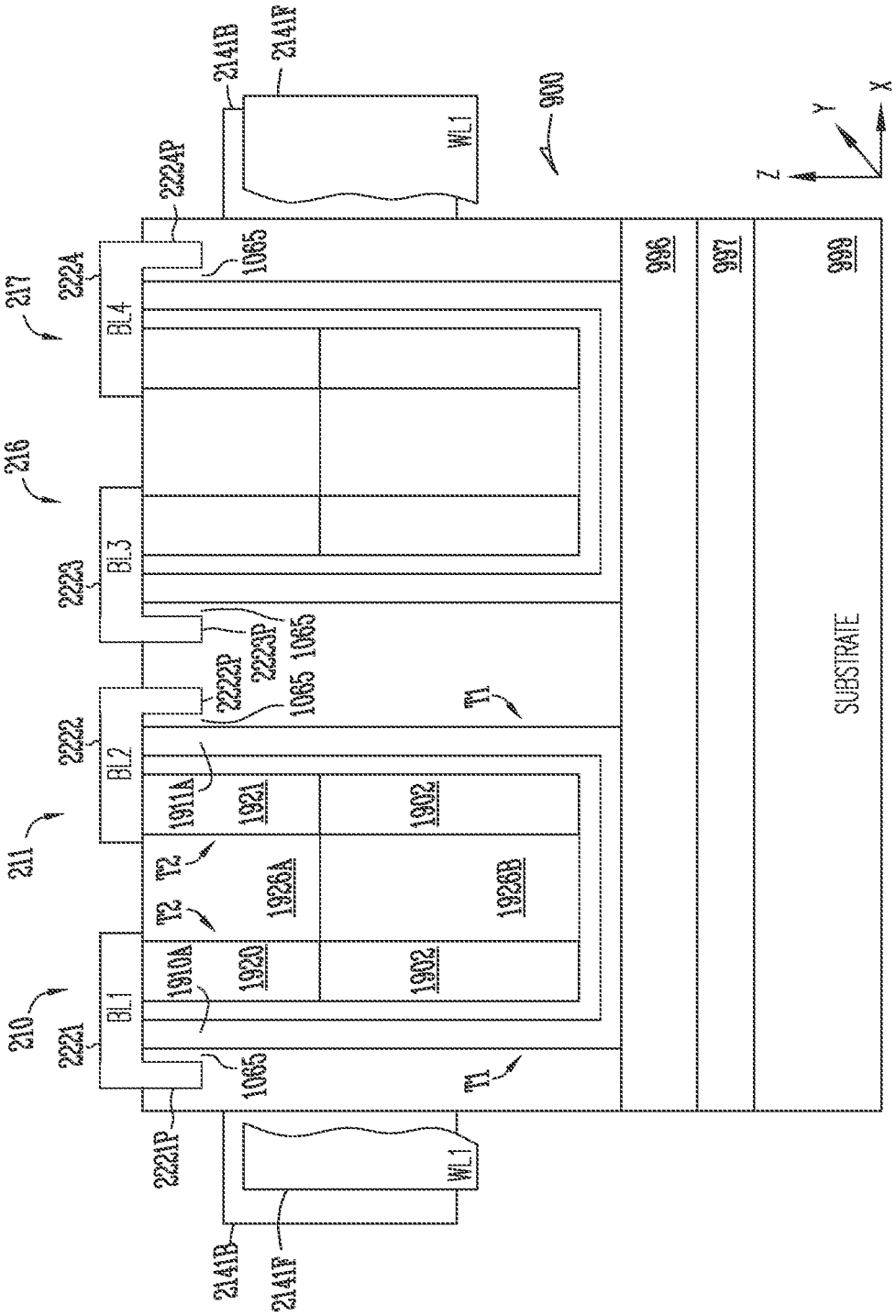

2141B
2141F
WL1
900
Z
Y
X
2224P
1065
2224
217
BL4
216
BL3
2223
2223P
1065
2222P
1065
2222
BL2
T1
1911A
1921
1902
211
T2
T2
1926A
1926B
1910A
1920
1902
210
2221
BL1
1065
T1
2221P
WL1
2141B
2141F
906
907
909
SUBSTRATE

FIG. 22D

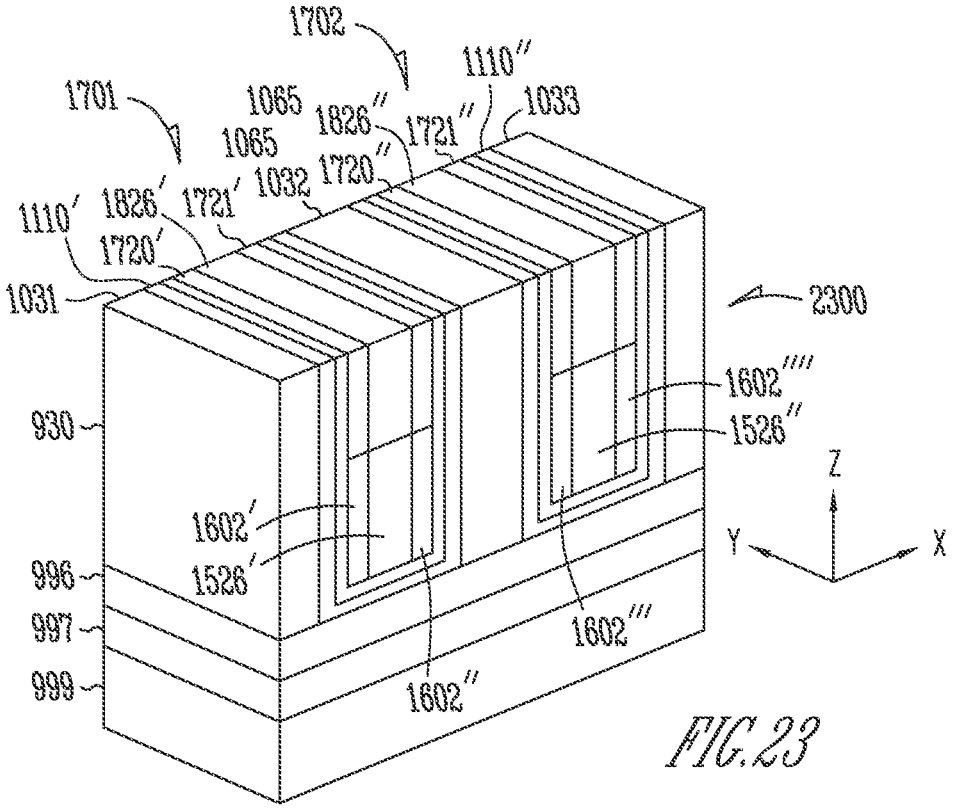

1702
1110″
1701
1065
1826″
1721″
1033
1065
1720″
1032
1826′
1721′
1110′
1720′
1031
2300
1602″″
930
1526″
Z
1602′
Y
X
996
1526′
997
1602‴
999
1602″

FIG.23

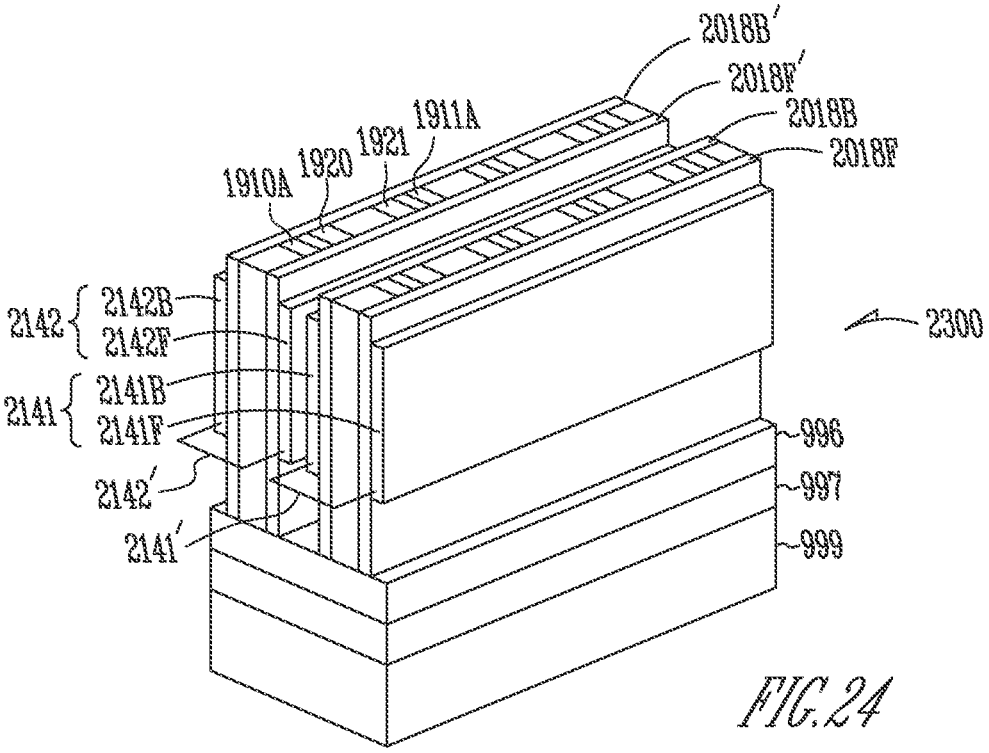

2018B′
2018F′
2018B
2018F
1911A
1921
1920
1910A
2142
2142B
2142F
2141
2141B
2141F
2142′
2141′
2300
996
997
999

FIG.24

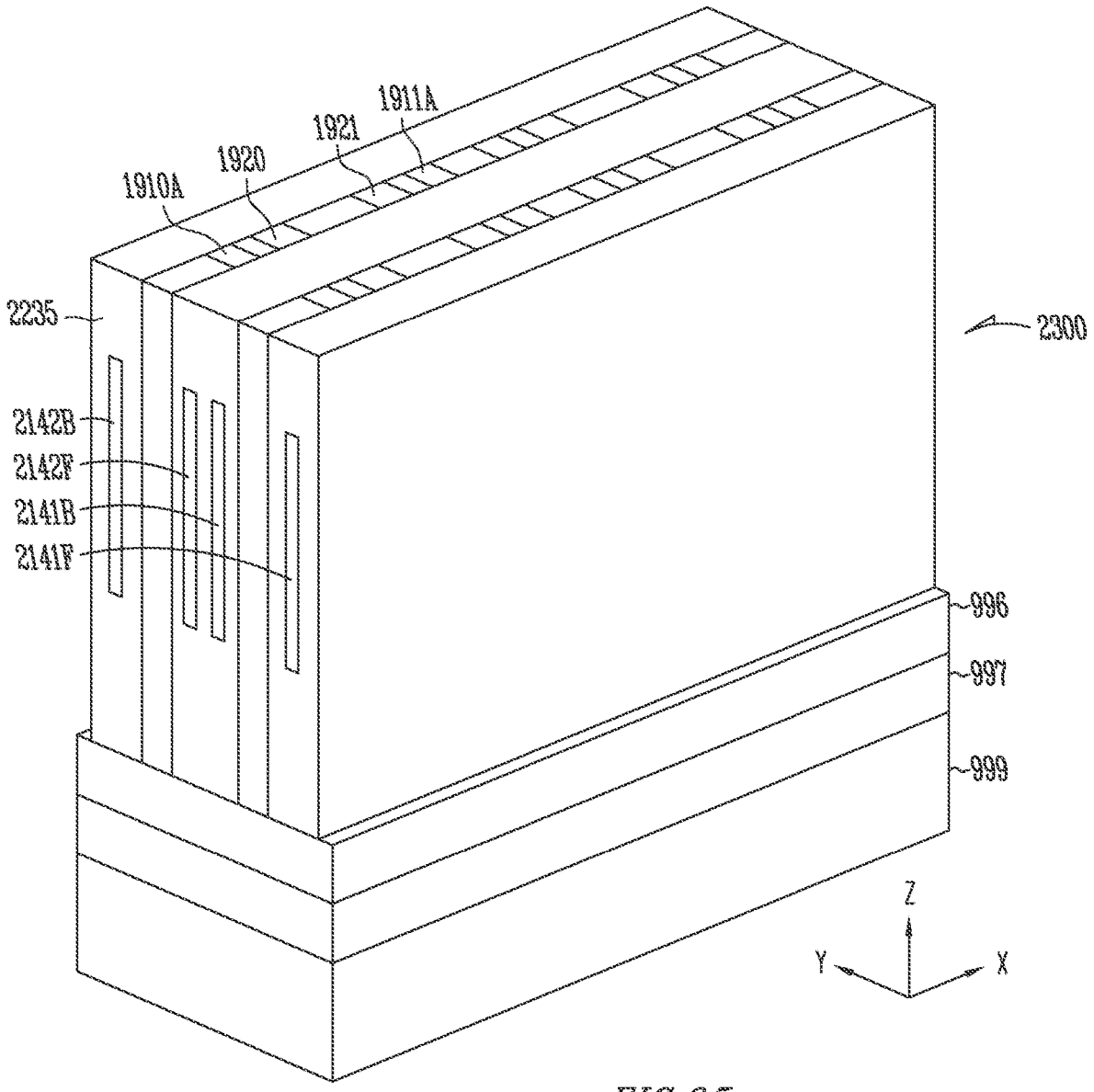

1911A
1921
1920
1910A
2235
2300
2142B
2142F
2141B
2141F
996
997
999
Z
Y
X

FIG.25

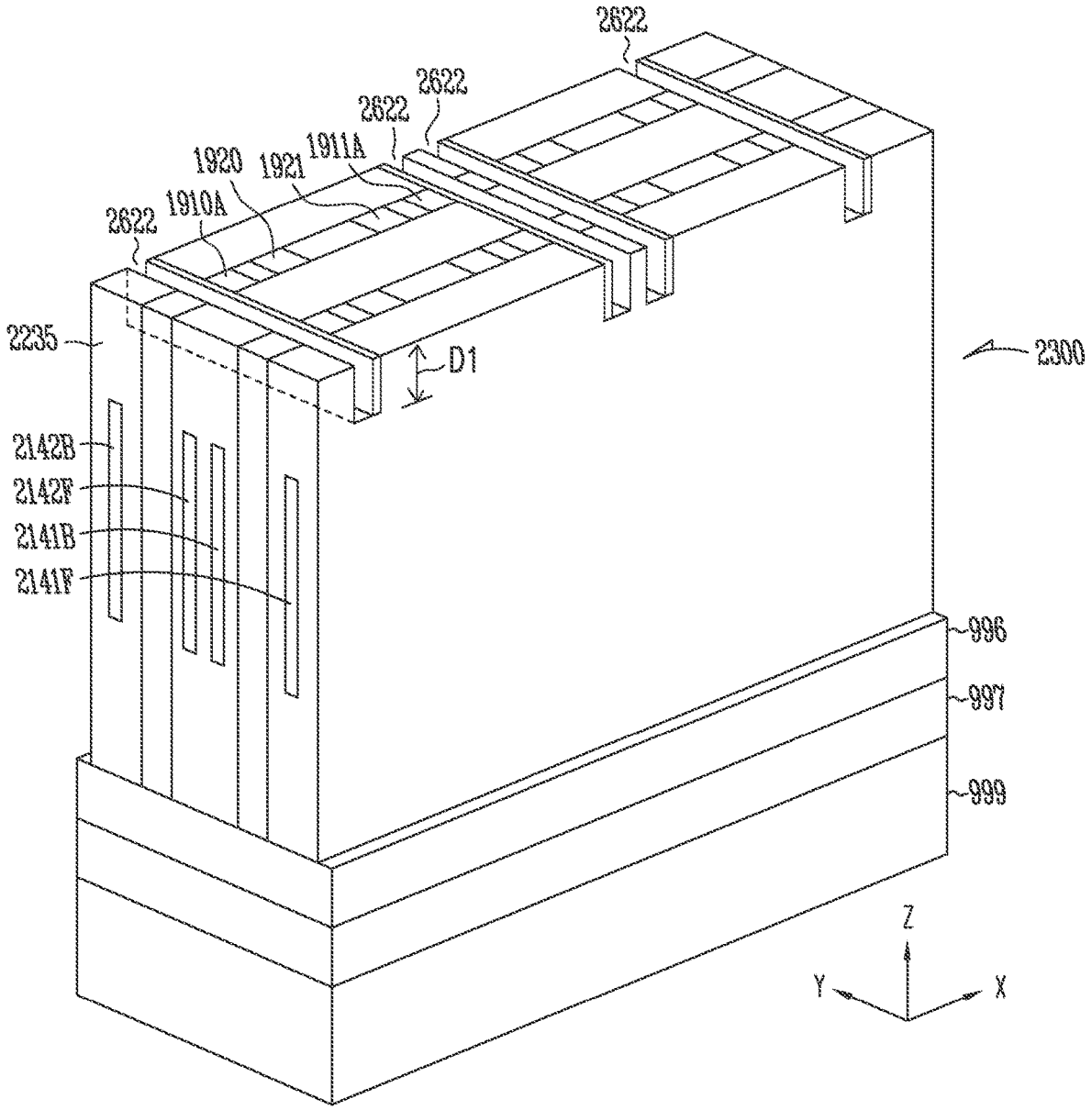

2622
2622
2622
1911A
1921
1920
1910A
2622
2235
D1
2300
2142B
2142F
2141B
2141F
996
997
999
Z
Y
X

FIG.26

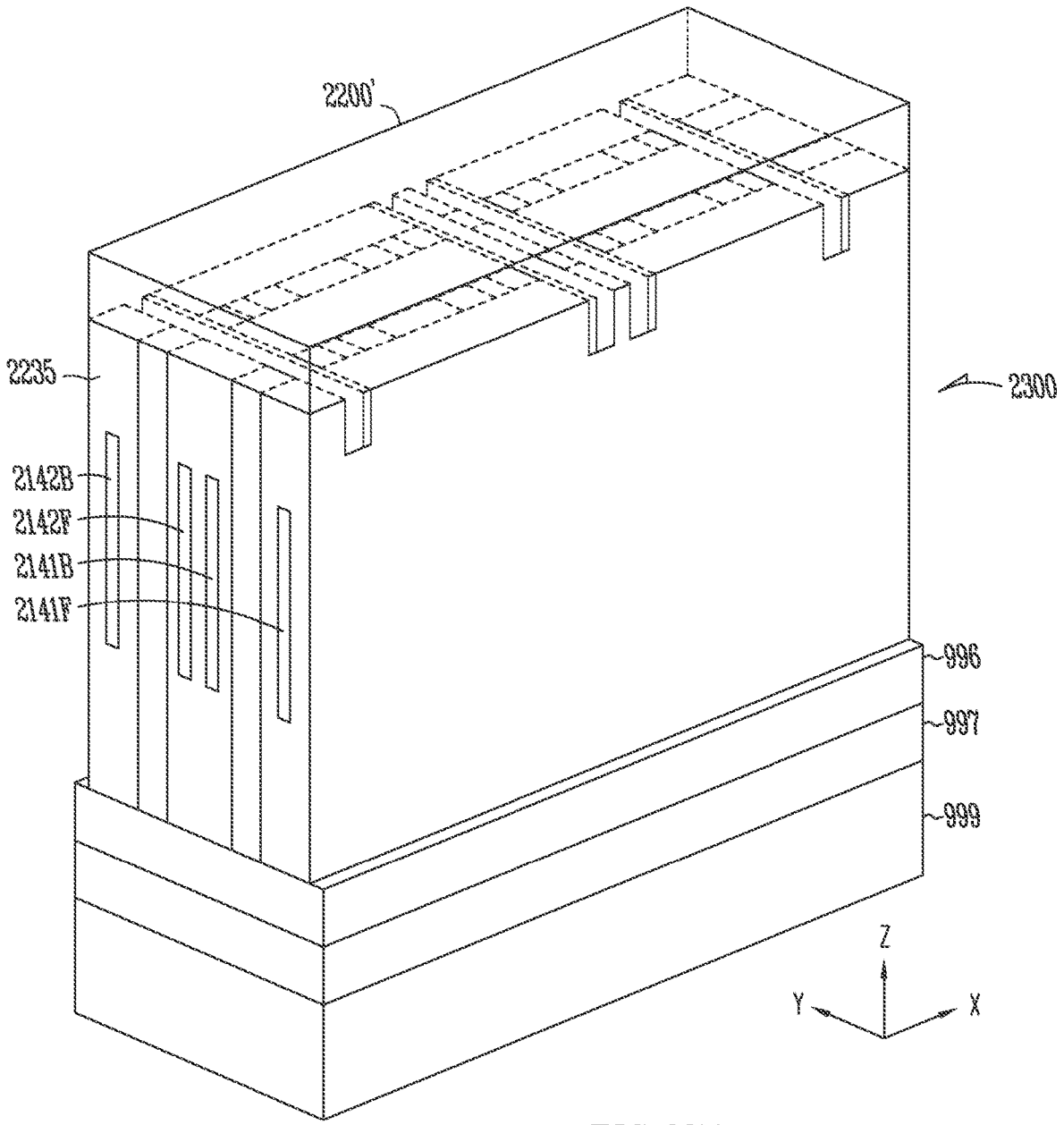


FIG.27A

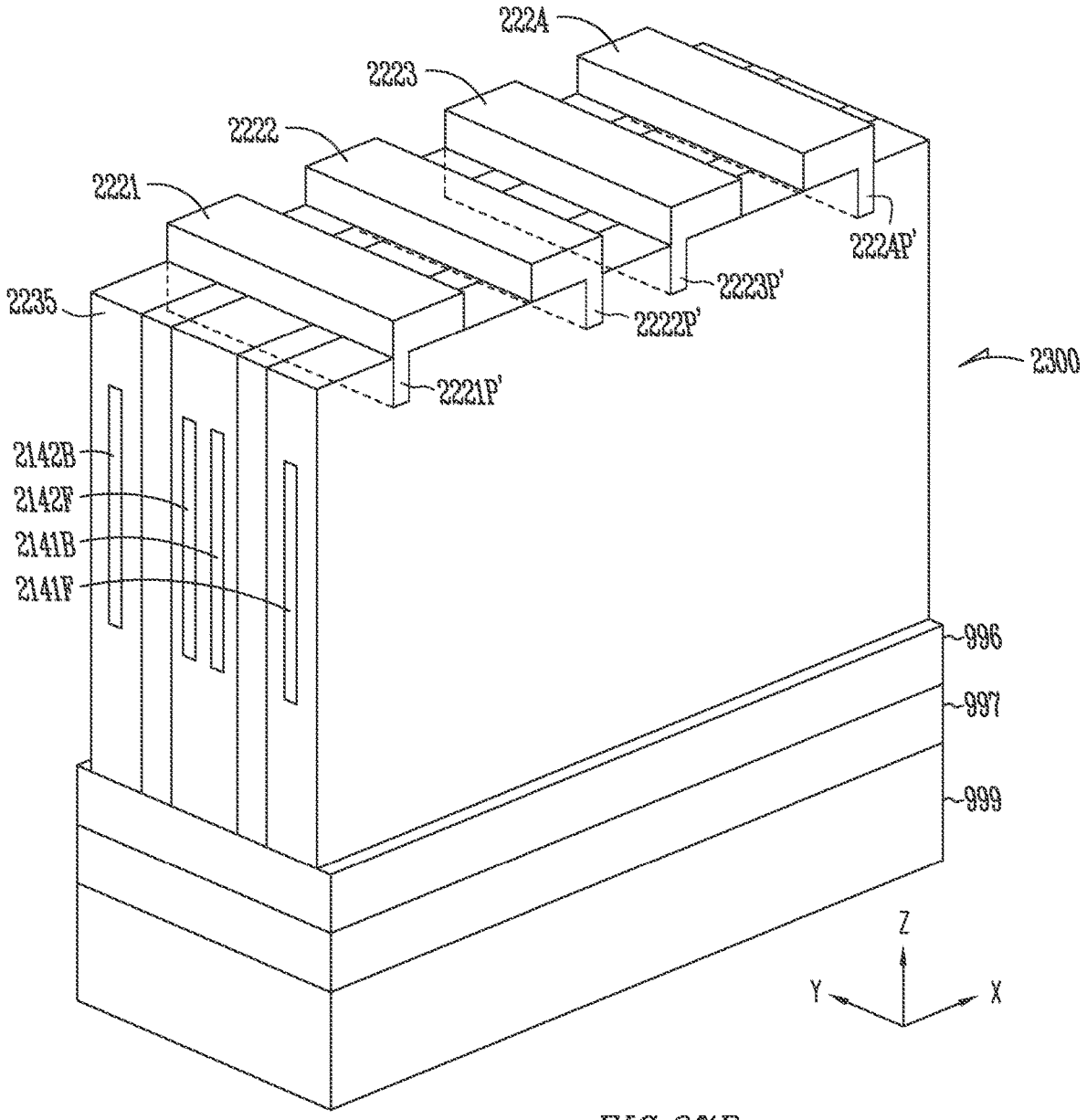

222A
2223
2222
2221
2235
222AP'
2223P'
2222P'
2221P'
2300
2142B
2142F
2141B
2141F
996
997
999
Z
Y
X

FIG.27B

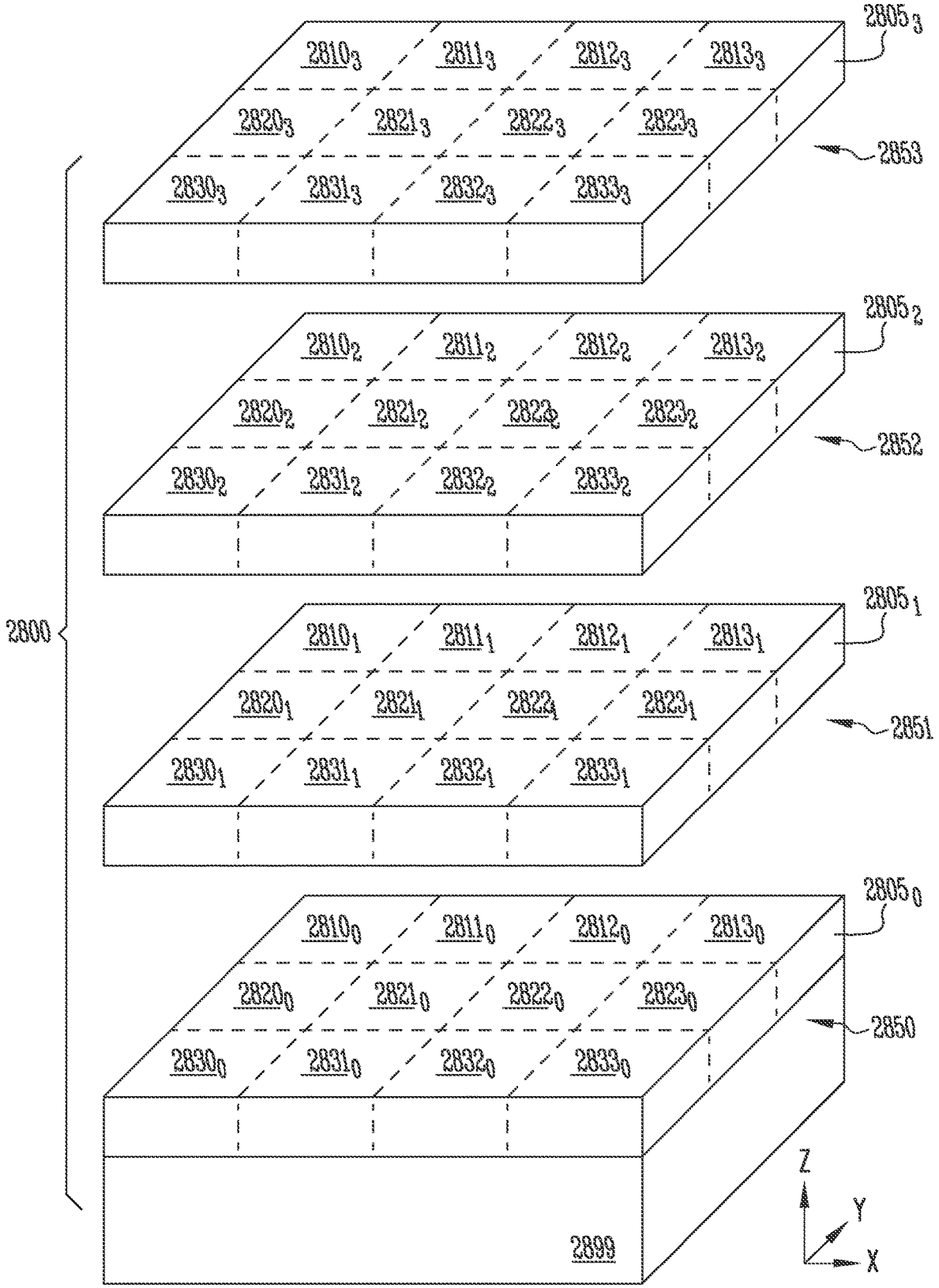

2805 3
2810 3
2811 3
2812 3
2813 3
2820 3
2821 3
2822 3
2823 3
2830 3
2831 3
2832 3
2833 3
2853
2805 2
2810 2
2811 2
2812 2
2813 2
2820 2
2821 2
2822 2
2823 2
2830 2
2831 2
2832 2
2833 2
2852
2800
2805 1
2810 1
2811 1
2812 1
2813 1
2820 1
2821 1
2822 1
2823 1
2830 1
2831 1
2832 1
2833 1
2851
2805 0
2810 0
2811 0
2812 0
2813 0
2820 0
2821 0
2822 0
2823 0
2830 0
2831 0
2832 0
2833 0
2850
2899
Z
Y
X

FIG. 28A

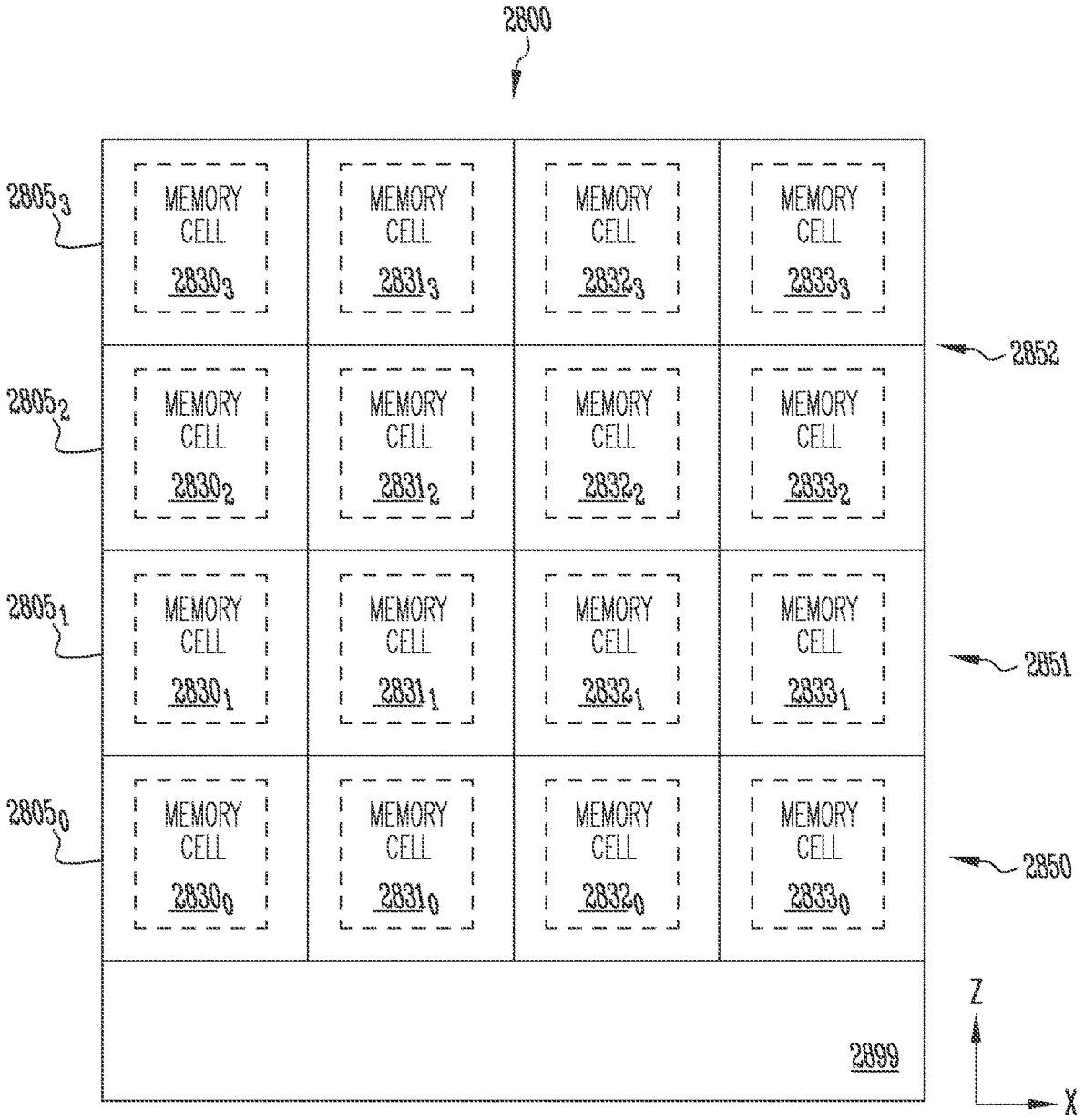

2800
2805₃
2805₂
2805₁
2805₀
MEMORY CELL 2830₃
MEMORY CELL 2831₃
MEMORY CELL 2832₃
MEMORY CELL 2833₃
MEMORY CELL 2830₂
MEMORY CELL 2831₂
MEMORY CELL 2832₂
MEMORY CELL 2833₂
MEMORY CELL 2830₁
MEMORY CELL 2831₁
MEMORY CELL 2832₁
MEMORY CELL 2833₁
MEMORY CELL 2830₀
MEMORY CELL 2831₀
MEMORY CELL 2832₀
MEMORY CELL 2833₀
2852
2851
2850
2899
Z
X

FIG.28B

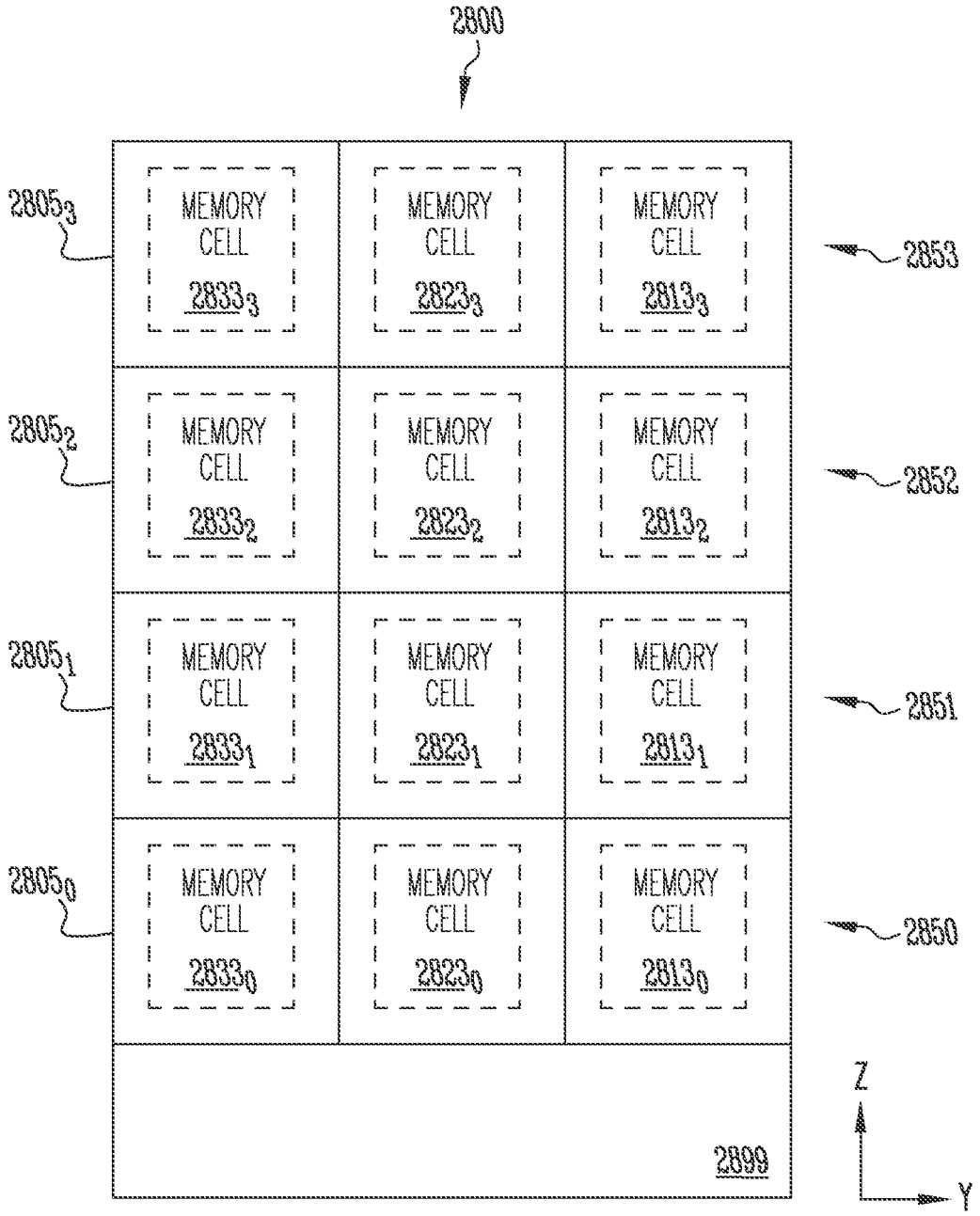

2800
2805$_3$
2805$_2$
2805$_1$
2805$_0$
MEMORY CELL 2833$_3$
MEMORY CELL 2823$_3$
MEMORY CELL 2813$_3$
MEMORY CELL 2833$_2$
MEMORY CELL 2823$_2$
MEMORY CELL 2813$_2$
MEMORY CELL 2833$_1$
MEMORY CELL 2823$_1$
MEMORY CELL 2813$_1$
MEMORY CELL 2833$_0$
MEMORY CELL 2823$_0$
MEMORY CELL 2813$_0$
2853
2852
2851
2850
2899
Z
Y

FIG. 28C

MEMORY DEVICE HAVING 2-TRANSISTOR VERTICAL MEMORY CELL AND WRAPPED DATA LINE STRUCTURE

PRIORITY APPLICATION

[0001] This application is a continuation of U.S. application Ser. No. 18/126,679, filed Mar. 27, 2023, which is a divisional of U.S. application Ser. No. 17/514,979, filed Oct. 29, 22021, now issued as U.S. Pat. No. 11,616,073, all of which are incorporated herein by reference in their entirety.

BACKGROUND

[0002] Memory devices are widely used in computers and many other electronic items to store information. Memory devices are generally categorized into two types: volatile memory device and non-volatile memory device. A memory device usually has numerous memory cells in which to store information. In a volatile memory device, information stored in the memory cells is lost if power supply is disconnected from the memory device. In a non-volatile memory device, information stored in the memory cells is retained even if supply power is disconnected from the memory device.

[0003] The description herein involves volatile memory devices. Most conventional volatile memory devices store information in the form of charge in a capacitor structure included in the memory cell. As demand for device storage density increases, many conventional techniques provide ways to shrink the size of the memory cell in order to increase device storage density for a given device area. However, physical limitations and fabrication constraints may pose a challenge to such conventional techniques if the memory cell size is to be shrunk to a certain dimension. Further, increased device storage density for a given area may cause excessive capacitive coupling between elements of adjacent memory cells. Unlike some conventional memory devices, the memory devices described herein include features that can overcome challenges faced by conventional techniques.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. **1** shows a block diagram of an apparatus in the form of a memory device including memory cells, according to some embodiments described herein.

[0005] FIG. **2** shows a schematic diagram of a portion of a memory device including a memory array of two-transistor (2T) memory cells, according to some embodiments described herein.

[0006] FIG. **3** shows the memory device of FIG. **2**, including example voltages used during a read operation of the memory device, according to some embodiments described herein.

[0007] FIG. **4** shows the memory device of FIG. **2**, including example voltages used during a write operation of the memory device, according to some embodiments described herein.

[0008] FIG. **5**, FIG. **6**, FIG. **7**A, FIG. **7**B, and FIG. **7**C show different views of a structure of the memory device of FIG. **2** including data lines having discontinuous wrapped portions, according to some embodiments described herein.

[0009] FIG. **8**A, FIG. **8**B, FIG. **8**C show different views of a structure of the memory device including data lines having continuous wrapped portions, according to some embodiments described herein.

[0010] FIG. **9** through FIG. **22**D show processes of forming a memory device, according to some embodiments described herein.

[0011] FIG. **23** through FIG. **27**B show processes of forming another memory device, according to some embodiments described herein.

[0012] FIG. **28**A, FIG. **28**B, and FIG. **28**C show different views of a structure of a memory device including multiple decks of memory cells, according to some embodiments described herein.

DETAILED DESCRIPTION

[0013] The memory device described herein includes volatile memory cells in which each of the memory cells can include two transistors (2T). One of the two transistors has a charge storage structure, which can form a memory element of the memory cell to store information. The memory device described herein can have a structure (e.g., a 4F2 cell footprint) that allows the size (e.g., footprint) of the memory device to be relatively smaller than the size (e.g., footprint) of similar conventional memory devices. The described memory device can include a single access line (e.g., word line) to control two transistors of a corresponding memory cell. This can lead to reduced power dissipation and improved processing. Each of the memory cells of the described memory device can include a cross-point gain cell structure (and cross-point operation), such that a memory cell can be accessed using a single access line (e.g., word line) and single data line (e.g., bit line) during an operation (e.g., a read or write operation) of the memory device. The described memory device can include data lines having respective wrapped portions that wrap around part of a channel region of a transistor of a respective memory cell. The wrapped portions of the data lines can improve operations of the memory device. In an example, the wrapped portions can mitigate or prevent static power (e.g., current leakage) that may occur in the memory cells. Other improvements and benefits of the described memory device and its variations are discussed below with reference to FIG. **1** through FIG. **28**C.

[0014] FIG. **1** shows a block diagram of an apparatus in the form of a memory device **100** including volatile memory cells, according to some embodiments described herein. Memory device **100** includes a memory array **101**, which can contain memory cells **102**. Memory device **100** can include a volatile memory device such that memory cells **102** can be volatile memory cells. An example of memory device **100** includes a dynamic random-access memory (DRAM) device. Information stored in memory cells **102** of memory device **100** may be lost (e.g., invalid) if supply power (e.g., supply voltage Vcc) is disconnected from memory device **100**. Hereinafter, supply voltage Vcc is referred to as representing some voltage levels; however, they are not limited to a supply voltage (e.g., Vcc) of the memory device (e.g., memory device **100**). For example, if the memory device (e.g., memory device **100**) has an internal voltage generator (not shown in FIG. **1**) that generates an internal voltage based on supply voltage Vcc, such an internal voltage may be used instead of supply voltage Vcc.

[0015] In a physical structure of memory device **100**, each of memory cells **102** can include transistors (e.g., two transistors) formed vertically (e.g., stacked on different layers) in different levels over a substrate (e.g., semicon-

ductor substrate) of memory device **100**. Memory device **100** can also include multiple levels (e.g., multiple decks) of memory cells where one level (e.g., one deck) of memory cells can be formed over (e.g., stacked on) another level (e.g., another deck) of additional memory cells. The structure of memory array **101**, including memory cells **102**, can include the structure of memory arrays and memory cells described below with reference to FIG. **2** through FIG. **28**C.

[0016] As shown in FIG. **1**, memory device **100** can include access lines **104** (e.g., "word lines") and data lines (e.g., bit lines) **105**. Memory device **100** can use signals (e.g., word line signals) on access lines **104** to access memory cells **102** and data lines **105** to provide information (e.g., data) to be stored in (e.g., written) or read (e.g., sensed) from memory cells **102**.

[0017] Memory device **100** can include an address register **106** to receive address information ADDR (e.g., row address signals and column address signals) on lines **107** (e.g., address lines). Memory device **100** can include row access circuitry **108** (e.g., X-decoder) and column access circuitry **109** (e.g., Y-decoder) that can operate to decode address information ADDR from address register **106**. Based on decoded address information, memory device **100** can determine which memory cells **102** are to be accessed during a memory operation. Memory device **100** can perform a write operation to store information in memory cells **102**, and a read operation to read (e.g., sense) information (e.g., previously stored information) in memory cells **102**. Memory device **100** can also perform an operation (e.g., a refresh operation) to refresh (e.g., to keep valid) the value of information stored in memory cells **102**. Each of memory cells **102** can be configured to store information that can represent at most one bit (e.g., a single bit having a binary 0 ("0") or a binary 1 ("1"), or more than one bit (e.g., multiple bits having a combination of at least two binary bits).

[0018] Memory device **100** can receive a supply voltage, including supply voltages Vcc and Vss, on lines **130** and **132**, respectively. Supply voltage Vss can operate at a ground potential (e.g., having a value of approximately zero volts). Supply voltage Vcc can include an external voltage supplied to memory device **100** from an external power source such as a battery or an alternating current to direct current (AC-DC) converter circuitry.

[0019] As shown in FIG. **1**, memory device **100** can include a memory control unit **118**, which includes circuitry (e.g., hardware components) to control memory operations (e.g., read and write operations) of memory device **100** based on control signals on lines (e.g., control lines) **120**. Examples of signals on lines **120** include a row access strobe signal RAS*, a column access strobe signal CAS*, a write-enable signal WE*, a chip select signal CS*, a clock signal CK, and a clock-enable signal CKE. These signals can be part of signals provided to a DRAM device.

[0020] As shown in FIG. **1**, memory device **100** can include lines (e.g., global data lines) **112** that can carry signals DQ**0** through DQN. In a read operation, the value (e.g., "0" or "1") of information (read from memory cells **102**) provided to lines **112** (in the form of signals DQ**0** through DQN) can be based on the values of the signals on data lines **105**. In a write operation, the value (e.g., "0" or "1") of information provided to data lines **105** (to be stored in memory cells **102**) can be based on the values of signals DQ**0** through DQN on lines **112**.

[0021] Memory device **100** can include sensing circuitry **103**, select circuitry **115**, and input/output (I/O) circuitry **116**. Column access circuitry **109** can selectively activate signals on lines (e.g., select lines) based on address signals ADDR. Select circuitry **115** can respond to the signals on lines **114** to select signals on data lines **105**. The signals on data lines **105** can represent the values of information to be stored in memory cells **102** (e.g., during a write operation) or the values of information read (e.g., sensed) from memory cells **102** (e.g., during a read operation).

[0022] I/O circuitry **116** can operate to provide information read from memory cells **102** to lines **112** (e.g., during a read operation) and to provide information from lines **112** (e.g., provided by an external device) to data lines **105** to be stored in memory cells **102** (e.g., during a write operation). Lines **112** can include nodes within memory device **100** or pins (or solder balls) on a package where memory device **100** can reside. Other devices external to memory device **100** (e.g., a hardware memory controller or a hardware processor) can communicate with memory device **100** through lines **107**, **112**, and **120**.

[0023] Memory device **100** may include other components, which are not shown in FIG. **1** so as not to obscure the example embodiments described herein. At least a portion of memory device **100** (e.g., a portion of memory array **101**) can include structures and operations similar to or the same as any of the memory devices described below with reference to FIG. **2** through FIG. **28**C.

[0024] FIG. **2** shows a schematic diagram of a portion of a memory device **200** including a memory array **201**, according to some embodiments described herein. Memory device **200** can correspond to memory device **100** of FIG. **1**. For example, memory array **201** can form part of memory array **101** of FIG. **1**. As shown in FIG. **2**, memory device **200** can include memory cells **210** through **215**, which are volatile memory cells (e.g., DRAM cells). For simplicity, similar or identical elements among memory cells **210** through **215** are given the same labels.

[0025] Each of memory cells **210** through **215** can include two transistors T**1** and T**2**. Thus, each of memory cells **210** through **215** can be called a 2T memory cell (e.g., 2T gain cell). Each of transistors T**1** and T**2** can include a field-effect transistor (FET). As an example, transistor T**1** can be a p-channel FET (PFET), and transistor T**2** can be an n-channel FET (NFET). Part of transistor T**1** can include a structure of a p-channel metal-oxide semiconductor (PMOS) transistor. Thus, transistor T**1** can include an operation similar to that of a PMOS transistor. Part of transistor T**2** can include an n-channel metal-oxide semiconductor (NMOS). Thus, transistor T**2** can include an operation similar to that of a NMOS transistor.

[0026] Transistor T**1** of memory device **200** can include a charge-storage based structure (e.g., a floating-gate based). As shown in FIG. **2**, each of memory cells **210** through **215** can include a charge storage structure **202**, which can include the floating gate of transistor T**1**. Charge storage structure **202** can form the memory element of a respective memory cell among memory cells **210** through **215**. Charge storage structure **202** can store charge. The value (e.g., "0" or "1") of information stored in a particular memory cell among memory cells **210** through **215** can be based on the amount of charge in charge storage structure **202** of that particular memory cell. For example, the value of information stored in a particular memory cell among memory cells

210 through **215** can be "0" or "1" (if each memory cell is configured as a single-bit memory cell) or "00", "01", "10", "11" (or other multi-bit values) if each memory cell is configured as a multi-bit memory cell.

[0027] As shown in FIG. **2**, transistor T**2** (e.g., the channel region of transistor T**2**) of a particular memory cell among memory cells **210** through **215** can be electrically coupled to (e.g., directly coupled to (contact)) charge storage structure **202** of that particular memory cell. Thus, a circuit path (e.g., current path) can be formed directly between transistor T**2** of a particular memory cell and charge storage structure **202** of that particular memory cell during an operation (e.g., a write operation) of memory device **200**. During a write operation of memory device **200**, a circuit path (e.g., current path) can be formed between a respective data line (e.g., data line **221** or **222**) and charge storage structure **202** of a particular memory cell through transistor T**2** (e.g., through the channel region of transistor T**2**) of the particular memory cell.

[0028] Memory cells **210** through **215** can be arranged in memory cell groups $\mathbf{201}_0$ and $\mathbf{201}_1$. FIG. **2** shows two memory cell groups (e.g., $\mathbf{201}_0$ and $\mathbf{201}_1$) as an example. However, memory device **200** can include more than two memory cell groups. Memory cell groups $\mathbf{201}_0$ and $\mathbf{201}_1$ can include the same number of memory cells. For example, memory cell group $\mathbf{201}_0$ can include memory cells **210**, **212**, and **214**, and memory cell group $\mathbf{201}_1$ can include memory cells **211**, **213**, and **215**. FIG. **2** shows three memory cells in each of memory cell groups $\mathbf{201}_0$ and $\mathbf{201}_1$ as an example. The number of memory cells in memory cell groups $\mathbf{201}_0$ and $\mathbf{201}_1$ can be different from three.

[0029] Memory device **200** can perform a write operation to store information in memory cells **210** through **215**, and a read operation to read (e.g., sense) information from memory cells **210** through **215**. Memory device **200** can be configured to operate as a DRAM device. However, unlike some conventional DRAM devices that store information in a structure such as a container for a capacitor, memory device **200** can store information in the form of charge in charge storage structure **202** (which can be a floating gate structure). As mentioned above, charge storage structure **202** can be the floating gate of transistor T**1**. During an operation (e.g., a read or write operation) of memory device **200**, an access line (e.g., a single access line) and a data line (e.g., a single data line) can be used to access a selected memory cell (e.g., target memory cell).

[0030] As shown in FIG. **2**, memory device **200** can include access lines (e.g., word lines) **241**, **242**, and **243** that can carry respective signals (e.g., word line signals) WL**1**, WL**2**, and WLn. Access lines **241**, **242**, and **243** can be used to access both memory cell groups $\mathbf{201}_0$ and $\mathbf{201}_1$. In the physical structure of memory device **200**, each of access lines **241**, **242**, and **243** can be structured as (can be formed from) at least one conductive line (one conductive line or multiple conductive lines where the multiple conductive lines can be electrically coupled (e.g., shorted) to each other).

[0031] Access lines **241**, **242**, and **243** can be selectively activated (e.g., activated one at a time) during an operation (e.g., read or write operation) of memory device **200** to access a selected memory cell (or selected memory cells) among memory cells **210** through **215**. A selected memory cell can be referred to as a target memory cell. In a read operation, information can be read from a selected memory cell (or selected memory cells). In a write operation, information can be stored in a selected memory cell (or selected memory cells).

[0032] In memory device **200**, a single access line (e.g., a single word line) can be used to control (e.g., turn on or turn off) transistors T**1** and T**2** of a respective memory cell during either a read or write operation of memory device **200**. Some conventional memory devices may use multiple (e.g., two separate) access lines to control access to a respective memory cell during read and write operations. In comparison with such conventional memory devices (that use multiple access lines for the same memory cell), memory device **200** uses a single access line (e.g., shared access line) in memory device **200** to control both transistors T**1** and T**2** of a respective memory cell to access the respective memory cell. This technique can save space and simplify operation of memory device **200**. Further, some conventional memory devices may use multiple data lines to access a selected memory cell (e.g., during a read operation) to read information from the selected memory cell. In memory device **200**, a single data line (e.g., data line **221** or **222**) can be used to access a selected memory cell (e.g., during a read operation) to read information from the selected memory cell. This may also simplify the structure, operation, or both of memory device **200** in comparison with conventional memory devices that use multiple data lines to access a selected memory cell.

[0033] In memory device **200**, the gate (not labeled in FIG. **2**) of each of transistors T**1** and T**2** can be part of a respective access line (e.g., a respective word line). As shown in FIG. **2**, the gate of each of transistors T**1** and T**2** of memory cell **210** can be part of access line **241**. The gate of each of transistors T**1** and T**2** of memory cell **211** can be part of access line **241**. For example, in the physical structure of memory device **200**, four different portions of a conductive material (e.g., four different portions of continuous piece of metal or polysilicon) that forms access line **241** can form the gates (e.g., four gates) of transistors T**1** and T**2** of memory cell **210** and the gates of transistors T**1** and T**2** of memory cell **211**, respectively.

[0034] The gate of each of transistors T**1** and T**2** of memory cell **212** can be part of access line **242**. The gate of each of transistors T**1** and T**2** of memory cells **213** can be part of access line **242**. For example, in the structure of memory device **200**, four different portions of a conductive material (e.g., four different portions of continuous piece of metal or polysilicon) that form access line **242** can form the gates (e.g., four gates) of transistors T**1** and T**2** of memory cell **212** and the gates of transistors T**1** and T**2** of memory cell **213**, respectively.

[0035] The gate of each of transistors T**1** and T**2** of memory cell **214** can be part of access line **243**. The gate of each of transistors T**1** and T**2** of memory cell **215** can be part of access line **243**. For example, in the structure of memory device **200**, four different portions of a conductive material (e.g., four different portions of continuous piece of metal or polysilicon) that form access line **243** can form the gates (e.g., four gates) of transistors T**1** and T**2** of memory cell **214** and the gates of transistors T**1** and T**2** of memory cell **215**, respectively.

[0036] In this description, a material can include a single material or a combination of multiple materials. A conductive material can include a single conductive material or combination multiple conductive materials.

[0037] Memory device **200** can include data lines (e.g., bit lines) **221** and **222** that can carry respective signals (e.g., bit line signals) BL**1** and BL**2**. During a read operation, memory device **200** can use data line **221** to obtain information read (e.g., sensed) from a selected memory cell of memory cell group $\mathbf{201}_0$, and data line **222** to read information from a selected memory cell of memory cell group $\mathbf{201}_1$. During a write operation, memory device **200** can use data line **221** to provide information to be stored in a selected memory cell of memory cell group $\mathbf{201}_0$, and data line **222** to provide information to be stored in a selected memory cell of memory cell group $\mathbf{201}_1$.

[0038] Memory device **200** can include a ground connection (e.g., ground plate) **297** coupled to each of memory cells **210** through **215**. Ground connection **297** can be structured from a conductive plate (e.g., a layer of conductive material) that can be coupled to a ground terminal of memory device **200**.

[0039] As an example, ground connection **297** can be part of a common conductive structure (e.g., a common conductive plate) that can be formed on a level of memory device **200** that is under the memory cells (e.g., memory cells **210** through **215**) of memory device **200**. In this example, the elements (e.g., part of transistors T**1** and T**2** or the entire transistors T**1** and T**2**) of each of the memory cells (e.g., memory cells **210** through **215**) of memory device **200** can be formed (e.g., formed vertically) over the common conductive structure (e.g., a common conductive plate) and electrically coupled to the common conductive structure.

[0040] In another example, ground connection **297** can be part of separate conductive structures (e.g., separate conductive strips) that can be formed on a level of memory device **200** that is under the memory cells (e.g., memory cells **210** through **215**) of memory device **200**. In this example, the elements (e.g., part of transistors T**1** and T**2**) of each of the memory cells (e.g., memory cells **210** through **215**) of memory device **200** can be formed over (e.g., formed vertically) respective conductive structures (e.g., respective conductive strips) among the separate conductive structures (e.g., separate conductive strips) and electrically coupled to the respective conductive structures.

[0041] As shown in FIG. **2**, transistor T**1** (e.g., the channel region of transistor T**1**) of a particular memory cell among memory cells **210** through **215** can be electrically coupled to (e.g., directly coupled to) ground connection **297** and electrically coupled to (e.g., directly coupled to) a respective data line (e.g., data line **221** or **222**). Thus, a circuit path (e.g., current path) can be formed between a respective data line (e.g., data line **221** or **222**) and ground connection **297** through transistor T**1** of a selected memory cell during an operation (e.g., a read operation) performed on the selected memory cell.

[0042] Memory device **200** can include read paths (e.g., circuit paths). Information read from a selected memory cell during a read operation can be obtained through a read path coupled to the selected memory cell. In memory cell group $\mathbf{201}_0$, a read path of a particular memory cell (e.g., memory cell **210**, **212**, or **214**) can include a current path (e.g., read current path) through a channel region of transistor T**1** of that particular memory cell, data line **221**, and ground connection **297**. In memory cell group $\mathbf{201}_1$, a read path of a particular memory cell (e.g., memory cell **211**, **213**, or **215**) can include a current path (e.g., read current path) through a channel region of transistor T**1** of that particular memory cell, data line **222**, and ground connection **297**. In the example where transistor T**1** is a PFET (e.g., a PMOS), the current in the read path (e.g., during a read operation) can include a hole conduction (e.g., hole conduction in the direction from data line **221** to ground connection **297** through the channel region (e.g., p-channel region) of transistor T**1**). Since transistor T**1** can be used in a read path to read information from the respective memory cell during a read operation, transistor T**1** can be called a read transistor and the channel region of transistor T**1** can be called a read channel region.

[0043] Memory device **200** can include write paths (e.g., circuit paths). Information to be stored in a selected memory cell during a write operation can be provided to the selected memory cell through a write path coupled to the selected memory cell. In memory cell group $\mathbf{201}_0$, a write path of a particular memory cell can include transistor T**2** (e.g., can include a write current path through a channel region of transistor T**2**) of that particular memory cell and data line **221**. In memory cell group $\mathbf{201}_1$, a write path of a particular memory cell (e.g., memory cell **211**, **213**, or **215**) can include transistor T**2** (e.g., can include a write current path through a channel region of transistor T**2**) of that particular memory cell and data line **222**. In the example where transistor T**2** is an NFET (e.g., NMOS), the current in a write path (e.g., during a write operation) can include an electron conduction (e.g., electron conduction in the direction from data line **221** to charge storage structure **202**) through the channel region (e.g., n-channel region) of transistor T**2**. Since transistor T**2** can be used in a write path to store information in a respective memory cell during a write operation, transistor T**2** can be called a write transistor and the channel region of transistor T**2** can be called a write channel region.

[0044] Each of transistors T**1** and T**2** can have a threshold voltage (Vt). Transistor T**1** has a threshold voltage Vt**1**. Transistor T**2** has a threshold voltage Vt**2**. The values of threshold voltages Vt**1** and Vt**2** can be different (unequal values). For example, the value of threshold voltage Vt**2** can be greater than the value of threshold voltage Vt**1**. The difference in values of threshold voltages Vt**1** and Vt**2** allows reading (e.g., sensing) of information stored in charge storage structure **202** in transistor T**1** on the read path during a read operation without affecting (e.g., without turning on) transistor T**2** on the write path (e.g., path through transistor T**2**). This can prevent leaking of charge (e.g., during a read operation) from charge storage structure **202** through transistor T**2** of the write path.

[0045] In a structure of memory device **200**, transistors T**1** and T**2** can be formed (e.g., engineered) such that threshold voltage Vt**1** of transistor T**1** can be less than zero volts (e.g., Vt**1**<0V) regardless of the value (e.g., "0" or "1") of information stored in charge storage structure **202** of transistor T**1**, and Vt**1**<Vt**2**. Charge storage structure **202** can be in state "0" when information having a value of "0" is stored in charge storage structure **202**. Charge storage structure **202** can be in state "1" when information having a value of "1" is stored in charge storage structure **202**. Thus, in this structure, the relationship between the values of threshold voltages Vt**1** and Vt**2** can be expressed as follows: Vt**1** for state "0"<Vt**1** for state "1"<0V, and Vt**2**=0V (or alternatively Vt**2**>0V).

[0046] In an alternative structure of memory device **200**, transistors T**1** and T**2** can be formed (e.g., engineered) such

that Vt**1** for state "0"<Vt**1** for state "1", where Vt**1** for state "0"<0V (or alternatively Vt**1** for state "0"=0V), Vt**1** for state "1">0V, and Vt**1**<Vt**2**.

[0047] In another alternative structure, transistors T**1** and T**2** can be formed (e.g., engineered) such that Vt**1** for state "0"<Vt**1** for state "1", where Vt**1** for state "0"=0V (or alternatively Vt**1** for state "0">0V), and Vt**1**<Vt**2**.

[0048] During a read operation of memory device **200**, only one memory cell of the same memory cell group can be selected one at a time to read information from the selected memory cell. For example, memory cells **210**, **212**, and **214** of memory cell group $\mathbf{201}_0$ can be selected one at a time during a read operation to read information from the selected memory cell (e.g., one of memory cells **210**, **212**, and **214** in this example). In another example, memory cells **211**, **213**, and **215** of memory cell group $\mathbf{201}_1$ can be selected one at a time during a read operation to read information from the selected memory cell (e.g., one of memory cells **211**, **213**, and **215** in this example).

[0049] During a read operation, memory cells of different memory cell groups (e.g., memory cell groups $\mathbf{201}_0$ and $\mathbf{201}_1$) that share the same access line (e.g., access line **241**, **242**, or **243**) can be concurrently selected (or alternatively can be sequentially selected). For example, memory cells **210** and **211** can be concurrently selected during a read operation to read (e.g., concurrently read) information from memory cells **210** and **211**. Memory cells **212** and **213** can be concurrently selected during a read operation to read (e.g., concurrently read) information from memory cells **212** and **213**. Memory cells **214** and **215** can be concurrently selected during a read operation to read (e.g., concurrently read) information from memory cells **214** and **215**.

[0050] The value of information read from the selected memory cell of memory cell group $\mathbf{201}_0$ during a read operation can be determined based on the value of a current detected (e.g., sensed) from a read path (described above) that includes data line **221**, transistor T**1** of the selected memory cell (e.g., memory cell **210**, **212**, or **214**), and ground connection **297**. The value of information read from the selected memory cell of memory cell group $\mathbf{201}_1$ during a read operation can be determined based on the value of a current detected (e.g., sensed) from a read path that includes data line **222**, transistor T**1** of the selected memory cell (e.g., memory cell **211**, **213**, or **215**), and ground connection **297**.

[0051] Memory device **200** can include detection circuitry (not shown) that can operate during a read operation to detect (e.g., sense) a current (e.g., current I**1**, not shown) on a read path that includes data line **221**, and detect a current (e.g., current I**2**, not shown) on a read path that includes data line **222**. The value of the detected current can be based on the value of information stored in the selected memory cell. For example, depending on the value of information stored in the selected memory cell of memory cell group $\mathbf{201}_0$, the value of the detected current (e.g., the value of current I**1**) on data line **221** can be zero or greater than zero. Similarly, depending on the value of information stored in the selected memory cell of memory cell group $\mathbf{201}_1$, the value of the detected current (e.g., the value of current I**2**) on data line **222** can be zero or greater than zero. Memory device **200** can include circuitry (not shown) to translate the value of a detected current into the value (e.g., "0", "1", or a combination of multi-bit values) of information stored in the selected memory cell.

[0052] During a write operation of memory device **200**, only one memory cell of the same memory cell group can be selected at a time to store information in the selected memory cell. For example, memory cells **210**, **212**, and **214** of memory cell group $\mathbf{201}_0$ can be selected one at a time during a write operation to store information in the selected memory cell (e.g., one of memory cell **210**, **212**, and **214** in this example). In another example, memory cells **211**, **213**, and **215** of memory cell group $\mathbf{201}_1$ can be selected one at a time during a write operation to store information in the selected memory cell (e.g., one of memory cell **211**, **213**, and **215** in this example).

[0053] During a write operation, memory cells of different memory cell groups (e.g., memory cell groups $\mathbf{201}_0$ and $\mathbf{201}_1$) that share the same access line (e.g., access line **241**, **242**, or **243**) can be concurrently selected. For example, memory cells **210** and **211** can be concurrently selected during a write operation to store (e.g., concurrently store) information in memory cells **210** and **211**. Memory cells **212** and **213** can be concurrently selected during a write operation to store (e.g., concurrently store) information in memory cells **212** and **213**. Memory cells **214** and **215** can be concurrently selected during a write operation to store (e.g., concurrently store) information in memory cells **214** and **215**.

[0054] Information to be stored in a selected memory cell of memory cell group $\mathbf{201}_0$ during a write operation can be provided through a write path (described above) that includes data line **221** and transistor T**2** of the selected memory cell (e.g., memory cell **210**, **212**, or **214**). Information to be stored in a selected memory cell of memory cell group $\mathbf{201}_1$ during a write operation can be provided through a write path (described above) that includes data line **222** and transistor T**2** of the selected memory cell (e.g., memory cell **211**, **213**, or **215**). As described above, the value (e.g., binary value) of information stored in a particular memory cell among memory cells **210** through **215** can be based on the amount of charge in the charge storage structure **202** of that particular memory cell.

[0055] In a write operation, the amount of charge in the charge storage structure **202** of a selected memory cell can be changed (to reflect the value of information stored in the selected memory cell) by applying a voltage on a write path that includes transistor T**2** of that particular memory cell and the data line (e.g., data line **221** or **222**) coupled to that particular memory cell. For example, a voltage having one value (e.g., 0V) can be applied on data line **221** (e.g., provide 0V to signal BL**1**) if information to be stored in a selected memory cell among memory cells **210**, **212**, and **214** has one value (e.g., "0"). In another example, a voltage having another value (e.g., a positive voltage) can be applied on data line **221** (e.g., provide a positive voltage to signal BL**1**) if information to be stored in a selected memory cell among memory cells **210**, **212**, and **214** has another value (e.g., "1"). Thus, information can be stored (e.g., directly stored) in the charge storage structure **202** of a particular memory cell by providing the information to be stored (e.g., in the form of a voltage) on a write path (that includes transistor T**2**) of that particular memory cell.

[0056] FIG. **3** shows memory device **200** of FIG. **2** including example voltages V**1**, V**2**, and V**3** used during a read operation of memory device **200**, according to some embodiments described herein. The example of FIG. **3** assumes that memory cells **210** and **211** are selected memory

cells (e.g., target memory cells) during a read operation to read (e.g., to sense) information stored (e.g., previously stored) in memory cells **210** and **211**. Memory cells **212** through **215** are assumed to be unselected memory cells. This means that memory cells **212** through **215** are not accessed, and information stored in memory cells **212** through **215** is not read while information is read from memory cells **210** and **211** in the example of FIG. **3**. In this example, access line **241** can be called a selected access line (e.g., selected word line), which is the access line associated with (e.g., coupled to) selected memory cells (e.g., memory cells **210** and **211** in this example). In this example, access lines **242** and **243** can be called unselected access lines (e.g., unselected word line), which are the access lines associated with (e.g., coupled to) unselected memory cells (e.g., memory cells **212**, **213**, **214**, and **215** in this example).

[0057] In FIG. **3**, voltages V**1**, V**2**, and V**3** can represent different voltages applied to respective access lines **241**, **242**, and **243** and data lines **221** and **222** during a read operation of memory device **200**. Voltage V**1** can be applied to the selected access line (e.g., access line **241**). In a read operation, Voltage V**2** can be applied to the unselected access lines (e.g., access lines **242** and **243**).

[0058] Voltages V**1**, V**2**, and V**3** can have different values. As an example, voltages V**1**, V**2**, and V**3** can have values −1V, 0V, and 0.5V, respectively. The specific values of voltages used in this description are only example values. Different values may be used. For example, voltage V**1** can have a negative value range (e.g., the value of voltage V**1** can be from −3V to −1V).

[0059] In the read operation shown in FIG. **3**, voltage V**1** can have a value (voltage value) to turn on transistor T**1** of each of memory cells **210** and **211** (selected memory cells in this example) and turn off (or keep off) transistor T**2** of each of memory cells **210** and **211**. This allows information to be read from memory cells **210** and **211**. Voltage V**2** can have a value, such that transistors T**1** and T**2** of each of memory cells **212** through **215** (unselected memory cells in this example) are turned off (e.g., kept off). Voltage V**3** can have a value, such that a current (e.g., read current) may be formed on a read path that includes data line **221** and transistor T**1** of memory cell **210**, and a read path (a separate read path) that includes data line **222** and transistor T**1** of memory cell **212**. This allows a detection of current on the read paths (e.g., on respective data lines **221** and **222**) coupled to memory cells **210** and **211**, respectively. A detection circuitry (not shown) of memory device **200** can operate to translate the value of the detected current (during reading of information from the selected memory cells) into the value (e.g., "0", "1", or a combination of multi-bit values) of information read from the selected memory cell. In the example of FIG. **3**, the value of the detected currents on data lines **221** and **222** can be translated into the values of information read from memory cells **210** and **211**, respectively.

[0060] In the read operation shown in FIG. **3**, the voltages applied to respective access lines **241**, **242**, and **243** can cause transistors T**1** and T**2** of each of memory cells **212** through **215**, except transistor T**1** of each of memory cells **210** and **211** (selected memory cells), to turn off (or to remain turned off). Transistor T**1** of memory cell **210** (selected memory cell) may or may not turn on, depending on the value of the threshold voltage Vt**1** of transistor T**1** of memory cell **210**. Transistor T**1** of memory cell **211** (selected memory cell) may or may not turn on, depending on the value of the threshold voltage Vt**1** of transistor T**1** of memory cell **211**. For example, if transistor T**1** of each of memory cells (e.g., **210** through **215**) of memory device **200** is configured (e.g., structured) such that the threshold voltage of transistor T**1** is less than zero (e.g., Vt**1**<−1V) regardless of the value (e.g., the state) of information stored in a respective memory cell **210**, then transistor T**1** of memory cell **210**, in this example, can turn on and conduct a current on data line **221** (through transistor T**1** of memory cell **210**). In this example, transistor T**1** of memory cell **211** can also turn on and conduct a current on data line **222** (through transistor T**1** of memory cell **211**). Memory device **200** can determine the value of information stored in memory cells **210** and **211** based on the value of the currents on data lines **221** and **222**, respectively. As described above, memory device **200** can include detection circuitry to measure the value of currents on data lines **221** and **222** during a read operation.

[0061] FIG. **4** shows memory device **200** of FIG. **2** including example voltages V**4**, V**5**, V**6**, and V**7** used during a write operation of memory device **200**, according to some embodiments described herein. The example of FIG. **4** assumes that memory cells **210** and **211** are selected memory cells (e.g., target memory cells) during a write operation to store information in memory cells **210** and **211**. Memory cells **212** through **215** are assumed to be unselected memory cells. This means that memory cells **212** through **215** are not accessed and information is not to be stored in memory cells **212** through **215** while information is stored in memory cells **210** and **211** in the example of FIG. **4**.

[0062] In FIG. **4**, voltages V**4**, V**5**, V**6**, and V**7** can represent different voltages applied to respective access lines **241**, **242**, and **243** and data lines **221** and **222** during a write operation of memory device **200**. In a write operation, voltage V**4** can be applied to the selected access line (e.g., access line **241**). Voltage V**5** can be applied to the unselected access lines (e.g., access lines **242** and **243**).

[0063] Voltages V**4**, V**5**, V**6**, and V**7** can have different values. As an example, voltages V**4** and V**5** can have values of 3V and 0V, respectively. These values are example values. Different values may be used.

[0064] The values of voltages V**6** and V**7** can be the same or different depending on the value (e.g., "0" or "1") of information to be stored in memory cells **210** and **211**. For example, the values of voltages V**6** and V**7** can be the same (e.g., V**6**=V**7**) if the memory cells **210** and **211** are to store information having the same value. As an example, V**6**=V**7**=0V if information to be stored in each memory cell **210** and **211** is "0". In another example, V**6**=V**7**=V+ (e.g., V+ is a positive voltage (e.g., from 1V to 3V)) if information to be stored in each memory cell **210** and **211** is "1".

[0065] In another example, the values of voltages V**6** and V**7** can be different (e.g., V**6**/V**7**) if the memory cells **210** and **211** are to store information having different values. As an example, V**6**=0V if "0" is to be stored in memory cell **210**, and V**7**=V+ (e.g., V+ is a positive voltage (e.g., from 1V to 3V)) if "1" is to be stored in memory cell **211**. As another example, V**6**=V+ (e.g., V+ is a positive voltage (e.g., from 1V to 3V)) if "1" is to be stored in memory cell **210**, and V**7**=0V if "0" is to be stored in memory cell **211**.

[0066] The range of voltage of 1V to 3V is used here as an example. A different range of voltages can be used. Further, instead of applying 0V (e.g., V**6**=0V or V**7**=0V) to a

particular write data line (e.g., data line **221** or **222**) for storing information having a value of "0" to the memory cell (e.g., memory cell **210** or **211**) coupled to that particular write data line, a positive voltage (e.g., V**6**>0V or V**7**>0V) may be applied to that particular data line.

[0067] In a write operation of memory device **200** of FIG. **4**, voltage V**5** can have a value (e.g., V**5**=0V or V**5**<0V), such that transistors T**1** and T**2** of each of memory cells **212** through **215** (unselected memory cells, in this example) are turned off (e.g., kept off). Voltage V**4** can have a value (e.g., V**4**>0V) to turn on transistor T**2** of each of memory cells **210** and **211** (selected memory cells in this example) and form a write path between charge storage structure **202** of memory cell **210** and data line **221**, and a write path between charge storage structure **202** of memory cell **211** and data line **222**. A current (e.g., write current) may be formed between charge storage structure **202** of memory cell **210** (selected memory cell) and data line **221**. This current can affect (e.g., change) the amount of charge on charge storage structure **202** of memory cell **210** to reflect the value of information to be stored in memory cell **210**. A current (e.g., another write current) may be formed between charge storage structure **202** of memory cell **211** (selected memory cell) and data line **222**. This current can affect (e.g., change) the amount of charge on charge storage structure **202** of memory cell **211** to reflect the value of information to be stored in memory cell **211**.

[0068] In the example write operation of FIG. **4**, the value of voltage V**6** may cause charge storage structure **202** of memory cell **210** to discharge or to be charged, such that the resulting charge (e.g., charge remaining after the discharge or charge action) on charge storage structure **202** of memory cell **210** can reflect the value of information stored in memory cell **210**. Similarly, the value of voltage V**7** in this example may cause charge storage structure **202** of memory cell **211** to discharge or to be charged, such that the resulting charge (e.g., charge remaining after the discharge or charge action) on charge storage structure **202** of memory cell **211** can reflect the value of information stored in memory cell **211**.

[0069] FIG. **5**, FIG. **6**, FIG. **7**A, FIG. **7**B, and FIG. **7**C show different views of a structure of memory device **200** of FIG. **2** with respect to the X, Y, and Z directions, according to some embodiments described herein. For simplicity, cross-sectional lines (e.g., hatch lines) are omitted from most of the elements shown in FIG. **5**, FIG. **6**, FIG. **7**A, FIG. **7**B, and FIG. **7**C and other figures (e.g., FIG. **8**A through FIG. **28**C) in the drawings described herein. Some elements of memory device **200** (and other memory devices described herein) may be omitted from a particular figure of the drawings so as to not obscure the description of the element (or elements) being described in that particular figure. The dimensions (e.g., physical structures) of the elements shown in the drawings described herein are not scaled.

[0070] FIG. **5** and FIG. **6** show different 3-dimensional views (e.g., isometric views) of memory device **200** including memory cell **210** with respect to the X, Y, and Z directions. FIG. **7**A shows a side view (e.g., cross-sectional view) of memory device **200** including memory cells **210**, **211**, **216**, and **217** with respect to the X-Z direction taken along line **7**A in FIG. **5** and FIG. **6**. FIG. **7**B shows a view (e.g., cross-sectional view) taken along line **7**B of FIG. **7**A. FIG. **7**C shows a top view (e.g., plan view) of memory device **200** of FIG. **7**A including relative locations of data lines **221**, **222**, **223**, and **224** (and associated signals BL**1**, BL**2**, BL**3**, and BL**4**), and access lines **241**, **242**, and **243** (associated signals WL**1**, WL**2**, WL**3**, and WL**4**). For simplicity, other elements of memory device **200** are omitted from FIG. **7**C.

[0071] The following description refers to FIG. **5**, FIG. **6**, FIG. **7**A, FIG. **7**B, and FIG. **7**C. FIG. **5** and FIG. **6** show the structure of one memory cell (e.g., memory cell **210**) of memory device **200**. The structures of other memory cells (e.g., memory cells **211** through **215** in FIG. **2**) of memory device **200** can be similar to or the same as the structure of memory cell **210** in FIG. **5** through FIG. **7**C. In FIG. **2** through FIG. **7**C, the same elements are given the same reference numbers. Some portions (e.g., gate oxide and cell isolation structures) of memory device **200** are omitted from FIG. **5** through FIG. **7**C so as to not obscure the elements of memory device **200** in the embodiments described herein.

[0072] As shown in FIG. **5**, memory device **200** can include a substrate **599** over which memory cell **210** (and other memory cells (not shown) of memory device **200**) can be formed. Transistors T**1** and T**2** of memory cell **210** can be formed vertically with respect to substrate **599**. Substrate **599** can be a semiconductor substrate (e.g., silicon-based substrate) or other type of substrate. The Z-direction (e.g., vertical direction) is a direction perpendicular to (e.g., outward from) substrate **599**. The Z-direction is also perpendicular to (e.g., extended vertically from) the X-direction and the Y-direction. The X-direction and Y-direction are perpendicular to each other.

[0073] As shown in FIG. **5** and FIG. **6**, ground connection **297** can include a structure (e.g., a piece (e.g., a layer)) of conductive material (e.g., conductive region) located over (formed over) substrate **599**. Example materials for ground connection **297** include a piece of metal, conductively doped polysilicon, or other conductive materials. Ground connection **297** can be coupled to a ground terminal (not shown) of memory device **200**. FIG. **5** and FIG. **6** show ground connection **297** contacting (e.g., directly coupled to) substrate **599** as an example. In an alternative structure, memory device **200** can include a dielectric (e.g., a layer of dielectric material, not shown) between ground connection **297** and substrate **599**.

[0074] As shown in FIG. **5**, FIG. **6**, FIG. **7**A, and FIG. **7**B, memory device **200** can include a semiconductor material **596** formed over ground connection **297**. Semiconductor material **596** can include a structure (e.g., a piece (e.g., a layer)) of silicon, polysilicon, or other semiconductor material, and can include a doped region (e.g., p-type doped region), or other conductive materials.

[0075] FIG. **7**A shows memory cells **216** and **217** and associated data lines **223** and **224** that are not shown in FIG. **2**. However, as shown in FIG. **7**A and FIG. **7**C, memory cells **216** and **217** can share access line **241** with memory cells **210** and **211**.

[0076] As shown in FIG. **5**, FIG. **6**, and FIG. **7**A, access line **241** can be structured by (can include) a combination of portions **541**F and **541**B (e.g., front and back conductive portions) that can be opposite from each other in respect to (looking from) the Y-direction. Each of portions **541**F and **541**B can include a conductive material (or a combination of materials) that can be structured as a conductive line (e.g., conductive region) having a length extending continuously in the X-direction. Thus, portions **541**F and **541**B can be part

of conductive lines that are opposite from each other (e.g., opposite from each other in the Y-direction).

[0077] Each of portions **541**F and **541**B can include a structure (e.g., a piece (e.g., a layer)) of conductive material (e.g., metal, conductively doped polysilicon, or other conductive materials). Each of portions **541**F and **541**B can have a length (shown in FIG. **5**) in the X-direction, a width (shown in FIG. **5**) in the Z-direction, and a thickness (shown in FIG. **8**A) in the Y-direction.

[0078] Portions **541**F and **541**B can be electrically coupled to each other. For example, memory device **200** can include a conductive material (e.g., not shown) that can contact (e.g., electrically couple to) portions **541**F and **541**B, such that portions **541**F and **541**B (which are part of a single access line **241**) can be concurrently applied by the same signal (e.g., signal WL**1**).

[0079] In an alternative structure of memory device **200**, one of the two portions (e.g., portions **541**F and **541**B) of each of the access lines of memory device **200** can be omitted. For example, either portion **541**F or portion **541**B be omitted, such that access line **241** can include only either portion **541**F or portion **541**B. In the structure shown in FIG. **5**, FIG. **6**, FIG. **7**A, and FIG. **7**B, including two portions (e.g., portions **541**F and **541**B) in each access line and can help better control transistor T**1** (e.g., transistor T**1**, shown schematically in FIG. **2**) of each of the memory cells of memory device **200** during a read operation.

[0080] Charge storage structure **202** (FIG. **5** through FIG. **7**B) of each memory cell of memory device **200** can include a charge storage material (or a combination of materials), which can include a piece (e.g., a layer) of semiconductor material (e.g., polysilicon), a piece (e.g., a layer) of metal, or a piece of material (or materials) that can trap charge. The materials for charge storage structure **202** and the portions (e.g., portions **541**F and **541**B in FIG. **5**) of the access lines (e.g., access line **241**) of memory device **200** can be the same or can be different. As shown in FIG. **5**, charge storage structure **202** can include a portion (e.g., bottom portion) that is closer (e.g., extends in the Z-direction closer) to substrate **599** than the bottom portion of each of portions **541**F and **541**B of access line **241**.

[0081] As shown in FIG. **7**A, each charge storage structure **202** can include an edge (e.g., top edge) **202'**, and portions **541**F and **541**B of access line **241** can include respective edges (e.g., bottom edges) **541'**. FIG. **7**A shows an example where edge **202'** is at a specific distance (e.g., distance shown in FIG. **7**A) from edges **541'**. However, the distance between edge **202'** of charge storage structure **202** and edges **541'** of portions **541**F and **541**B may vary. For example, FIG. **7**A shows edges **541'** being below edge **202'** with respect to the Z-direction, such that portions **541**F and **541**B can overlap (in the Z-direction) charge storage structure **202**. However, edges **541'** can alternatively be above edge **202'** with respect to the Z-direction, such that portions **541**F and **541**B may not overlap (in the Z-direction) charge storage structure **202**.

[0082] As shown in FIG. **5**, FIG. **6**, FIG. **7**A, FIG. **7**B, memory device **200** can include material **520** located between data line **221** and charge storage structure **202**. Material **520** can be electrically coupled to (e.g., directly coupled to (contact)) data line **221**. Material **520** can also be electrically coupled to (e.g., directly coupled to (contact)) charge storage structure **202** of memory cell **210**. As described above, charge storage structure **202** of memory cell **210** can form the memory element of memory cell **210**. Thus, memory cell **210** can include a memory element (which is charge storage structure **202**) located between substrate **599** and material **520** with respect to the Z-direction, and the memory element contacts (e.g., directly coupled to) material **520**.

[0083] Material **520** can form a source (e.g., source terminal), a drain (e.g., drain terminal), and a channel region (e.g., write channel region) between the source and the drain of transistor T**2** of memory cell **210**. Thus, as shown in FIG. **5**, FIG. **6**, and FIG. **7**A, the source, channel region, and the drain of transistor T**2** of memory cell **210** can be formed from a single piece of the same material (or alternatively, a single piece of the same combination of materials), such as material **520**. Therefore, the source, the drain, and the channel region of transistor T**2** of memory cell **210** can be formed from the same material (e.g., material **520**) of the same conductivity type (e.g., either n-type or p-type). Other memory cells of memory device **200** can also include material **520** like memory cell **210**.

[0084] Material **520** can include a structure (e.g., a piece (e.g., a layer)) of semiconductor material. In the example where transistor T**2** is an NFET (as described above), material **520** can include n-type semiconductor material (e.g., n-type silicon).

[0085] In another example, the semiconductor material that forms material **520** can include a structure (e.g., a piece) of oxide material. Examples of the oxide material used for material **520** include semiconducting oxide materials, transparent conductive oxide materials, and other oxide materials.

[0086] As an example, material **520** can include at least one of zinc tin oxide (ZTO), indium zinc oxide (IZO), zinc oxide (ZnO_x), indium gallium zinc oxide (IGZO), indium gallium silicon oxide (IGSO), indium oxide (InO_x, In_2O_3), tin oxide (SnO_2), titanium oxide (TiO_x), zinc oxide nitride ($Zn_xO_yN_z$), magnesium zinc oxide ($Mg_xZn_yO_z$), indium zinc oxide ($In_xZn_yO_z$), indium gallium zinc oxide ($In_xGa_yZn_zO_a$), zirconium indium zinc oxide ($Zr_xIn_yZn_zO_a$), hafnium indium zinc oxide ($Hf_xIn_yZn_zO_a$), tin indium zinc oxide ($Sn_xIn_yZn_zO_a$), aluminum tin indium zinc oxide ($Al_xSn_yIn_zZn_aO_a$), silicon indium zinc oxide ($Si_xIn_yZn_zO_a$), zinc tin oxide ($Zn_xSn_yO_z$), aluminum zinc tin oxide ($Al_xZn_ySn_zO_a$), gallium zinc tin oxide ($Ga_xZn_ySn_zO_a$), zirconium zinc tin oxide ($Zr_xZn_ySn_zO_a$), indium gallium silicon oxide (InGaSiO), and gallium phosphide (GaP).

[0087] Using the materials listed above in memory device **200** provides improvement and benefits for memory device **200**. For example, during a read operation, to read information from a selected memory cell (e.g., memory cell **210**), charge from charge storage structure **202** of the selected memory cell may leak to transistor T**2** of the selected memory cell. Using the material listed above for the channel region (e.g., material **520**) of transistor T**2** can reduce or prevent such a leakage. This improves the accuracy of information read from the selected memory cell and improves the retention of information stored in the memory cells of the memory device (e.g., memory device **200**) described herein.

[0088] The materials listed above are examples of material **520**. However, other materials (e.g., a relatively high bandgap material) different from the above-listed materials can be used.

[0089] As shown in FIG. **5**, FIG. **6**, and FIG. **7**A, material **520** and charge storage structure **202** of memory cell **210** can be electrically coupled (e.g., directly coupled) to each other, such that material **520** can contact charge storage structure **202** of memory cell **210** without an intermediate material (e.g., without a conductive material) between charge storage structure **202** of memory cell **210** and material **520**. In an alternative structure (not shown), material **520** can be electrically coupled to charge storage structure **202** of memory cell **210**, such that material **520** is not directly coupled to (not contacting) charge storage structure **202** of memory cell **210**, but material **520** is coupled to (e.g., indirectly contacting) charge storage structure **202** of memory cell **210** through an intermediate material (e.g., a conductive material) between charge storage structure **202** of memory cell **210** and material **520**.

[0090] As shown in FIG. **5**, FIG. **6**, and FIG. **7**A, memory cell **210** can include a material **510**, which can include a structure (e.g., a piece (e.g., a layer)) of semiconductor material. Example materials for material **510** can include silicon, polysilicon (e.g., undoped or doped polysilicon), germanium, silicon-germanium, or other semiconductor materials and semiconducting oxide materials (oxide semiconductors, e.g., SnO or other oxide semiconductors).

[0091] As described above with reference to FIG. **2**, transistor T**1** of memory cell **210** includes a channel region (e.g., read channel region). In FIG. **5**, FIG. **6**, and FIG. **7**A, the channel region of transistor T**1** of memory cell **210** can include (e.g., can be formed from) material **510**. Material **510** can be electrically coupled to (e.g., directly coupled to (contact) data line **221**. As described above with reference to FIG. **2**, memory cell **210** can include a read path. In FIG. **5**, FIG. **6**, and FIG. **7**A, material **510** (e.g., the read channel region of transistor T**1** of memory cell **210**) can be part of the read path of memory cell **210** that can carry a current (e.g., read current) during a read operation of reading information from memory cell **210**. For example, during a read operation, to read information from memory cell **210**, material **510** can conduct a current (e.g., read current (e.g., holes)) between data line **221** and ground connection **297** (through part of semiconductor material **596**). The direction of the read current can be from data line **221** to ground connection **297** (through material **510** and part of semiconductor material **596**). In the example where transistor T**1** is a PFET and transistor T**2** is an NFET, the material that forms material **510** can have a different conductivity type from material **520**. For example, material **510** can include p-type semiconductor material (e.g., p-type silicon) regions, and material **520** can include n-type semiconductor material (e.g., n-type gallium phosphide (GaP)) regions.

[0092] As shown in FIG. **5**, FIG. **6**, and FIG. **7**A, memory cell **210** can include dielectric materials **515**A and **515**B. Dielectric materials **515**A and **515**B can be gate oxide regions that electrically separate each of charge storage structure **202** and material **520** from material **510** (e.g., the channel region of transistor T**1**). Dielectric materials **515**A and **515**B can also electrically separate charge storage structure **202** from semiconductor material **596**.

[0093] Example materials for dielectric materials **515**A and **515**B include silicon dioxide, hafnium oxide (e.g., HfO_2), aluminum oxide (e.g., Al_2O_3), or other dielectric materials. In an example structure of memory device **200**, dielectric materials **515**A and **515**B include a high-k dielectric material (e.g., a dielectric material having a dielectric constant greater than the dielectric constant of silicon dioxide). Using such a high-k dielectric material (instead of silicon dioxide) can improve the performance (e.g., reduce current leakage, increase drive capability of transistor T**1**, or both) of memory device **200**.

[0094] As shown in FIG. **7**A, the memory cells (e.g., memory cells **210**, **211**, **216**, and **217**) of memory device **200** can share (e.g., can electrically couple to) semiconductor material **596**. For example, the read channel regions of the memory cells (e.g., material **510** of each of memory cells **210**, **211**, **216**, and **217**) of memory device **200** can contact (e.g., can be electrically coupled to) semiconductor material **596**.

[0095] As shown in FIG. **5**, FIG. **6**, and FIG. **7**A, memory device **200** can include a conductive region **597** (e.g., a common conductive plate) under the memory cells (e.g., memory cells **210**, **211**, **216**, and **217** in FIG. **7**A) of memory device **200**. Conductive region **597** can include at least one of the materials (e.g., doped polysilicon) of semiconductor material **596** and the material (e.g., metal or doped polysilicon) of ground connection **297**. For example, conductive region **597** can include the material of semiconductor material **596**, the material of ground connection **297**, or the combination of the materials of semiconductor material **596** and ground connection **297**. Thus, as shown FIG. **7**A, the memory cells (e.g., memory cells **210**, **211**, **216**, and **217**) of memory device **200** can share conductive region **597** (which can include any combination of semiconductor material **596** and ground connection **297**).

[0096] As shown in FIG. **5** and FIG. **6**, part of portion **541**F can be adjacent part of material **510** and part of material **520** and can span across (e.g., overlap in the X-direction) part of material **510** and part of material **520**. As described above, material **510** can form part of a read channel region of transistor T**1** and material **520** can form part of a write channel region of transistor T**2**. Thus, as shown in FIG. **5** and FIG. **6**, part of portion **541**F can span across (e.g., overlap) part of (e.g., on a side (e.g., front side) in the Y-direction) both read and write channel regions of transistors T**1** and T**2**, respectively. Similarly, part of portion **541**B can be adjacent material **510** and a part of material **520**, and can span across (e.g., overlap in the X-direction) part of (e.g., on another side (e.g., back side opposite from the front side) in the Y-direction) material **510** and a part of material **520**. As shown in FIG. **7**A, each of portions **541**F and **541**B of access line **241** can also span across (e.g., overlap in the X-direction) part of material **510** (e.g., a portion of the read channel region of transistor T**1**) and part of material **520** (e.g., a portion of write channel region of transistor T**2**) of other memory cells (e.g., memory cells **211**, **216**, and **217**) of memory device **200**. The spanning (e.g., overlapping) of access line **241** across material **510** and material **520** allows access line **241** (a single access line) to control (e.g., to turn on or turn off) both transistors T**1** and T**2** of memory cells **210**, **211**, **216**, and **217**.

[0097] As shown in FIG. **7**A, memory device **200** can include dielectric material (e.g., silicon dioxide) **526** that can form a structure (e.g., a dielectric) to electrically separate (e.g., isolate) parts of two adjacent (in the X-direction) memory cells of memory device **200**. For example, dielectric material **526** between memory cells **210** and **211** can electrically separate material **520** (e.g., write channel region of transistor T**2**) of memory cell **210** from material **520** (e.g., write channel region of transistor T**2**) of memory cell **211**,

and electrically separate charge storage structure **202** of memory cell **210** from charge storage structure **202** of memory cell **211**.

[0098] As shown in FIG. **7**A, memory device **200** can include dielectric portions **555**. Material (e.g., read channel region) **510** of two adjacent memory cells (e.g., memory cells **211** and **216**) can be electrically separated from each other by one of dielectric portions **555**. Some of portions (e.g., materials) of the memory cells of memory device **200** can be formed adjacent (e.g., formed on) a side wall (e.g., vertical portion with respect to the Z-direction) of a respective dielectric portion among dielectric portions **555**. For example, as shown in FIG. **7**A, material **510** (e.g., semiconductor material portion) of memory cell **210** can be formed adjacent (e.g., formed on) a side wall (not labeled) of dielectric portion **555** (on the left of memory cell **210**). In another example, material **510** (e.g., semiconductor material portion) of memory cell **211** can be formed adjacent (e.g., formed on) a side wall (not labeled) of dielectric portion **555** between memory cells **211** and **216**.

[0099] As shown in FIG. **7**B, memory device **200** can include dielectric materials **518**F and **518**B (e.g., gate oxide regions) to electrically separate portions **541**F and **541**B of access line **241** from other elements (e.g., from material **510**), charge storage structure **202**, and material **520** of memory cell **210**. The material (or materials) for dielectric materials **518**F and **518**B can be the same as (or alternatively, different from) the material (or materials) of dielectric materials **515**A and **515**B. Example materials for dielectric materials **518**F and **518**B can include silicon dioxide, hafnium oxide (e.g., HfO_2), aluminum oxide (e.g., Al_2O_3), or other dielectric materials.

[0100] As shown in FIG. **7**B, portions **541**F and **541**B can be adjacent respective sides of material **520** and charge storage structure **202** of memory cell **210**. For example, portion **541**F can be adjacent a side (e.g., right side (or front side) in the X-direction in the view of FIG. **7**B) of a portion of each of material **520** and charge storage structure **202**. In another example, portion **541**B can be adjacent another side (e.g., left side or back side (opposite from the right side) in the X-direction in the view of FIG. **7**B) of a portion of each of material **520** and charge storage structure **202**.

[0101] The above description focuses on the structure of memory cell **210**. Other memory cells (e.g., memory cells **211**, **216**, and **217** in FIG. **7**A) of memory device **200** can include elements structured in ways similar or the same as the elements of memory cell **210**, described above. For example, as shown in FIG. **7**A, memory cell **211** can include charge storage structure **202**, material (e.g., write channel region) **520**, material **510** (e.g., read channel region), and dielectric materials **525**A and **525**B. The material (or materials) for dielectric materials **525**A and **525**B can the same as the material (or materials) for dielectric materials **515**A and **515**B. Memory cells **216** and **217** can include elements structured in ways similar or the same as the elements of memory cells **210** and **211**, respectively.

[0102] As described above, FIG. **7**C shows a top view (e.g., plan view) of a portion of memory device **200** of FIG. **2** and FIG. **7**A. FIG. **7**C also shows relative locations of portions (e.g., wrapped portions) **221**P, **222**P, **223**P, and **224**P of data lines **221**, **222**, **223**, and **224**, respectively.

[0103] The following description describes data line **221**. Other data lines (e.g., data lines **222**, **223**, and **224**) of memory device **200** have similar structure and material as data line **221**. As shown in FIG. **5** through FIG. **7**C, data line **221** (associated with signal BL**1**) can have a length in the Y-direction, a width in the X-direction, and a thickness in the Z-direction. Data line **221** can include a conductive material (or a combination of materials) that can be structured as a conductive line (e.g., conductive region) having a length in the Y-direction. Example materials for data line **221** include metal, conductively doped polysilicon, or other conductive materials. Other data lines **222**, **223**, and **224** (associated with signals BL**2**, BL**3**, and BL**4**, respectively) can have a length, a width, a thickness, and a material similar to or the same as data line **221**.

[0104] As shown in FIG. **5** through FIG. **7**C, data line **221** can have portions **221**P adjacent respective materials **510** (e.g., read channel regions) of respective memory cells **212** and **214** (FIG. **7**C). Portions **221**P of data line **221** can have the same material (e.g., conductive material) as the rest (e.g., as top portion) of data line **221**. Portion **221**P can be part (e.g., side part) of data line **221** that joins a top part of data line **221** and forms 90 degrees with the top part (e.g., portion **221**P can be part of data line **221** that is perpendicular to the top part of data line **221**).

[0105] As shown in FIG. **7**A, portion **221**P of data line **221** can partially wrap around a side (e.g., left side in FIG. **7**A) of part (e.g., top part) of material **510** (e.g., a read channel region) of memory cell **210**. Thus, portion **221**P can be called a wrapped portion of data line **221**. The wrapped portion (e.g., portion **221**P) can also be called an overhang portion, which overhangs the side (e.g., left side in FIG. **7**A) of part (e.g., top part) of material **510** (e.g., a read channel region) and extends toward substrate **599**.

[0106] As shown in FIG. **7**C, data line **221** can include a continuous top portion contacting material **510** (e.g., read channel region) and material **520** (e.g., write channel region) of respective memory cells **210**, **212**, and **214**. Portions **221**P are discontinuous (e.g., patterned) portions of data line **221**, such that a gap void of the material of data line **221** is between vertical sides (sides parallel to the Z-direction) of two adjacent portions **221**P. In an alternative structure (FIG. **8**A, FIG. **8**B, and FIG. **8**C) of memory device **200**, there is no gap between vertical sides of adjacent portions **221**P (e.g., no void in the material of data line **221** between vertical sides of adjacent portions **221**P).

[0107] As shown in FIG. **7**A, material **510** includes opposite sides in the X-direction, such as a side (e.g., left side) adjacent portion **221**P and another side (e.g., right side) adjacent material **520**. Data line **221** can contact material **510** and material **520** at an interface **221***i*. Portion **221**P can have a length L**1** in the Z-direction and can extend (toward substrate **599**) to a level below the level of interface **221***i*.

[0108] Portion **221**P (FIG. **7**A and FIG. **7**C) can be located (e.g., can be formed) in a trench (not labeled) adjacent material **510**. The trench is separated from material **510** by dielectric material **565**. Portion **221**P is separated from material **510** by dielectric material **565**, such that dielectric material **565** is between and contacts portion **221**P and material **510**.

[0109] As shown in FIG. **7**A and FIG. **7**C, other data lines **221**, **223**, and **224** can have similar wrapped portions (e.g., portions **222**P, **223**P, and **224**P) adjacent respective materials **510** of other memory cells. For simplicity, details of portions **222**P, **223**P, and **224**P are not described here.

[0110] The structure of memory device **200** allows it to have a relatively smaller size (e.g., smaller footprint) and

improved (e.g., reduced) power consumption (as result of using a single access line (e.g., word line) to control two transistors of a corresponding memory cell). Further, the structure of data lines (e.g., data lines **221**, **222**, **223**, and **224**) of memory device **200** also allows memory device **200** to have an improved operation (e.g., improved write operation) that can further provide power reduction in which static power (in write operation) can be mitigated or prevented, as discussed below with reference to FIG. **4** and FIG. **7**C.

[0111] As shown in FIG. **7**A, portion **221**P can have a length L**1** (in the Z-direction), which can be less than the length (not labeled) of material **510** (e.g., read channel region) and less than the length (not labeled) of material **520** (e.g., write channel region) of memory cell **210**. The length of material **510** can be measured in the Z-direction from interface **221***i* to a surface (not labeled) of semiconductor material **596**. As shown in FIG. **7**A, the Z-direction is also a direction from material **520** (e.g., write channel region) to charge storage structure **202**. The length of material **520** can be measured in the Z-direction from interface **221***i* to edge **202'** of charge storage structure **202**.

[0112] The length (e.g., length L**1**) of portion **221**P can be selected such that power consumption in operations (e.g., write operations) of memory device **200** can be improved (e.g., reduced) without incurring too much coupling capacitance between data line **221** and other elements. For example, as shown in FIG. **7**A, portion **221**P can be formed such that length L**1** can be less than the length (in the Z-direction) of material **510** and less than the length (in the Z-direction) of material **520**. The relationship between the length (e.g., length L**1**) of portion **221**P and the length of each of material **510** and material **520** as described here and as shown in FIG. **7**A can provide improvement in memory device **200**, as discussed in detail below.

[0113] In an alternative structure of memory device **200**, each data line can have an alternative wrapped portion (e.g., a mirror of portion **221**P in the X-direction) formed adjacent a write channel region (e.g., adjacent material **520** in FIG. **7**A) of a respective memory cell instead of adjacent the read channel region (e.g., material **510**). In another alternative structure of memory device **200**, each data line can have two wrapped portions, such that each data line can have an additional wrapped portion (e.g., besides the wrapped portion shown in FIG. **7**A) formed adjacent a write channel region (e.g., adjacent material **520** in FIG. **7**A). However, both alternative structures mentioned here may provide less improvement and benefit in comparison with the structure shown in FIG. **7**A for some conditions during some operations of memory device **200**, as discussed below.

[0114] As shown in FIG. **4** and FIG. **7**C, memory cells **210**, **212**, and **214** are associated with different access lines **241**, **242**, and **243** and share data line **221**. In a write operation as described above with reference to FIG. **4**, voltage V**4** (e.g., V**4**>0V) can be applied to access line **241** (selected access line) to turn on transistor T**2** of memory cell **210** (selected memory cell) to access memory cell **210**. In this write operation, voltage V**5** (e.g., V**5**=0V or V**5**<0V) can be applied to access lines **242** and **243** to turn off transistor T**1** and T**2** of memory cells **212** and **214** (unselected memory cells). However, static power (e.g., leakage current) may occur in the unselected memory cells. For example, in FIG. **4**, if voltage V**6** applied to data line **221** (as part of storing information (e.g., "1") in selected memory cell **210**) is greater than voltage V**5** (e.g., V**6**>V**5**) applied to access lines **242** and **243**, then static power (e.g., leakage current) may occur in the read channel region (e.g., in material **510** in FIG. **7**A) of transistor T**1** of the unselected memory cell (memory cell **212** or **214**). Portion **221**P (FIG. **5**, FIG. **7**A, and FIG. **7**C) is formed to mitigate or prevent such a static power. For example, as shown in FIG. **7**C, since portion **221**P is adjacent a side (in the X-direction) of material **510** (e.g., read channel region) of memory cell **212**, portion **221**P can impede a static power from occurring in the unselected memory cell (e.g., occurring in material **510** of the unselected memory cell) or to mitigate such a static power. This can improve the write operation of memory device **200** and reduce power consumption associated with the write operation.

[0115] As described above, portion **221**P of data line **221** in FIG. **7**A can be alternatively formed adjacent material **520** (instead of adjacent material **510**). However, at some value of voltage V**6** (e.g., V**6**=0V) applied on data line **221** as part of storing information (e.g., "0") in the selected memory cell **210** during a write operation, portion **221**P (if formed adjacent material **520** (e.g., write channel region) of memory cell **210**) of data line **221** can impede current provided (through material **520**) to the selected memory cell **210**. This can reduce the efficiency to the write operation compared with the write operation described above with reference to FIG. **4**. Thus, a wrapped portion (e.g., portion **221**P) of a data line can be formed adjacent material **510** (e.g., read channel region), adjacent material **520** (e.g., write channel region), or two wrapped portions can be formed adjacent material **510** and material **520**, respectively, of a respective memory cell. However, forming portion **221**P as shown in FIG. **7**A can be more beneficial than forming portion **221**P in the alternative structures, as discussed above. Therefore, in some structures of memory device **200**, data line **271** does not have a portion (e.g., a wrapped portion) horizontally adjacent material (e.g., write channel region) **520**. For example, in some structures of memory device, data line **271** does not have a portion adjacent material **520** that is opposite from portion **221**P in the X-direction (e.g., horizontal direction).

[0116] FIG. **8**A, FIG. **8**B, and FIG. **8**C show different views of a structure of memory device **800**, according to some embodiments described herein. Memory device **800** includes elements similar to or the same as those of memory device **200** described above. Differences between memory devices **200** and **800** include the continuous structure of the wrapped portions of each of data lines **221**, **222**, **223**, and **224** of memory device **800**.

[0117] As shown in FIG. **8**A, FIG. **8**B, and FIG. **8**C, data line **221** includes portion **221**P'. Like portion **221**P (FIG. **7**A and FIG. **7**C), portion **221**P' (FIG. **8**A and FIG. **8**B) can extend (toward substrate **599**) in the Z-direction below a level (e.g., at interface **221***i* in FIG. **7**A) where the top portion of data line **221** contacts material **510** and material **520** of respective memory cells **210**, **212**, and **214**. However, unlike portion **221**P (FIG. **7**A and FIG. **7**C), portion **221**P' (FIG. **8**A, FIG. **8**B, and FIG. **8**C) can extend continuously in the Y-direction along the length of data line **221**. In FIG. **7**A and FIG. **7**C, a gap void of the material of data line **221** is between vertical sides (sides parallel to the Z-direction) of two adjacent portions **221**P. However, in FIG. **8**A, FIG. **8**B, and FIG. **8**C, portion **221**P' is a continuous portion along the entire length of data line **221**.

[0118] As shown in FIG. **8**C, data line **221** can include a top part extending the entire length of data line **221** and another part (e.g., a side part, which includes portion **211**P') perpendicular to the top part (e.g., joining the top part and forming 90 degrees with the top part) also extending the entire length of data line **221**. Thus, as shown in FIG. **8**C, a top part of data line **221** can extend from one memory cell to the next (e.g., from memory cell **210** to memory cell **212** and to memory cell **214**), and another part (e.g., which includes portion **211**P') perpendicular to the top part and also extending from one memory cell to the next (e.g., from memory cell **210** to memory cell **212** and to memory cell **214**).

[0119] As described above, portion **221**P (FIG. **7**C) of data line **221** is adjacent a respective read channel (e.g., adjacent only one material **510**) of a respective memory cell (e.g., memory cell **210**). In FIG. **8**C, since portion **221**P' can extend continuously in the Y-direction along the length of data line **221**, portion **221**P' can be adjacent multiple read channel regions (e.g., adjacent multiple materials **510**) of respective memory cells (e.g., memory cells **210**, **212**, and **214**) coupled to data line **221**. Similarly, each of data lines **222**, **223**, and **224** (FIG. **8**C) can have a wrapped portion (e.g., portion **222**P', **223**P', or **224**P') that extends continuously in the Y-direction along the length of a respective data line and adjacent multiple respective read channel regions (e.g., adjacent multiple portions of material **510**). Memory device **800** can have improvements and benefits similar to those of memory device **700** described above, for example, relatively smaller footprint, reduced power consumption, and improved operation (e.g., static power mitigation or prevention during write operation).

[0120] FIG. **9** through FIG. **22**D show different views of elements during processes of forming a memory device **900**, according to some embodiments described herein. Some or all of the processes used to form memory device **900** can be used to form memory devices **200** and **800** described above with reference to FIG. **2** through FIG. **8**.

[0121] FIG. **9** shows memory device **900** after different levels (e.g., layers) of materials are formed in respective levels (e.g., layers) of memory device **900** in the Z-direction over a substrate **999**. The different levels of materials include a dielectric material **930**, a semiconductor material **996**, and a conductive material **997**. Dielectric material **930**, semiconductor material **996**, and conductive material **997** can be formed in a sequential fashion one material after another over substrate **999**. For example, the processes used in FIG. **9** can include forming (e.g., depositing) conductive material **997** over substrate **999**, forming (e.g., depositing) semiconductor material **996** over conductive material **997**, and forming (e.g., depositing) dielectric material **930** over semiconductor material **996**.

[0122] Substrate **999** can be similar to or the same as substrate **599** of FIG. **5**. Conductive material **997** can include a material (or materials) similar to or the same as that of the material for ground connection **297** of memory devices **200** and **800** (FIG. **5** through FIG. **7**C). For example, conductive material **997** can include metal, conductively doped polysilicon, or other conductive materials.

[0123] Semiconductor material **996** includes a material (or materials) similar to or the same as that of the material for semiconductor material **596** of memory devices **200** and **800** (FIG. **5** through FIG. **7**C). For example, semiconductor material **996** can include silicon, polysilicon, or other semiconductor material, and can include a doped region (e.g., p-type doped region). As described below in subsequent processes of forming memory device **900**, semiconductor material **996** can be structured to form part of a channel region (e.g., read channel region) for a respective memory cell of memory device **900**.

[0124] Dielectric materials **930** of FIG. **9** can include a nitride material (e.g., silicon nitride (e.g., Si_3N_4)), oxide material (e.g., SiO_2), or other dielectric materials. As described below in subsequent processes of forming memory device **900**, dielectric material **930** can be processed into dielectric portions to form part of cell isolation structures to electrically isolate one memory cell from another memory cell of memory device **900**.

[0125] FIG. **10**A shows memory device **900** after trenches (e.g., openings) **1001** and **1002** are formed. Forming trenches **1001** and **1002** can include removing (e.g., by patterning) part of dielectric material **930** (FIG. **9**) at the locations of trenches **1001** and **1002** and leaving portions (e.g., dielectric portions) **1031**, **1032**, and **1033** (which are remaining portions of dielectric material **930**) as shown in FIG. **10**A. Each of trenches **1001** and **1002** can have a length in the Y-direction, a width (shorter than the length) in the X-direction, and a bottom (not labeled) resting on (e.g., bounded by) a respective portion of semiconductor material **996**. Each of trenches **1001** and **1002** can include opposing side walls (e.g., vertical side walls) formed by respective portions **1031**, **1032**, and **1033**. For example, trench **1001** can include a side wall **1011** (formed by portion **1031**) and a side wall **1012** (formed by portion **1032**). Trench **1002** can include a side wall **1013** (formed by portion **1032**) and a side wall **1014** (formed by portion **1033**).

[0126] FIG. **10**B shows memory device **900** after dielectric materials **1065** are formed (e.g., deposited) on respective side wall **1011**, **1012**, **1013**, and **1014** (labeled in FIG. **10**A) of trenches **1001** and **1002**, respectively. Dielectric materials **1022** include silicon dioxide, silicon nitride, or other dielectric materials. In subsequent process (FIG. **18**B) of forming memory device **900**, a portion (e.g., top portion) of dielectric materials **1022** can be removed to form trenches (e.g., trenches **1822** in FIG. **18**B) in respective dielectric materials **1022**. A conductive material (e.g., metal) can be formed (e.g., filled) in the shallow trenches (formed in dielectric materials **1022**) to create wrapped portions (e.g., portions **221**P, **222**P, **223**P, and **225**P in FIG. **7**A) of respective data lines of memory device **900**.

[0127] FIG. **11** shows memory device **900** after a material **1110'** and a material **1110"** are formed (e.g., deposited) in trenches **1001** and **1002**, respectively. As shown in FIG. **11**, material **1110'** can be formed on respective side walls (not labeled) of dielectric material **1065** and the bottom (e.g., on a portion of semiconductor material **996**) of trench **1001**. Material **1110"** can be formed on respective side walls (not labeled) of dielectric material **1065** and the bottom (e.g., on another portion of semiconductor material **996**) of trench of trench **1002**.

[0128] Materials **1110'** and **1110"** can be the same material. An example of material **1110'** a material **1110"** includes a semiconductor material. Materials **1110'** and **1110"** can have the same properties as the materials that form portions **510** (e.g., read channel regions) of transistors T**1** of respective memory cells of memory device **200** of FIG. **5** through FIG. **7**C. As described below in subsequent processes (e.g., FIG. **19**A) of forming memory device **900**, materials **1110'** and

1110" can be structured to form channel regions (e.g., read channel regions) of transistors (e.g., transistors T**1**) of respective memory cells of memory device **900**. Thus, each of materials **1110'** and **1110"** can conduct a current (e.g., conduct holes) during an operation (e.g., a read operation) of memory device **900**.

[0129] The process of forming materials **1110'** and **1110"** can include a doping process. Such a doping process can include introducing dopants into materials **1110'** and **1110"** to allow a transistor (e.g., transistor T**1**) of a respective memory cell of memory device **900** to include a specific structure. For example, the doping process used in FIG. **9** can include introducing dopants (e.g., using a laser anneal process) with different dopant concentrations for different parts of materials **1110'** and **1110"**, such that the transistor that includes material **1110'** (or material **1110"**) can have a PFET structure. In such a PFET structure, part of material **1110'** (or material **1110"**) can form a channel region (e.g., read channel region of P-type conductivity) to conduct currents (e.g., holes) during an operation (e.g., read operation) of memory device **900**.

[0130] FIG. **12** shows memory device **900** after dielectric materials (e.g., oxide materials) **1215'** and **1215"** are formed (e.g., deposited) on materials **1110'** and **1110"**, respectively. Dielectric materials **1215'** and **1215"** can be deposited, such that dielectric materials **1215'** and **1215"** can be conformal to materials **1110'** and **1110"**, respectively. Dielectric materials **1215'** and **1215"** can have the same properties as the materials that form dielectric materials (gate oxide regions) **515**A, **515**B, **525**A, and **525**B of memory device **200** of FIG. **5** through FIG. **7**C.

[0131] FIG. **13** shows memory device **900** after materials (e.g., charge storage materials) **1302'**, **1302"**, **1302'"**, and **1302""** are formed on respective side walls of dielectric materials **1215'** and **1215"**. Materials **1302'**, **1302"**, **1302'"**, and **1302""** are electrically separated from each other. As described below in subsequent processes (FIG. **19**A) of forming memory device **900**, each of materials **1302'**, **1302"**, **1302'"**, and **1302""** can be structured to form a charge storage structure of a respective memory cell of memory device **900**. Materials **1302'**, **1302"**, **1302'"**, and **1302""** can include material (e.g., polysilicon) similar or the same as the material of charge storage structure **202** of the memory cells (e.g., memory cell **210** or **211**) of memory device **200** (FIG. **5** through FIG. **7**C).

[0132] FIG. **14** shows memory device **900** after dielectric materials **1426'** and **1426"** are formed (e.g., filled) in opened spaces in trenches **1001** and **1002**, respectively. Dielectric materials **1426'** and **1426"** can include an oxide material. As described below in subsequent processes of forming memory device **900**, dielectric materials **1426'** and **1426"** can form part of an isolation structure that can electrically isolate parts of (e.g., charge storage structures) two adjacent (in the X-direction) memory cells of memory device **900**.

[0133] FIG. **15** shows memory device **900** after dielectric materials **1526'** and **1526"** are formed at locations **1501** and **1502**, respectively. Forming dielectric materials **1526'** and **1526"** can include removing (e.g., by using an etch process) part (e.g., top part) of each of dielectric materials **1426'** and **1426"** (FIG. **14**), such that the remaining parts of dielectric materials **1426'** and **1426"** are dielectric materials **1526'** and **1526"** (FIG. **15**), respectively.

[0134] FIG. **16** shows memory device **900** after materials **1602'**, **1602"**, **1602'"**, and **1602""** are formed at locations **1611** and **1612**, respectively. Forming materials **1602'**, **1602"**, **1602'"**, and **1602""** can include removing (e.g., by using an etch process) part (e.g., top part) of each of materials (e.g., charge storage materials) **1302'**, **1302"**, **1302"**, and **1302""** (FIG. **13**), such that the remaining parts of materials **1302'**, **1302"**, **1302"**, and **1302'"** are materials **1602'**, **1602"**, **1602'"**, and **1602""** (FIG. **16**), respectively.

[0135] In FIG. **15** and FIG. **16**, top part of dielectric materials **1426'** and **1426"** (labeled in FIG. **14**) and top part of materials **1302'**, **1302"**, **1302"**, **1302""** (labeled in FIG. **13**) were removed in separate processes (e.g., multiple steps one after another) as described with reference to FIG. **15** and FIG. **16**. However, from FIG. **14**, a single process (e.g., single step) can be used to remove part of dielectric materials **1426'** and **1426"** and part of materials **1302'**, **1302"**, **1302""**, **1302""** (FIG. **13**).

[0136] FIG. **17** shows memory device **900** after materials **1720'**, **1721'**, **1720"**, and **1721"** are formed. Forming materials **1720'**, **1721'**, **1720"**, and **1721"** can include depositing an initial material (or materials) on dielectric materials **1526'** and **1526"** and materials **1602'**, **1602"**, **1602"**, and **1602""**. Then, the process used in FIG. **17** can include removing (e.g., by using an etch process) a portion of the initial material at locations **1701** and **1702**. Materials **1720'**, **1721'**, **1720"**, and **1721"** are the remaining portions of the initial material. As shown in FIG. **17**, materials **1720'**, **1721'**, **1720"**, and **1721"** are electrically separated from each other. However, materials **1720'**, **1721'**, **1720"**, and **1721"** are electrically coupled to (e.g., directly coupled to) materials **1602'**, **1602"**, **1602"**, and **1602"""**, respectively.

[0137] Materials **1720'**, **1721'**, **1720"**, and **1721"** can include materials similar or the same as material (e.g., write channel region) **520** (FIG. **5**) of transistor T**2** of memory device **200** of FIG. **5**A and FIG. **6**A. As described below in subsequent processes (FIG. **19**A) of forming memory device **900**, each of materials **1720'**, **1721'**, **1720"**, and **1721"** can form a channel region (e.g., write channel region) of a transistor (e.g., transistor T**2**) of a respective memory cell of memory device **900**. Thus, each of materials **1720'**, **1721'**, **1720"**, and **1721"** can conduct a current (e.g., conduct electrons) during an operation (e.g., a write operation) of memory device **900**.

[0138] FIG. **18**A shows memory device **900** after dielectric materials **1826'** and **1826"** are formed at (e.g., filled in) locations **1701** and **1702**. Dielectric materials **1826'** and **1826"** can be the same as dielectric materials **1426'** and **1426"**. As described below in subsequent processes of forming memory device **900**, dielectric materials **1826'** and **1826"** can form part of an isolation structure that can electrically isolate parts of (e.g., write channel regions) two adjacent (in the X-direction) memory cells of memory device **900**. In subsequent processes, shallow trenches will be formed in dielectric materials **1065** (which were formed in FIG. **10**A).

[0139] FIG. **18**B shows memory device **900** after trenches (e.g., shallow trenches) **1822** are formed in dielectric materials **1065**. Each trench **1822** can include a depth D**1**. As described above and shown in FIG. **7**A, length L**1** of portion **221**P can be less than the length of material **510** (e.g., read channel region) and less than the length of material **520** (e.g., write channel region) of memory cell **210**. Length L**1** (FIG. **7**A) of portion **221**P is based on depth D**1** (FIG. **18**B). For example, length L**1** is the same as depth D**1**. Thus, in FIG. **18**B, depth D**1** can be less than the length of material

510 (FIG. **7**A) of memory cell **210** and less than the length of material **520** (FIG. **7**A) of memory cell **210**. In subsequent processes (FIG. **22**C), a conductive material (e.g., metal) can be formed (e.g., filled) in trenches **1822** to create wrapped portions (e.g., portions **221**P, **222**P, **223**P, and **225**P in FIG. **7**A) of respective data lines of memory device **900**.

[0140] FIG. **19**A shows memory device **900** after trenches **1911**, **1912**, and **1913** are formed (in the X-direction) across the materials of memory device **900**. Each of trenches **1911**, **1912**, and **1913** can have a length in the X-direction, a width (shorter than the length) in the Y-direction, and a bottom (not labeled) resting on (e.g., bounded by) a respective portion of semiconductor material **996**. In the structure of FIG. **19**A, memory device **900** can include a common conductive structure (e.g., a common conductive plate) formed on a level of memory device **900** that is under the memory cells of memory device **900**. In an alternative structure (not shown in FIG. **19**A) of memory device **900**, each of trenches **1911**, **1912**, and **1913** can have a bottom (not labeled) resting on (e.g., bounded by) a respective portion of conductive material **997** (instead of semiconductor material **996**).

[0141] In the FIG. **19**A, forming trenches **1911**, **1912**, and **1913** can include removing (e.g., by cutting (e.g., etching) in the Z-direction) part of the materials of memory device **900** at locations of trenches **1911**, **1912**, and **1913** and leaving portions (e.g., slices) of the structure of memory device **900** shown in FIG. **19**A. After portions (at the locations of trenches **1911**, **1912**, and **1913**) of memory device **900** are removed (e.g., cut), the remaining portions can form parts of memory cells of memory device **900**. For example, memory device **900**, as shown in FIG. **19**A, can include memory cells **210'**, **211'**, **210"**, and **211"** in one row along the X-direction, and memory cells **212'**, **213'**, **212"**, and **213"** in another row along the X-direction. Memory cells **210'**, **211'**, **210"**, and **211"** can correspond to memory cells **210**, **211**, **216**, and **217**, respectively, of memory device **200** of FIG. **7**A.

[0142] For simplicity, only some of similar elements (e.g., portions) of memory device **900** in FIG. **19**A are labeled. For example, memory device **900** can include dielectric portions (e.g., cell isolation structures) **1931**, **1932**, **1933**, **1934**, **1935**, and **1936**, and dielectric materials **1926**A and **1926**B. Dielectric portions **1931** and **1932** can correspond to two respective dielectric portions **555** of memory device **200** of FIG. **7**A.

[0143] FIG. **19**B shows an enlarged portion of memory device **900** of FIG. **19**A. As shown in FIG. **19**B, memory cell **210'** can include portions **1910**A and **1910**B (which can be part of the read channel region of memory cell **210'**), dielectric materials **1915**A and **1915**B, material (e.g., write channel region) **1920**, and charge storage structure **1902** (directly below material **1920**). Memory cell **211'** can include portions **1911**A and **1911**B (which can be part of the read channel region of memory cell **211'**), dielectric materials **1925**A and **1925**B, material (e.g., write channel region) **1921**, and charge storage structure **1902** (directly below material **1921**).

[0144] As described above with reference to FIG. **9** through FIG. **19**B, part of each of the memory cells of memory device **900** can be formed from a self-aligned process, which can include formation of trenches **1001** and **1002** (FIG. **10**A) in the Y-direction and trenches **1911**, **1912**, and **1913** (FIG. **19**A) in the X-direction. The self-aligned process can improve (e.g., increase) memory cell density, improve process (e.g., provide a higher process margin), or both. The self-aligned process, as described above, includes a reduced number of critical masks that can allow forming of multiple decks of memory cells in the same memory device. An example of a multi-deck memory device is described below with reference to FIG. **28**A through FIG. **28**C.

[0145] FIG. **20** shows memory device **900** after dielectric materials **2018**F, **2018**B, **2018**F', and **2018**B' (e.g., gate oxide regions) are formed. The material (or materials) for dielectric materials **2018**F, **2018**B, **2018**F', and **2018**B' can be the same as (or alternatively, different from) the material (or materials) of dielectric materials **515**A, **515**B, **525**A, and **525**B (FIG. **7**A). Example materials for dielectric materials **2018**F, **2018**B, **2018**F', and **2018**B' can include silicon dioxide, hafnium oxide (e.g., HfO_2), aluminum oxide (e.g., Al_2O_3), or other dielectric materials (e.g., other high-k dielectric materials).

[0146] FIG. **21** shows memory device **900** after conductive lines (e.g., conductive regions) **2141**F, **2141**B, **2142**F, and **2142**B are formed. Each of conductive lines **2141**F, **2141**B, **2142**F, and **2142**B can include metal, conductively doped polysilicon, or other conductive materials. As shown in FIG. **21**, conductive lines **2141**F, **2141**B, **2142**F, and **2142**B are electrically separated from other elements of memory device **900** by dielectric materials **2018**F, **2018**B, **2018**F', and **2018**B', respectively.

[0147] Conductive lines **2141**F and **2141**B can form part of an access line (e.g., word line) **2141** to control the read and write transistors (e.g., transistor T**1** and T**2**, respectively) of respective memory cells **210'**, **211'**, **210"**, and **211"** (labeled in FIG. **19**A) of memory device **900**. For example, conductive lines **2141**F and **2141**B can form front and back conductive portions, respectively, of access line **2141**. Conductive lines **2142**F and **2142**B can form part of an access line (e.g., word line) **2142** to access memory cells **212'**, **213'**, **212"**, and **213"** (labeled in FIG. **19**A) of memory device **900**. For example, conductive lines **2142**F and **2142**B can form front and back conductive portions, respectively, of access line **2142**. Access lines **2141** and **2412** can correspond to access lines **241** and **242**, respectively, of memory device **200** of FIG. **2**.

[0148] The processes of forming memory device **900** in FIG. **21** can include forming a conductive connection **2141'** (which can include a conductive material (e.g., metal)) to electrically couple conductive lines **2141**F and **2141**B to each other. This allows conductive lines **2141**F and **2141**B to form part of a single access line (e.g., access line **2141**). Similarly, the processes of forming memory device **900** can include forming a conductive connection **2142'** to electrically couple conductive lines **2142**F and **2142**B to each other. This allows conductive lines **2142**F and **2142**B to form part of a single access line (e.g., access line **2142**).

[0149] FIG. **22**A shows memory device **900** after a dielectric material **2235** is formed. Dielectric material **2235** can fill the structure of memory device **900** as shown in FIG. **22**A. As shown in FIG. **22**A, trenches **1822** (formed in FIG. **18**A) are not filled with dielectric material **2235**. Portion **1910**A and material **1920** (e.g., read channel region and write channel region, respectively) of memory cell **210'** are exposed. Portion **1911**A and material **1921** (e.g., read channel region and write channel region, respectively) of memory cell **211'** are exposed. Read and write channel regions (not labeled) of other memory cells are also exposed.

[0150] FIG. **22**B shows memory device **900** after a conductive material **2220** is formed. Conductive material **2220** can be formed (e.g., deposited) in trenches **1822** (FIG. **22**A) and over exposed portion **1910**A, material **1920**, portion **1911**A, and material **1921** (labeled in FIG. **22**A) and other elements of memory device **900**.

[0151] FIG. **22**C shows memory device **900** after data lines **2221**, **2222**, **2223**, and **2224** and respective portions (e.g., wrapped portions) **2221**P, **2222**P, **2223**P, and **2224**P are formed. FIG. **22**D shows a side view of memory device **900** taken along line **22**D of FIG. **22**C. Data lines **2221**, **2222**, **2223**, and **2224** and respective portions **2221**P, **2222**P, **2223**P, and **2224**P can be concurrently formed. For example, a process (e.g., patterning process) can be performed to remove a portion of conductive material **2200** (FIG. **22**B). In FIG. **22**C, data lines **2221**, **2222**, **2223**, and **2224** and respective portions **2221**P, **2222**P, **2223**P, and **2224**P are the remaining portion of conductive material **2200**.

[0152] As shown in FIG. **22**C, data lines **2221**, **2222**, **2223**, and **2224** are electrically separated from each other. Each of data lines **2221**, **2222**, **2223**, and **2224** can have a length in the Y-direction, a width in the X-direction, and a thickness in the Z-direction. Data lines data lines **2221**, **2222**, **2223**, and **2224** can correspond to data lines data lines **221**, **222**, **223**, and **224**, respectively, of memory device **200** of FIG. **7**A. Portions **2221**P, **2222**P, **2223**P, and **2224**P can correspond to portions (e.g., wrapped portions) **221**P, **222**P, **223**P, and **224**P, respectively, of memory device **200** of FIG. **7**A.

[0153] As shown in FIG. **22**D, portions **2221**P, **2222**P, **2223**P, and **2224**P of respective data lines **2221**, **2222**, **2223**, and **2224** can be adjacent respective read channel regions (e.g., portions **1910**A and **1911**A) of respective memory cells. Portions **2221**P, **2222**P, **2223**P, and **2224**P of also separated from respective read channel regions by respective dielectric materials **1065**. Dielectric materials **1065** shown in FIG. **22**D are the remaining portions of dielectric materials **1065** formed in FIG. **10**A and etched in FIG. **18**A.

[0154] The description of forming memory device **900** with reference to FIG. **9** through FIG. **22**D can include other processes to form a complete memory device. Such processes are omitted from the above description so as to not obscure the subject matter described herein.

[0155] The process of forming memory device **900** as described above can have a relatively reduced number of masks (e.g., reduced number of critical masks) in comparison with some conventional processes. For example, by forming trenches **1001** and **1002** in the process associated with FIG. **10**A, and forming trenches **1911**, **1912**, and **1913** in the process of FIG. **19**A, the number of critical masks used to form the memory cells of memory device **900** can be reduced. The reduced number of masks can simplify the process, reduce cost, or both, of forming memory device **900**. Further, forming data lines **2221**, **2222**, **2223**, and **2224** that have respective portions **2221**P, **2222**P, **2223**P, and **2224**P allows memory device **900** to have improvements and benefits (e.g., reduce leakage current and other improvements) similar to those of memory device **200** (FIG. **2** through FIG. **7**C).

[0156] FIG. **23** through FIG. **28**C show processes of forming a memory device **2300** including data lines having continuous wrapped portions, according to some embodiments described herein. The processes of forming memory device **2300** can be a variation of the processes of forming memory device **900** (FIG. **9** through FIG. **22**D). Thus, similar elements (which have the same labels) between the processes of forming memory devices **900** and **2300** are not repeated.

[0157] FIG. **23** shows the elements of memory device **2300** that can be formed using similar or identical processes used to form the elements of memory device **900** of FIG. **9** through FIG. **18**A. However, unlike memory device **900** of FIG. **19**A, dielectric materials **1065** (formed in FIG. **10**A) can be omitted (not formed) in the processes of forming memory device **2300**. Thus, in memory device **2300**, material **1110'** and material **1110"** can be formed (e.g., deposited) on side walls of trenches **1001** and **1002** (FIG. **10**A) and on semiconductor material **996** in trenches **1001** and **1002** (FIG. **10**A).

[0158] FIG. **24** shows memory device **2300** after dielectric materials (e.g., gate oxide regions) **2018**F, **2018**B, **2018**F', and **2018**B', conductive lines (e.g., conductive regions) **2141**F, **2141**B, **2142**F, and **2142**B, and conductive connections **2141'** and **2142'** are formed.

[0159] FIG. **25** shows memory device **2300** after dielectric material **2235** is formed. Dielectric material **2235** can fill the structure of memory device **230** as shown in FIG. **25**.

[0160] FIG. **26** shows memory device **2300** after trenches **2622** are formed. Forming trenches **2622** can include removing (e.g., etching) materials at the locations of trenches **2622**. Each trench **2622** can have depth (e.g., D**1**) similar to or the same as the depth (e.g., D**1**) of trench **1822** (FIG. **18**A).

[0161] FIG. **27**A shows memory device **2300** after a conductive material **2200'** is formed. Conductive material **2200'** can be formed (e.g., deposited) in trenches **2622** (FIG. **22**A) and over other exposed portions **1910**A, material **1920**, **1911**A, and material **1921** (shown in FIG. **26**).

[0162] FIG. **27**B shows memory device **2300** after data lines **2221**, **2222**, **2223**, and **2224** and respective portions (e.g., wrapped portions) **2221**P', **2222**P', **2223**P', and **2224**P' are formed. Data lines **2221**, **2222**, **2223**, and **2224** and respective portions **2221**P', **2222**P', **2223**P', and **2224**P' can be concurrently formed. For example, an initial conductive material can be formed (e.g., deposited) in trenches **2622** (FIG. **26**) and over other exposed portion **1910**A, material **1920**, portion **1911**A, and material **1921** (shown in FIG. **26**). Then, a process (e.g., patterning process) can be performed to remove a portion of the initial conductive material. In FIG. **27**B, data lines **2221**, **2222**, **2223**, and **2224** and respective portions **2221**P', **2222**P', **2223**P', and **2224**P' are the remaining portion of the initial conductive material.

[0163] As shown in FIG. **27**B, data lines **2221**, **2222**, **2223**, and **2224** are electrically separated from each other. Each of data lines **2221**, **2222**, **2223**, and **2224** can have a length in the Y-direction, a width in the X-direction, and a thickness in the Z-direction. Data lines **2221**, **2222**, **2223**, and **2224** and respective portions **2221**P', **2222**P', **2223**P', and **2224**P' can be concurrently formed. For example, a process (e.g., patterning process) can be performed to remove a portion of conductive material **2200'** (FIG. **27**A). In FIG. **27**B, data lines **2221**, **2222**, **2223**, and **2224** and respective portions **2221**P', **2222**P', **2223**P', and **2224**P' are the remaining portion of conductive material **2200'**.

[0164] As shown in FIG. **27**B, each of portions **2221**P', **2222**P', **2223**P', and **2224**P' can be a continuous structure (e.g., a continuous piece) of conductive material along the length of a respective data line. Each of portions **2221**P',

2222P', **2223**P', and **2224**P' can be adjacent multiple read channel regions of respective memory cells. Each of portions **2221**P', **2222**P', **2223**P', and **2224**P' can be separated from respective read channel regions by a respective dielectric material between trench **2622** (FIG. **26**) and respective read channel regions. The description of forming memory device **2300** with reference to FIG. **23** through FIG. **27**B can include other processes to form a complete memory device. Such processes are omitted from the above description so as to not obscure the subject matter described herein. Memory device **2300** can include improvements and benefits similar to those of memory devices **200**, **800**, and **900**.

[0165] FIG. **28**A, FIG. **28**B, and FIG. **28**C show different views of a structure of a memory device **2800** including multiple decks of memory cells, according to some embodiments described herein. FIG. **28**A shows an exploded view (e.g., in the Z-direction) of memory device **2800**. FIG. **28**B shows a side view (e.g., cross-sectional view) in the X-direction and the Z-direction of memory device **2800**. FIG. **28**C shows a side view (e.g., cross-sectional view) in the Y-direction and the Z-direction of memory device **2800**.

[0166] As shown in FIG. **28**A, FIG. **28**B, and FIG. **28**C, memory device **2800** can include decks (decks of memory cells) $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ that are shown separately from each other in an exploded view to help ease of viewing the deck structure of memory device **2800**. In reality, decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ can be attached to each other in an arrangement where one deck can be formed (e.g., stacked) over another deck over a substrate (e.g., a semiconductor (e.g., silicon) substrate) **2899**. For example, as shown in FIG. **28**A, decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ can be formed in the Z-direction perpendicular to substrate **2899** (e.g., formed vertically in the Z-direction with respect to substrate **2899**).

[0167] As shown in FIG. **28**A, FIG. **28**B, and FIG. **28**C, each of decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ can have memory cells arranged in the X-direction and the Y-direction (e.g., arranged in rows in the X-direction and in columns in the Y-direction). For example, deck $\mathbf{2805}_0$ can include memory cells $\mathbf{2810}_0$, $\mathbf{2811}_0$, $\mathbf{2812}_0$, and $\mathbf{2813}_0$ (e.g., arranged in a row), memory cells $\mathbf{2820}_0$, $\mathbf{2821}_0$, $\mathbf{2822}_0$, and $\mathbf{2823}_0$ (e.g., arranged in a row), and memory cells $\mathbf{2830}_0$, $\mathbf{2831}_0$, $\mathbf{2832}_0$, and $\mathbf{2833}_0$ (e.g., arranged in a row).

[0168] Deck $\mathbf{2805}_1$ can include memory cells $\mathbf{2810}_1$, $\mathbf{2811}_1$, $\mathbf{2812}_1$, and $\mathbf{2813}_1$ (e.g., arranged in a row), memory cells $\mathbf{2820}_1$, $\mathbf{2821}_1$, $\mathbf{2822}_1$, and $\mathbf{2823}_1$ (e.g., arranged in a row), and memory cells $\mathbf{2830}_1$, $\mathbf{2831}_1$, $\mathbf{2832}_1$, and $\mathbf{2833}_1$ (e.g., arranged in a row).

[0169] Deck $\mathbf{2805}_2$ can include memory cells $\mathbf{2810}_2$, $\mathbf{2811}_2$, $\mathbf{2812}_2$, and $\mathbf{2813}_2$ (e.g., arranged in a row), memory cells $\mathbf{2820}_2$, $\mathbf{2821}_2$, $\mathbf{2822}_2$, and $\mathbf{2823}_2$ (e.g., arranged in a row), and memory cells $\mathbf{2830}_2$, $\mathbf{2831}_2$, $\mathbf{2832}_2$, and $\mathbf{2833}_2$ (e.g., arranged in a row).

[0170] Deck $\mathbf{2805}_3$ can include memory cells $\mathbf{2810}_3$, $\mathbf{2811}_3$, $\mathbf{2812}_3$, and $\mathbf{2813}_3$ (e.g., arranged in a row), memory cells $\mathbf{2820}_3$, $\mathbf{2821}_3$, $\mathbf{2822}_3$, and $\mathbf{2823}_3$ (e.g., arranged in a row), and memory cells $\mathbf{2830}_3$, $\mathbf{2831}_3$, $\mathbf{2832}_3$, and $\mathbf{2833}_3$ (e.g., arranged in a row).

[0171] As shown in FIG. **28**A, FIG. **28**B, and FIG. **28**C, decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ can be located (e.g., formed vertically in the Z-direction) on levels (e.g., portions) **2850**, **2851**, **2852**, and **2853**, respectively, of memory device **2800**. The arrangement of decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ forms a 3-dimensional (**3**-D) structure of memory cells of memory device **2800** in that different levels of the memory cells of memory device **2800** can be located (e.g., formed) in different levels (e.g., different vertical portions) **2850**, **2851**, **2852**, and **2853** of memory device **2800**.

[0172] Decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ can be formed one deck at a time. For example, decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ can be formed sequentially in the order of decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ (e.g., deck $\mathbf{2805}_1$ is formed first and deck $\mathbf{2805}_3$ is formed last). In this example, the memory cell of one deck (e.g., deck $\mathbf{2805}_1$) can be formed either after formation of the memory cells of another deck (e.g., deck $\mathbf{2805}_0$) or before formation of the memory cells of another deck (e.g., deck $\mathbf{2805}_2$). Alternatively, decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ can be formed concurrently (e.g., simultaneously), such that the memory cells of decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ can be concurrently formed. For example, the memory cells in levels **2850**, **2851**, **2852**, and **2853** of memory device **2800** can be concurrently formed.

[0173] The structures decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ can include the structures of memory devices described above with reference to FIG. **1** through FIG. **27**B. For example, memory device **2800** can include data lines (e.g., bit lines) and access lines (e.g., word lines) to access the memory cells of decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$. For simplicity, data lines and access lines of memory cells are omitted from FIG. **28**A. However, the data lines and access lines of memory device **2800** can be similar to the data lines and access lines, respectively, of the memory devices described above with reference to FIG. **1** through FIG. **27**B.

[0174] FIG. **28**A, FIG. **28**B, and FIG. **28**C show memory device **2800** including four decks (e.g., $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$) as an example. However, the number of decks can be different from four. FIG. **28**A shows each of decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ including one level (e.g., layer) of memory cells as an example. However, at least one of the decks (e.g., one or more of decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$) can have two (or more) levels of memory cells. FIG. **28**A shows an example where each of decks $\mathbf{2805}_0$, $\mathbf{2805}_1$, $\mathbf{2805}_2$, and $\mathbf{2805}_3$ includes four memory cells (e.g., in a row) in the X-direction and three memory cells (e.g., in a column) in the Y-direction. However, the number of memory cells in a row, in a column, or both, can vary. Since memory device **2800** can include the structures of memory devices **200**, **800**, **900**, and **2300**, memory device **2800** can also have improvements and benefits like memory devices **200**, **800**, **900**, **2300**, and **2300**.

[0175] The illustrations of apparatuses (e.g., memory devices **100**, **200**, **800**, **900**, **2300**, and **2800**) and methods (e.g., methods of forming memory devices **900** and **2300**) are intended to provide a general understanding of the structure of various embodiments and are not intended to provide a complete description of all the elements and features of apparatuses that might make use of the structures described herein. An apparatus herein refers to, for example, either a device (e.g., any of memory devices **100**, **200**, **800**, **900**, **2300**, and **2800**) or a system (e.g., an electronic item that can include any of memory devices **100**, **200**, **800**, **900**, **2300** and **2800**).

[0176] Any of the components described above with reference to FIG. **1** through FIG. **28**C can be implemented in a number of ways, including simulation via software. Thus,

apparatuses (e.g., memory devices **100**, **200**, **800**, **900**, **2300**, and **2800**) or part of each of these memory devices described above, may all be characterized as "modules" (or "module") herein. Such modules may include hardware circuitry, single- and/or multi-processor circuits, memory circuits, software program modules and objects and/or firmware, and combinations thereof, as desired and/or as appropriate for particular implementations of various embodiments. For example, such modules may be included in a system operation simulation package, such as a software electrical signal simulation package, a power usage and ranges simulation package, a capacitance-inductance simulation package, a power/heat dissipation simulation package, a signal transmission-reception simulation package, and/or a combination of software and hardware used to operate or simulate the operation of various potential embodiments.

[0177] The memory devices (e.g., memory devices **100**, **200**, **800**, **900**, **2300**, and **2800**) described herein may be included in apparatuses (e.g., electronic circuitry) such as high-speed computers, communication and signal processing circuitry, single- or multi-processor modules, single or multiple embedded processors, multicore processors, message information switches, and application-specific modules including multilayer, multichip modules. Such apparatuses may further be included as subcomponents within a variety of other apparatuses (e.g., electronic systems), such as televisions, cellular telephones, personal computers (e.g., laptop computers, desktop computers, handheld computers, tablet computers, etc.), workstations, radios, video players, audio players (e.g., MP3 (Motion Picture Experts Group, Audio Layer 3) players), vehicles, medical devices (e.g., heart monitor, blood pressure monitor, etc.), set top boxes, and others.

[0178] The embodiments described above with reference to FIG. **1** through FIG. **28**C include apparatuses and methods of operating the apparatuses. One of the apparatuses includes a first transistor including a first channel region, and a charge storage structure separated from the first channel region; a second transistor including a second channel region formed over the charge storage structure; and a data line formed over and contacting the first channel region and the second channel region, the data line including a portion adjacent the first channel region and separated from the first channel region by a dielectric material. Other embodiments, including additional apparatuses and methods, are described.

[0179] In the detailed description and the claims, the term "on" used with respect to two or more elements (e.g., materials), one "on" the other, means at least some contact between the elements (e.g., between the materials). The term "over" means the elements (e.g., materials) are in close proximity, but possibly with one or more additional intervening elements (e.g., materials) such that contact is possible but not required. Neither "on" nor "over" implies any directionality as used herein unless stated as such.

[0180] In the detailed description and the claims, a list of items joined by the term "at least one of" can mean any combination of the listed items. For example, if items A and B are listed, then the phrase "at least one of A and B" means A only; B only; or A and B. In another example, if items A, B, and C are listed, then the phrase "at least one of A, B, and C" means A only; B only; C only; A and B (excluding C); A and C (excluding B); B and C (excluding A); or all of A, B, and C. Item A can include a single element or multiple elements. Item B can include a single element or multiple elements. Item C can include a single element or multiple elements.

[0181] In the detailed description and the claims, a list of items joined by the term "one of" can mean only one of the list items. For example, if items A and B are listed, then the phrase "one of A and B" means A only (excluding B), or B only (excluding A). In another example, if items A, B, and C are listed, then the phrase "one of A, B, and C" means A only; B only; or C only. Item A can include a single element or multiple elements. Item B can include a single element or multiple elements. Item C can include a single element or multiple elements.

[0182] The above description and the drawings illustrate some embodiments of the inventive subject matter to enable those skilled in the art to practice the embodiments of the inventive subject matter. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Examples merely typify possible variations. Portions and features of some embodiments may be included in, or substituted for, those of others. Many other embodiments will be apparent to those of skill in the art upon reading and understanding the above description.

1. An apparatus comprising:

a memory cell including:

a first transistor including a first channel region, and a charge storage structure separated from the first channel region; and

a second transistor including a second channel region coupled to the charge storage structure; and

a data line coupled to the first channel region and the second channel region, the data line including a portion adjacent the first channel region and separated from the first channel region by a dielectric material.

2. The apparatus of claim **1**, wherein the second channel region is between the data line and the charge storage structure.

3. The apparatus of claim **1**, wherein the second channel region includes semiconducting oxide material.

4. The apparatus of claim **1**, wherein the first channel region and the second channel region have different conductivity types.

5. The apparatus of claim **1**, further comprising a ground connection coupled to the first channel region.

6. The apparatus of claim **1**, further comprising a conductive line separated from the first and second channel regions, the conductive line spanning across part of the first and second channel regions and forming a gate of the first and second transistors.

7. The apparatus of claim **6**, further comprising an additional conductive line separated from the first and second channel regions and opposite from the conductive line, such that the first and second channel regions are between the conductive line and the additional conductive line, wherein:

the additional conductive line spans across an additional part of the first and second channel regions and forms the gates of the first and second transistors.

8. The apparatus of claim **7**, wherein the conductive line is coupled to the additional conductive line.

9. The apparatus of claim **1**, wherein the data line does not have a portion separate from the second channel region by an additional dielectric material.

10. The apparatus of claim **1**, wherein the second channel region includes at least one of zinc tin oxide (ZTO), indium

zinc oxide (IZO), zinc oxide (ZnO_x), indium gallium zinc oxide (IGZO), indium gallium silicon oxide (IGSO), indium oxide (InO_x, In_2O_3), tin oxide (SnO_2), titanium oxide (TiO_x), zinc oxide nitride ($Zn_xO_yN_z$), magnesium zinc oxide ($Mg_xZn_yO_z$), indium zinc oxide ($In_xZn_yO_z$), indium gallium zinc oxide ($In_xGa_yZn_zO_a$), zirconium indium zinc oxide ($Zr_xIn_yZn_zO_a$), hafnium indium zinc oxide ($Hf_xIn_yZn_zO_a$), tin indium zinc oxide ($Sn_xIn_yZn_zO_a$), aluminum tin indium zinc oxide ($Al_xSn_yIn_zZn_aO_d$), silicon indium zinc oxide ($Si_xIn_yZn_zO_a$), zinc tin oxide ($Zn_xSn_yO_z$), aluminum zinc tin oxide ($Al_xZn_ySn_zO_a$), gallium zinc tin oxide ($Ga_xZn_ySn_zO_a$), zirconium zinc tin oxide ($Zr_xZn_ySn_zO_a$), indium gallium silicon oxide (InGaSiO), and gallium phosphide (GaP).

11. An apparatus comprising:

a memory cell including:

a semiconductor material including a first side and a second side opposite from the first side, a charge storage structure located on the first side of the semiconductor material, and a first dielectric material between the semiconductor material and the charge storage structure; and

a semiconducting oxide material adjacent the charge storage structure and located on the first side of the semiconductor material;

a data line coupled to the semiconductor material and the semiconducting oxide material, wherein the data line includes a portion adjacent the second side of the semiconductor material; and

a second dielectric material between and contacting the portion of the data line and the semiconductor material.

12. The apparatus of claim **11**, wherein the data line contacts the semiconducting oxide material at an interface, and wherein:

the semiconducting oxide material has a length in a direction from the interface to the charge storage structure; and

the portion of the data line has a length in the direction from the interface to the charge storage structure, and wherein the length of the portion of the data line is less than the length of the semiconducting oxide material.

13. The apparatus of claim **11**, wherein the semiconductor material and the semiconducting oxide material have different conductivity types.

14. The apparatus of claim **11**, wherein the semiconductor material is p-type conductivity and semiconducting oxide material is n-type conductivity.

15. An apparatus comprising:

a first memory cell including:

a first transistor including a first channel region, and a first charge storage structure separated from the first channel region; and

a second transistor including a second channel region coupled to the charge storage structure;

a second memory cell including:

a third transistor including a third channel region, and a second charge storage structure separated from the third channel region; and

a fourth transistor including a fourth channel region coupled to the second charge storage structure; and

a data line coupled to the first, second, third, and fourth channel regions, the data line including:

a first portion adjacent the first channel region and separated from the first channel region by a first dielectric material; and

a second portion adjacent the third channel region and separated from the third channel region by a second dielectric material.

16. The apparatus of claim **15**, wherein a side of the first portion of the data line is separated from a side of the second portion of the data line by a gap, and wherein the gap is void of a material of the data line.

17. The apparatus of claim **15**, wherein the data line includes a first part extending from the first memory cell to the second memory cell, a second part perpendicular to the first part and extending from the first memory cell to the second memory cell, and wherein the first and second portions of the data line are included in the second part of the data line.

18. The apparatus of claim **15**, wherein the first and third channel regions have a first conductivity type; and the second and fourth channel regions have a second conductivity type.

19. The apparatus of claim **17**, further comprising a conductive line separated from the first, second, third, and fourth channel regions, the conductive line spanning across part of the first, second, third, and fourth channel regions.

20. The apparatus of claim **19**, further comprising an additional conductive line separated from the first, second, third, and fourth channel regions and opposite from the conductive line, wherein the first, second, third, and fourth channel regions are between the conductive line and the additional conductive line, and the additional conductive line spans across an additional part of the from the first, second, third, and fourth channel regions.

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