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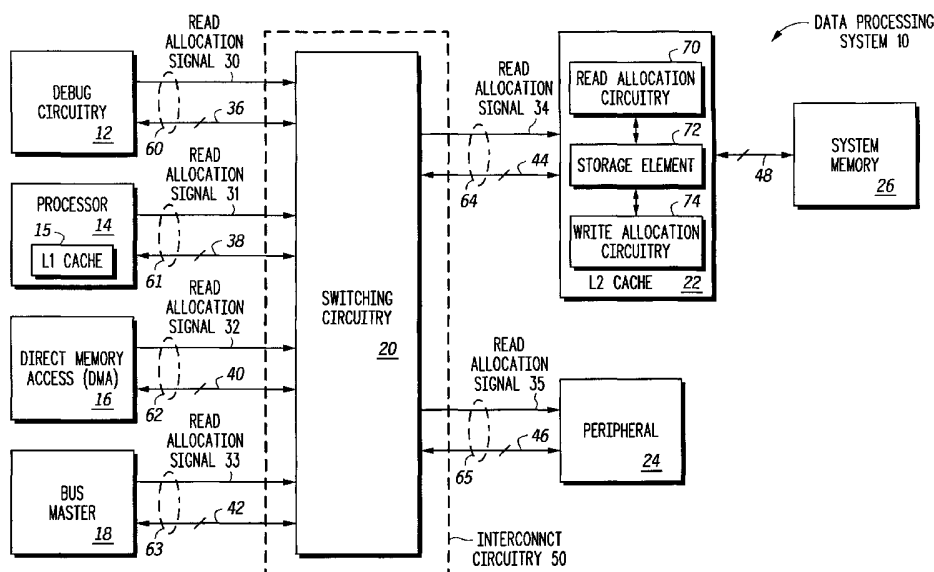
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[Continued on next page]

(54) Title: READ ACCESS AND STORAGE CIRCUITRY READ ALLOCATION APPLICABLE TO A CACHE



(57) Abstract: A read allocation indicator (e.g. read allocation signal 30) is provided to storage circuitry (e.g. cache 22) to selectively determine whether read allocation will be performed for the read access. Read allocation may include modification of the information content of the cache (22) and/or modification of the read replacement algorithm state implemented by the read allocation circuitry (70) in cache (22). For certain types of debug operations, it may be very useful to provide a read allocation indicator that ensures that no unwanted modification are made to the storage circuitry during a read access. Yet other types of debug operations may want the storage circuitry to be modified in the standard manner when a read access occurs.

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— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

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7 April 2005

**INTERNATIONAL SEARCH REPORT**

International application No.  
PCT/US04/13372

**A. CLASSIFICATION OF SUBJECT MATTER**  
 IPC(7) : GO6F 12/00, 13/00  
 US CL : 711/100, 118, 119, 170.  
 According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**  
 Minimum documentation searched (classification system followed by classification symbols)  
 U.S. : 711/100, 118, 119, 170.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
 Microsoft Dictionary.

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
 Please See Continuation Sheet

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,496,902 B1 (FAANES et al) 17 December 2002 (17.12.2002), column 14, line 25 bridging column 15, line 35.	1-10
A	US 6,353,829 A (KOBLENZ et al) 05 March 2002 (05.03.2002), column 8, lines 57 et seq.	1-10
A	US 5,471,598 A (QUATTROMANI et al.) 28 November 1995 (28.11.1995), Abstract, see entire patent.	1-10

Further documents are listed in the continuation of Box C.  See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

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Name and mailing address of the ISA/US: Mail Stop PCT, Attn: ISA/US, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, Facsimile No. (703)305-3230  
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**INTERNATIONAL SEARCH REPORT**

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**Continuation of B. FIELDS SEARCHED Item 3:**

EAST, DERWENT, UPPGPUB, EPO/JPO ABST, IBMTDB

Search terms: read allocation, write allocation, allocation indicator(s)/signal(s), debug/test operation, cache hit/miss, memory allocation.