US 20150015753A1

(19) **United States**

(12) **Patent Application Publication**

Inobe

(10) **Pub. No.: US 2015/0015753 A1**

(43) **Pub. Date: Jan. 15, 2015**

(54) **IMAGE PROCESSOR**

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(21) Appl. No.: **14/189,195**

(22) Filed: **Feb. 25, 2014**

(30) **Foreign Application Priority Data**

Jul. 10, 2013 (JP) 2013-144534

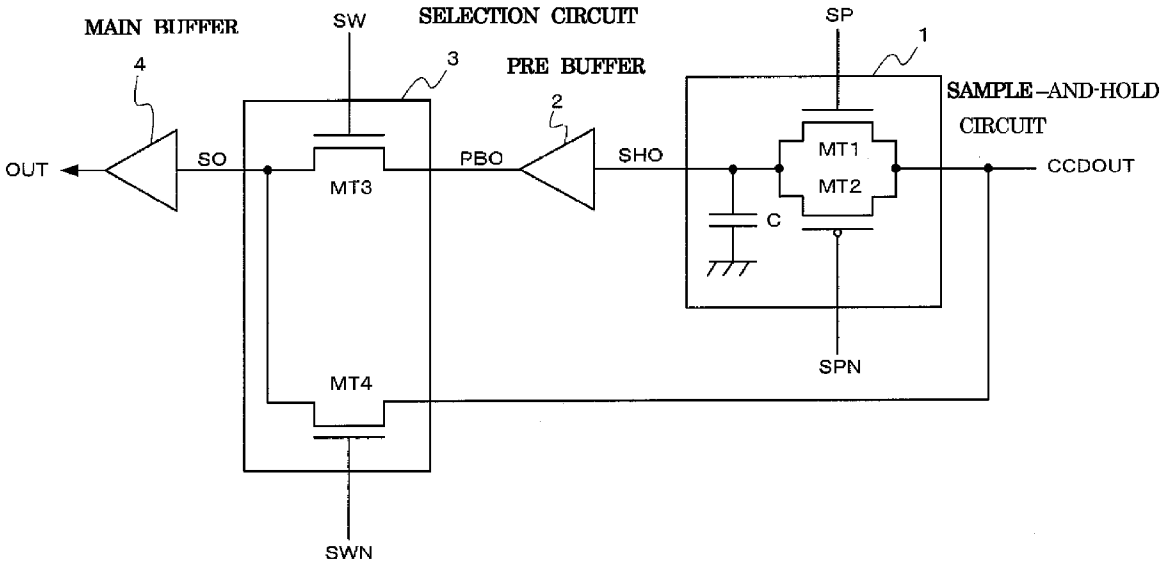
Publication Classification

(51) **Int. Cl.**
H04N 5/372 (2006.01)

(52) **U.S. Cl.**
CPC *H04N 5/37213* (2013.01)
USPC **348/298**

(57) **ABSTRACT**

An aspect of one present embodiment, there is provided a solid state image processer, including a sample-and-hold circuit sampling an output signal of the CCD to hold the output signal of the CCD as voltage, a pre-buffer receiving an output signal of the sample-and-hold circuit, a selection circuit receiving the output signal of the pre-buffer as a first input signal and the output signal of the CCD as a second input signal to select the first input signal or the second input signal as an output signal of the selection circuit according to an instruction of a selection signal, and a main buffer receiving the output signal of the selection circuit.



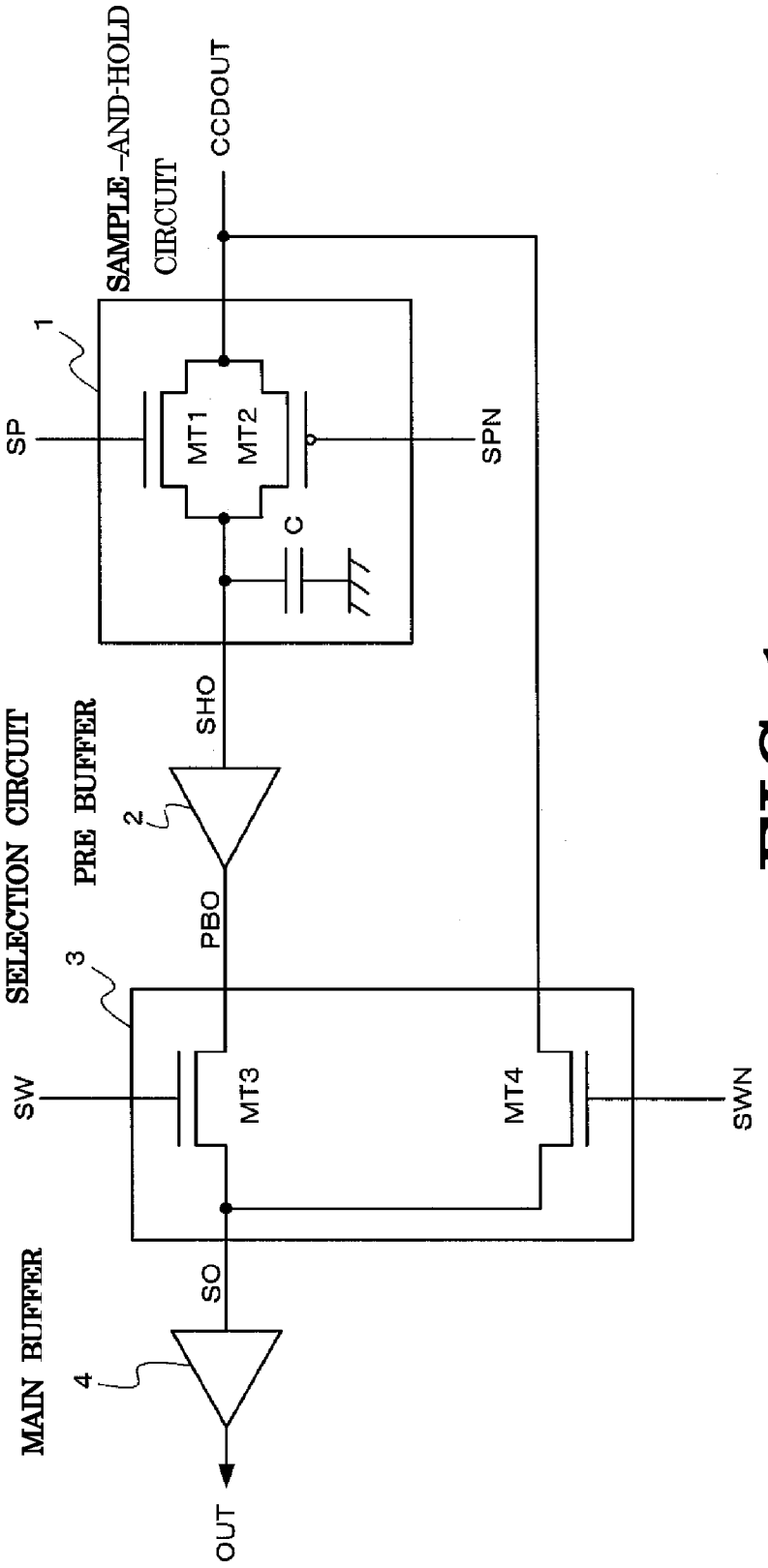

SAMPLE-AND-HOLD CIRCUIT
CCDOUT
1
SP
MT1
MT2
SPN
C
SHO
PRE BUFFER
2
PBO
SELECTION CIRCUIT
3
SW
MT3
MT4
SWN
SO
MAIN BUFFER
4
OUT

FIG.1

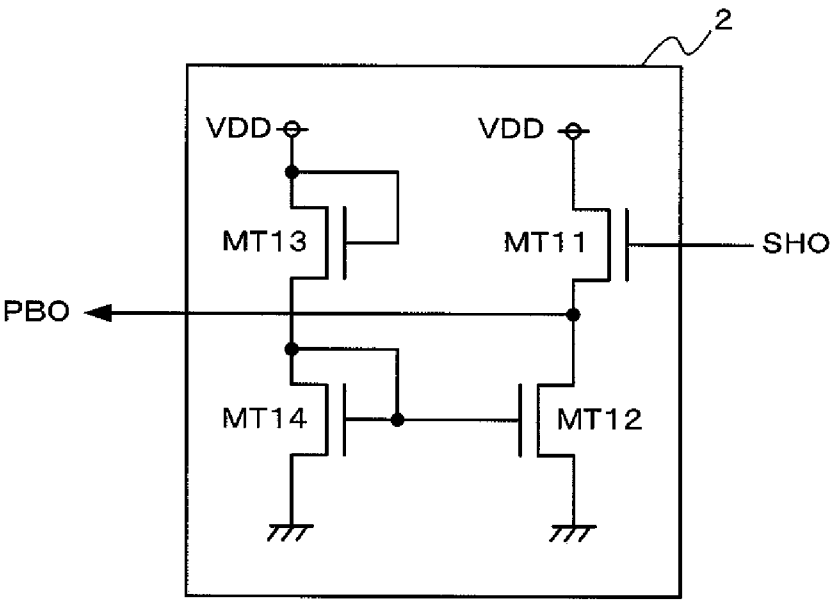


FIG.2

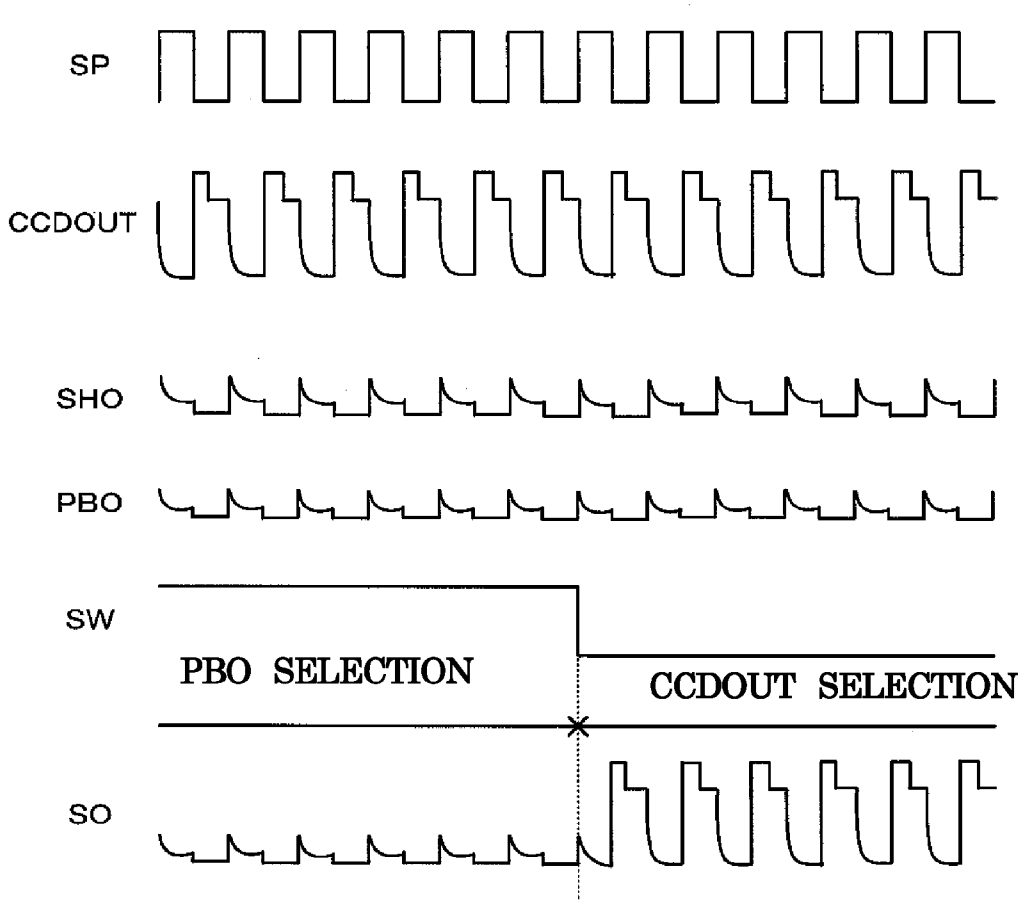


FIG.3

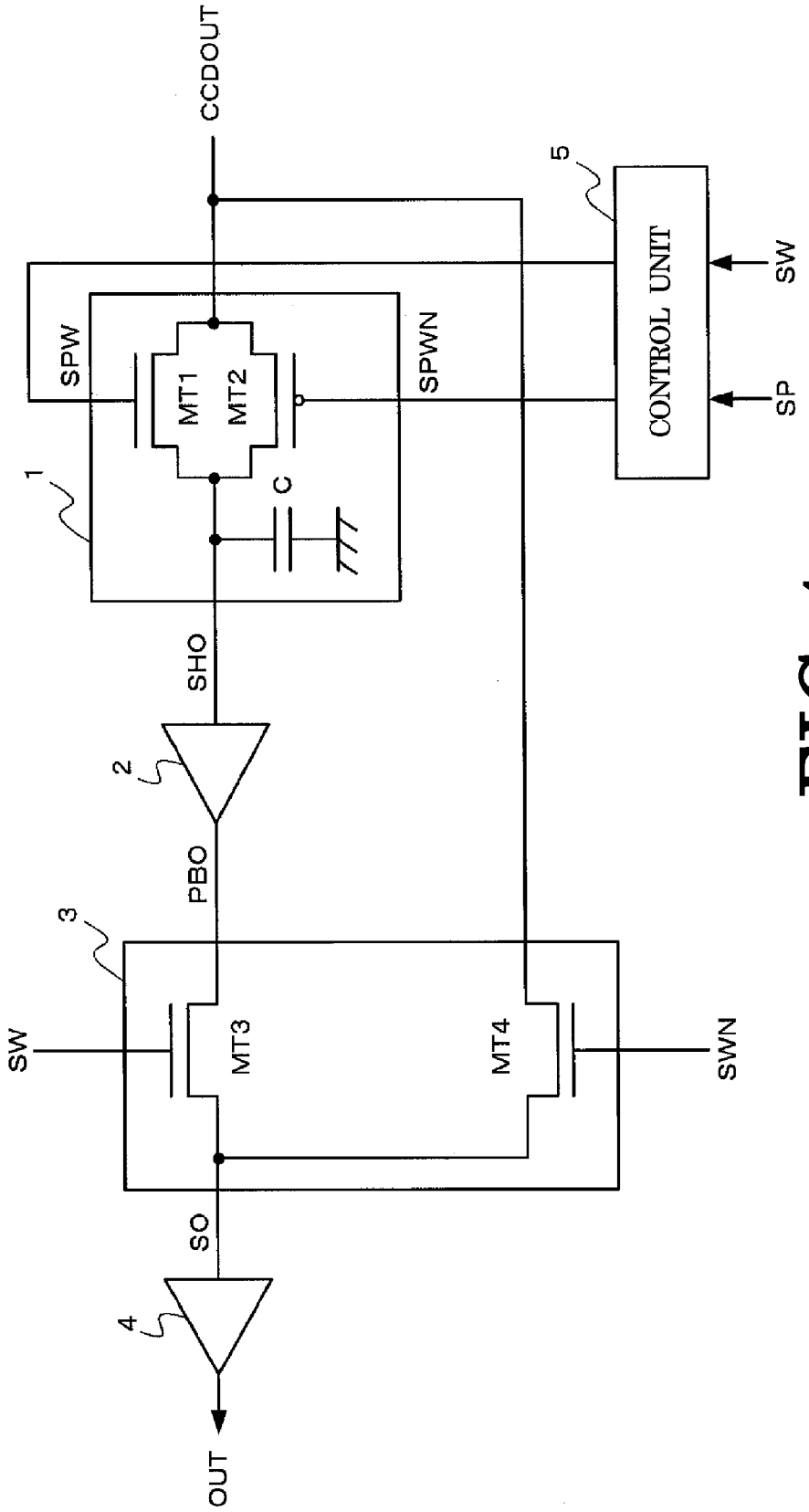

CCDOUT
5
CONTROL UNIT
SW
SP
SPW
SPWN
MT1
MT2
C
1
SHO
2
PBO
3
SW
MT3
MT4
SWN
SO
4
OUT

FIG.4

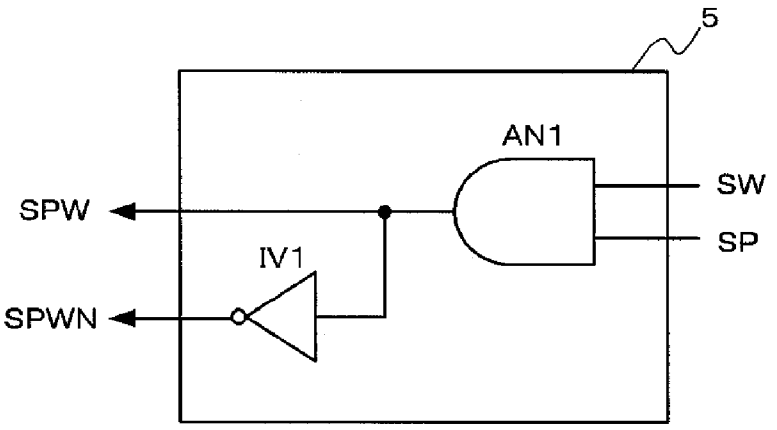


FIG.5A

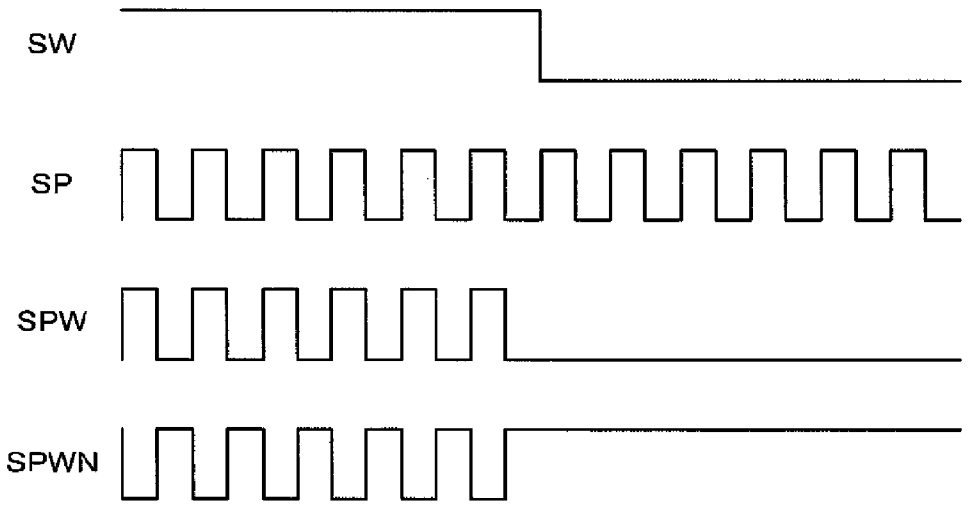


FIG.5B

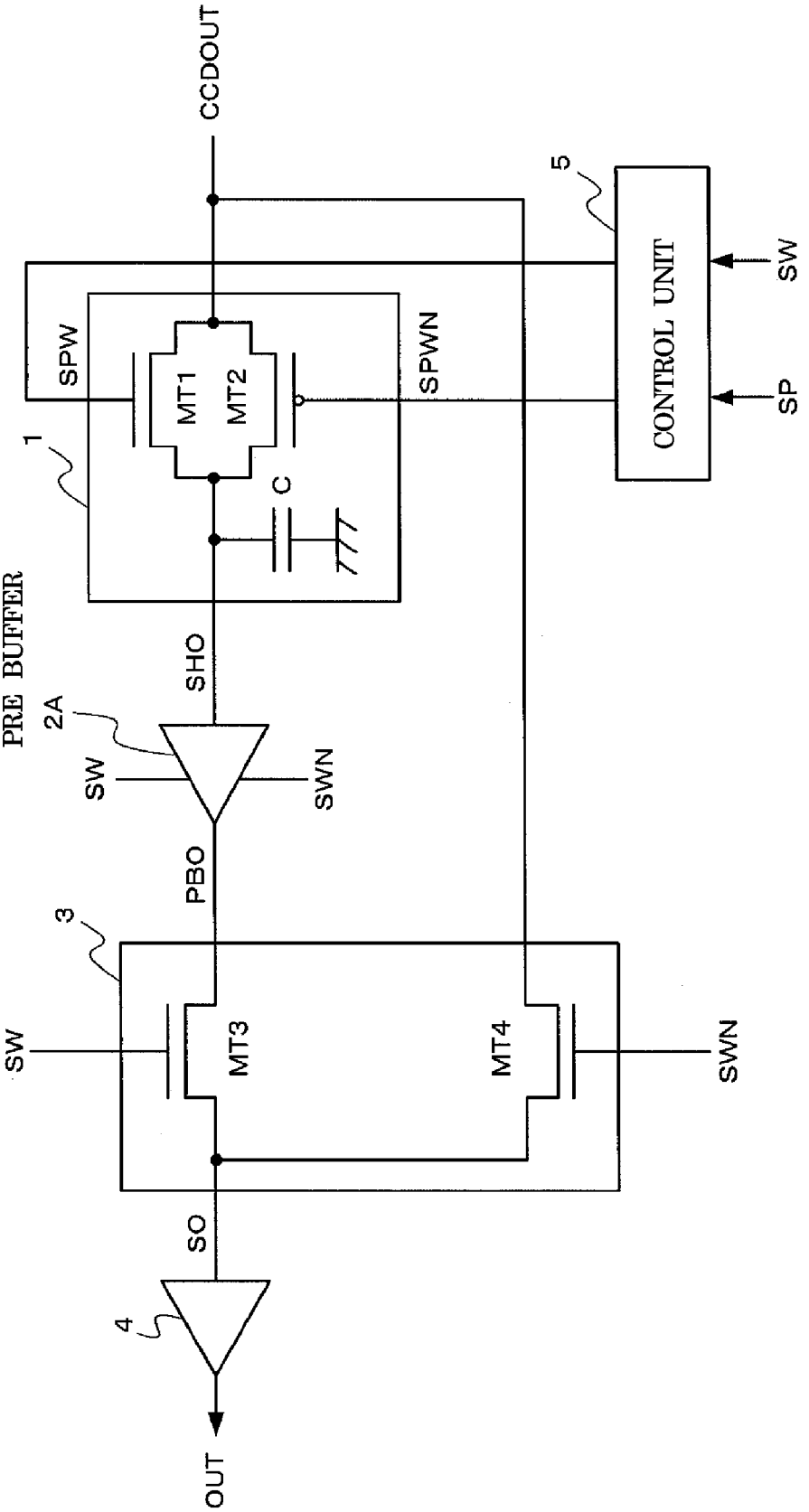

CCDOUT
5
CONTROL UNIT
SW
SP
SPW
SPWN
MT1
MT2
C
1
PRE BUFFER
SHO
2A
SW
SWN
PBO
3
SW
MT3
MT4
SWN
SO
4
OUT

FIG.6

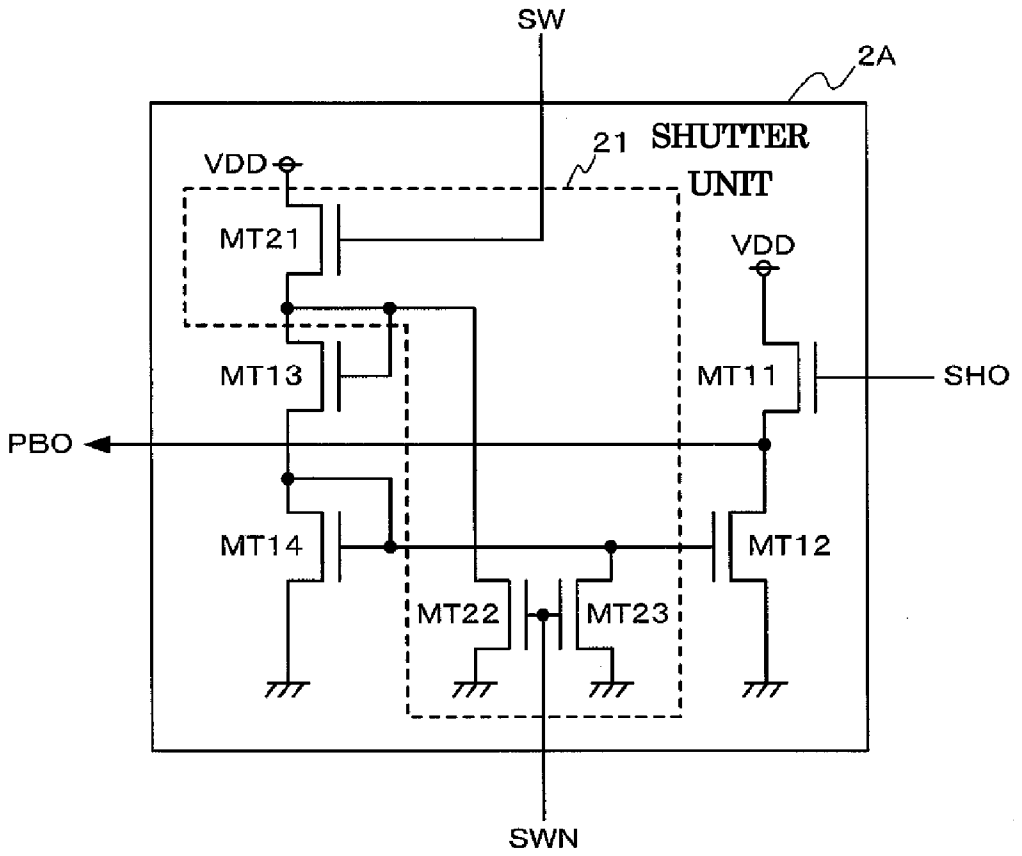

SW
2A
21
SHUTTER
UNIT
VDD
MT21
VDD
MT13
MT11
SHO
PBO
MT14
MT12
MT22
MT23
SWN

FIG.7

IMAGE PROCESSOR

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is based upon and claims the benefit of priority from prior Japanese Patent Application No. 2013-144534, filed on Jul. 10, 2013, the entire contents of which are incorporated herein by reference.

FIELD

[0002] Exemplary embodiments described herein generally relate to an image processor.

BACKGROUND

[0003] In an image reader such as a copy machine, a scanner or the like, photoelectric conversion is conducted by an image processor installing a charge coupled device (CCD). Recently, a sample-and-hold circuit is provided in the image processor to stabilize a level of an output signal for corresponding to highly increasing of reading speed of the image reader. In the stabilization, an output signal of the CCD is performed to be held in a sampling process.

[0004] In such the situation, a pre-buffer having smaller driving force is provided at a latter part of the sample-and-hold circuit to stabilize the sampling step during higher driving. Accordingly, a constitution of two-step buffer in which a main buffer with larger driving force is driven by the pre-buffer, is provided.

[0005] When the copy machine, the scanner or the like using such the image processor is provided as series products, sample-and-hold function may be not necessary dependent on a kind of the products.

[0006] In such a case, an output data of the CCD is directly conducted to input into the pre-buffer where the sample-and-hold circuit is set to be usually in the sampling state.

[0007] When the pre-buffer is constituted with one conductive-type MOS transistors, the output level is lower than the input level.

[0008] A problem is conventionally generated in a case that the sample-and-hold function is not necessary. Namely sensitivity of the image processor is lowered as the signal is passed through the pre-buffer. Further, electrical current consumption due to the pre-buffer is also remained a significant problem.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. **1** is a block diagram showing a constitution of an image processor according to a first embodiment;

[0010] FIG. **2** is a block diagram showing a constitution of a pre-buffer of the image processor according to the first embodiment;

[0011] FIG. **3** is a wave form diagram showing an action of the image processor according to the first embodiment;

[0012] FIG. **4** is a block diagram showing a constitution of an image processor according to a second embodiment;

[0013] FIG. **5**A is a block diagram showing a constitution of a sampling abort control unit of the image processor according to the second embodiment;

[0014] FIG. **5**B is a wave form diagram showing the sampling abort control unit of an action of the image processor according to the second embodiment;

[0015] FIG. **6** is a block diagram showing a constitution of the image processor according to a third embodiment;

[0016] FIG. **7** is a block diagram showing a constitution of a constitution of a pre-buffer of the image processor according to the third embodiment.

DETAILED DESCRIPTION

[0017] An aspect of one embodiment, there is provided an image processor, including claim **1**.

[0018] Embodiments will be described below in detail with reference to the attached drawings mentioned above. Throughout the attached drawings, similar or same reference numerals show similar, equivalent or same components, and the description is not repeated.

First Embodiment

[0019] FIG. **1** is a block diagram showing a constitution of an image processor according to a first embodiment.

[0020] An image processor according to the first embodiment includes a sample-and-hold circuit **1**, a pre-buffer **2**, a selection circuit **3** and a main buffer **4**. The sample-and-hold circuit **1** performs sampling an output signal CCDOUT of the CCD to hold as a sampling voltage. The pre-buffer **2** receives an output signal SHO from the sample-and-hold circuit **1**. The selection circuit **3** receives an output signal SHO of the pre-buffer **2** as a first input signal and an output signal CCDOUT of the CCD as a second input signal to select the first input signal PBO or the second input signal CCDOUT as an output signal according to an instruction of a selection signal SW where an inverse signal SWN is an inversion signal of the selection signal SW. A main buffer **4** receives an output signal SO of the selection circuit **3**

[0021] The sample-and-hold circuit **1** includes an analog switch and a capacitor C. The analog switch is combined with an n-type MOS transistor MT**1** and a p-type MOS transistor MT**2**. A gate terminal of the n-type MOS transistor MT**1** receives the sampling signal SP. A gate terminal of the p-type MOS transistor MT**2** receives an inverse sampling signal SPN. The capacitor C is connected to an output terminal of the analog switch.

[0022] The output signal CCDOUT of the CCD is passed through the sample-and-hold circuit **1** when the sampling signal SP is 'H' (high level). A level of the output signal CCDOUT of the CCD is held in the sample-and-hold circuit **1** during the level of the sampling signal SP being set to be 'L' (low level) when the sampling signal SP is changed from 'H' to 'L'.

[0023] The pre-buffer **2** acts as a middle buffer to transmit the output signal of the sample-and-hold circuit **1** to the main buffer **4**. The sample-and-hold circuit **1** has not driving force, as a result, the pre-buffer **2** is provided to drive the main buffer **4**.

[0024] FIG. **2** is a block diagram showing a constitution of a pre-buffer of the image processor, for example, according to the first embodiment. In an example as shown in FIG. **2**, the pre-buffer **2** is constituted with n-type MOS transistors MT**11**-MT**14**.

[0025] The MOS transistor MT**11** and the MOS transistor MT**12** are formed as a source follower in the pre-buffer **2** as shown in FIG. **2**. Bias potential provided to the MOS transistor MT**12** is generated by the MOS transistor MT**13** and the MOS transistor MT**14**.

[0026] A signal having a same phase as a signal transmitted into a gate terminal of the MOS transistor MT**11**, constituting the source follower, is transmitted from a drain terminal of the MOS transistor MT**11**.

[0027] On the other hand, an amplitude ratio of the source follower is small than one. Accordingly, a level of the output signal PBO of the pre-buffer **2** is lower than a level of the input signal SHO.

[0028] The selection circuit **3** includes an n-type MOS transistor MT**3** received a first input signal PBO and an n-type MOS transistor MT**4** received a second input signal CCDOUT.

[0029] A gate terminal of the MOS transistor MT**3** is received the selection signal SW and a gate terminal of the MOS transistor MT**4** is received an inverse selection signal SWN.

[0030] Accordingly, the MOS transistor MT**3** is conducted when the selection signal SW is set to be 'H' and the MOS transistor MT**4** is conducted when the selection signal SW is set to be 'L'.

[0031] In other words, the selection circuit **3** selects the first signal PBO when the selection signal SW is set to be 'H' and selects the second input signal CCDOUT when the selection signal SW is set to be 'L'. The selection circuit **3** transmits each of the signals as the output signal SO.

[0032] The main buffer **4** transmits the output signal SO transmitted from the selection circuit **3** as an output signal OUT to an external portion.

[0033] FIG. **3** is a wave form diagram showing an action of the image processor, for example, according to the first embodiment.

[0034] In the image processor according to the first embodiment, when the selection signal SW is set to be 'H' as the output signal SO of the selection circuit **3**, the output signal CCDOUT of the CCD is sampled and held in the sample-and-hold circuit **1** so that the output signal PBO is transmitted through the pre-buffer **2**. The output signal CCDOUT is directly transmitted when the selection signal SW is set to be 'L'.

[0035] When sample-and-hold function is not necessary, the selection signal SW is set to be 'L'. In such a manner, the output signal CCDOUT of the CCD can be directly transmitted as the output signal SO of the selection circuit **3**. In such the case, the output signal SO is not influenced by level lowering due to the pre-buffer **2**, as being not passed through the pre-buffer **2**.

[0036] The selection signal SW of the selection circuit **3** is set to be 'L' to be able to directly transmit the output signal CCDOUT of the CCD without passing through the pre-buffer **2** when the sample-and-hold function is not necessary according to the first embodiment.

[0037] In such a manner, the level lowering due to the pre-buffer **2** can be suppressed to block sensitivity lowering when the sample-and-hold circuit is not utilized.

Second Embodiment

[0038] In the image processor according to the first embodiment, the sample-and-hold circuit **1** is operated when sample-and-hold function is not necessary. In a second embodiment, action of the sample-and-hold circuit **1** can be aborted in an image processor when the sample-and-hold function is not necessary, for example.

[0039] FIG. **4** is a block diagram showing a constitution of an image processor, for example, according to the second embodiment.

[0040] In the image processor according to the second embodiment, a sampling abort control unit **5** is added to the image processor according to the first embodiment.

[0041] The sampling abort control unit **5** is received the sampling signal SP and the selection signal SW as an input signals to transmit a sampling signal SPW and an inverse sampling signal SPWN which are generated therein.

[0042] In the second embodiment, the sampling signal SPW is inputted into the gate terminal of the MOS transistor MT**1** of a sample-and-hold circuit **1**, and the inverse sampling signal SPWN is inputted into the gate terminal of the MOS transistor MT**2** of the sample-and-hold circuit **1**.

[0043] FIG. **5**A is a block diagram showing a constitution of the sampling abort control unit **5** in the image processor, for example, according to the second embodiment.

[0044] The sampling abort control unit **5** includes an AND gate AN**1** and an inverter IV**1**. The AND gate AN**1** is received the sampling signal SP and the selection signal SW. The inverter IV**1** inverses an output signal of the AND gate AN**1**.

[0045] The output signal of the AND gate **1** is transmitted as the sampling signal SPW. The output signal of the inverter IV**1** is transmitted as the inverse sampling signal SPWN.

[0046] FIG. **5**B is a wave form diagram showing an action of the sample abort control unit **5** of the image processor, for example, according to the second embodiment

[0047] The sampling signal SPW is the same as the sampling signal SP when the signal selection signal SW is set to be 'H'. On the other hand, the sampling signal SPW is fixed to be 'L' level when the selection signal SW is set to be 'L'.

[0048] The inverse sampling signal SPWN is an inverse signal of the sampling signal SP when the selection signal SW is set to be 'H'. On the other hand, the inverse sampling signal SPWN is fixed to the 'H' level when the selection signal SW is 'L'.

[0049] Accordingly, the sampling signal SPW is fixed to the 'L' level and the inverse sampling signal SPWN is fixed to the 'H' level, when the selection signal SW is set to be 'L' not to be necessary with respect to the sample-and-hold function.

[0050] Therefore, the MOS transistor MT**1** and the MOS transistor MT**2** in the sample-and-hold circuit **1** are not conducted in a period of the selection signal SW being set to be 'L'. Accordingly, the sample-and-hold circuit **1** is aborted the sampling action.

[0051] The sampling action of the sample-and-hold circuit **1** can be aborted when the sample-and-hold function is not necessary according to the second embodiment. In such a manner, electrical current consumption with respect to the sampling of the sample-and-hold circuit **1** can be reduced.

Third Embodiment

[0052] In the image processor according to the first and second embodiments, electrical current flows in the pre-buffer **2** in a case that the sample-and-hold function is not necessary. In a third embodiment, electrical current flowed in the pre-buffer **2** can be cut off as the image processor when the sample-and-hold function is not necessary.

[0053] FIG. **6** is a block diagram showing a constitution of an image processor, for example according to the third embodiment.

[0054] In the image processor according to the third embodiment, the pre-buffer **2** of the image processor accord-

ing to the second embodiment is exchange to a pre-buffer **2**A having current path interception function.

[0055] The pre-buffer **2**A has a function including exchanging function between conducting and cutting off on an electrical current path corresponding to the selection signal SW.

[0056] FIG. **7** is a block diagram showing a constitution of the pre-buffer **2**A of the image processor, for example, according to the third embodiment.

[0057] The current path interception unit **21** in the pre-buffer **2**A is added to the pre-buffer **2** of the circuit as shown in FIG. **2**.

[0058] The current path interception unit **21** includes n-type MOS transistors MT**21**, MT**22**, MT**23**.

[0059] The MOS transistor MT**21** is inserted between a power supply terminal VDD and the MOS transistor MT**13** and a gate terminal of the MOS transistor MT**21** is received the selection signal SW. The MOS transistor MT**21** is set to be off when the selection signal SW is set to be 'L' to cut off the electrical current path between the power supply terminal VDD and the MOS transistor MT**13**.

[0060] Each of the source terminals of the MOS transistors MT**22**, MT**23** is connected to the earth terminal and the inverse selection signal SWN is received in each of the gate terminals. A drain terminal of the MOS transistor MT**22** is connected to the gate terminal of the MOS transistor MT**13** and a drain terminal of the MOS transistor MT**23** is connected to each of the gate terminals of the MOS transistors MT**14**, MT**12**.

[0061] Accordingly, when the selection signal SW is set to be 'L', namely, the inverse selection signal SWN is set to be 'H', each of the MOS transistors MT**22**, MT**23** is set to be on so that a gate potential of each gate terminal of the MOS transistors MT**13**, MT**14**, MT**12** is set to be the earth potential. In such a manner, each of the MOS transistors MT**13**, MT**14**, MT**12** is set to be off so that each of the electrical current paths is cut off.

[0062] Namely, all of the electrical current paths in the pre-buffer **2**A are cut off, when the selection signal SW is set to be 'L' so that the sample-hold function is not necessary.

[0063] The electrical current paths in the pre-buffer **2**A can be cut off when the sample-hold function is not necessary according to the third embodiment. In such a manner, electrical current consumption of the pre-buffer **2**A can be reduced.

[0064] As described above, sensitivity lowering of the sample-and-hold circuit in non-use can be suppressed and electrical current consumption can be reduced, according to at least one of the embodiments of the image processor.

[0065] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A solid state image processing device, comprising:

a sample-and-hold circuit sampling an output signal of the CCD to hold the output signal of the CCD as voltage;

a pre-buffer receiving an output signal of the sample-and-hold circuit;

a selection circuit receiving the output signal of the pre-buffer as a first input signal and the output signal of the CCD as a second input signal to select the first input signal or the second input signal as an output signal of the selection circuit according to an instruction of a selection signal; and

a main buffer received the output signal of the selection circuit.

2. The solid state image processing device of claim **1**, wherein

the sample-and-hold circuit includes an analog switch and a capacitor connected to an output terminal of the analog switch.

3. The solid state image processing device of claim **2**, wherein

the analog switch includes a first transistor and a second transistor having a reverse conductive type to the conductive type of the first transistor.

4. The solid state image processing device of claim **1**, wherein

a first sampling signal and an inverse first sampling signal are inputted into the sample-and-hold circuit.

5. The solid state image processing device of claim **4**, wherein

the first sampling signal and the inverse first sampling signal are inputted into the first transistor and the second transistor, respectively.

6. The solid state image processing device of claim **1**, wherein

the pre-buffer includes a plurality of transistors, each of the transistors has a same conductive type.

7. The solid state image processing device of claim **1**, wherein

the selection circuit includes a third transistor and a fourth transistor which has a same conductive type of the third transistor.

8. The solid state image processing device of claim **7**, wherein

the selection signal and an inverse selection signal are inputted into the third transistor and the fourth transistor.

9. The solid state image processing device of claim **1**, further comprising:

a sampling abort control unit controlling to abort the sample-and-hold circuit.

10. The solid state image processing device of claim **9**, wherein

the sampling abort control unit aborts the sampling of the sample-and-hold circuit when the selection signal instructs the selection of the second input signal.

11. The solid state image processing device of claim **9**, wherein

the first sampling signal and the selection signal are inputted into the sampling abort control unit, the sampling abort control unit generates a second sampling signal and an inverse second sampling signal to be outputted to the sample-and-hold circuit.

12. The solid state image processing device of claim **9**, wherein

the sampling abort control unit includes an AND gate and an inverter to inverse an output signal of the AND gate.

13. The solid state image processing device of claim **12**, wherein

the first sampling signal and the selection signal inputted into the AND gate, and the AND gate and the inverter generate the second sampling signal and the inverse second sampling signal, respectively, to transmit to the sample-and-hold circuit.

14. The solid state image processing device of claim **1**, wherein

the pre-buffer includes a current path interception unit which cuts off an electrical current path in the pre-buffer.

15. The solid state image processing device of claim **14**, wherein

the current path interception unit cut off the electrical current path when the selection signal instructs the selection of the second input signal.

* * * * *