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(54) SEMICONDUCTOR DEVICE, STATIC RANDOM ACCESS MEMORY CELL AND MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

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(52) **U.S. Cl.**

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(58) **Field of Classification Search**

CPC H01L 27/1104; H01L 21/823878; H01L 21/823814; H01L 21/823821;
(Continued)

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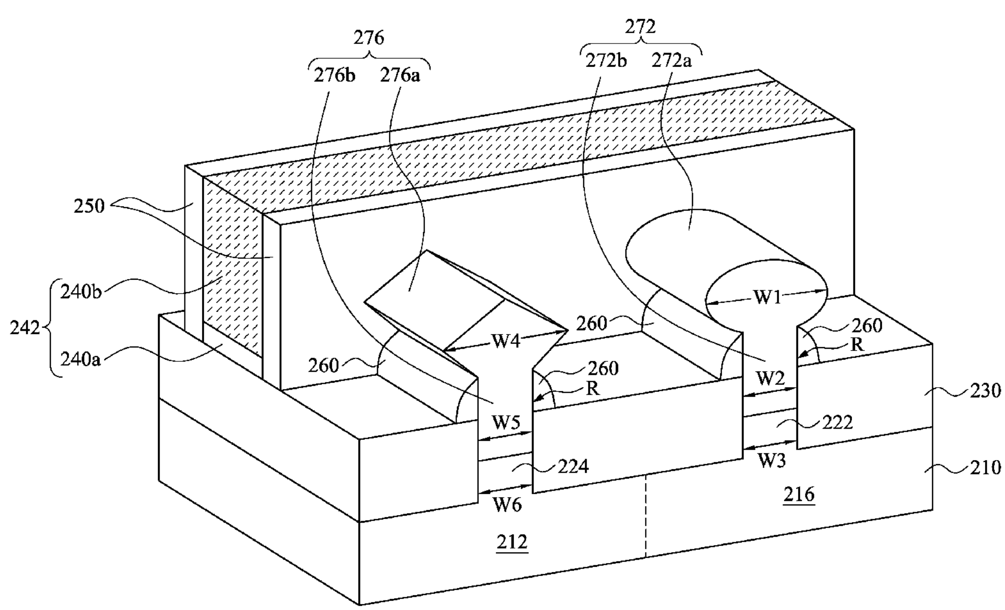
(57) **ABSTRACT**

A semiconductor device includes a substrate, a first semiconductor fin, a second semiconductor fin, an n-type epitaxy structure, a p-type epitaxy structure, and a plurality of dielectric fin sidewall structures. The first semiconductor fin is disposed on the substrate. The second semiconductor fin is disposed on the substrate and adjacent to the first semiconductor fin. The n-type epitaxy structure is disposed on the first semiconductor fin. The p-type epitaxy structure is disposed on the second semiconductor fin and separated from the n-type epitaxy structure. The dielectric fin sidewall structures are disposed on opposite sides of at least one of the n-type epitaxy structure and the p-type epitaxy structure.

20 Claims, 11 Drawing Sheets



(51) **Int. Cl.**
H01L 27/092 (2006.01)
H01L 29/06 (2006.01)
H01L 29/08 (2006.01)
H01L 29/78 (2006.01)
H01L 27/02 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 21/823821*** (2013.01); ***H01L 21/823878*** (2013.01); ***H01L 27/0207*** (2013.01); ***H01L 27/0924*** (2013.01); ***H01L 29/0653*** (2013.01); ***H01L 29/0847*** (2013.01); ***H01L 29/7853*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 29/7853; H01L 29/0653; H01L 21/823807; H01L 29/0847; H01L 27/0924
USPC 257/369
See application file for complete search history.

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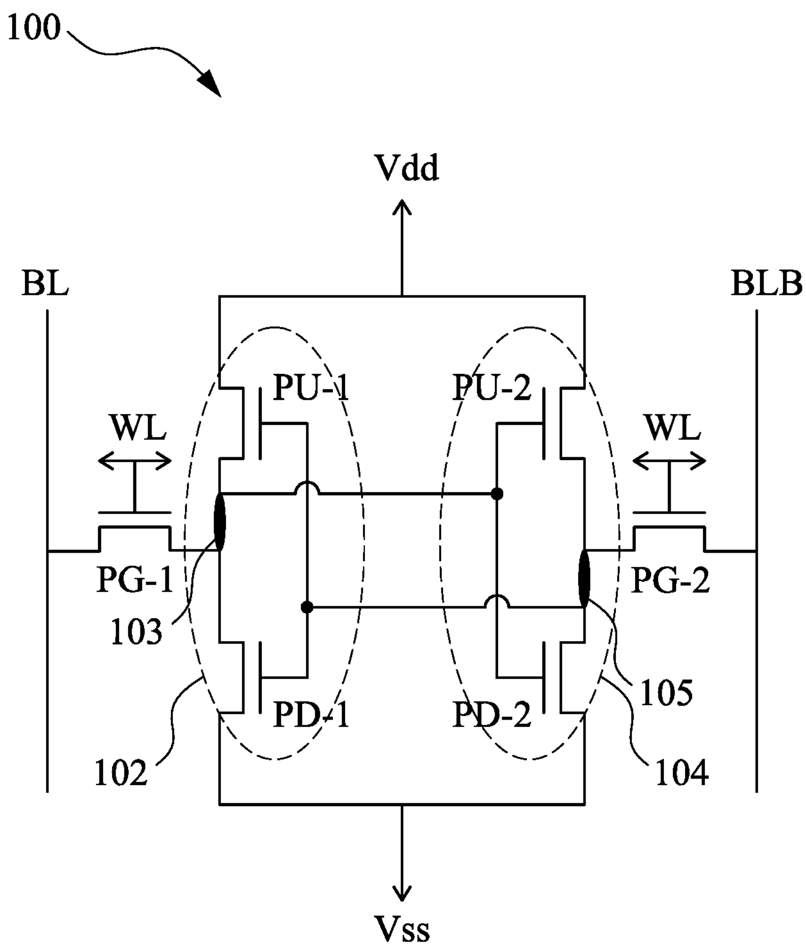

Fig. 1

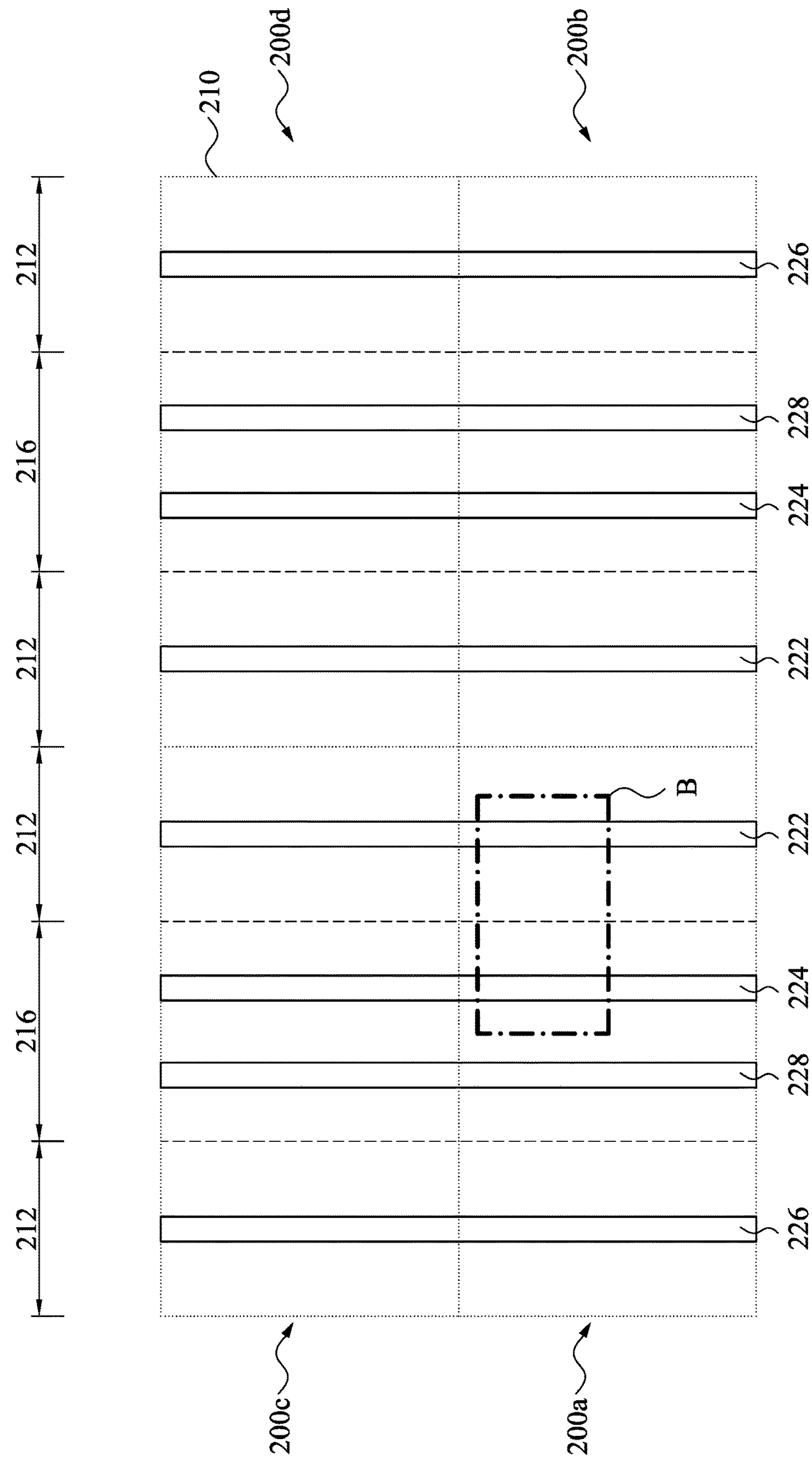
200d
200b
210
212
216
212
212
216
212
226
228
224
222
B
222
224
228
226
200c
200a

Fig. 2A

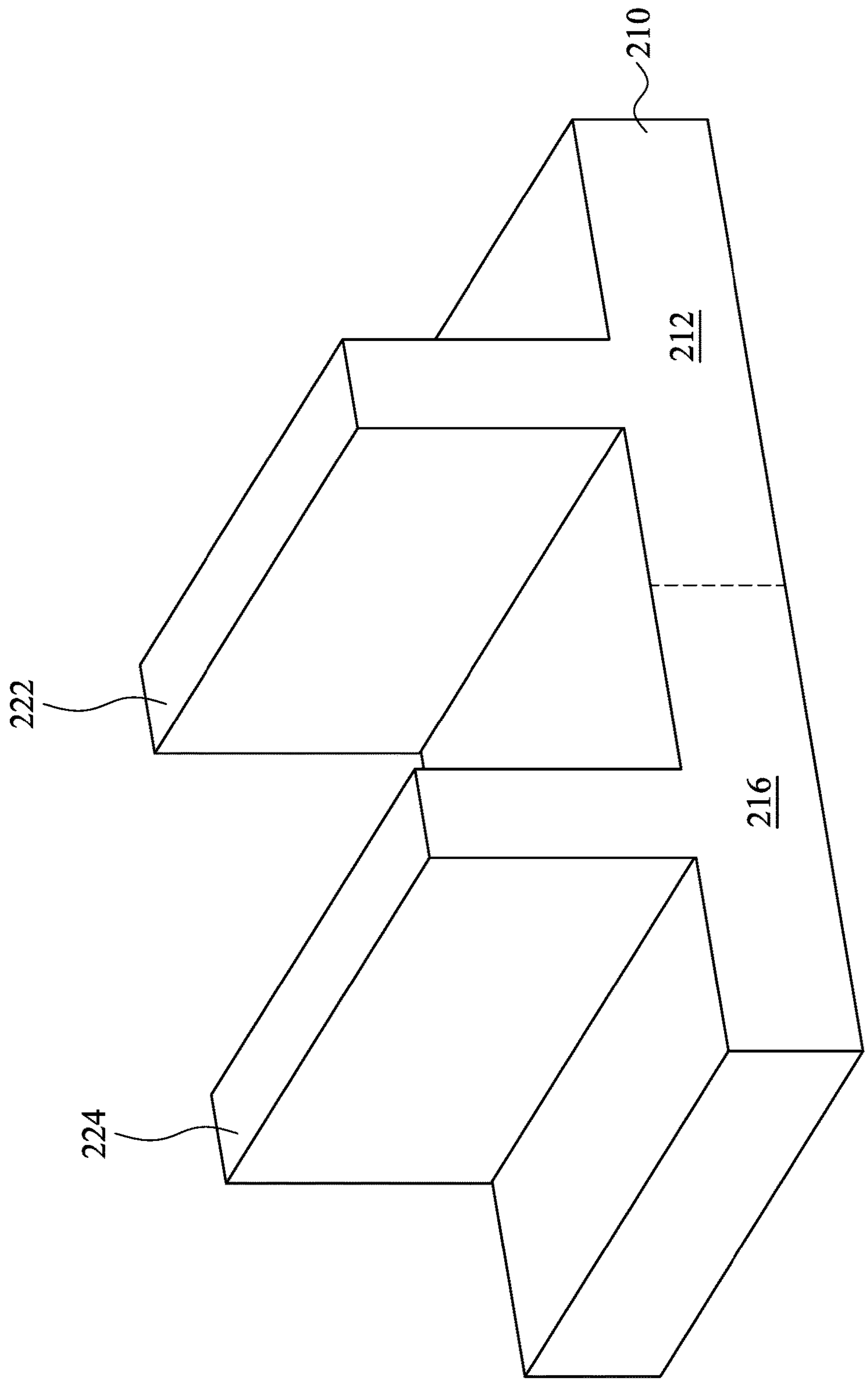

Fig. 2B

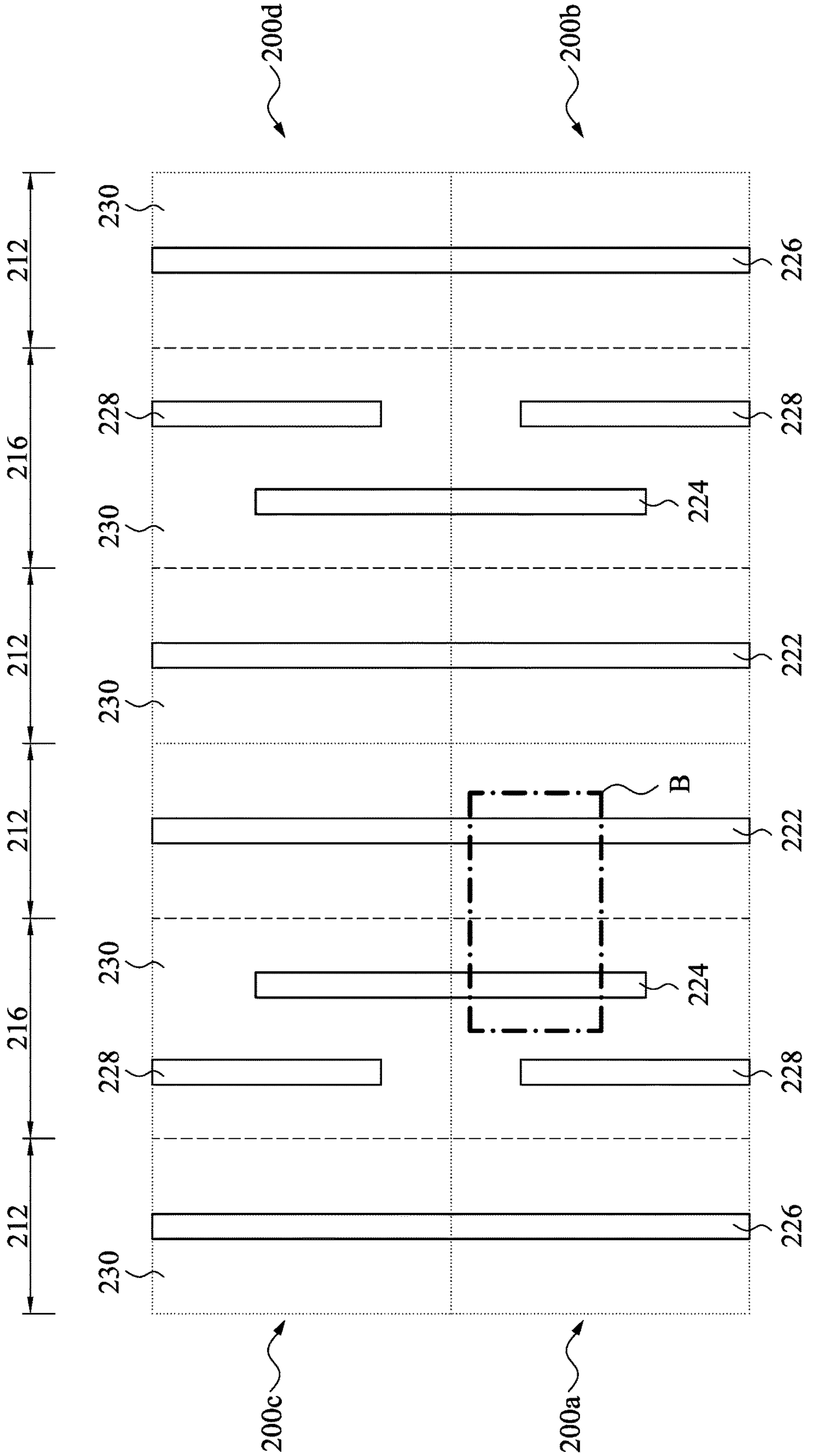
200d
200b
212
216
212
212
216
212
230
226
228
228
224
230
222
230
B
222
230
224
228
228
226
230
200c
200a

Fig. 3A

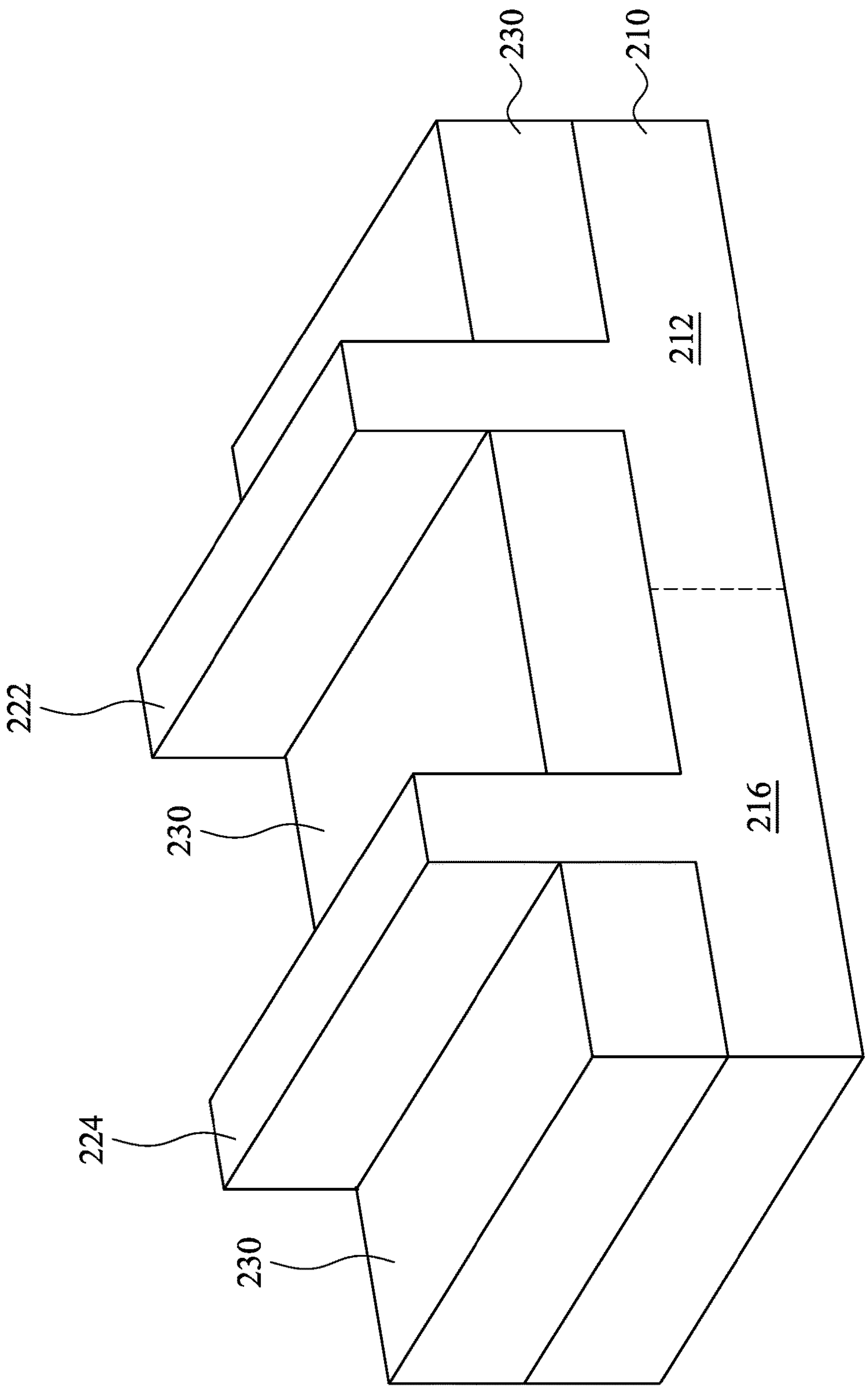

Fig. 3B

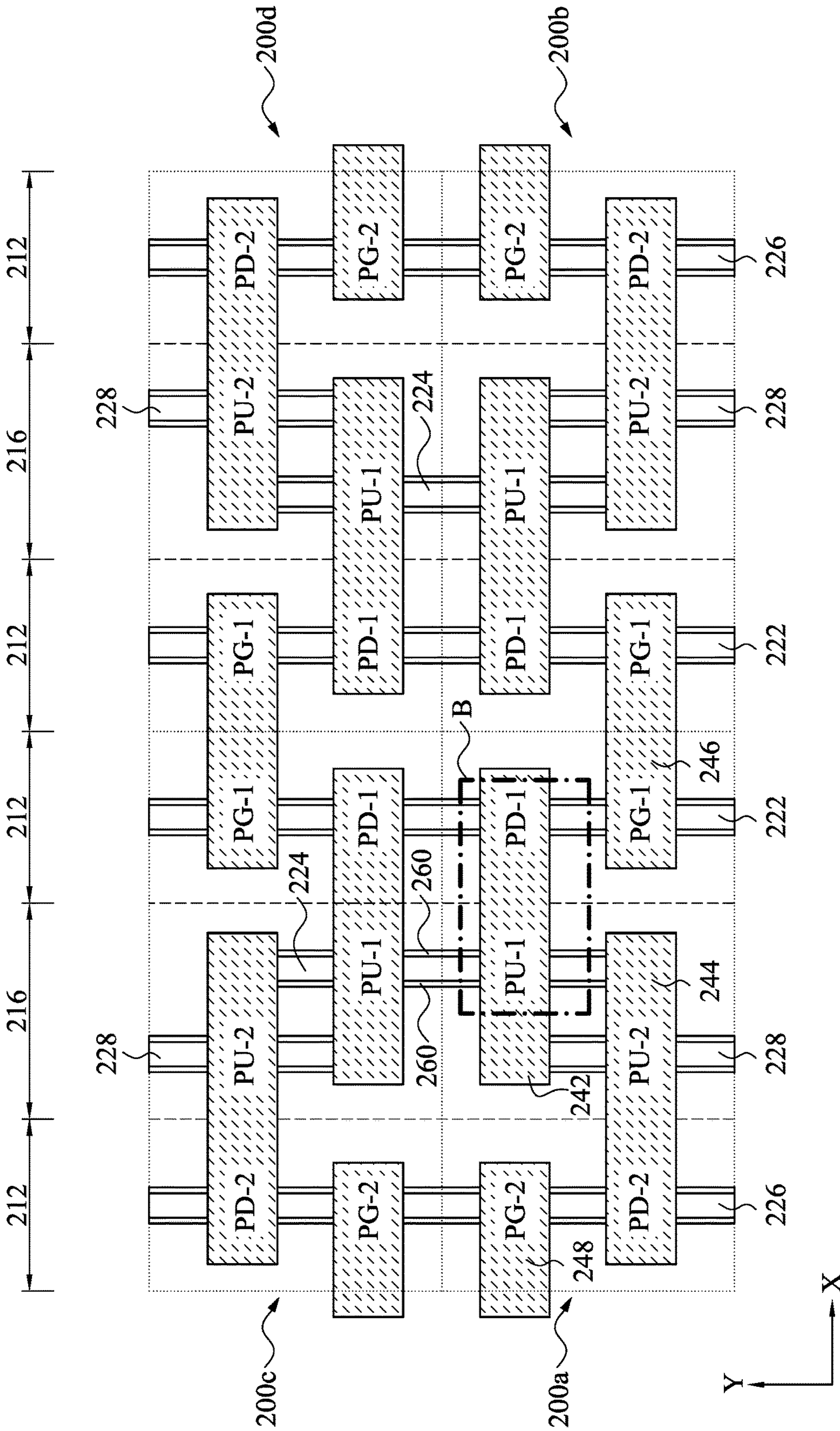
200d
200b
200c
200a
212
216
212
212
216
212
PD-2
PG-2
PU-2
PU-1
PG-1
PD-1
224
226
228
222
246
244
242
248
260
B
X
Y

Fig. 4A

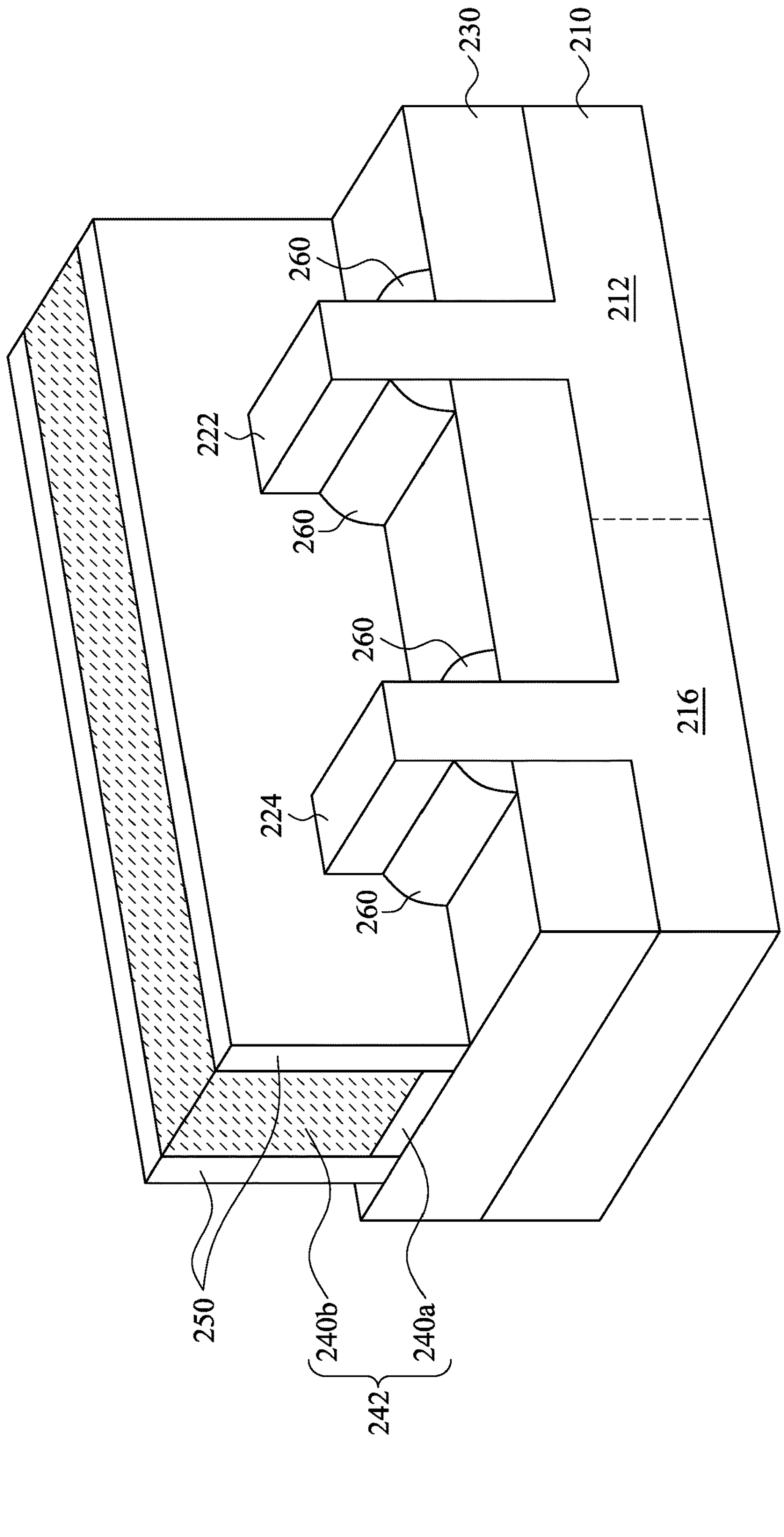

Fig. 4B

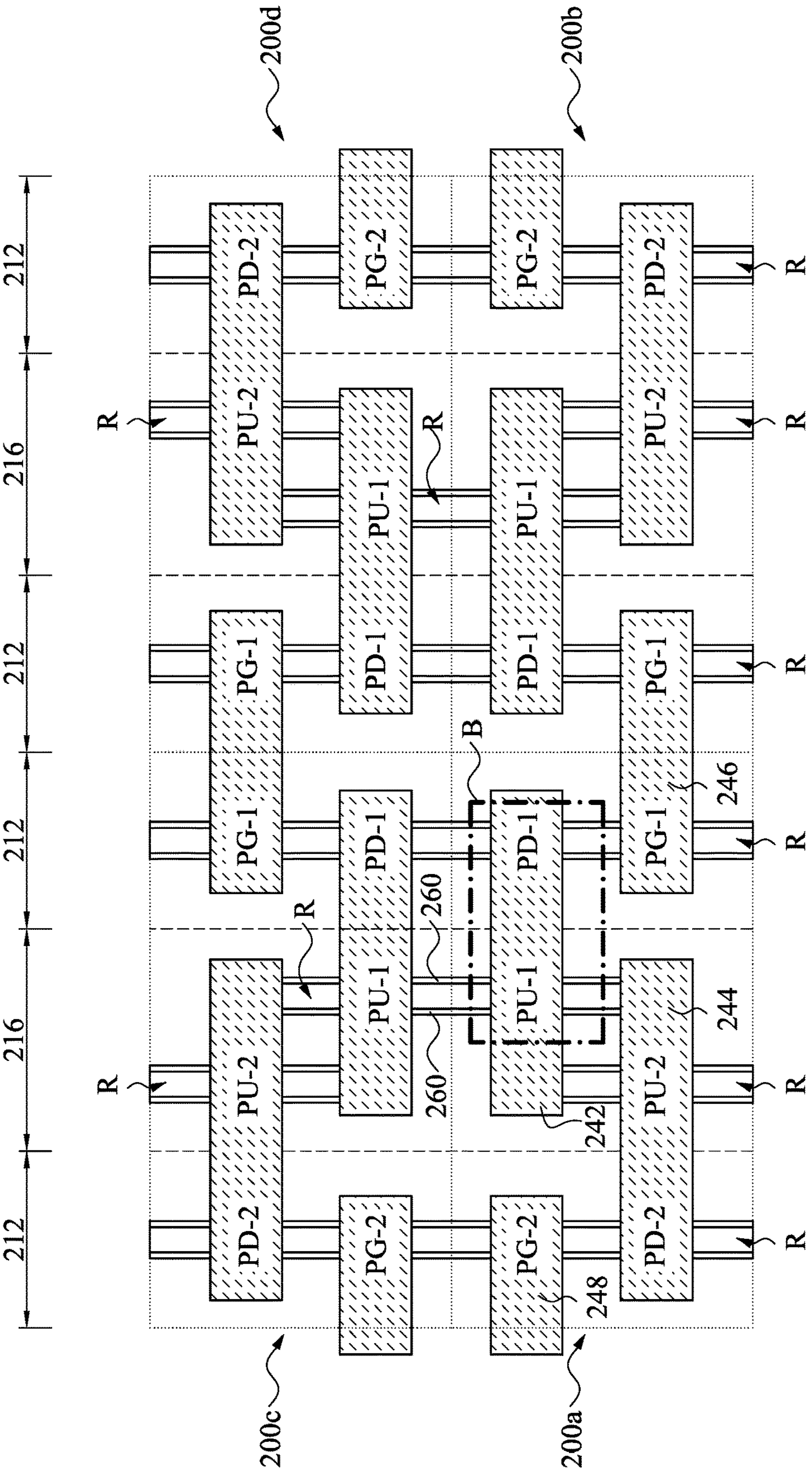
200d
200b
200c
200a
212
216
212
212
216
212
PD-2
PG-2
PG-2
PD-2
PU-2
PU-1
PU-1
PU-2
PG-1
PD-1
PD-1
PG-1
PG-1
PD-1
PD-1
PG-1
PU-2
PU-1
PU-1
PU-2
PD-2
PG-2
PG-2
PD-2
R
B
260
260
242
244
246
248

Fig. 5A

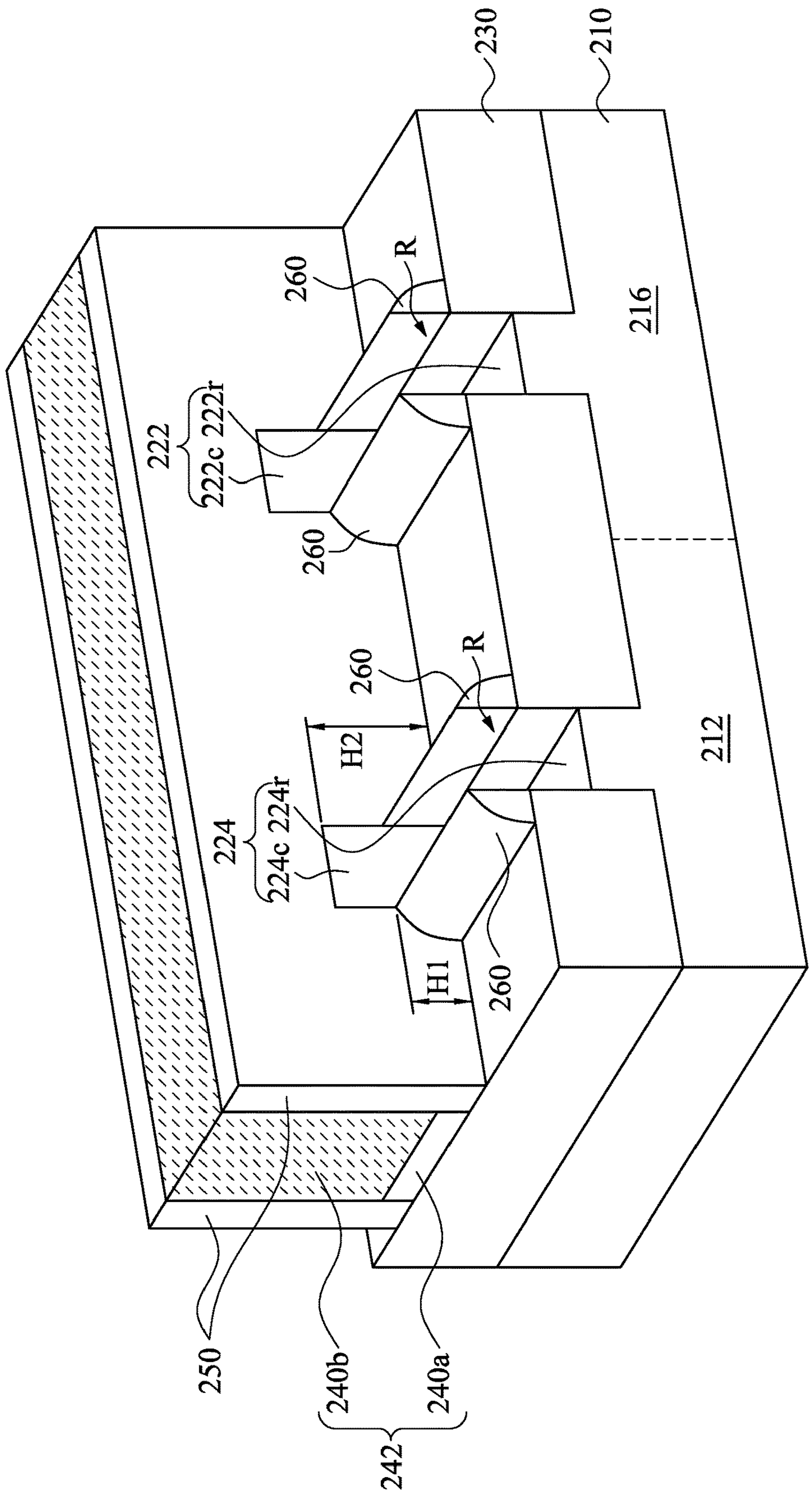
230
210
R
260
216
222
222c
222r
260
R
260
H2
224
224c
224r
212
H1
260
250
240b
240a
242

Fig. 5B

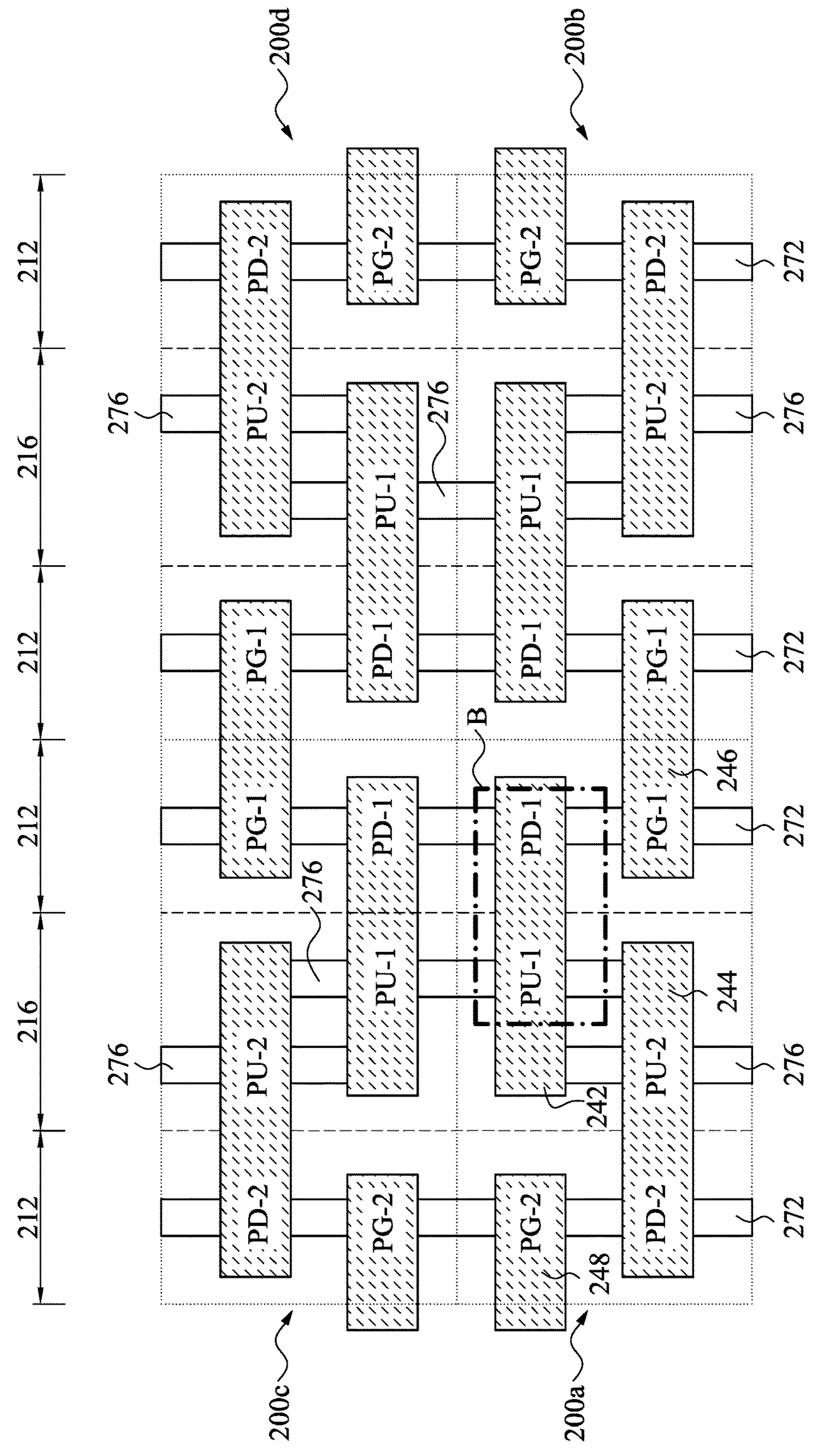
200d
200b
200c
200a
212
216
212
212
216
212
PD-2
PG-2
PU-2
PU-1
PD-1
PG-1
276
272
B
246
244
242
248

Fig. 6A

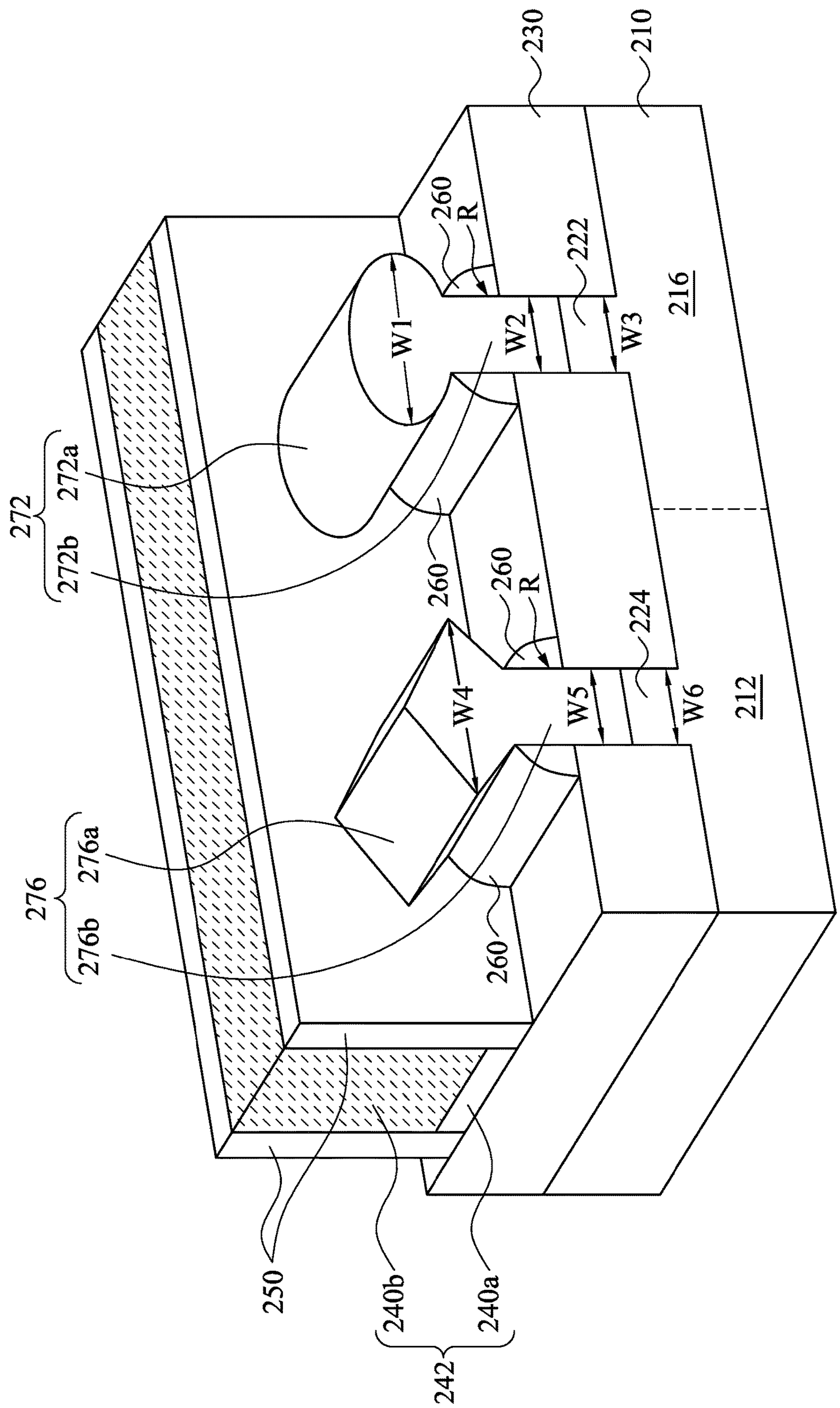
230
210
260
R
222
216
W1
W2
W3
272
272a
272b
260
260
R
224
W4
W5
W6
212
276
276a
276b
260
250
240b
240a
242

Fig. 6B

SEMICONDUCTOR DEVICE, STATIC RANDOM ACCESS MEMORY CELL AND MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

PRIORITY CLAIM AND CROSS-REFERENCE

The present application is a divisional of the application Ser. No. 14/938,311, filed on Nov. 11, 2015, which are incorporated herein by reference in their entireties.

BACKGROUND

Static Random Access Memory (Static RAM or SRAM) is a semiconductor memory that retains data in a static form as long as the memory has power. SRAM is faster and more reliable than the more common dynamic RAM (DRAM). The term static is derived from the fact that it doesn't need to be refreshed like DRAM. SRAM is used for a computer's cache memory and as part of the random access memory digital-to-analog converter on a video card.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** is a circuit diagram of a six transistor (6T) SRAM cell.

FIGS. **2**A to **6**A are top views of a method for manufacturing an SRAM device at various stages in accordance with some embodiments of the present disclosure.

FIGS. **2**B to **6**B are perspective views of area B of FIGS. **2**A to **6**A.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90

degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

The present disclosure will be described with respect to embodiments in a specific context, a static random-access memory (SRAM) formed of fin field effect transistors (FinFETs). The embodiments of the disclosure may also be applied, however, to a variety of semiconductor devices. Various embodiments will be explained in detail with reference to the accompanying drawings.

Static random-access memory (SRAM) is a type of volatile semiconductor memory that uses bistable latching circuitry to store each bit. Each bit in an SRAM is stored on four transistors (PU-**1**, PU-**2**, PD-**1**, and PD-**2**) that form two cross-coupled inverters. This memory cell has two stable states which are used to denote **0** and **1**. Two additional access transistors (PG-**1** and PG-**2**) are electrically connected to the two cross-coupled inventers and serve to control the access to a storage cell during read and write operations.

FIG. **1** is a circuit diagram of a six transistor (6T) SRAM cell. The SRAM cell **100** includes a first inverter **102** formed by a pull-up transistor PU-**1** and a pull-down transistor PD-**1**. The SRAM cell **100** further includes a second inverter **104** formed by a pull-up transistor PU-**2** and a pull-down transistor PD-**2**. Furthermore, both the first inverter **102** and second inverter **104** are coupled between a voltage bus Vdd and a ground potential Vss. In some embodiment, the pull-up transistor PU-**1** and PU-**2** can be p-type transistors while the pull-down transistors PD-**1** and PD-**2** can be n-type transistors, and the claimed scope of the present disclosure is not limited in this respect.

In FIG. **1**, the first inverter **102** and the second inverter **104** are cross-coupled. That is, the first inverter **102** has an input connected to the output of the second inverter **104**. Likewise, the second inverter **104** has an input connected to the output of the first inverter **102**. The output of the first inverter **102** is referred to as a storage node **103**. Likewise, the output of the second inverter **104** is referred to as a storage node **105**. In a normal operating mode, the storage node **103** is in the opposite logic state as the storage node **105**. By employing the two cross-coupled inverters, the SRAM cell **100** can hold the data using a latched structure so that the stored data will not be lost without applying a refresh cycle as long as power is supplied through Vdd.

In an SRAM device using the 6T SRAM cells, the cells are arranged in rows and columns. The columns of the SRAM array are formed by a bit line pairs, namely a first bit line BL and a second bit line BLB. The cells of the SRAM device are disposed between the respective bit line pairs. As shown in FIG. **1**, the SRAM cell **100** is placed between the bit line BL and the bit line BLB.

In FIG. **1**, the SRAM cell **100** further includes a first pass-gate transistor PG-**1** connected between the bit line BL and the output **103** of the first inverter **102**. The SRAM cell **100** further includes a second pass-gate transistor PG-**2** connected between the bit line BLB and the output **105** of the second inverter **104**. The gates of the first pass-gate transistor PG-**1** and the second pass-gate transistor PG-**2** are connected to a word line WL, which connects SRAM cells in a row of the SRAM array.

In operation, if the pass-gate transistors PG-**1** and PG-**2** are inactive, the SRAM cell **100** will maintain the complementary values at storage nodes **103** and **105** indefinitely as long as power is provided through Vdd. This is so because each inverter of the pair of cross coupled inverters drives the input of the other, thereby maintaining the voltages at the storage nodes. This situation will remain stable until the power is removed from the SRAM, or, a write cycle is performed changing the stored data at the storage nodes.

In the circuit diagram of FIG. **1**, the pull-up transistors PU-**1**, PU-**2** are p-type transistors. The pull-down transistors PD-**1**, PD-**2**, and the pass-gate transistors PG-**1**, PG-**2** are n-type transistors. According to various embodiments, the pull-up transistors PU-**1**, PU-**2**, the pull-down transistors PD-**1**, PD-**2**, and the pass-gate transistors PG-**1**, PG-**2** are implemented by FinFETs.

The structure of the SRAM cell **100** in FIG. **1** is described in the context of the 6T-SRAM. One of ordinary skill in the art, however, should understand that features of the various embodiments described herein may be used for forming other types of devices, such as an 8T-SRAM memory device, or memory devices other than SRAMs, such as standard cell, gated diode or ESD (Electrostatic Discharge) devices. Furthermore, embodiments of the present disclosure may be used as stand-alone memory devices, memory devices integrated with other integrated circuitry, or the like.

FIGS. **2**A to **6**A are top views of a method for manufacturing an SRAM device at various stages in accordance with some embodiments of the present disclosure, and FIGS. **2**B to **6**B are perspective views of area B of FIGS. **2**A to **6**A. In FIGS. **2**A to **6**A, a SRAM device including four SRAM cells **200***a*, **200***b*, **200***c*, and **200***d* are illustrated. In some other embodiments, however, the number of the SRAM cells **200***a*, **200***b*, **200***c*, and **200***d* in the SRAM device is not limited in this respect. Reference is made to FIGS. **2**A and **2**B. A substrate **210** is provided. In some embodiments, the substrate **210** may be a semiconductor material and may include known structures including a graded layer or a buried oxide, for example. In some embodiments, the substrate **210** includes bulk silicon that may be undoped or doped (e.g., p-type, n-type, or a combination thereof). Other materials that are suitable for semiconductor device formation may be used. Other materials, such as germanium, quartz, sapphire, and glass could alternatively be used for the substrate **210**. Alternatively, the silicon substrate **210** may be an active layer of a semiconductor-on-insulator (SOI) substrate or a multi-layered structure such as a silicon-germanium layer formed on a bulk silicon layer.

A plurality of p-well regions **212** and a plurality of n-well regions **216** are formed in the substrate **210**. One of the n-well regions **216** is formed between two of the p-well regions **212**. The p-well regions **212** are implanted with P dopant material, such as boron ions, and the n-well regions **216** are implanted with N dopant material such as arsenic ions. During the implantation of the p-well regions **212**, the n-well regions **216** are covered with masks (such as photoresist), and during implantation of the n-well regions **216**, the p-well regions **212** are covered with masks (such as photoresist).

A plurality of semiconductor fins **222**, **224**, **226**, and **228** are formed on the substrate **210**. In greater detail, the semiconductor fins **222** and **226** are formed on the p-well regions **212**, and the semiconductor fins **224** and **228** are formed on the n-well regions **216**. The semiconductor fin **222** is adjacent to the semiconductor fin **224**, and the semiconductor fin **226** is adjacent to the semiconductor fin **228**. In some embodiments, the semiconductor fins **222**, **224**, **226**, and **228** include silicon. It is note that the number of the semiconductor fins **222**, **224**, **226**, and **228** in FIG. **2**A is illustrative, and should not limit the claimed scope of the present disclosure. A person having ordinary skill in the art may select suitable number for the semiconductor fins **222**, **224**, **226**, and **228** according to actual situations.

The semiconductor fins **222**, **224**, **226**, and **228** may be formed, for example, by patterning and etching the substrate **210** using photolithography techniques. In some embodiments, a layer of photoresist material (not shown) is deposited over the substrate **210**. The layer of photoresist material is irradiated (exposed) in accordance with a desired pattern (the semiconductor fins **222**, **224**, **226**, and **228** in this case) and developed to remove a portion of the photoresist material. The remaining photoresist material protects the underlying material from subsequent processing steps, such as etching. It should be noted that other masks, such as an oxide or silicon nitride mask, may also be used in the etching process.

Reference is made to FIGS. **3**A and **3**B. A portion of the semiconductor fins **224** and **228** are removed. For example, a photomask (not shown) containing patterns for both the semiconductor fins **224** and **228** are used to protect portions of the semiconductor fins **224** and **228** to be kept. Exposed portions of both the semiconductor fins **224** and **228** are then etched at the same time.

Subsequently, a plurality of isolation structures **230** are formed on the substrate **210**. The isolation structures **230**, which act as a shallow trench isolation (STI) around the semiconductor fins **222**, **224**, **226**, and **228**, may be formed by chemical vapor deposition (CVD) techniques using tetra-ethyl-ortho-silicate (TEOS) and oxygen as a precursor. In some other embodiments, the isolation structures **230** may be formed by implanting ions, such as oxygen, nitrogen, carbon, or the like, into the substrate **210**. In yet some other embodiments, the isolation structures **230** are insulator layers of a SOI wafer.

Reference is made to FIGS. **4**A and **4**B. A plurality of gate stacks **242**, **244**, **246**, and **248** are formed on portions of the semiconductor fins **222**, **224**, **226**, and **228** and expose another portions of the semiconductor fins **222**, **224**, **226**, and **228**. In greater detail, the gate stack **242** is formed on portions of the semiconductor fins **222**, **224**, and further on a portion of the semiconductor fin **228** in some embodiments; the gate stack **244** is formed on portions of the semiconductor fins **226** and **228**, and further on a portion of the semiconductor fin **224** in some embodiments; the gate stack **246** is formed on portions of the semiconductor fins **222**, and the gate stack **248** is formed on portions of the semiconductor fins **226**.

As shown in FIG. **4**B, at least one of the gate stacks **242**, **244**, **246**, and **248** includes a gate insulator layer **240***a* and a gate electrode layer **240***b*. The gate insulator layer **240***a* is disposed between the gate electrode layer **240***b* and the substrate **210**, and is formed on the semiconductor fins **222**, **224**, **226**, and **228**. The gate insulator layer **240***a*, which prevents electron depletion, may include, for example, a high-k dielectric material such as metal oxides, metal nitrides, metal silicates, transition metal-oxides, transition metal-nitrides, transition metal-silicates, oxynitrides of metals, metal aluminates, zirconium silicate, zirconium aluminate, or combinations thereof. Some embodiments may include hafnium oxide (HfO_2), hafnium silicon oxide (HfSiO), hafnium silicon oxynitride (HfSiON), hafnium tantalum oxide (HfTaO), hafnium titanium oxide (HfTiO), hafnium zirconium oxide (HfZrO), lanthanum oxide (LaO), zirconium oxide (ZrO), titanium oxide (TiO), tantalum oxide (Ta_2O_5), yttrium oxide (Y_2O_3), strontium titanium oxide ($SrTiO_3$, STO), barium titanium oxide ($BaTiO_3$, BTO), barium zirconium oxide (BaZrO), hafnium lanthanum oxide (HfLaO), lanthanum silicon oxide (LaSiO), aluminum silicon oxide (AlSiO), aluminum oxide (Al_2O_3), silicon nitride (Si_3N_4), oxynitrides (SiON), and combinations thereof. The gate insulator layer **240***a* may have a multilayer structure such as one layer of silicon oxide (e.g., interfacial layer) and another layer of high-k material.

The gate insulator layer **240***b* may be formed using chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), thermal oxide, ozone oxidation, other suitable processes, or combinations thereof. The gate electrode layers **240***b* are formed over the substrate **210** to cover the gate insulator layers **240***a* and the portions of the semiconductor fins **222**, **224**, **226**, and **228**. In some embodiments, the gate electrode layer **240***b* includes a semiconductor material such as polysilicon, amorphous silicon, or the like. The gate electrode layer **240***b* may be deposited doped or undoped. For example, in some embodiments, the gate electrode layer **240***b* includes polysilicon deposited undoped by low-pressure chemical vapor deposition (LPCVD). The polysilicon may also be deposited, for example, by furnace deposition of an in-situ doped polysilicon. Alternatively, the gate electrode layer **240***b* may include a polysilicon metal alloy or a metal gate including metals such as tungsten (W), nickel (Ni), aluminum (Al), tantalum (Ta), titanium (Ti), or any combination thereof.

In FIG. **4**B, a plurality of gate spacers **250** are formed over the substrate **210** and along the side of the gate stacks **242**, **244**, **246**, and **248**. For clarity, the gate spacers **250** are illustrated in FIG. **4**B and are omitted in FIG. **4**A. In some embodiments, the gate spacers **250** may include silicon oxide, silicon nitride, silicon oxy-nitride, or other suitable material. The gate spacers **250** may include a single layer or multilayer structure. A blanket layer of the gate spacers **250** may be formed by CVD, PVD, ALD, or other suitable technique. Then, an anisotropic etching is performed on the blanket layer to form a pair of the gate spacers **250** on two sides of the gate stacks **242**, **244**, **246**, and **248**. In some embodiments, the gate spacers **250** are used to offset subsequently formed doped regions, such as source/drain regions. The gate spacers **250** may further be used for designing or modifying the source/drain region (junction) profile.

A plurality of dielectric fin sidewall structures **260** are formed on opposite sides of the semiconductor fins **222**, **224**, **226**, and **228**. The dielectric fin sidewall structures **260** are formed along the semiconductor fins **222**, **224**, **226**, and **228**. The dielectric fin sidewall structures **260** may include a dielectric material such as silicon oxide. Alternatively, the dielectric fin sidewall structures **260** may include silicon nitride, SiC, SiON, or combinations thereof. The formation methods for the dielectric fin sidewall structures **260** may include depositing a dielectric material over the semiconductor fins **222**, **224**, **226**, and **228**, and then anisotropically etching back the dielectric material. The etching back process may include a multiple-step etching to gain etch selectivity, flexibility and desired overetch control.

In some embodiments, the gate spacers **250** and the dielectric fin sidewall structures **260** may be formed in the same manufacturing process. For example, a blanket layer of dielectric layer may be formed to cover the gate stacks **242**, **244**, **246**, and **248** and the semiconductor fins **222**, **224**, **226**, and **228** by CVD, PVD, ALD, or other suitable technique. Then, an etching process is performed on the blanket layer to form the gate spacers **250** on opposite sides of the gate stacks **242**, **244**, **246**, and **248** and form the dielectric fin sidewall structures **260** on opposite sides of the semiconductor fins **222**, **224**, **226**, and **228**. However, in some other embodiments, the gate spacers **250** and the dielectric fin sidewall structures **260** can be formed in different manufacturing processes.

In FIG. **4**A, the semiconductor fin **222** and the gate stack **242** form a pull-down transistor PD-**1**, and the semiconductor fin **224** and the gate stack **242** form a pull-up transistor PU-**1**. In other words, the pull-down transistor PD-**1** and the pull-up transistor PU-**1** share the gate stack **242**. The semiconductor fin **226** and the gate stack **244** form another pull-down transistor PD-**2**, and the semiconductor fin **228** and the gate stack **244** form another pull-up transistor PU-**2**. In other words, the pull-down transistor PD-**2** and the pull-up transistor PU-**2** share the gate stack **244**. Moreover, the semiconductor fin **222** and the gate stack **246** form a pass-gate transistor PG-**1**. In other words, the pass-gate transistor PG-**1** and the pull-down transistor PD-**1** share the semiconductor fin **222**. The semiconductor fin **226** and the gate stack **248** form another pass-gate transistor PG-**2**. In other words, the pass-gate transistor PG-**2** and the pull-down transistor PD-**2** share the semiconductor fin **226**. Therefore, the SRAM cell **200***a* is a six-transistor (6T) SRAM. One of ordinary skill in the art, however, should understand that features of the various embodiments described herein may be used for forming other types of devices, such as an 8T-SRAM memory device.

In some embodiments, the number of the semiconductor fins **222** can be plural, and/or the number of the semiconductor fins **226** can be plural. Therefore, the pull-down transistors PD-**1**, PD-**2**, and the pass-gate transistors PG-**1**, PG-**2** have a plurality of semiconductor fins per transistor, and the pull-up transistors PU-**1** and PU-**2** have one semiconductor fin per transistor, and the claimed scope is not limited in this respect.

In FIG. **4**A, when the SRAM cells **200***a*-**200***d* are arranged together to form an array (the SRAM device herein), the cell layouts may be flipped or rotated to enable higher packing densities. Often by flipping the cell over a cell boundary or axis and placing the flipped cell adjacent the original cell, common nodes and connections can be combined to increase packing density. For example, the SRAM cells **200***a*-**200***d* are mirror images and in rotated images of each other. Specifically, the SRAM cells **200***a* and **200***b* are mirror images across a Y-axis, as is SRAM cells **200***c* and **200***d*. The cells **200***a* and **200***c* are mirror images across an X-axis, as is SRAM cells **200***b* and **200***d*. Further, the diagonal SRAM cells (the SRAM cells **200***a* and **200***d*; the SRAM cells **200***b* and **200***c*) are rotated images of each other at 180 degrees.

Reference is made to FIGS. **5**A and **5**B. A portion of the semiconductor fins **222**, **224**, **226**, and **228** exposed both by the gate stacks **242**, **244**, **246**, and **248** and the gate spacers **250** are partially removed (or partially recessed) to form recesses R in the semiconductor fins **222**, **224**, **226**, and **228**. In FIGS. **5**A and **5**B, the recesses R are formed with the dielectric fin sidewall structures **260** as its upper portion. In some embodiments, sidewalls of the recesses R are substantially and vertical parallel to each other. In some other embodiments, the recesses R are formed with a non-vertical parallel profile.

In FIG. **5**B, the semiconductor fin **222** includes at least one recessed portion **222***r* and at least one channel portion **222***c*. The recess R is formed on the recessed portion **222***r*, and the gate stack **242** covers the channel portion **222***c*. The semiconductor fin **224** includes at least one recessed portion **224***r* and at least one channel portion **224***c*. The recess R is formed on the recessed portion **224***r*, and the gate stack **242** covers the channel portion **224***c*. Also, the semiconductor fins **226** and **228** (see FIG. **4**A) individually include at least one recessed portion and at least one channel portion (not shown). Since the recessed portions and the channel portions of the semiconductor fins **226** and **228** have similar configurations to the recessed portions **222***r* and **224***r* and the channel portions **222***c* and **224***c*, and therefore, a description in this regard will not be repeated hereinafter.

At least one of the dielectric fin sidewall structures **260** has a height H**1**, and at least one of the semiconductor fins **222**, **224**, **226**, and **228** has a height H**2** protruding from the isolation structures **230** (i.e., the channel portions **222***c*, **224***c*). The height H**1** is lower than the height H**2**. In some embodiments, the height H**1** and the height H**2** satisfies the condition: $0.1 \leq (H1/H2) \leq 0.5$, and the claimed scope is not limited in this respect. The height H**1** of the dielectric fin sidewall structures **260** can be tuned, for example, by etching, to adjust the profile of the epitaxy structures **272** and **276** (see FIGS. **6**A and **6**B) formed thereon.

The recessing process may include dry etching process, wet etching process, and/or combination thereof. The recessing process may also include a selective wet etch or a selective dry etch. A wet etching solution includes a tetramethylammonium hydroxide (TMAH), a $HF/HNO_3/CH_3COOH$ solution, or other suitable solution. The dry and wet etching processes have etching parameters that can be tuned, such as etchants used, etching temperature, etching solution concentration, etching pressure, source power, RF bias voltage, RF bias power, etchant flow rate, and other suitable parameters. For example, a wet etching solution may include NH_4OH, KOH (potassium hydroxide), HF (hydrofluoric acid), TMAH (tetramethylammonium hydroxide), other suitable wet etching solutions, or combinations thereof. Dry etching processes include a biased plasma etching process that uses a chlorine-based chemistry. Other dry etchant gasses include CF_4, NF_3, SF_6, and He. Dry etching may also be performed anisotropically using such mechanisms as DRIE (deep reactive-ion etching).

Reference is made to FIGS. **6**A and **6**B. A plurality of epitaxy structures **272** are respectively formed in the recesses R of the semiconductor fins **222** and **226** (see FIG. **4**A), and a plurality of epitaxy structures **276** are respectively formed in the recesses R of the semiconductor fins **224** and **228** (see FIG. **4**A). The epitaxy structure **272** is separated from the adjacent epitaxy structure **276**. The epitaxy structures **272** and **276** protrude from the recesses R. The epitaxy structures **272** can be n-type epitaxy structures, and the epitaxy structures **276** can be p-type epitaxy structures. The epitaxy structures **272** and **276** may be formed using one or more epitaxy or epitaxial (epi) processes, such that Si features, SiGe features, and/or other suitable features can be formed in a crystalline state on the semiconductor fins **222**, **224**, **226**, and **228**. In some embodiments, lattice constants of the epitaxy structures **272** and **276** are different from lattice constants of the semiconductor fins **222**, **224**, **226**, and **228**, and the epitaxy structures **272** and **276** are strained or stressed to enable carrier mobility of the SRAM device and enhance the device performance. The epitaxy structures **272** and **276** may include semiconductor material such as germanium (Ge) or silicon (Si); or compound semiconductor materials, such as gallium arsenide (GaAs), aluminum gallium arsenide (AlGaAs), silicon germanium (SiGe), silicon carbide (SiC), or gallium arsenide phosphide (GaAsP).

In some embodiments, the epitaxy structures **272** and **276** are formed in different epitaxy processes. The epitaxy structures **272** may include SiP, SiC, SiPC, Si, III-V compound semiconductor materials or combinations thereof, and the epitaxy structures **276** may include SiGe, SiGeC, Ge, Si, III-V compound semiconductor materials, or combinations thereof. During the formation of the epitaxy structures **272**, n-type impurities such as phosphorous or arsenic may be doped with the proceeding of the epitaxy. For example, when the epitaxy structure **272** includes SiC or Si, n-type impurities are doped. Moreover, during the formation of the epitaxy structures **276**, p-type impurities such as boron or BF_2 may be doped with the proceeding of the epitaxy. For example, when the epitaxy structure **276** includes SiGe, p-type impurities are doped. The epitaxy processes include CVD deposition techniques (e.g., vapor-phase epitaxy (VPE) and/or ultra-high vacuum CVD (UHV-CVD)), molecular beam epitaxy, and/or other suitable processes. The epitaxy process may use gaseous and/or liquid precursors, which interact with the composition of the semiconductor fins **222**, **224**, **226**, and **228** (e.g., silicon). Thus, a strained channel can be achieved to increase carrier mobility and enhance device performance. The epitaxy structures **272** and **276** may be in-situ doped. If the epitaxy structures **272** and **276** are not in-situ doped, a second implantation process (i.e., a junction implant process) is performed to dope the epitaxy structures **272** and **276**. One or more annealing processes may be performed to activate the epitaxy structures **272** and **276**. The annealing processes include rapid thermal annealing (RTA) and/or laser annealing processes.

In some embodiments, the epitaxy structure **272** has a top portion **272***a* and a body portion **272***b* disposed between the top portion **272***a* and the substrate **210**. The top portion **272***a* has a width W**1**, and the body portion **270***b* has a width W**2** shorter than the width W**1**. At least one of the semiconductor fins **222** and **226** has a width W**3** substantially the same as the width W**2**. The dielectric fin sidewall structures **260** are disposed on opposite sides of the body portions **272***b* of the epitaxy structures **272**, and the top portion **272***a* of the epitaxy structures **272** is disposed on the dielectric fin sidewall structures **260**.

Moreover, the epitaxy structure **276** has a top portion **276***a* and a body portion **276***b* disposed between the top portion **276***a* and the substrate **210**. The top portion **276***a* has a width W**4**, and the body portion **276***b* has a width W**5** shorter than the width W**4**. At least one of the semiconductor fins **222** and **226** has a width W**6** substantially the same as the width W**5**. The dielectric fin sidewall structures **260** are disposed on opposite sides of the body portions **276***b* of the epitaxy structures **276**, and the top portion **276***a* of the epitaxy structures **276** is disposed on the dielectric fin sidewall structures **260**.

In some embodiments, the epitaxy structures **272** and **276** have different shapes. The top portions **272***a* of the epitaxy structures **272** can have at least one substantially facet surface presented above the dielectric fin sidewall structures **260**, and the top portions **276***a* of the epitaxy structures **276** can have at least one non-facet (or round) surface presented above the dielectric fin sidewall structures **260**, and the claimed scope is not limited in this respect.

In FIG. **6**A, the semiconductor fin **222** (see FIG. **4**A), the epitaxy structure **272** formed thereon, the dielectric fin sidewall structures **260** formed on opposite sides of the epitaxy structure **272**, and the gate stack **242** together form the pull-down transistor PD-**1**, where the semiconductor fin **222** and the epitaxy structure **272** serve as a source/drain of the pull-down transistor PD-**1**. The semiconductor fin **224** (see FIG. **4**A), the epitaxy structure **276** formed thereon, the dielectric fin sidewall structures **260** formed on opposite sides of the epitaxy structure **276**, and the gate stack **242** together form the pull-up transistor PU-**1**, where the semiconductor fin **224** and the epitaxy structure **276** serve as a source/drain of the pull-up transistor PU-**1**. The semiconductor fin **226** (see FIG. **4**A), the epitaxy structure **272** formed thereon, the dielectric fin sidewall structures **260** formed on opposite sides of the epitaxy structure **272**, and the gate stack **244** together form the pull-down transistor PD-**2**, where the semiconductor fin **226** and the epitaxy structure **272** serve as a source/drain of the pull-down transistor PD-**2**. The semiconductor fin **228** (see FIG. **4**A), the epitaxy structure **276** formed thereon, the dielectric fin sidewall structures **260** formed on opposite sides of the epitaxy structure **276**, and the gate stack **244** together form the pull-up transistor PU-**2**, where the semiconductor fin **228** and the epitaxy structure **276** serve as a source/drain of the pull-up transistor PU-**2**. The semiconductor fin **222**, the epitaxy structure **272** formed thereon, the dielectric fin sidewall structures **260** formed on opposite sides of the epitaxy structure **272**, and the gate stack **246** together form the pass-gate transistor PG-**1**, where the semiconductor fin **222** and the epitaxy structure **272** serve as a source/drain of the pass-gate transistor PG-**1**. The semiconductor fin **226**, the epitaxy structure **272** formed thereon, the dielectric fin sidewall structures **260** formed on opposite sides of the epitaxy structure **272**, and the gate stack **248** together form the pass-gate transistor PG-**2**, where the semiconductor fin **226** and the epitaxy structure **272** serve as a source/drain of the pass-gate transistor PG-**2**. Therefore, the SRAM cell **200***a* is a six-transistor (6T) SRAM. One of ordinary skill in the art, however, should understand that features of the various embodiments described herein may be used for forming other types of devices, such as an 8T-SRAM memory device.

According to the aforementioned embodiments, since the dielectric fin sidewall structures are disposed on opposite sides of at least one of the semiconductor fins, the formation of the epitaxy structures can be tuned by the dielectric fin sidewall structures. In greater detail, the epitaxy growth of the epitaxy structures extends both vertically and laterally. The lateral epitaxy growth will enlarge the dimension of the epitaxy structures and narrow the spacing therebetween. However, the dielectric fin sidewall structures can suppress the lateral epitaxy growth of the epitaxy structures, such that the spaces therebetween can be reduced to prevent the epitaxy structures from merging together. Hence, the performance of the SRAM device can be improved.

According to some embodiments, a semiconductor device includes a substrate, a first semiconductor fin, a second semiconductor fin, an n-type epitaxy structure, a p-type epitaxy structure, and a plurality of dielectric fin sidewall structures. The first semiconductor fin is disposed on the substrate. The second semiconductor fin is disposed on the substrate and adjacent to the first semiconductor fin. The n-type epitaxy structure is disposed on the first semiconductor fin. The p-type epitaxy structure is disposed on the second semiconductor fin and separated from the n-type epitaxy structure. The dielectric fin sidewall structures are disposed on opposite sides of at least one of the n-type epitaxy structure and the p-type epitaxy structure.

According to some embodiments, a static random access memory (SRAM) cell includes two pull-up (PU) transistors, two pass-gate (PG) transistors, and two pull-down (PD) transistors. The PU transistors and the PD transistors are configured to form two cross-coupled inverters. The PG transistors are electrically connected to the cross-coupled inverters. At least one of the PU transistors, the PG transistors, and the PD transistors includes a semiconductor fin, an epitaxy structure, and a plurality of dielectric fin sidewall structures. The semiconductor fin includes at least one recessed portion and at least one channel portion. The epitaxy structure is disposed on the recessed portion of the semiconductor fin. The dielectric fin sidewall structures are disposed on opposite sides of the epitaxy structure.

According to some embodiments, a method for manufacturing a semiconductor device includes forming a first semiconductor fin and a second semiconductor fin on a substrate. The first semiconductor fin is adjacent to the second semiconductor fin. A plurality of dielectric fin sidewall structures are formed at least on opposite sides of the first semiconductor fin. The first semiconductor fin is recessed. A first epitaxy structure is formed on the recessed first semiconductor fin. The second semiconductor fin is recessed. A second epitaxy structure is formed on the recessed second semiconductor fin. The first and second epitaxy structures are of different types. A plurality of first dielectric fin sidewall structures are formed on opposite sides of the first semiconductor fin. A plurality of second dielectric fin sidewall structures are formed on opposite sides of the second semiconductor fin. A portion of the first semiconductor fin disposed between the first dielectric fin sidewall structures is recessed. A portion of the second semiconductor fin disposed between the second dielectric fin sidewall structures is recessed. An n-type epitaxy structure is formed on the recessed portion of the first semiconductor fin. A p-type epitaxy structure is formed on the recessed portion of the second semiconductor fin.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A static random access memory (SRAM) cell comprising:

two pull-up (PU) transistors, two pass-gate (PG) transistors, and two pull-down (PD) transistors, wherein the PU transistors and the PD transistors are configured to form two cross-coupled inverters, the PG transistors are electrically connected to the cross-coupled inverters, and at least one of the PU transistors, the PG transistors, and the PD transistors comprises:
- a semiconductor fin comprising at least one channel portion;
- an epitaxy structure over the semiconductor fin;
- at least one isolation structure adjacent to the semiconductor fin; and
- a plurality of dielectric fin sidewall structures on opposite sides of the epitaxy structure and over the isolation structure.

2. The SRAM cell of claim **1**, wherein the epitaxy structure comprises:

a top portion having a first width; and

a body portion between the top portion and the semiconductor fin and having a second width shorter than the first width, wherein the dielectric fin sidewall structures are disposed on opposite sides of the body portion of the epitaxy structure, and the top portion of the epitaxy structure is over the dielectric fin sidewall structures.

3. The SRAM cell of claim 2, wherein the semiconductor fin has a third width substantially the same as the second width of the body portion of the epitaxy structure.

4. The SRAM cell of claim 1, wherein said at least one of the PU transistors, the PG transistors, and the PD transistors further comprises a gate stack covering the channel portion of the semiconductor fin, and a height of one of the dielectric fin sidewall structures is shorter than a height of the channel portion of the semiconductor fin protruding from the isolation structure.

5. The SRAM cell of claim 1, further comprising a substrate having at least one p-well region and at least one n-well region, wherein at least one of the PG transistors and the PD transistors is over the p-well region.

6. The SRAM cell of claim 5, wherein at least one of the PU transistors is over the n-well region.

7. The SRAM cell of claim 1, wherein the epitaxy structure includes a body portion above a top surface of the semiconductor fin and in contact with the dielectric fin sidewall structures.

8. A static random access memory (SRAM) cell comprising:

a substrate;

a first semiconductor fin over the substrate and electrically coupled as a source/drain of a first pull-down (PD) transistor and a source/drain of a first pass-gate (PG) transistor;

a second semiconductor fin over the substrate and electrically coupled as a source/drain of a first pull-up (PU) transistor;

a third semiconductor fin over the substrate and electrically coupled as a source/drain of a second PD transistor and a source/drain of a second PG transistor;

a fourth semiconductor fin over the substrate and electrically coupled as a source/drain of a second PU transistor;

at least one epitaxy structure over at least one of the first semiconductor fin, the second semiconductor fin, the third semiconductor fin, and the fourth semiconductor fin; and

a plurality of dielectric fin sidewall structures on opposite sides of the epitaxy structure.

9. The SRAM cell of claim 8, wherein the epitaxy structure comprises:

a top portion having a first width; and

a body portion between the top portion and said at least one of the first semiconductor fin, the second semiconductor fin, the third semiconductor fin, and the fourth semiconductor fin and having a second width shorter than the first width, wherein the dielectric fin sidewall structures are on opposite sides of the body portion of the epitaxy structure, and the top portion of the epitaxy structure is over the dielectric fin sidewall structures.

10. The SRAM cell of claim 8, wherein the epitaxy structure is an n-type epitaxy structure.

11. The SRAM cell of claim 10, wherein the epitaxy structure has a round surface above the dielectric fin sidewall structures.

12. The SRAM cell of claim 8, wherein the epitaxy structure is a p-type epitaxy structure.

13. The SRAM cell of claim 12, wherein the epitaxy structure has facet surfaces above the dielectric fin sidewall structures.

14. A method for manufacturing a static random access memory (SRAM) cell comprising:

forming two pull-up (PU) transistors, two pass-gate (PG) transistors, and two pull-down (PD) transistors electrically connected to form the SRAM cell, wherein the forming at least one of the PU transistors, the PG transistors, and the PD transistors comprises:

forming a semiconductor fin;

forming a plurality of dielectric fin sidewall structures on opposite sides of the semiconductor fin;

recessing a portion of the semiconductor fin between the dielectric fin sidewall structures;

forming an epitaxy structure on the recessed portion of the semiconductor fin; and

tuning heights of the dielectric fin sidewall structures.

15. The method of claim 14, wherein the epitaxy structure is an n-type epitaxy structure.

16. The method of claim 15, wherein the forming said at least one of the PU transistors, the PG transistors, and the PD transistors further comprises:

doping the n-type epitaxy structure with n-type impurities.

17. The method of claim 14, wherein the epitaxy structure is a p-type epitaxy structure.

18. The method of claim 17, wherein the forming said at least one of the PU transistors, the PG transistors, and the PD transistors further comprises:

doping the p-type epitaxy structure with p-type impurities.

19. The method of claim 14, wherein the heights of the dielectric fin sidewall structures are tuned by performing an etching process.

20. The method of claim 14, wherein forming the epitaxy structure is after forming the plurality of dielectric fin sidewall structures.

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