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(54) **WORDLINE DRIVING CIRCUIT AND MEMORY CELL**

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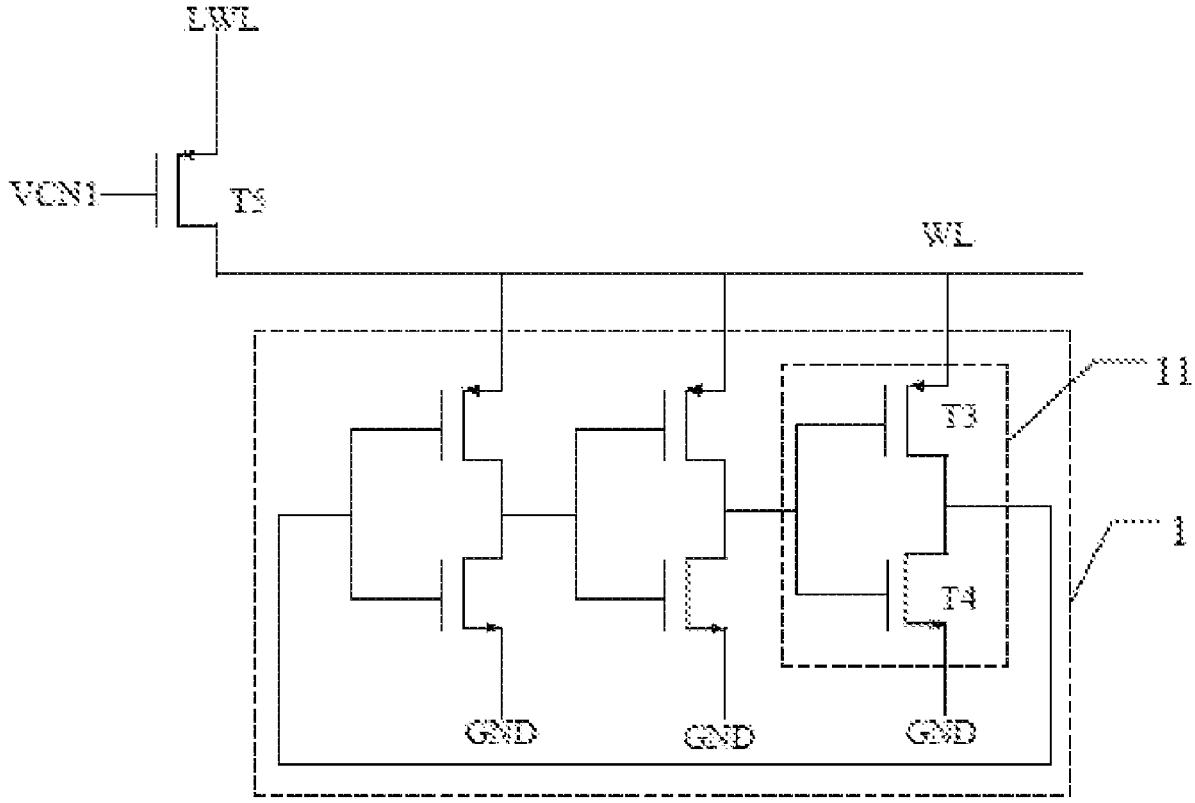
CPC ***G11C 11/4085*** (2013.01); ***G11C 11/4076*** (2013.01); ***H03K 3/0315*** (2013.01); ***G11C 5/06*** (2013.01); ***G11C 11/4074*** (2013.01)

(57) **ABSTRACT**

The present disclosure relates to the field of memory technologies. Various embodiments provide a wordline driving circuit. The wordline driving circuit includes a switching transistor and a ring oscillator. A control terminal of the switching transistor is connected to a first control signal terminal, a first terminal of the switching transistor is connected to a drive voltage terminal, and a second terminal of the switching transistor is connected to a wordline signal terminal. A power terminal of the ring oscillator is connected to the wordline signal terminal, and a ground terminal of the ring oscillator is a ground terminal of the wordline driving circuit. The wordline driving circuit in accordance with the present disclosure can enhance device reliability and service life for the wordline driving circuit.



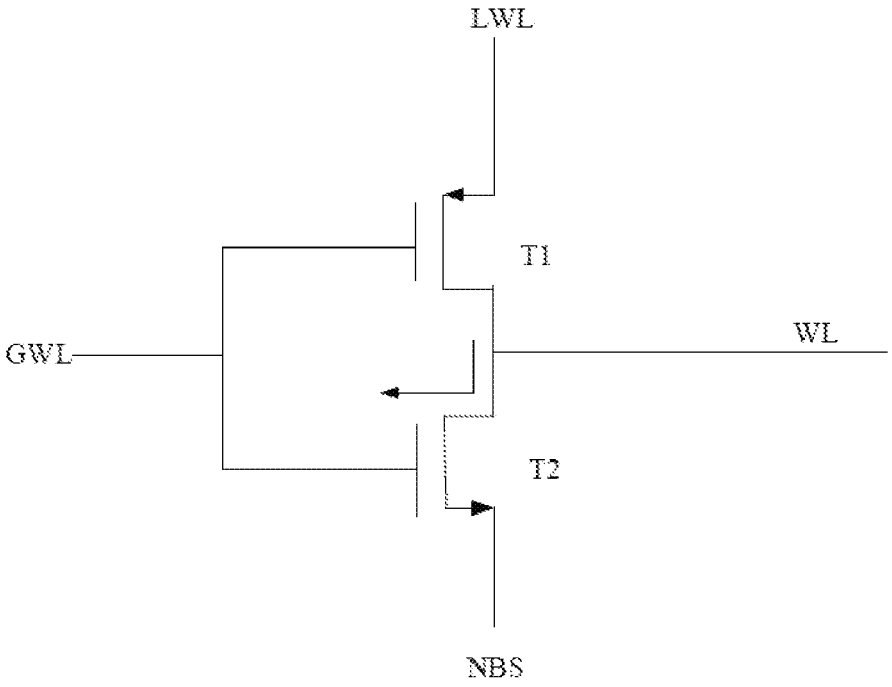


FIG. 1 (Prior Art)

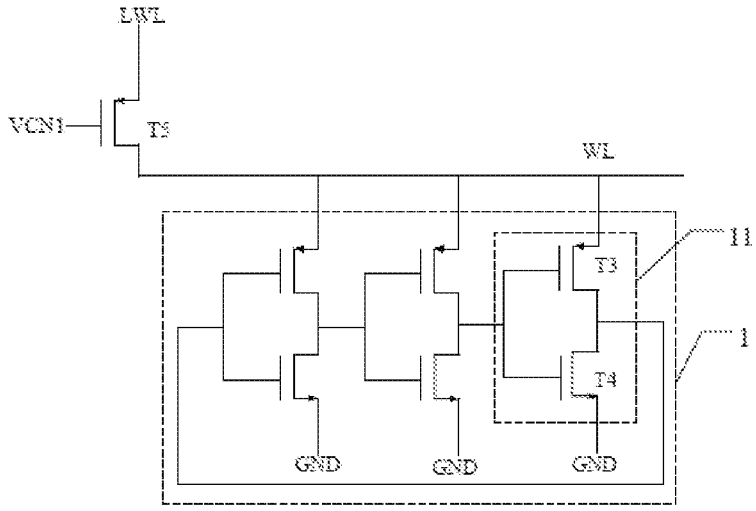


FIG. 2

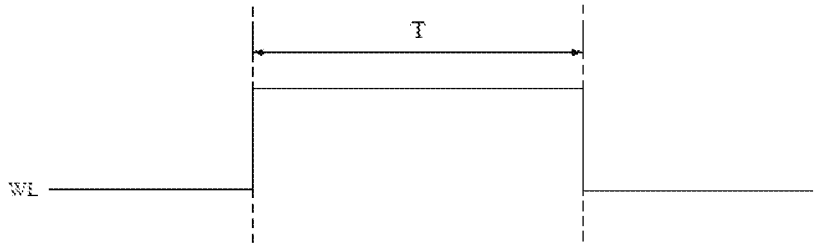


FIG. 3

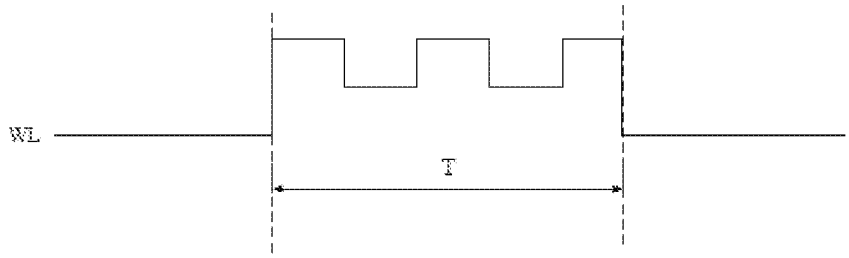


FIG. 4

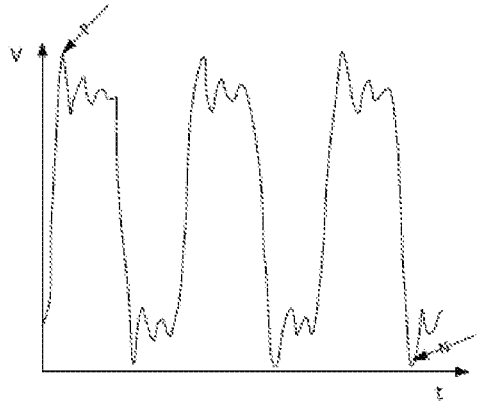


FIG. 5

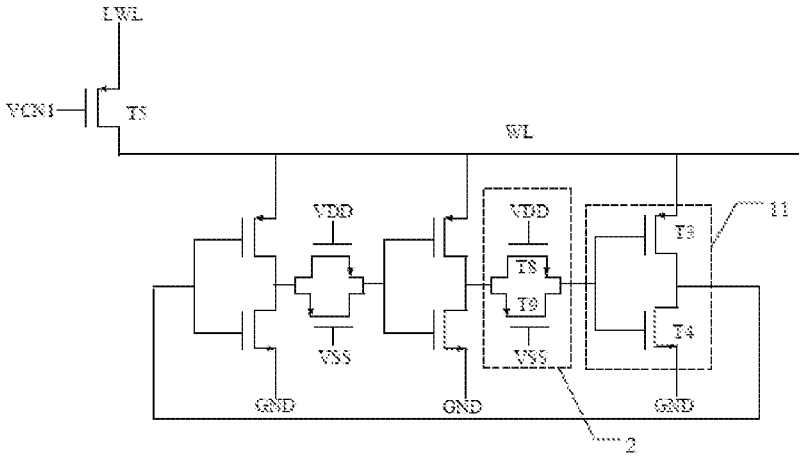

LWL
VCN1
T5
WL
VDD
VSS
T8
T9
T3
T4
11
GND
2

FIG. 6

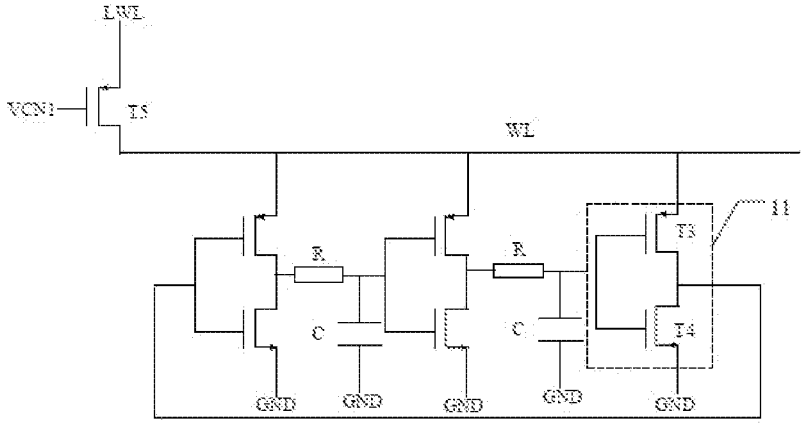

LWL
VCN1
T5
WL
R
C
T3
T4
11
GND

FIG. 7

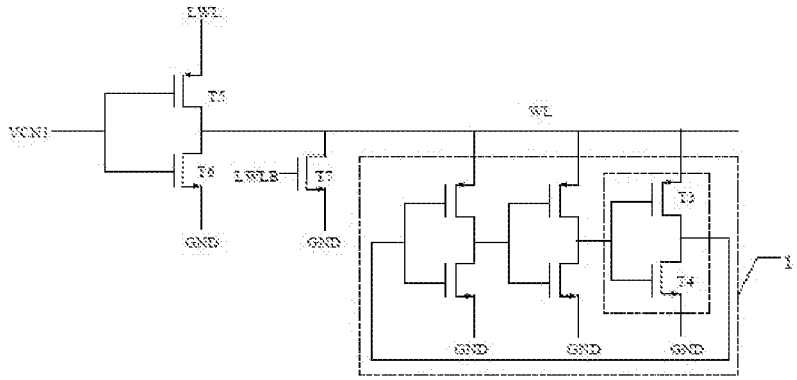


FIG. 8

WORDLINE DRIVING CIRCUIT AND MEMORY CELL

CROSS-REFERENCE

[0001] The present disclosure is a continuation of PCT/CN2019/126394, filed on Dec. 18, 2019, which claims priority to Chinese Patent Application No. 201910720182.2, titled "WORDLINE DRIVING CIRCUIT AND MEMORY CELL" and filed on Aug. 6, 2019, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure relates to the field of memory technologies, and more particularly, to a wordline driving circuit and a memory cell.

BACKGROUND

[0003] A memory cell generally includes a wordline driving circuit, and the wordline driving circuit is configured to output a high level or a low level to a wordline of the memory cell, such that the memory cell stores logic "1" or logic "0".

[0004] In related technologies, as shown in FIG. **1**, a diagram showing a circuit structure of a wordline driving circuit in the related technologies is illustrated. In the related technologies, the wordline driving circuit generally includes a P-type transistor T**1** and an N-type transistor T**2**. A first terminal of the P-type transistor T**1** is connected to a drive voltage terminal LWL, a control terminal of the P-type transistor T**1** is connected to a control signal terminal GWL, and a second terminal of the P-type transistor T**1** is connected to a wordline signal terminal WL. A first terminal of the N-type transistor T**2** is connected to a low-level signal terminal NBS, a control terminal of the N-type transistor T**2** is connected to the control signal terminal GWL, and a second terminal of the N-type transistor T**2** is connected to the wordline signal terminal WL. When the control signal terminal GWL outputs a low-level signal, the P-type transistor T**1** is enabled, and the wordline driving circuit outputs a high-level signal to the wordline signal terminal WL. When the control signal terminal GWL outputs the high-level signal, the N-type transistor T**2** is enabled, and the wordline driving circuit outputs the low-level signal to the wordline signal terminal WL.

[0005] However, with the miniaturization of the size of the memory cell, the thickness of a gate oxide layer of the N-type transistor T**2** in the memory cell is getting thinner and thinner. In the meanwhile, the wordline signal terminal WL is in a higher level state for a long time, such that a GIDL (Gate Induced Drain Leakage, that is, the N-type transistor T**2** may have a leakage current along the direction of arrow as shown in FIG. **1**) phenomenon may be caused to the N-type transistor T**2**, which may have a negative effect on the reliability and service life of the N-type transistor T**2**, and finally may have a negative effect on the reliability and service life of the memory cell.

[0006] It is to be noted that the above information disclosed in this Background section is only for enhancement of understanding of the background of the present disclosure and therefore it may contain information that does not form the related art that is already known to a person of ordinary skill in the art.

SUMMARY

[0007] According to an aspect of the present disclosure, there is provided a wordline driving circuit. The wordline driving circuit includes a switching transistor and a ring oscillator. A control terminal of the switching transistor is connected to a first control signal terminal, a first terminal of the switching transistor is connected to a drive voltage terminal, and a second terminal of the switching transistor is connected to a wordline signal terminal. A power terminal of the ring oscillator is connected to the wordline signal terminal, and a ground terminal of the ring oscillator is a ground terminal of the wordline driving circuit.

[0008] In an exemplary embodiment, the ring oscillator includes a plurality of inverters, and the number of the inverters is greater than or equal to 3 and is an odd number.

[0009] In an exemplary embodiment, the ring oscillator further includes a transmission gate, and the transmission gate is arranged between two adjacent inverters.

[0010] In an exemplary embodiment, the adjacent inverters include a first inverter and a second inverter, and the transmission gate includes a first N-type transistor and a first P-type transistor. A control terminal of the first N-type transistor is connected to a high-level signal terminal, a first terminal of the first N-type transistor is connected to an output terminal of the first inverter, and a second terminal of the first N-type transistor is connected to an input terminal of the second inverter. A control terminal of the first P-type transistor is connected to a low-level signal terminal, a first terminal of the first P-type transistor is connected to the output terminal of the first inverter, and a second terminal of the first P-type transistor is connected to the input terminal of the second inverter.

[0011] In an exemplary embodiment, the switching transistor is a P-type metal-oxide-semiconductor logic (PMOS) transistor.

[0012] In an exemplary embodiment, the wordline driving circuit further includes a second N-type transistor. A control terminal of the second N-type transistor is connected to a second control signal terminal, a first terminal of the second N-type transistor is connected to the wordline signal terminal, and a second terminal of the second N-type transistor is connected to the ground terminal. A signal from the second control signal terminal and a signal from the drive voltage terminal are opposite in phase.

[0013] In an exemplary embodiment, the ring oscillator further includes a delay cell, and the delay cell is arranged between two adjacent inverters.

[0014] In an exemplary embodiment, the delay cell includes a resistor and a capacitor, and the resistor and the capacitor constitute an RC delayer.

[0015] In an exemplary embodiment, the wordline driving circuit further includes a third N-type transistor. A first terminal of the third N-type transistor is connected to the ground terminal, a control terminal of the third N-type transistor is connected to the first control signal terminal, and a second terminal of the third N-type transistor is connected to the wordline signal terminal.

[0016] According to an aspect, there is provided a memory cell, which includes the above-mentioned wordline driving circuit.

[0017] It is to be understood that the above general description and the detailed description below are merely exemplary and explanatory, and do not limit the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The accompanying drawings herein are incorporated in and constitute a part of this specification, illustrate embodiments conforming to the present disclosure and, together with the description, serve to explain the principles of the present disclosure. Apparently, the accompanying drawings in the following description show merely some embodiments of the present disclosure, and persons of ordinary skill in the art may still derive other drawings from these accompanying drawings without creative efforts.

[0019] FIG. **1** is a diagram showing a circuit structure of a wordline driving circuit in related technologies;

[0020] FIG. **2** is a schematic structural diagram of a wordline driving circuit according to an exemplary embodiment of the present disclosure;

[0021] FIG. **3** illustrates a level state of a wordline signal output terminal in the related technologies;

[0022] FIG. **4** illustrates a level state of a wordline signal terminal of the wordline driving circuit according to an exemplary embodiment of the present disclosure;

[0023] FIG. **5** illustrates a timing diagram of a transmission signal from a ring oscillator of the wordline driving circuit according to an exemplary embodiment of the present disclosure;

[0024] FIG. **6** is a schematic structural diagram of the wordline driving circuit according to another exemplary embodiment of the present disclosure;

[0025] FIG. **7** is a schematic structural diagram of the wordline driving circuit according to still another exemplary embodiment of the present disclosure; and

[0026] FIG. **8** is a schematic structural diagram of the wordline driving circuit according to still another exemplary embodiment of the present disclosure.

DETAILED DESCRIPTION

[0027] The exemplary embodiment will now be described more fully with reference to the accompanying drawings. However, the exemplary embodiments can be implemented in a variety of forms and should not be construed as limited to the embodiments set forth herein. Rather, the embodiments are provided so that the present disclosure will be thorough and complete and will fully convey the concepts of exemplary embodiments to those skilled in the art. Throughout the drawings, similar reference signs indicate the same or similar structures, and their detailed description will be omitted.

[0028] Although relative terms such as "above" and "below" are used herein to describe a relative relation between one component and another component of icons, these terms are merely for convenience of this specification, for example, the directions of the examples in the accompanying drawings. It is to be understood that when the apparatus of the icon is turned upside down, components described as "above" will become components described as "below". Other relative terms such as "high", "low", "top", "bottom", "left", "right" and so on also have similar meanings. When a certain structure is "above" other structures, it likely means that a certain structure is integrally formed on other structures, or a certain structure is "directly" arranged on other structures, or a certain structure is "indirectly" arranged on other structures by means of another structure.

[0029] The terms "one", "a" and "the" are intended to mean that there exists one or more elements/constituent parts/etc. The terms "comprising" and "having" are intended to be inclusive and mean that there may be additional elements/constituent parts/etc. other than the listed elements/constituent parts/etc.

[0030] In an exemplary embodiment, a wordline driving circuit is provided. As shown in FIG. **2**, a schematic structural diagram of the wordline driving circuit according to an exemplary embodiment is illustrated. The wordline driving circuit includes a switching transistor T**5** and a ring oscillator **1**. A control terminal of the switching transistor T**5** is connected to a first control signal terminal VCN**1**, a first terminal of the switching transistor T**5** is connected to a drive voltage terminal LWL, and a second terminal of the switching transistor T**5** is connected to a wordline signal terminal WL. A power terminal of the ring oscillator **1** is connected to the wordline signal terminal WL, and a ground terminal GND of the ring oscillator **1** is a ground terminal of the wordline driving circuit. The switching transistor may be a PMOS transistor.

[0031] In this exemplary embodiment, as shown in FIG. **2**, the ring oscillator **1** may comprise a plurality of inverters **11** connected end to end, and the number of the inverters is an odd number. It is to be understood that in other exemplary embodiments, the odd number of inverters may also include other numbers of inverters, for example, 5, 7, 9, and so on. The number of the inverters may determine a ripple frequency and a ripple amplitude of a high level on the wordline signal terminal WL. For example, the larger the number of the inverters is, the smaller the ripple frequency is and the larger the ripple amplitude is, and vice versa.

[0032] Various embodiments can provide a wordline driving circuit. The wordline driving circuit includes a switching transistor and a ring oscillator. A control terminal of the switching transistor is connected to a first control signal terminal, a first terminal of the switching transistor is connected to a drive voltage terminal, and a second terminal of the switching transistor is connected to a wordline signal terminal. A power terminal of the ring oscillator is connected to the wordline signal terminal, and a ground terminal of the ring oscillator is a ground terminal of the wordline driving circuit. When the switching transistor T**5** is enabled, the drive voltage terminal LWL outputs a high-level signal to the wordline signal terminal WL. When the switching transistor T**5** is disabled, the transition of an output signal and an input signal from each inverter **11** in the ring oscillator does not change instantaneously between the logic level "1" and the logic level "0", which is a transition process. Under the action of different voltages of the inverter, a second P-type transistor T**3** and a second N-type transistor T**4** have different enabled states, and have different resistances between the wordline signal terminal WL and the ground terminal GND. As a result, the resistance formed by the ring oscillator may change periodically. Therefore, the ring oscillator can pull down a high level of the wordline signal terminal WL. The wordline driving circuit provided by the present disclosure can fundamentally solve the problem of electric leakage for the N-type transistor T**2** in the related technologies.

[0033] In this exemplary embodiment, as shown in FIG. **2**, the inverter may include an N-type transistor T**4** and a P-type transistor T**3**. A control terminal of the N-type transistor T**4** forms an input terminal of the inverter, a first terminal of the N-type transistor T**4** forms a ground terminal of the ring oscillator, and a second terminal of the N-type transistor T**4** forms an output terminal of the inverter. A

control terminal of the P-type transistor T3 is connected to the control terminal of the N-type transistor T4, a first terminal of the P-type transistor T3 is connected to the wordline signal terminal WL, and a second terminal of the P-type transistor T3 is connected to the second terminal of the N-type transistor T4.

[0034] FIG. **3** illustrates a level state of a wordline signal output terminal in the related technologies. FIG. **4** illustrates a level state of a wordline signal terminal of the wordline driving circuit according to an exemplary embodiment of the present disclosure. In FIG. **1** and FIG. **3**, in a time period T, the control signal terminal GWL outputs a low-level signal, the transistor T1 is enabled, and the wordline signal terminal WL maintains a stable high level. In FIG. **2** and FIG. **4**, in the time period T, the first control signal terminal VCN1 outputs a low-level signal, and the transistor T5 is enabled. Because the resistance formed by the ring oscillator changes periodically, the wordline signal terminal WL outputs a periodically-varying high-level signal. For instance, referring to FIG. **2** and FIG. **4**, when the three inverters are enabled at the same time, the resistance between the wordline signal terminal WL and the ground terminal GND is the smallest, which corresponds to the low-level section of the time period T. When the three inverters are disabled at the same time, it corresponds to the high-level section of the time period T. In the actual circuit, flip of the three inverters is not ideally to be turned on or off at the same time, thus a waveform in the corresponding time period T may likely be a square wave, a sawtooth wave, or a triangle wave, etc. Nevertheless, the waveform in the time period T presents a clear periodicity and has a low level and a high level. The size of the high level is equal to that of the wordline signal terminal WL, and the size of the low level is smaller than that of the wordline signal terminal WL. A specific value of the low level may be set based on level flip time of the inverters, the number of the inverters, the size of a transistor in the inverter, and the delay of a connection line, etc. As can be seen by comparing FIG. **3** and FIG. **4**, when the wordline signal terminal WL is at a high level, a square-wave signal is changed from a constant signal. Comparing FIG. **1** and FIG. **2**, a function of the ring oscillator in FIG. **2** is similar to that of the transistor T2 in FIG. **1**. The ring oscillator in FIG. **2** not only can achieve the transition of the wordline signal terminal WL from a low level to a high level and then to the low level, but also can solve the problem of reliability of the transistor caused when the wordline signal terminal WL is maintained at a high level.

[0035] In this exemplary embodiment, as shown in FIG. **5**, a timing diagram of a transmission signal from the ring oscillator of the wordline driving circuit according to an exemplary embodiment of the present disclosure is illustrated. A pulse signal transmitted by the ring oscillator has positive overshoot and negative overshoot. As shown in FIG. **5**, the position pointed by Arrow P is the position of the positive overshoot, and the position pointed by Arrow N is the position of the negative overshoot. An overshoot voltage exists in the position of the positive overshoot and the position of the negative overshoot, which may have a negative effect on the running stability of the wordline driving circuit.

[0036] As shown in FIG. **6**, a schematic structural diagram of the wordline driving circuit according to still another exemplary embodiment is illustrated. In this exemplary embodiment, the wordline driving circuit may further include a transmission gate **2** arranged between adjacent inverters. The adjacent inverters include a first inverter and a second inverter, and the transmission gate may include a first N-type transistor T8 and a first P-type transistor T9. A control terminal of the first N-type transistor T8 is connected to a high-level signal terminal VDD, a first terminal of the first N-type transistor T8 is connected to an output terminal of the first inverter, and a second terminal of the first N-type transistor T8 is connected to an input terminal of the second inverter. A control terminal of the first P-type transistor T9 is connected to a low-level signal terminal VSS, a first terminal of the first P-type transistor T9 is connected to the output terminal of the first inverter, and a second terminal of the first P-type transistor T9 is connected to the input terminal of the second inverter. The first N-type transistor T8 and the first P-type transistor T9 may form a filter structure, which may avoid the occurrence of the positive overshoot and the negative overshoot in FIG. **6**. In the meanwhile, the period of the pulse signal generated by the oscillator can be controlled by setting sizes of transistors T8 and T9. In the meanwhile, the first N-type transistor has no voltage drop to the high level, and the first P-type transistor has no voltage drop to the low level, and thus signal attenuation may be avoided for the ring oscillator.

[0037] As shown in FIG. **7**, a schematic structural diagram of the wordline driving circuit according to still another exemplary embodiment of the present disclosure is illustrated. In this exemplary embodiment, the ring oscillator may further include a delay cell arranged between two adjacent inverters. The delay cell includes a resistor and a capacitor, and the resistor and the capacitor constitute an RC delayer. The adjacent inverters include a first inverter and a second inverter. An output terminal of the first inverter is connected to an input terminal of the second inverter. The RC filter circuit may include a resistor R and a capacitor C. The resistor R is connected in series between the first inverter and the second inverter. The capacitor C is connected between the input terminal of the second inverter and the ground terminal. This setting may also avoid the occurrence of the positive overshoot and the negative overshoot in FIG. **5**.

[0038] In this exemplary embodiment, as shown in FIG. **8**, a schematic structural diagram of the wordline driving circuit according to still another exemplary embodiment is illustrated. The wordline driving circuit may further include a second N-type transistor T7. A control terminal of the second N-type transistor T7 is connected to a second control signal terminal LWLB, a first terminal of the second N-type transistor T7 is connected to the wordline signal terminal WL, and a second terminal of the second N-type transistor T7 is connected to the ground terminal GND. A signal from the second control signal terminal LWLB and a signal from the drive voltage terminal LWL are opposite in phase. The second N-type transistor T7 is enabled in response to the high level of the second control signal terminal LWLB before the drive voltage terminal LWL is initiated, to set the wordline signal terminal WL at the low level. When the drive voltage terminal LWL is at the high level, the transistor T7 will be disabled, wherein the transistor T7 plays a role in controlling an initial working state of the wordline signal terminal WL.

[0039] In this exemplary embodiment, as shown in FIG. **8**, the wordline driving circuit further includes a third N-type transistor T6. A first terminal of the third N-type transistor

T6 is connected to the ground terminal GND, a control terminal of the third N-type transistor T6 is connected to the first control signal terminal VCN1, and a second terminal of the third N-type transistor T6 is connected to the wordline signal terminal WL. When the wordline signal terminal WL needs to output the low-level signal, the first control signal terminal VCN1 turns to the high level. At this moment, the third N-type transistor T6 is enabled under the action of the first control signal terminal VCN1 to connect the wordline signal terminal WL to the ground terminal GND, such that a reset speed of the wordline signal terminal WL is increased. In the meanwhile, because the voltage of the wordline signal terminal WL may be periodically decreased, the wordline driving circuit can reduce the GIDL generated on the N-type transistor T6 by periodically decreasing the voltage of the wordline signal terminal WL, such that the reliability and service life of the N-type transistor T6 may be increased.

[0040] This exemplary embodiment also provides a memory cell, which includes the above-mentioned wordline driving circuit.

[0041] The memory cell provided by this exemplary embodiment has the same technical features and working principles as the above-mentioned wordline driving circuit, and no detailed description is made here because the above contents have provided a detailed description.

[0042] It is to be appreciated that the present disclosure is not limited the embodiments above and illustrated in the accompanying drawings, and that various modifications and changes can be made without departing from the scope thereof. It is intended that the scope of the present disclosure only be limited by the appended claims.

What is claimed is:

1. A wordline driving circuit, comprising:

a switching transistor comprising:

a control terminal connected to a first control signal terminal,

a first terminal connected to a drive voltage terminal, and

a second terminal connected to a wordline signal terminal; and

a ring oscillator comprising:

a power terminal connected to the wordline signal terminal, and

a ground terminal also being a ground terminal of the wordline driving circuit.

2. The wordline driving circuit according to claim **1**, wherein the ring oscillator comprises inverters, and a quantity of the inverters is greater than or equal to **3** and is an odd number.

3. The wordline driving circuit according to claim **2**, wherein the ring oscillator further comprises a transmission gate, and the transmission gate is arranged between two adjacent inverters.

4. The wordline driving circuit according to claim **3**, wherein the adjacent inverters comprise a first inverter and a second inverter, and the transmission gate comprises:

a first N-type transistor, a control terminal of the first N-type transistor being connected to a high-level signal terminal, a first terminal of the first N-type transistor being connected to an output terminal of the first inverter, and a second terminal of the first N-type transistor being connected to an input terminal of the second inverter; and

a first P-type transistor, a control terminal of the first P-type transistor being connected to a low-level signal terminal, a first terminal of the first P-type transistor being connected to the output terminal of the first inverter, and a second terminal of the first P-type transistor being connected to the input terminal of the second inverter.

5. The wordline driving circuit according to claim **1**, wherein the switching transistor is a P-type metal-oxide-semiconductor logic (PMOS) transistor.

6. The wordline driving circuit according to claim **1**, further comprising:

a second N-type transistor, a control terminal of the second N-type transistor being connected to a second control signal terminal, a first terminal of the second N-type transistor being connected to the wordline signal terminal, and a second terminal of the second N-type transistor being connected to the ground terminal; and, wherein, a signal from the second control signal terminal and a signal from the drive voltage terminal are opposite in phase.

7. The wordline driving circuit according to claim **2**, wherein the ring oscillator further comprises a delay cell, and the delay cell is arranged between two adjacent inverters.

8. The wordline driving circuit according to claim **7**, wherein the delay cell comprises a resistor and a capacitor, and the resistor and the capacitor constitute an RC delayer.

9. The wordline driving circuit according to claim **1**, further comprising:

a third N-type transistor, a first terminal of the third N-type transistor being connected to the ground terminal, a control terminal of the third N-type transistor being connected to the first control signal terminal, and a second terminal of the third N-type transistor being connected to the wordline signal terminal.

10. A memory cell, comprising the wordline driving circuit according to claim **1**.

* * * * *