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(54) **STACKED NANOSHEET TECHNOLOGY WITH UNIFORM VTH CONTROL**

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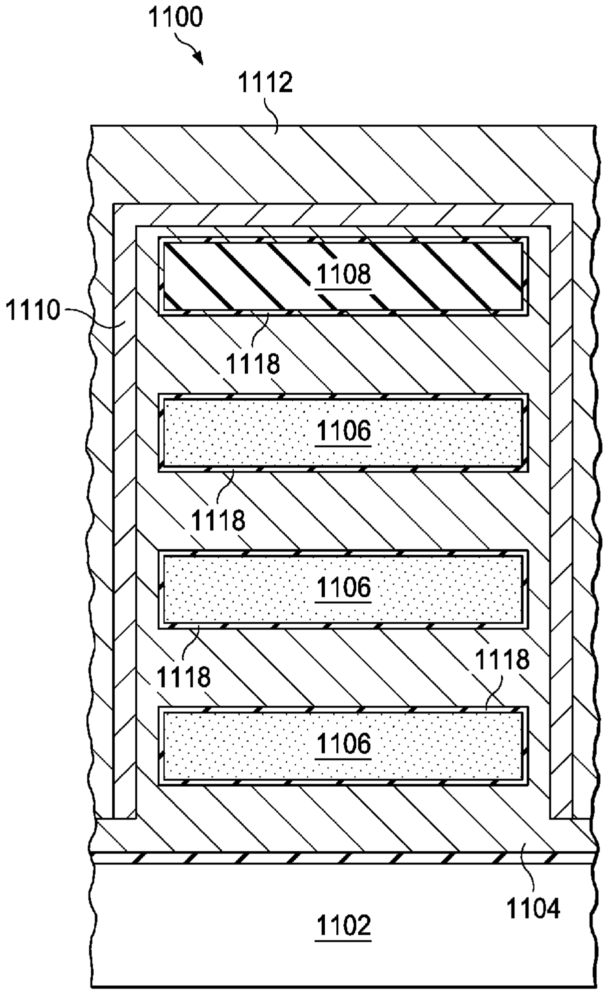
(57) **ABSTRACT**

A stacked nanosheet semiconductor device and method of forming are provided. In an illustrative embodiment, a gate all around (GAA) stacked nanosheet field effect transistor (FET) includes a plurality of stacked semiconductor channel nanosheet layers and a dummy nanosheet layer formed above a top one of the stacked semiconductor channel nanosheet layers, the dummy nanosheet formed from a dielectric material. The GAA stacked nanosheet FET also includes a high dielectric constant (high-k) material formed around each of the plurality of stacked semiconductor channel nanosheet layers and around the dummy nanosheet layer and a first work function (WF) metal formed around the plurality of stacked semiconductor channel nanosheet layers and the dummy nanosheet layer.



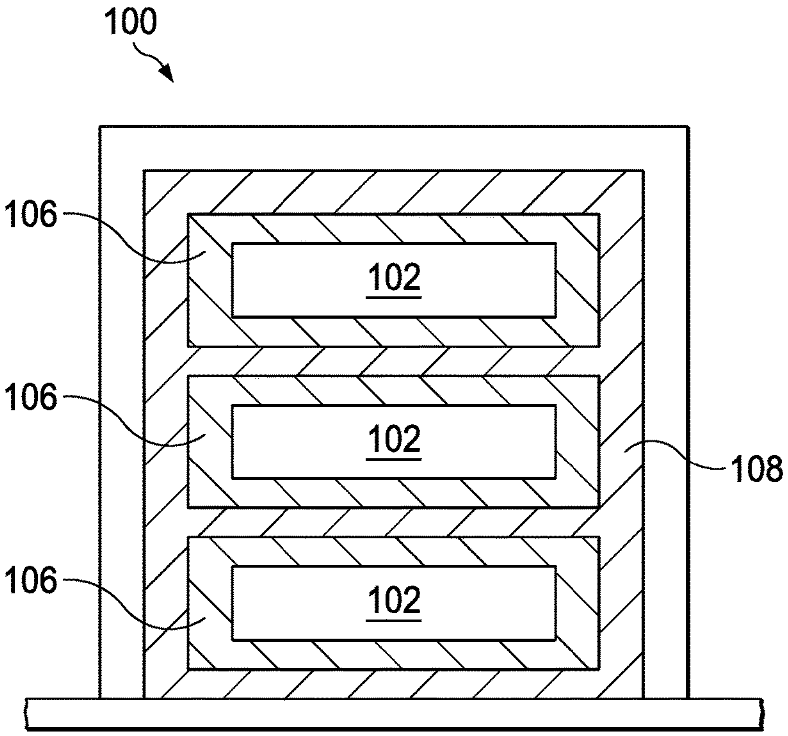


FIG. 1
(PRIOR ART)

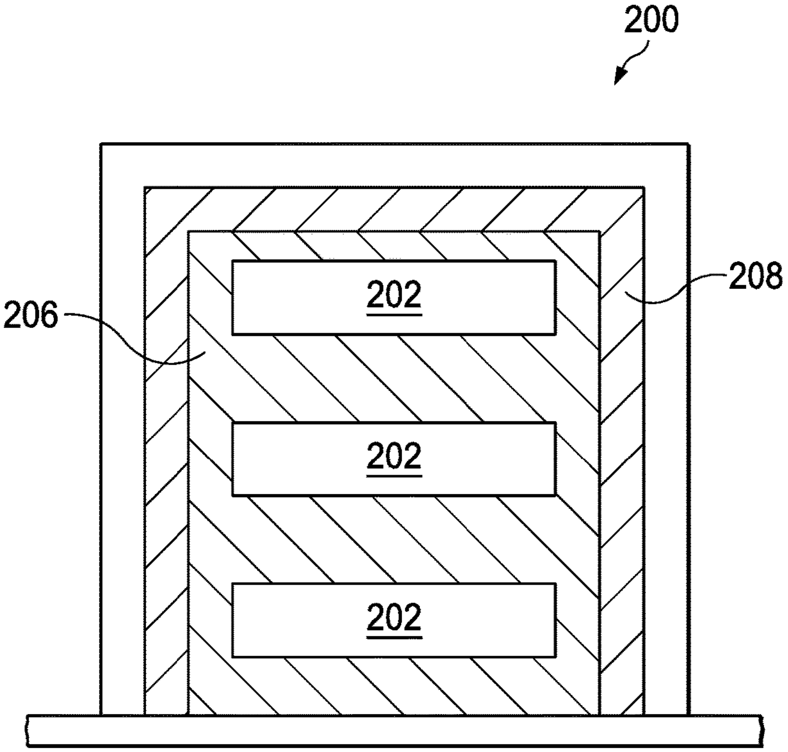


FIG. 2
(PRIOR ART)

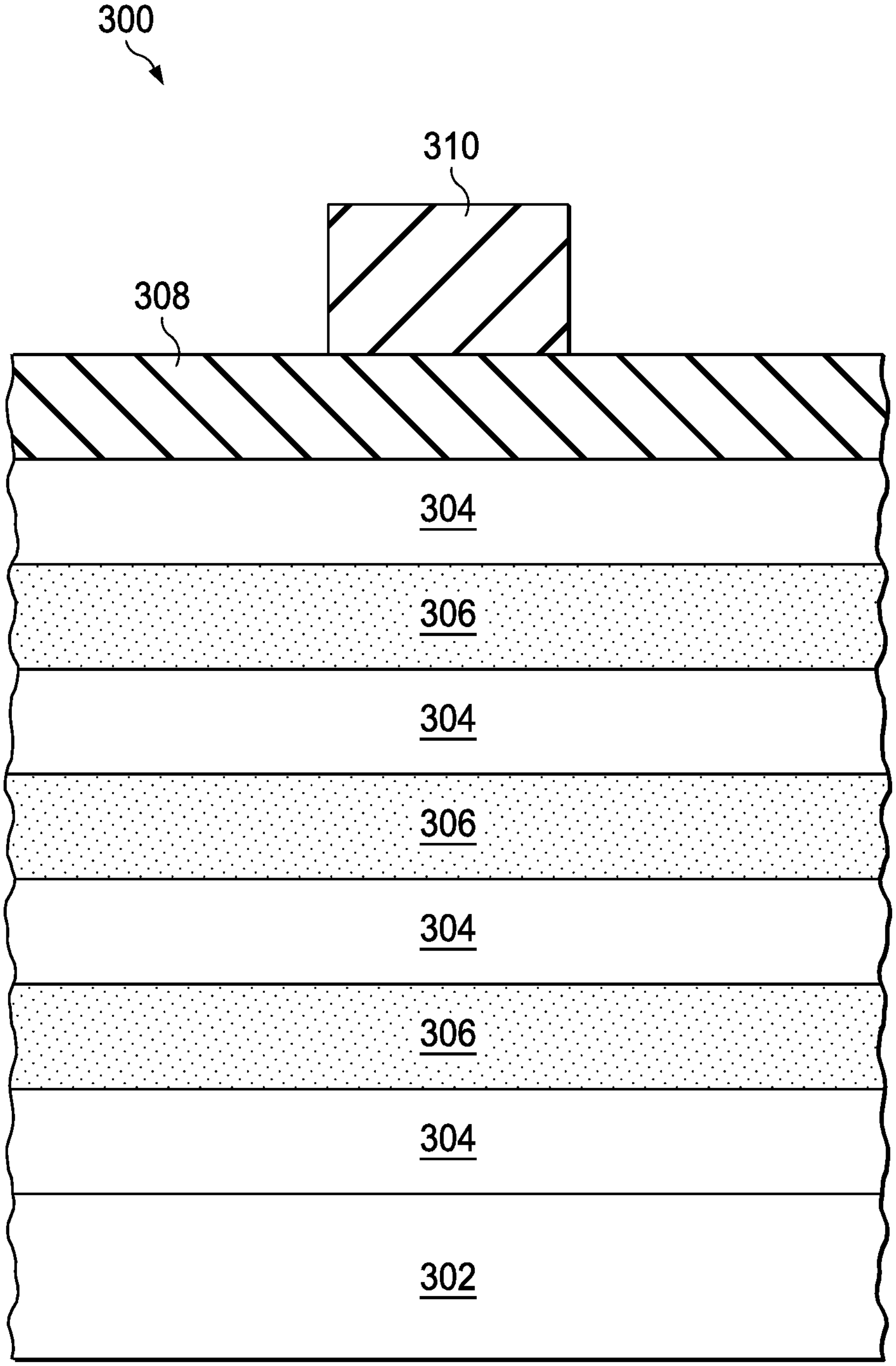


FIG. 3A

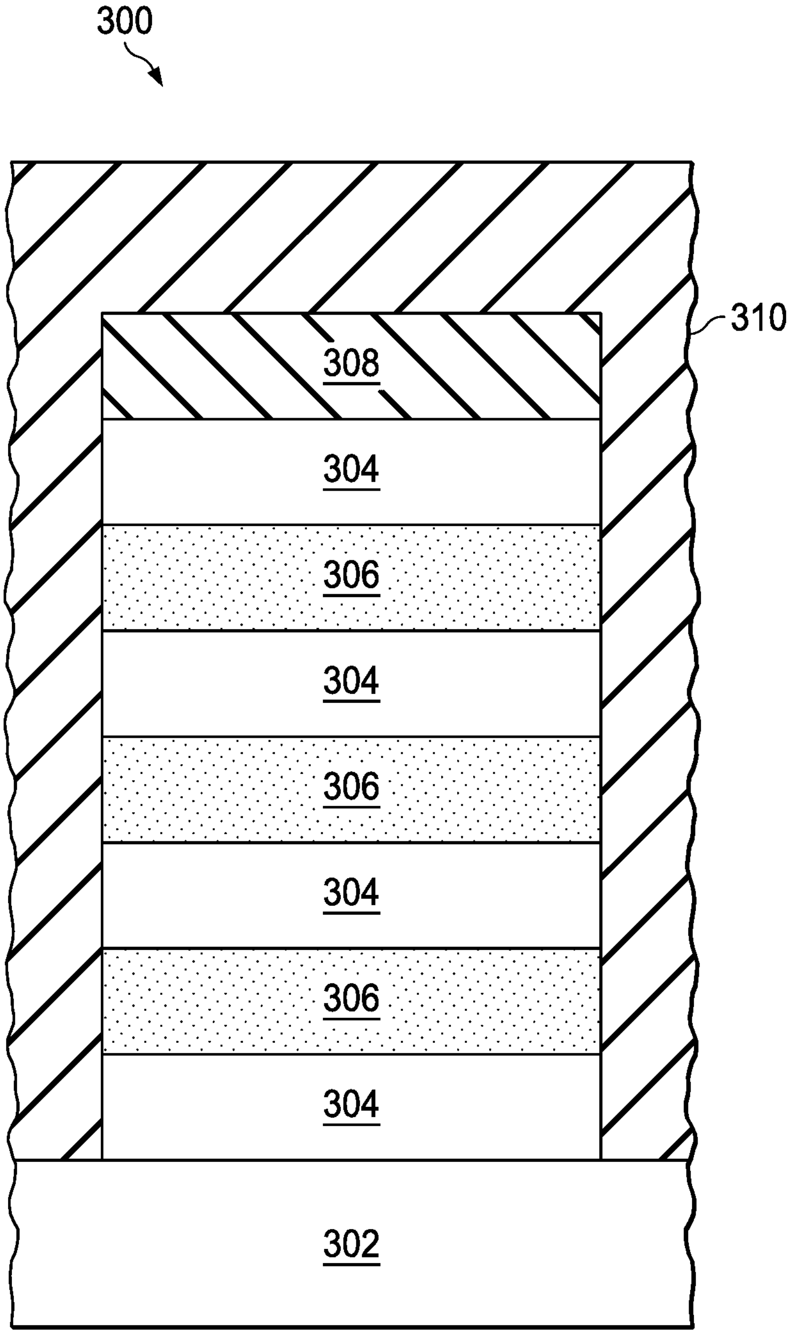


FIG. 3B

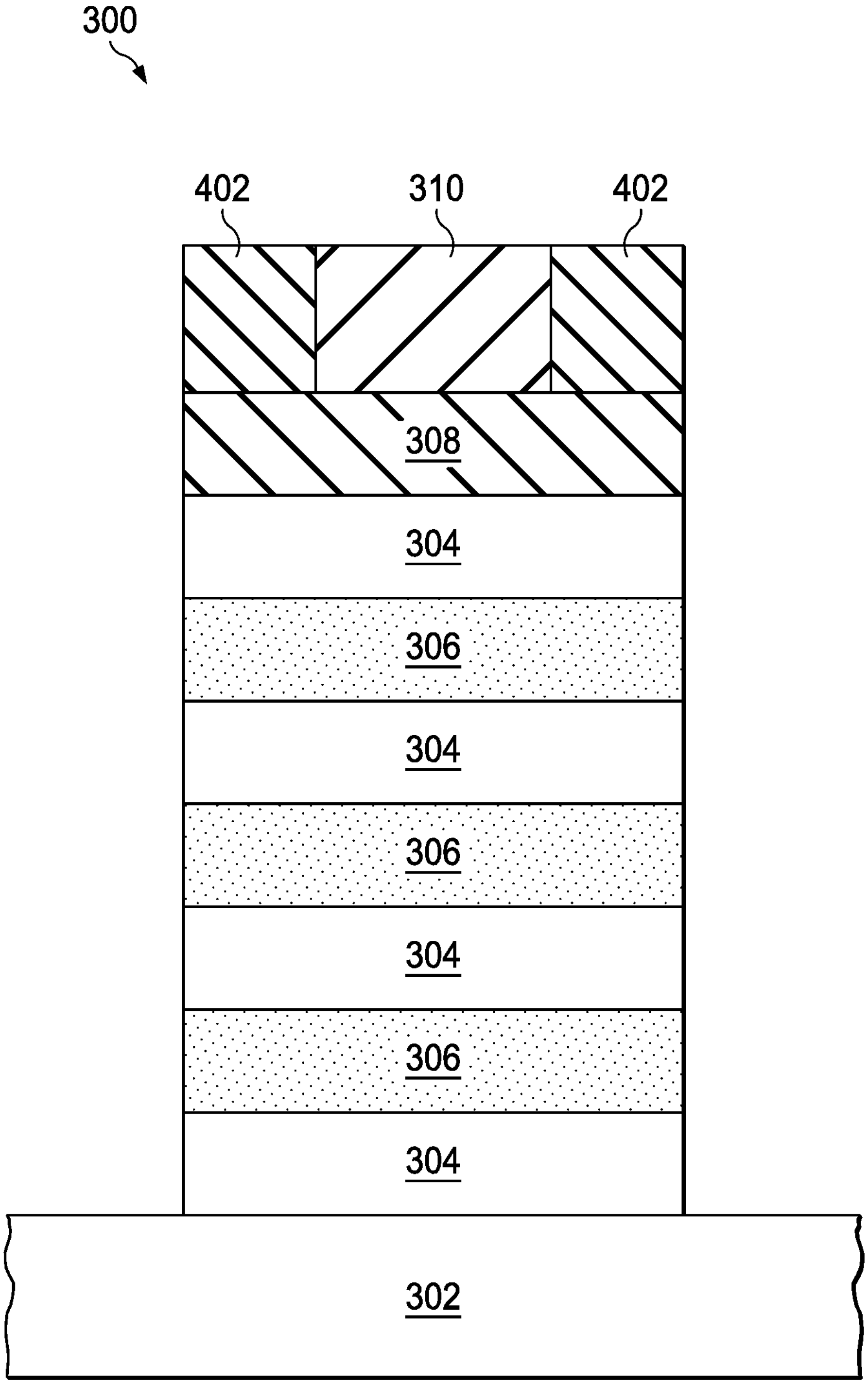


FIG. 4A

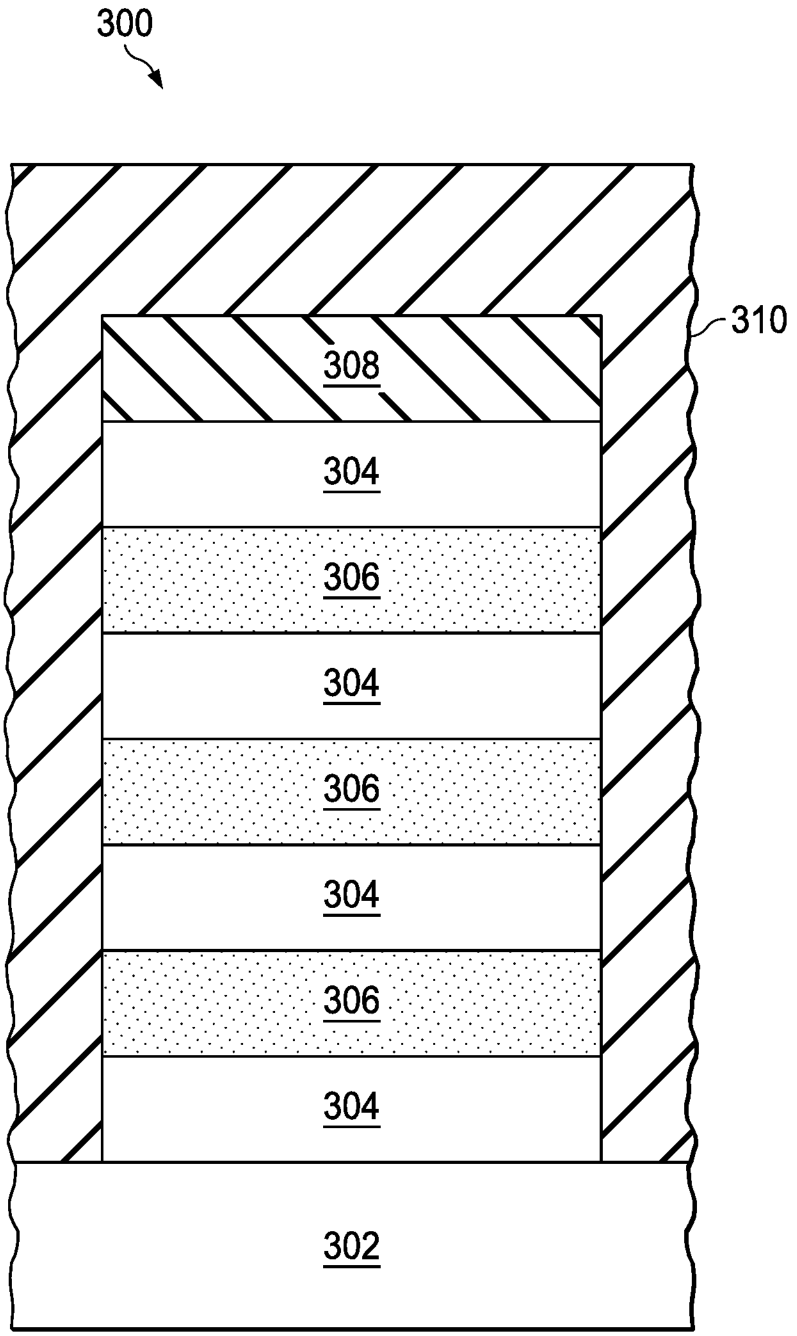


FIG. 4B

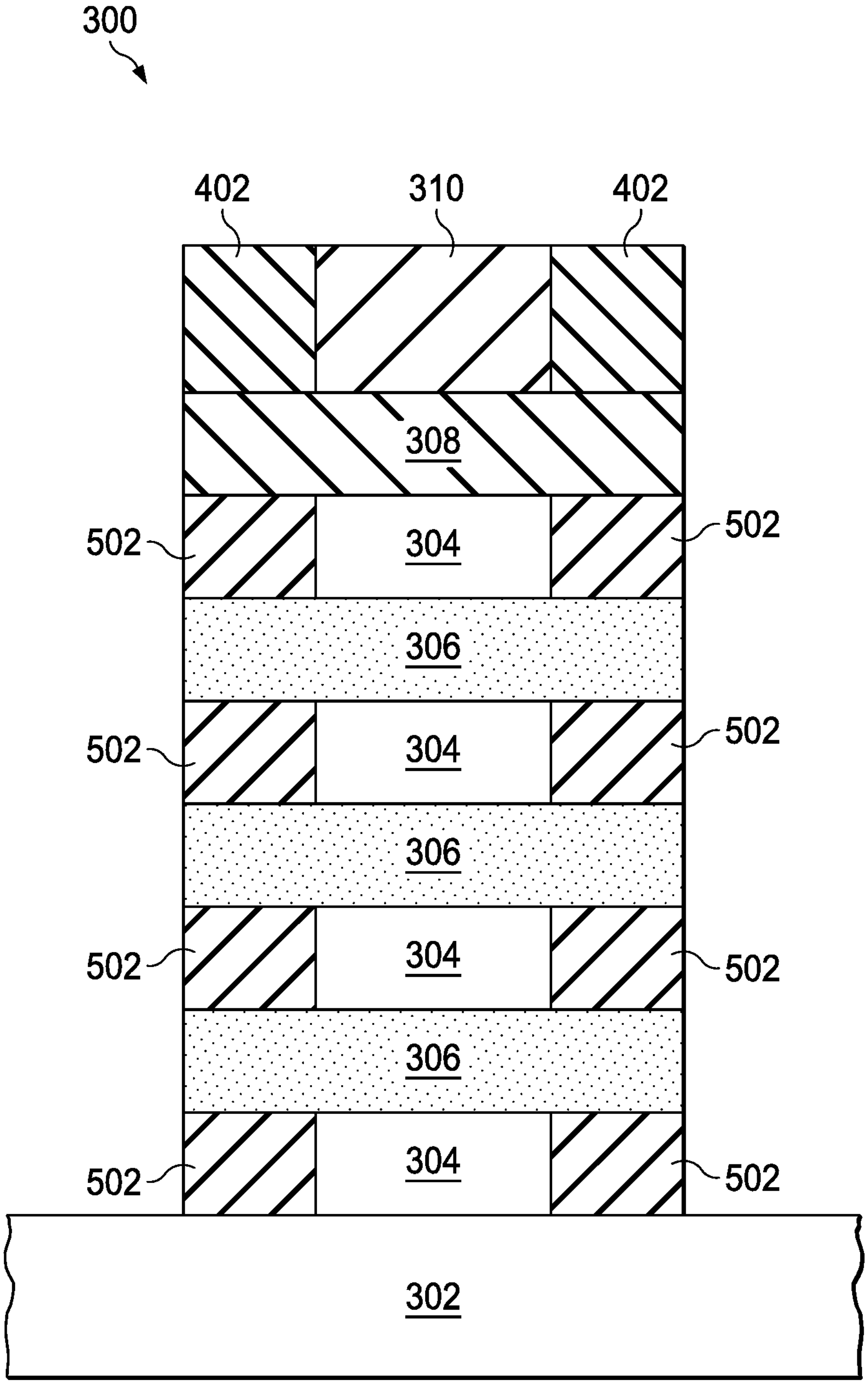

300
402
310
402
308
502
304
502
306
502
304
502
306
502
304
502
306
502
304
502
302

FIG. 5A

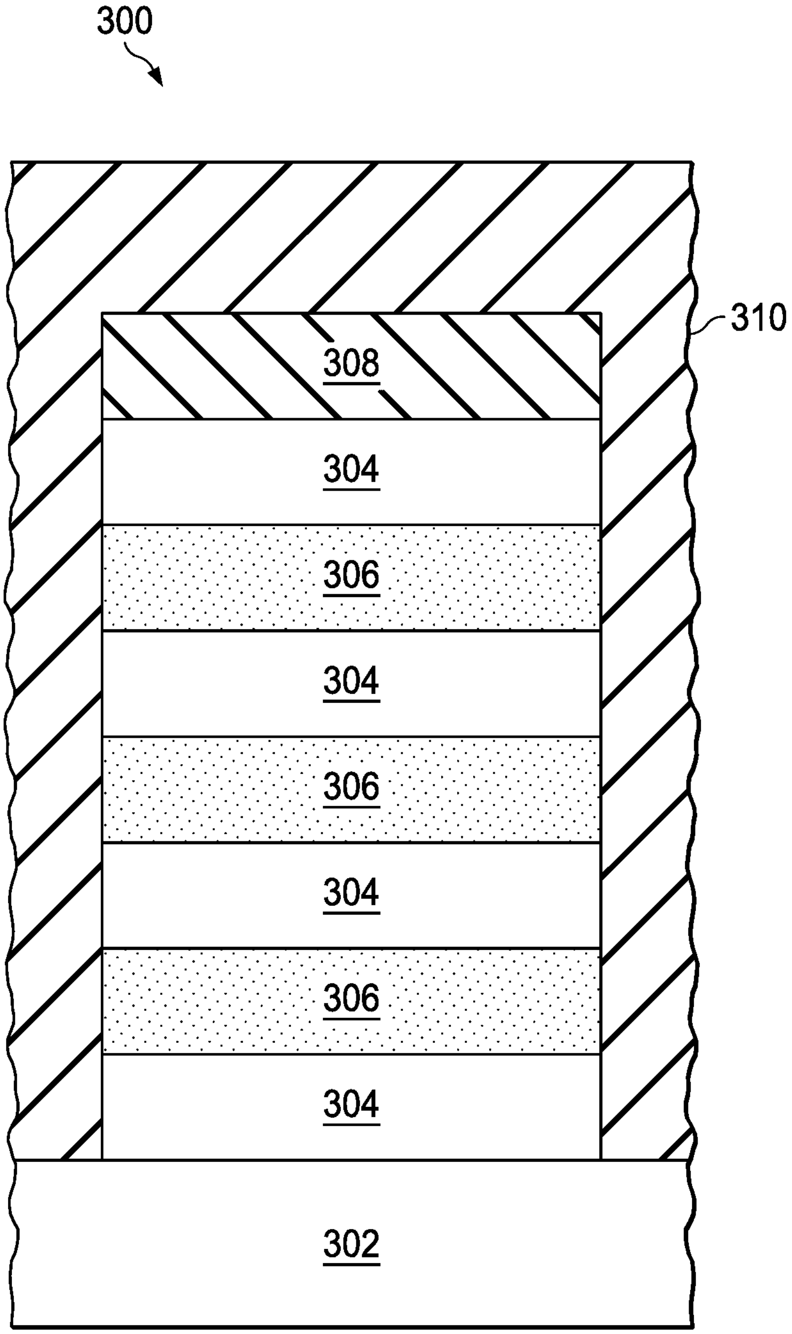


FIG. 5B

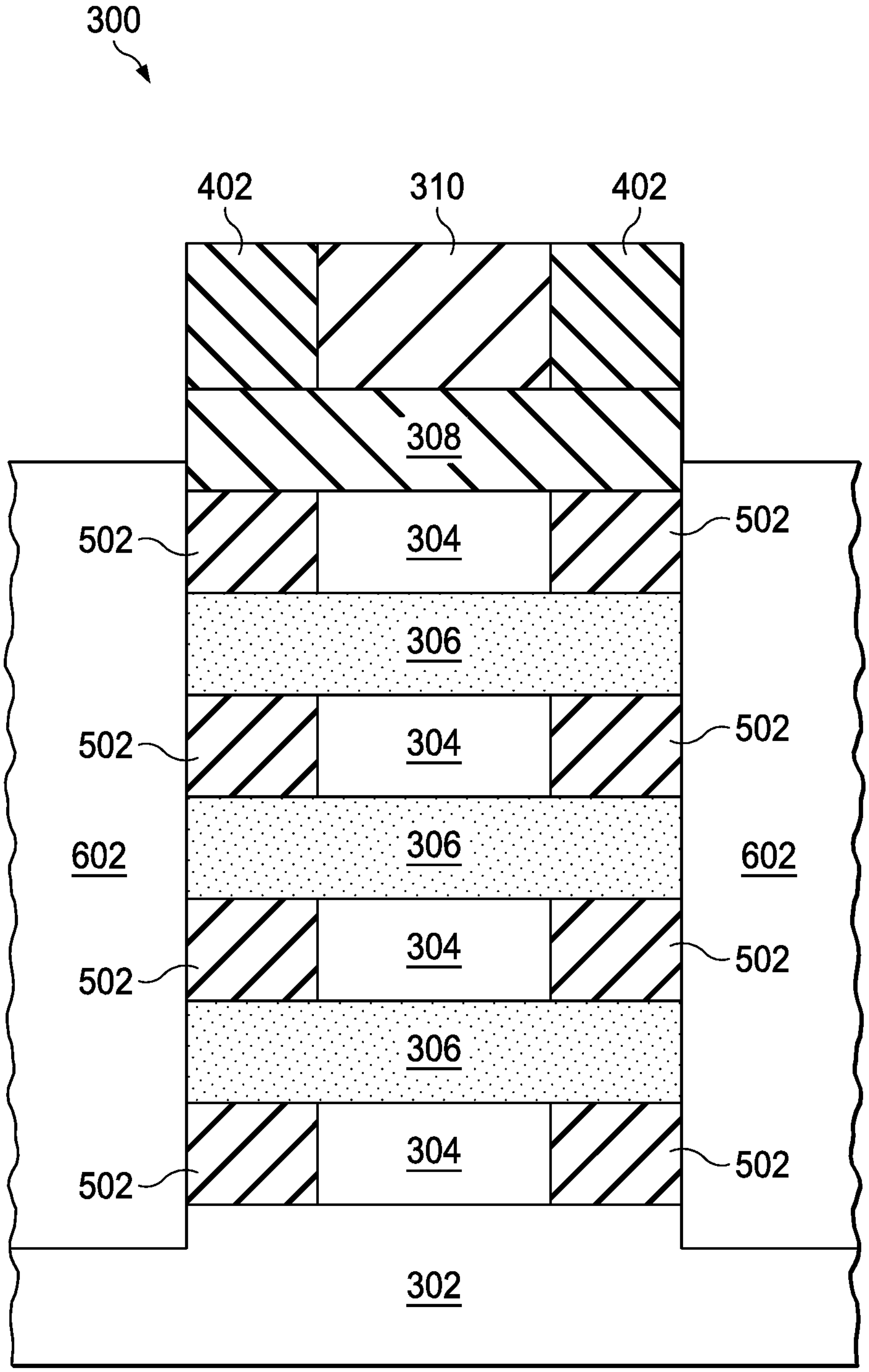

300
402
310
402
308
502
304
502
306
502
304
502
602
306
602
502
304
502
306
502
304
502
302

FIG. 6A

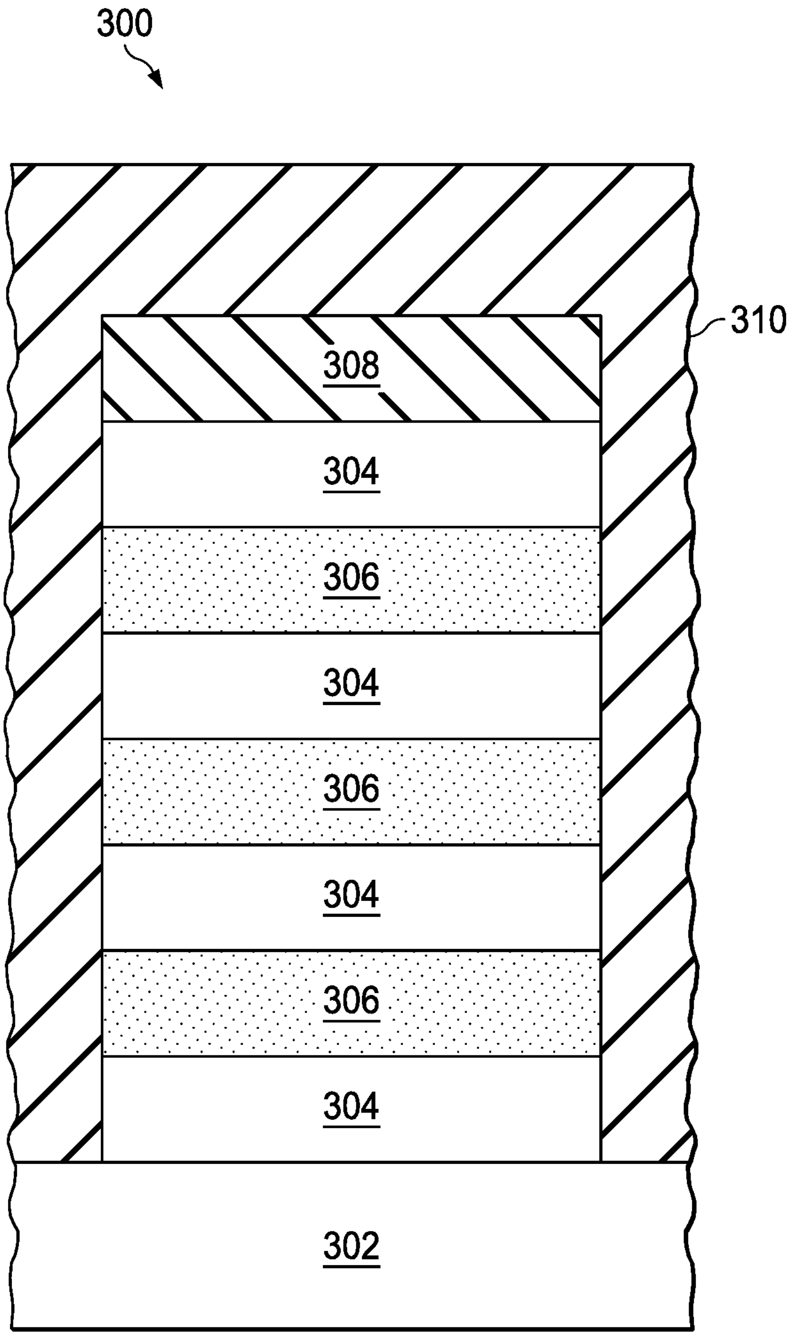


FIG. 6B

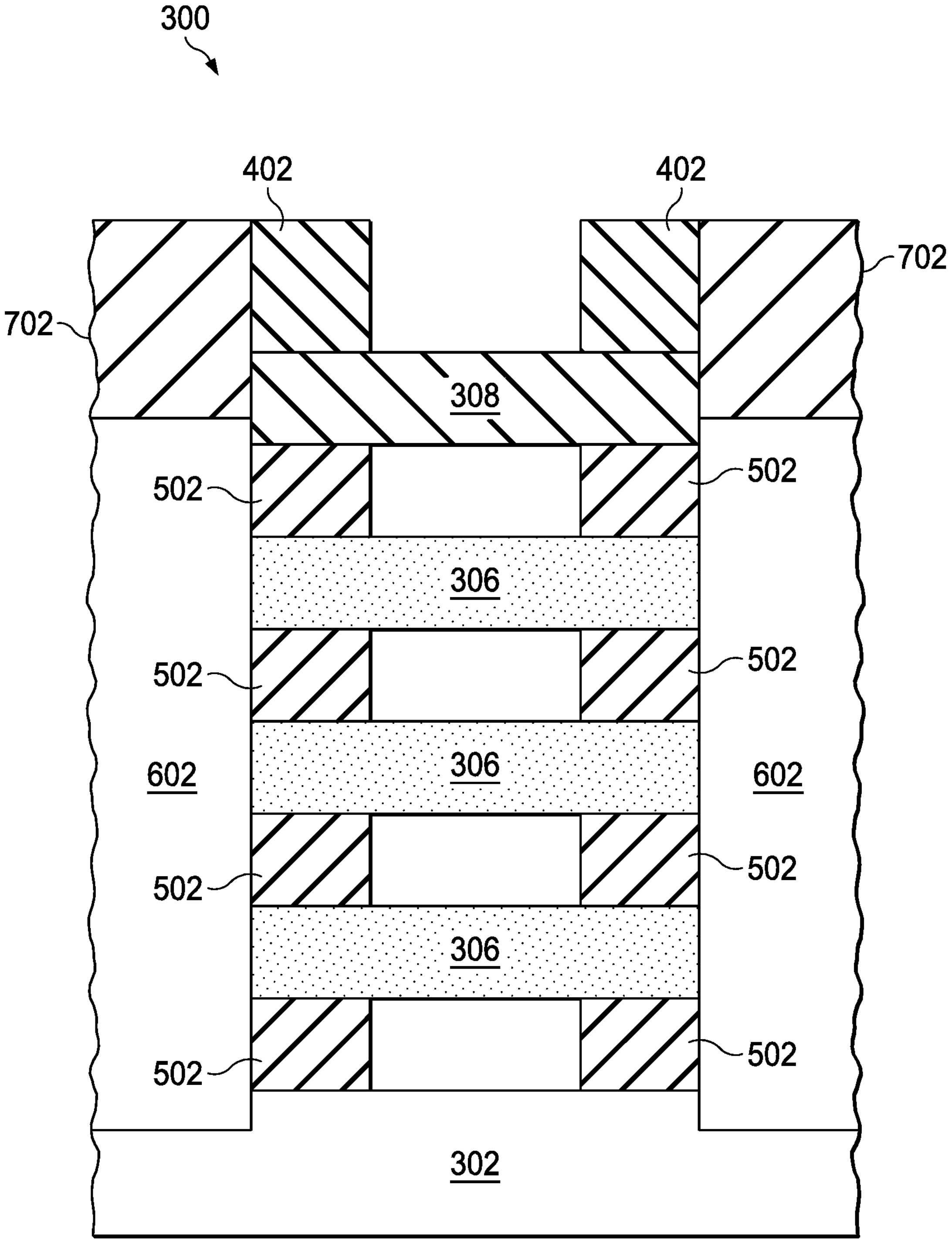

300
402
402
702
702
308
502
502
306
502
502
306
602
602
502
502
306
502
502
302

FIG. 7A

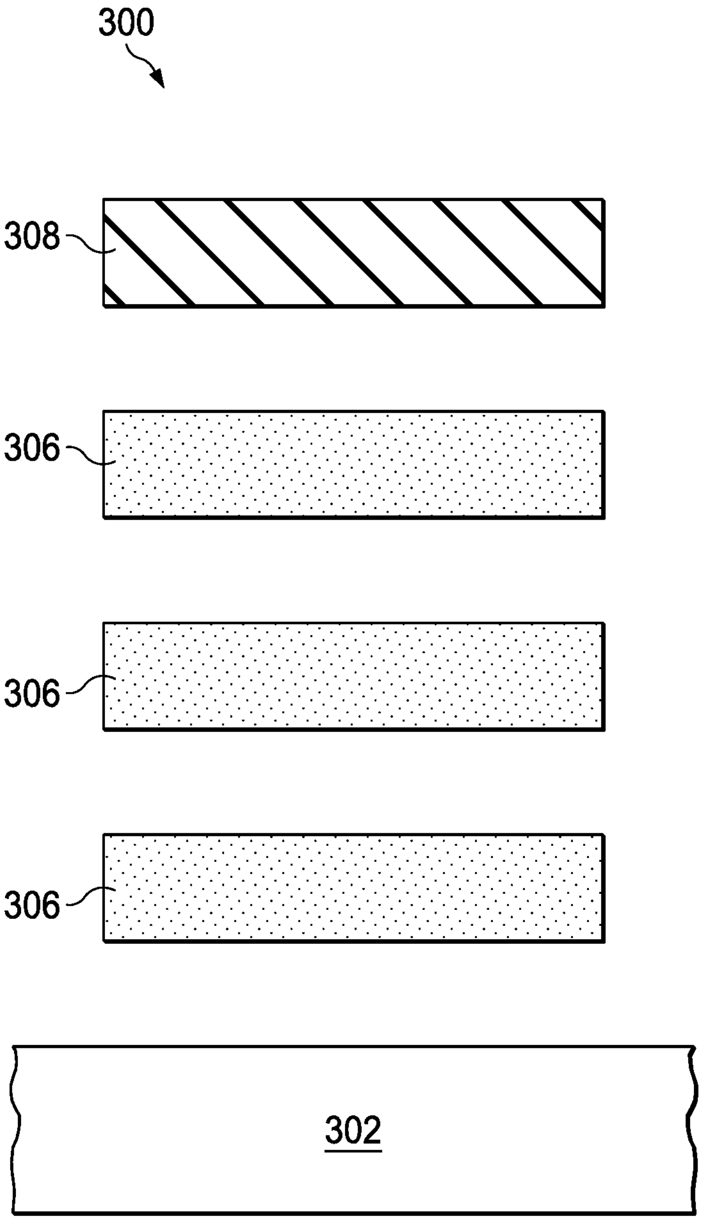


FIG. 7B

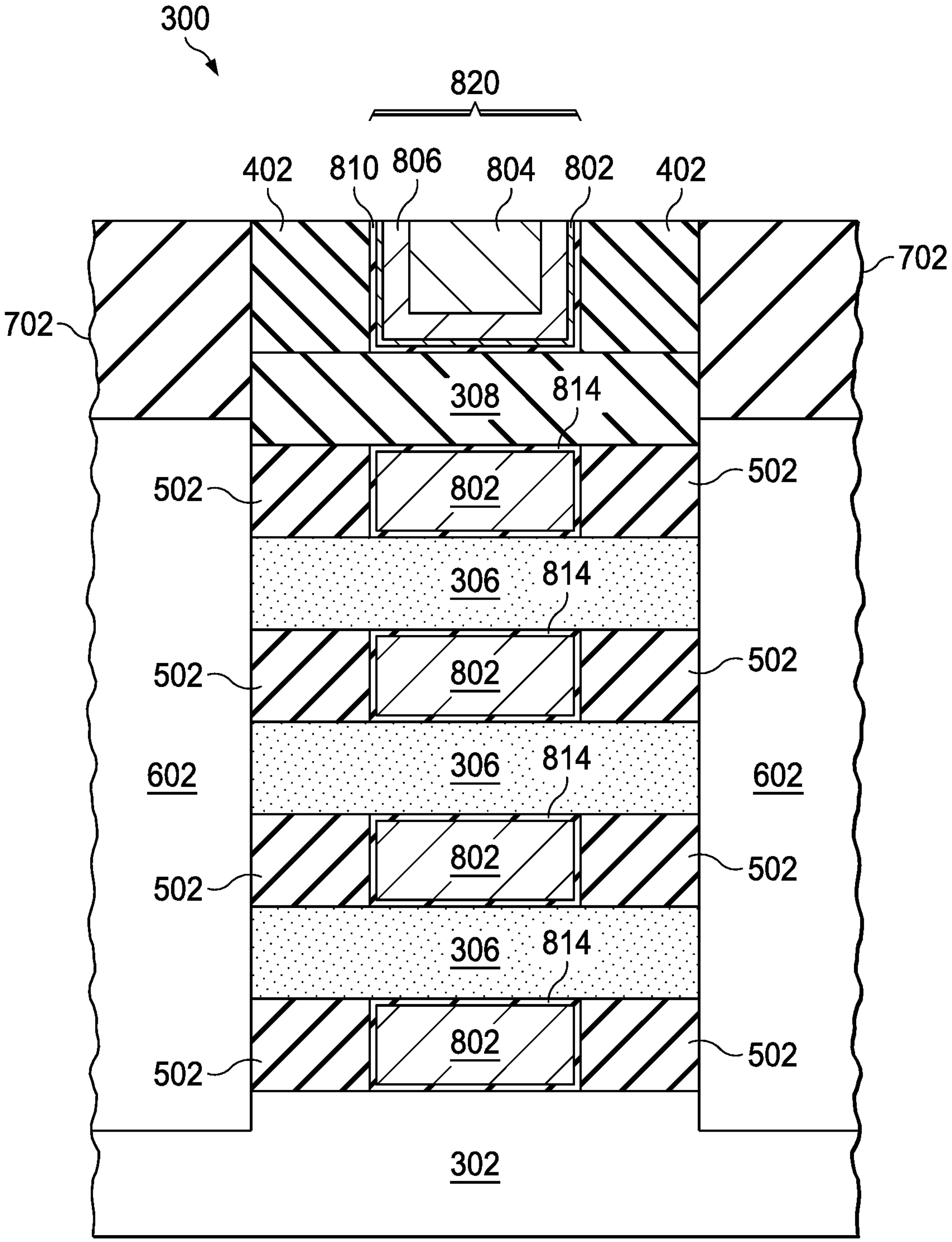

300
820
402
810
806
804
802
402
702
702
308
814
502
502
802
306
814
502
502
802
602
306
814
602
502
802
502
306
814
502
802
502
302

FIG. 8A

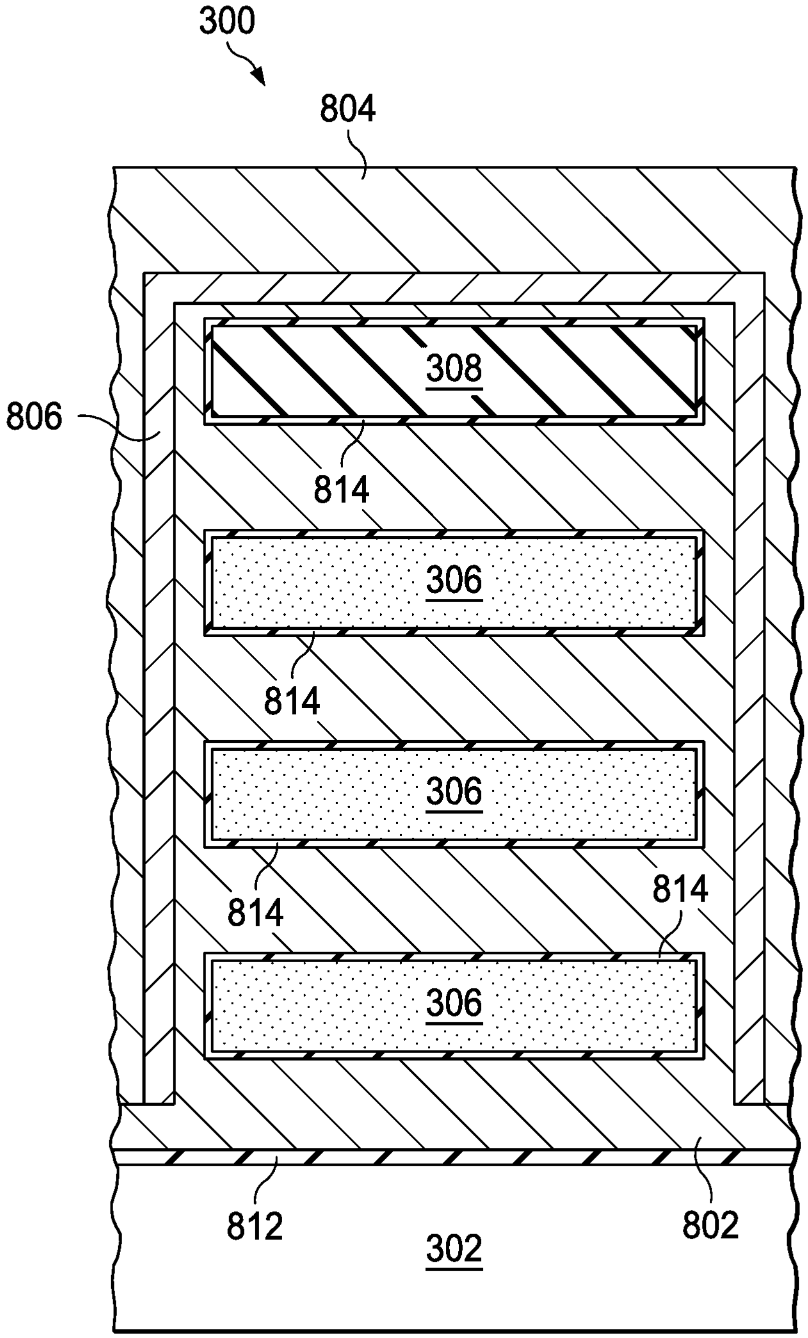


FIG. 8B

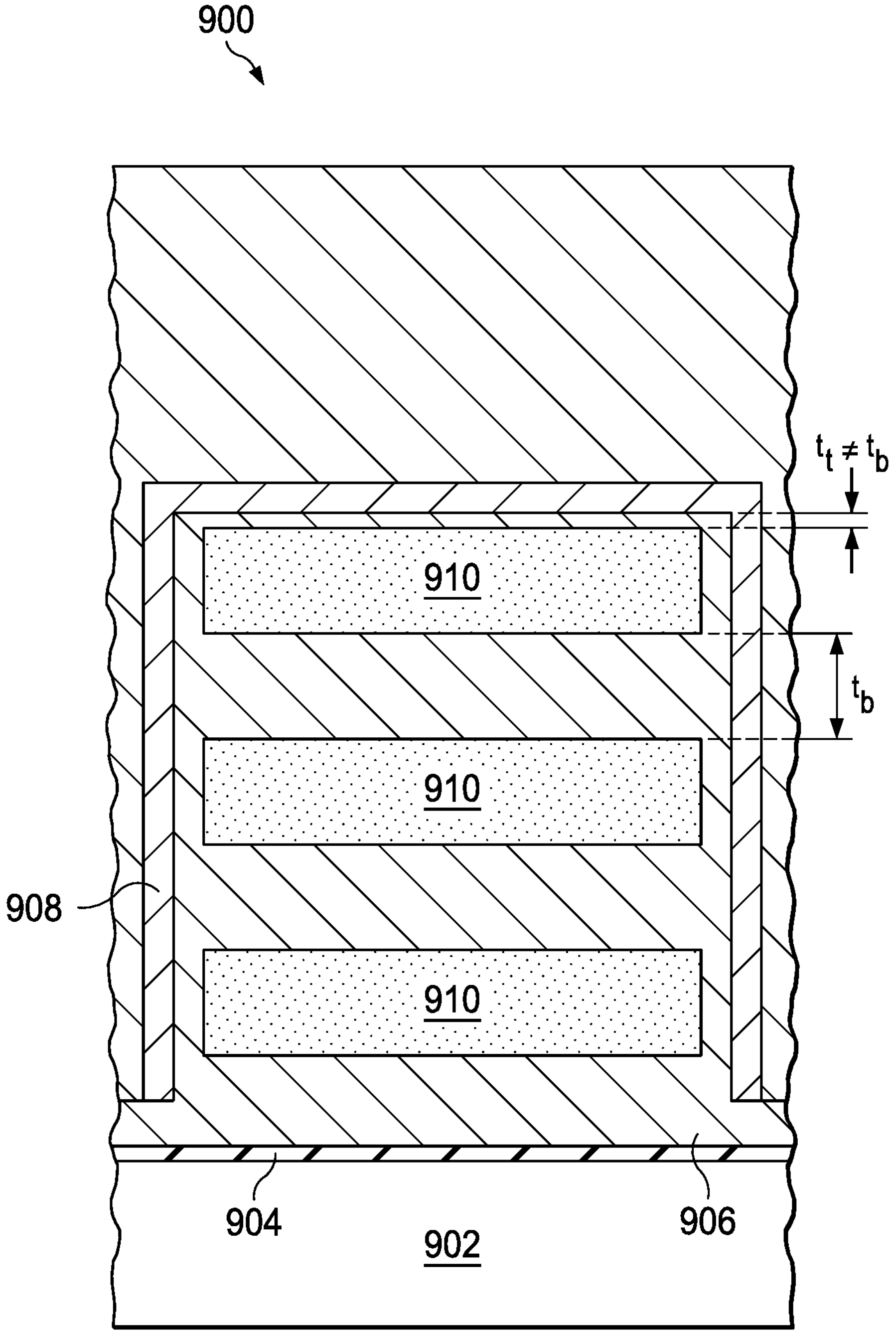


FIG. 9A

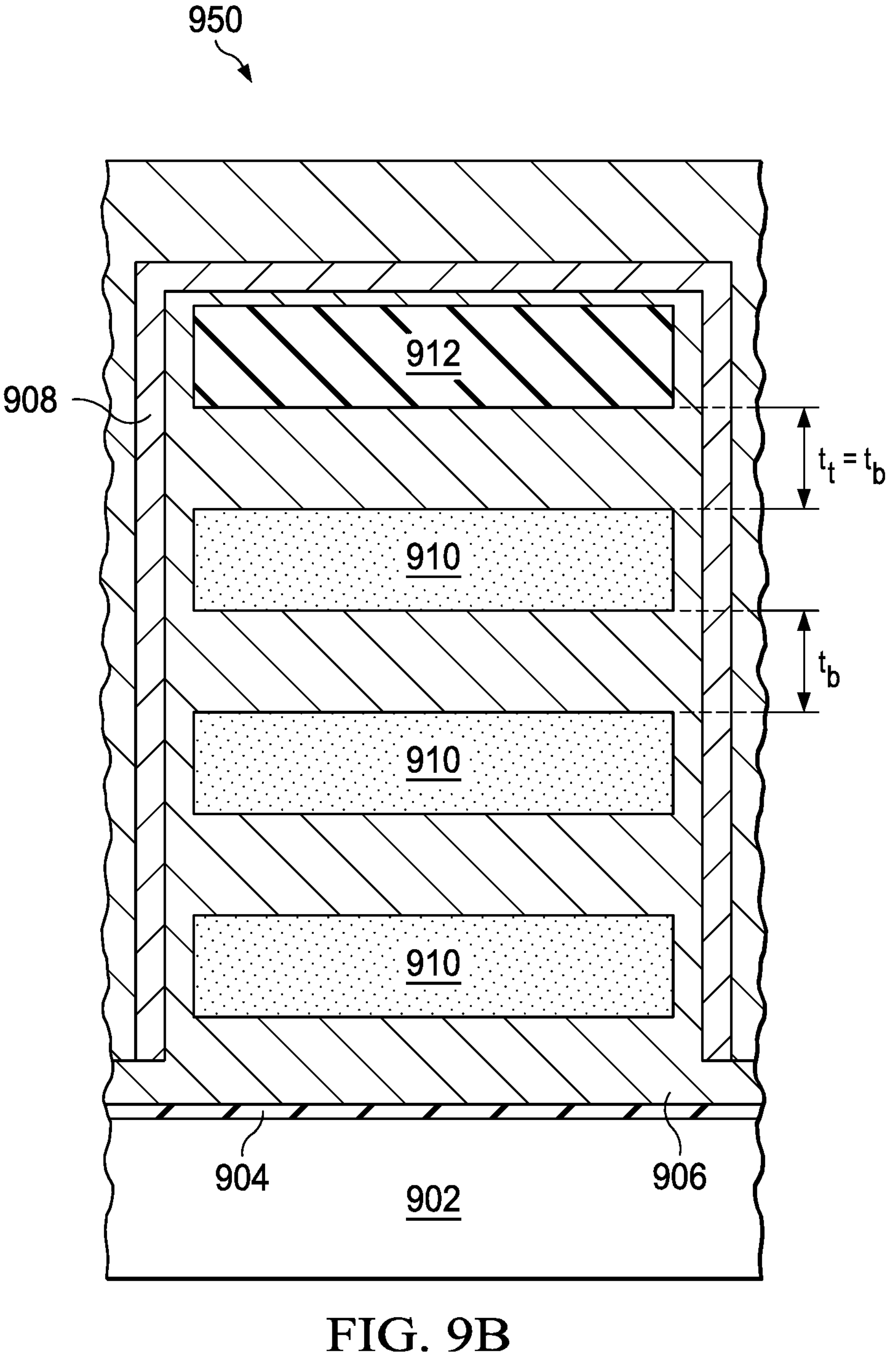
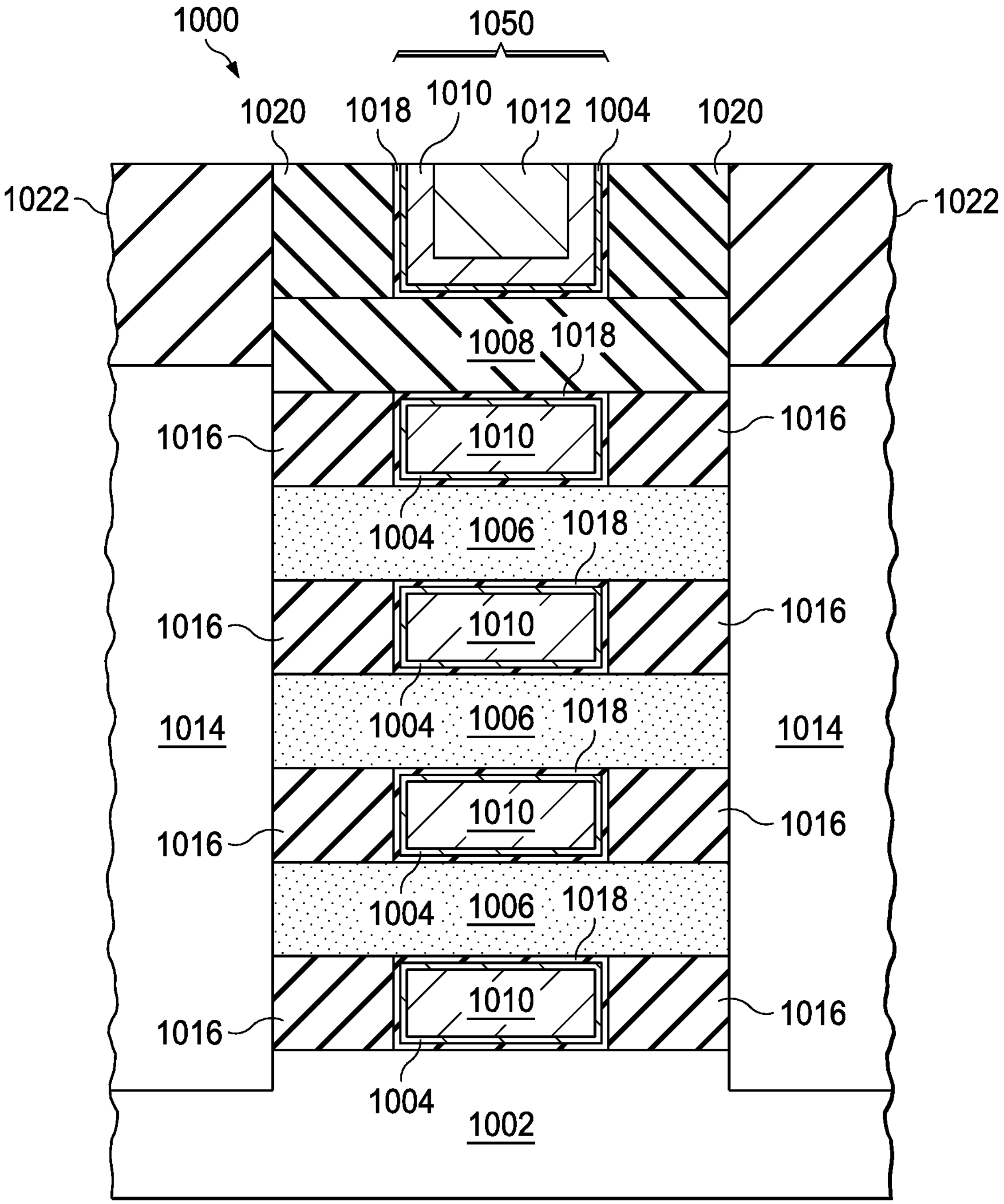


FIG. 9B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1050
1020
1018
1010
1012
1004
1020
1022
1022
1008
1018
1016
1010
1016
1004
1006
1018
1016
1010
1016
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1018
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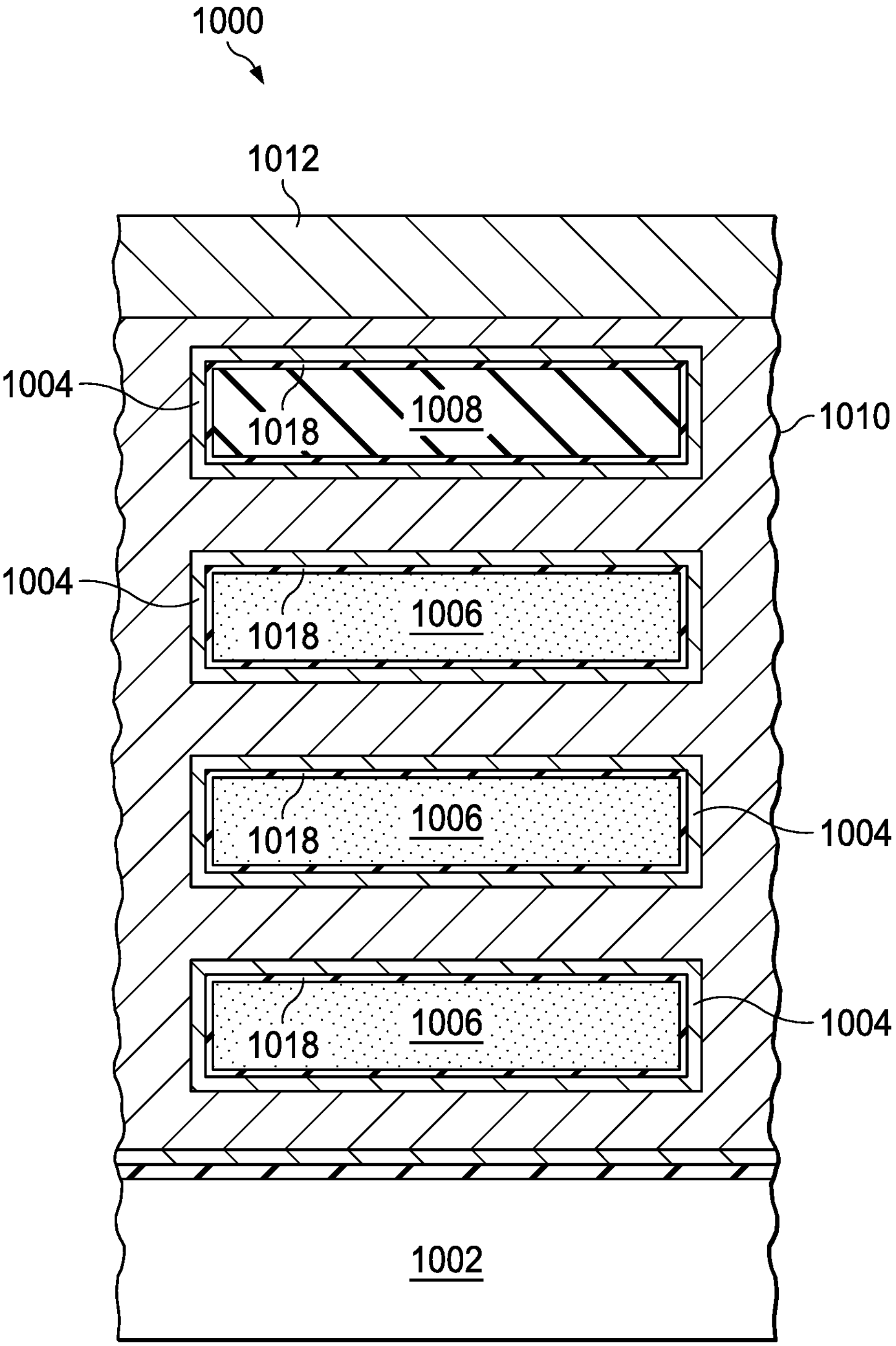
1010
1016
1004
1002

FIG. 10A


1000
1012
1004
1018
1008
1010
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1018
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1006
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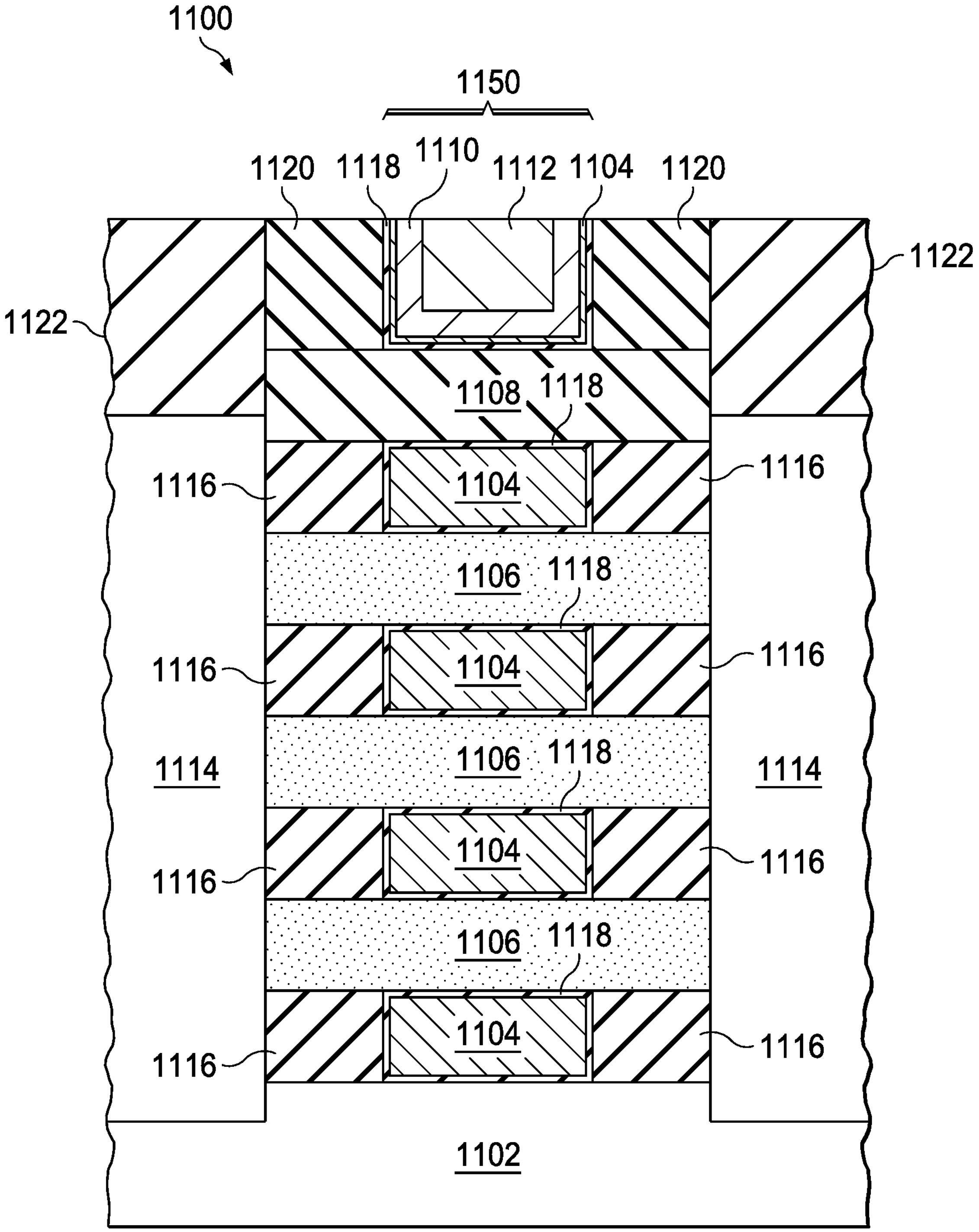
1018
1006
1004
1002

FIG. 10B


1100
1150
1120
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1112
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1122
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1104
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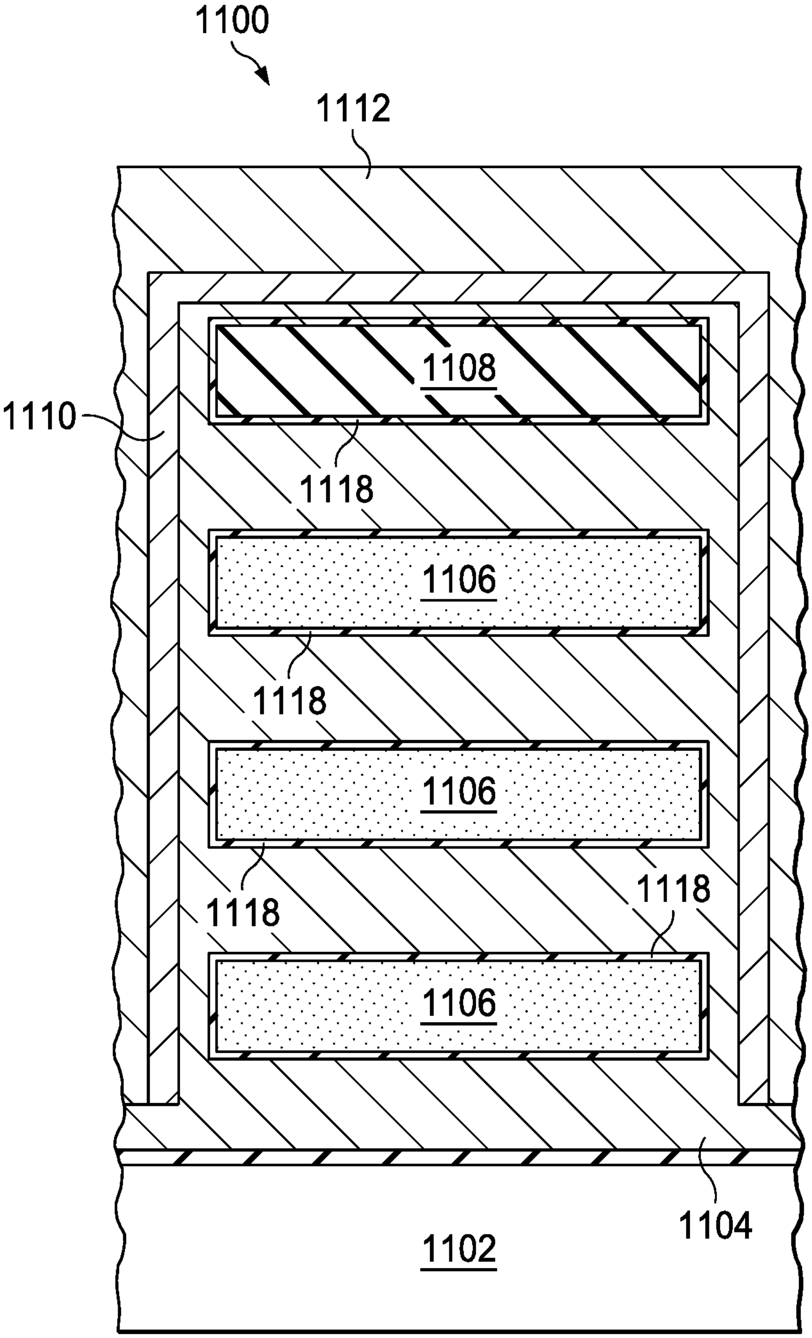
FIG. 11A


1100
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1108
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1106
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1106
1118
1118
1106
1104
1102

FIG. 11B

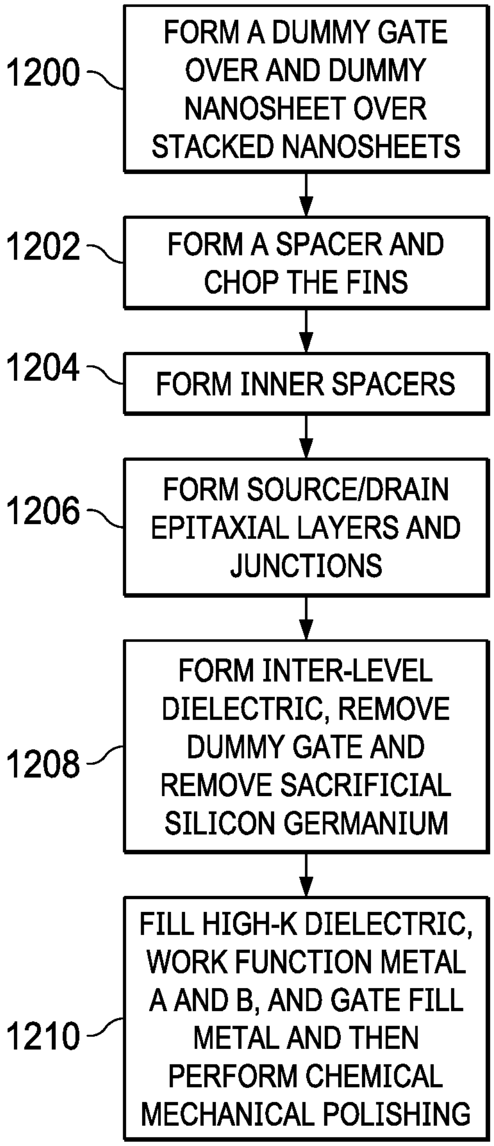
1200
FORM A DUMMY GATE OVER AND DUMMY NANOSHEET OVER STACKED NANOSHEETS
1202
FORM A SPACER AND CHOP THE FINS
1204
FORM INNER SPACERS
1206
FORM SOURCE/DRAIN EPITAXIAL LAYERS AND JUNCTIONS
1208
FORM INTER-LEVEL DIELECTRIC, REMOVE DUMMY GATE AND REMOVE SACRIFICIAL SILICON GERMANIUM
1210
FILL HIGH-K DIELECTRIC, WORK FUNCTION METAL A AND B, AND GATE FILL METAL AND THEN PERFORM CHEMICAL MECHANICAL POLISHING

FIG. 12

STACKED NANOSHEET TECHNOLOGY WITH UNIFORM VTH CONTROL

BACKGROUND

[0001] The disclosure relates generally to semiconductor devices and more specifically to stacked nanosheet transistors.

[0002] Gate-all-around (GAA) stacked nanosheet structures, such as GAA stacked nanosheet MOSFETs, are candidates for advanced technology nodes. GAA stacked nanosheet structures offer good electrostatic control, thereby enabling CMOS device scaling. Furthermore, GAA stacked nanosheet MOSFETs offer increased current drive per foot print. However, work function (WF) control as well as achieving multi threshold voltages (Vth) in stacked nanosheets are challenging due to the asymmetry of the structure, especially for the top sheet which is semi-confined compared to the bottom sheets.

[0003] Therefore, it would be desirable to have a method and apparatus that take into account at least some of the issues discussed above, as well as other possible issues.

SUMMARY

[0004] According to one embodiment of the present invention, a gate all around (GAA) stacked nanosheet field effect transistor (FET) includes a plurality of stacked semiconductor channel nanosheet layers and a dummy nanosheet layer formed above a top of one of the stacked semiconductor channel nanosheet layers, the dummy nanosheet layer formed from a dielectric material. The GAA stacked nanosheet FET also includes a high dielectric constant (high-k) material formed around each of the plurality of stacked semiconductor channel nanosheet layers and around the dummy nanosheet layer and a first work function (WF) metal formed around the plurality of stacked semiconductor channel nanosheet layers and the dummy nanosheet layer

[0005] According to another embodiment of the present invention, a method for forming a gate all around (GAA) stacked nanosheet field effect transistor (FET) includes forming alternating layers of sacrificial epitaxial nanosheet layers and semiconductor channel nanosheet layers. The method also includes forming a dummy nanosheet layer over the top of a sacrificial epitaxial nanosheet layer, the dummy nanosheet layer comprising a dielectric material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIGS. **1**-**2** are diagrams of cross-sectional views of prior art GAA stacked nano structures;

[0007] FIGS. **3**A&B-**8**A&B are cross-sectional views of a semiconductor device with a stacked nanosheets at various stages of processing depicted in accordance with illustrative embodiments;

[0008] FIG. **9**A is a cross-sectional view of a prior art convention nanosheet structure;

[0009] FIG. **9**B is a cross-section view of an illustrative embodiment of a nanosheet structure with a top dummy sheet;

[0010] FIG. **10**A is a cross sectional view across the gate line direction of a semiconductor device constructed with a first threshold voltage, V_{th1}, depicted in accordance with an illustrative embodiment;

[0011] FIG. **10**B is a cross sectional view along the gate line direction of the semiconductor device depicted in accordance with an illustrative embodiment;

[0012] FIG. **11**A is a cross sectional view across the gate line direction of a semiconductor device constructed with a second threshold voltage, V_{th2}, depicted in accordance with an illustrative embodiment;

[0013] FIG. **11**B is a cross sectional view along the gate line direction of the semiconductor device depicted in accordance with an illustrative embodiment; and

[0014] FIG. **12** is a flowchart of a process for fabricating a bi-layer composite PCM cell as depicted in accordance with an illustrative embodiment.

DETAILED DESCRIPTION

[0015] Detailed embodiments of the claimed structures and methods are disclosed herein; however, it is to be understood that the disclosed embodiments are merely illustrative of the claimed structures and methods that may be embodied in various forms. In addition, each of the examples given in connection with the various embodiments is intended to be illustrative, and not restrictive.

[0016] Further, the figures are not necessarily to scale, some features may be exaggerated to show details of particular components. Therefore, specific structural and functional details disclosed herein are not to be interpreted as limiting, but merely as a representative basis for teaching one skilled in the art to variously employ the methods and structures of the present disclosure.

[0017] For purposes of the description hereinafter, the terms "upper," "lower," "right," "left," "vertical," "horizontal," "top," "bottom," and derivatives thereof shall relate to the embodiments of the disclosure, as it is oriented in the drawing figures. The terms "positioned on" means that a first element, such as a first structure, is present on a second element, such as a second structure, wherein intervening elements, such as an interface structure, e.g. interface layer, may be present between the first element and the second element.

[0018] In this disclosure, when an element, such as a layer, region, or substrate is referred to as being "on" or "over" another element, the element can be directly on the other element or intervening elements can also be present. In contrast, when an element is referred to as being "directly on," "directly over," or "on and in direct contact with" another element, there are no intervening elements present, and the element is in contact with another element.

[0019] The processes, steps, and structures described below do not form a complete process flow for manufacturing integrated circuits. The disclosure can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as necessary for an understanding of the different examples of the present disclosure. The figures represent cross sections of a portion of an integrated circuit during fabrication and are not drawn to scale, but instead are drawn so as to illustrate different illustrative features of the disclosure.

[0020] With reference now to the figures and, in particular, with reference to FIGS. **1**-**2**, cross-sectional views of prior art GAA stacked nanostructures **100**, **200** are shown. The GAA stacked nanostructure **100** in FIG. **1** includes stacked nanolayers of silicon channel **102** each surrounded by a thin layer of work function metal A **106**. The work function metal

A **106** is surrounded by another work function metal B **108**. The work function metal A **106** is relatively thin (i.e., a thin suspension thickness, T_{sus}) and does not cover the entire gap between adjacent nanolayers **102**. The remaining part of the gap between adjacent nanolayers **102** is filled with the work function metal B **108**.

[0021] The GAA stacked nanostructure **200** in FIG. **2** includes stacked nanolayers of silicon channel **202** surrounded by a relatively thick (i.e., thick T_{sus}) layer of work function metal A **206**. The work function metal A **206** completely fills the gaps between adjacent layers of the nanolayers **202**. A work function metal B **208** covers the work function metal A **206**.

[0022] By adjusting the suspension thickness, T_{sus}, of the work function metal A **106**, **206**, field effect transistors (FETs) of different threshold voltages, V_{th}, (i.e., multi-V_{th} FETs) may be constructed. However, the thickness of a metal on top and bottom of the top sheet **102**, **202** is different from that of the other sheets **102**, **202**. Thus, the effective work function (WF) for the top sheet cannot be controlled by T_{sus}.

[0023] Disclosed herein are stacked nanosheet FETs with a dummy nitride nanosheet to confine the top nanosheet in a similar manner to the bottom nanosheet, thereby resulting in controlling the effective WF of the top nanosheet and controlling V_{th} uniformity of the top sheet is achieved. The disclosed nanosheet structures provide better control of multi-V_{th} with changing the metal thickness than is provided by prior art structures.

[0024] FIGS. **3A&B**-**11A&B** are cross-sectional views of a semiconductor device with a stacked nanosheets at various stages of processing depicted in accordance with illustrative embodiments.

[0025] FIG. **3A** is a cross sectional view across the gate line direction of a GAA semiconductor device **300** at a first stage of processing depicted in accordance with an illustrative embodiment. FIG. **3B** is a cross sectional view along the gate line direction of a GAA semiconductor device **300** at a first stage of processing depicted in accordance with an illustrative embodiment. The first stage of processing is not the initial stage, but the term "first stage" (as well as the terms "second stage", "third stage", etc. used below) is used merely to differentiate this stage from other stages in the processing of the GAA semiconductor device **300**. Some stages and steps of processing may be omitted in the description that follows.

[0026] The GAA semiconductor device **300** at the first stage of processing includes a silicon substrate **302** with alternating layers of a sacrificial epitaxial nanosheet layer **304** and a semiconductor channel nanosheet layer **306**. Each of the semiconductor channel nanosheet layers **306** and the sacrificial epitaxial nanosheet layers **304** are between 6 nanometers (nm) and 20 nm thick. In an embodiment, each of the semiconductor channel nanosheet layers **306** and the sacrificial epitaxial nanosheet layers **304** are about 10 nm thick. Typically, each of the semiconductor channel nanosheet layers **306** and the sacrificial epitaxial nanosheet layers **304** are of equal thickness. However, slight variations in thickness between the various layers **304**, **306** are acceptable. In some embodiments, the thicknesses of the various layers **304**, **306** are not equal.

[0027] The top sacrificial epitaxial layer **304**, covering the top semiconductor channel nanosheet layer **306**, is itself covered by a dummy nitride (Silicon Nitride (SiN)) nanosheet layer **308**. A dummy gate **310** is formed over the top of the dummy nitride nanosheet layer **308**. In an embodiment, the semiconductor channel nanosheet layer **306** is constructed from silicon (Si). In other embodiments, the semiconductor channel nanosheet layer **306** is constructed from germanium (Ge). In other embodiments, other materials may be used for the semiconductor channel nanosheet layer **306**. In an embodiment, the sacrificial layer is silicon germanium (SiGe). In other embodiments, other materials may be used for the sacrificial layer. In an embodiment, the dummy gate is a thin layer of oxide and polysilicon.

[0028] Although three stacked semiconductor channel nanosheet layers **306** are shown, in other embodiments, the number of stacked semiconductor channel nanosheet layers **306** may be more or less than three.

[0029] FIG. **4A** is a cross sectional view across the gate line direction of a GAA semiconductor device **300** at a second stage of processing depicted in accordance with an illustrative embodiment. FIG. **4B** is a cross sectional view along the gate line direction of a GAA semiconductor device **300** at a second stage of processing depicted in accordance with an illustrative embodiment.

[0030] In the second stage, gate spacers **402** are deposited over the dummy nitride sheet **308** using conformal deposition and then the GAA semiconductor device **300** is etched to remove the fins from the GAA semiconductor device **300**. The resulting structure is depicted in FIGS. **4A** & **4B**. The gate spacers **402** are a dielectric material such as, for example, silicon nitride (Si_3N_4), silicon oxynitride (SiOxNy), and silicon boron oxide nitride (SiBCN).

[0031] FIG. **5A** is a cross sectional view across the gate line direction of a GAA semiconductor device **300** at a third stage of processing depicted in accordance with an illustrative embodiment. FIG. **5B** is a cross sectional view along the gate line direction of a GAA semiconductor device **300** at a third stage of processing depicted in accordance with an illustrative embodiment.

[0032] In the third stage, inner spacers **502** are formed. The sacrificial epitaxial layers **304** are selectively etched laterally, using for example, a reactive ion etch, to produce recesses that are filled with inner spacers **502**. The inner spacers **502** are constructed, for example, from nitride.

[0033] FIG. **6A** is a cross sectional view across the gate line direction of a GAA semiconductor device **300** at a fourth stage of processing depicted in accordance with an illustrative embodiment. FIG. **6B** is a cross sectional view along the gate line direction of a GAA semiconductor device **300** at a fourth stage of processing depicted in accordance with an illustrative embodiment.

[0034] In the fourth stage, the source and drain (S/D) epitaxy and junctions **602** are formed in the region where, in the second stage, the fins were removed from the GAA semiconductor device **300**. In an embodiment, for n-type metal oxide-semiconductor (n-MOS), the S/D epitaxy and junctions **602** are silicon carbide (SiC) or germanium (Ge) highly doped with phosphorous (P) or arsenic (As). In an embodiment, for p-type MOS (p-MOS), the S/D epitaxy and junctions **602** are silicon (Si), Silicon Germanium (SiGe), or germanium (Ge) highly doped with boron.

[0035] FIG. **7A** is a cross sectional view across the gate line direction of a GAA semiconductor device **300** at a fifth stage of processing depicted in accordance with an illustrative embodiment. FIG. **7B** is a cross sectional view along the gate line direction of a GAA semiconductor device **300** at a fifth stage of processing depicted in accordance with an illustrative embodiment.

[0036] In the fifth stage, an inter level dielectric (ILD) **702** is formed. Also, in the fifth stage, the dummy gate **310** and the sacrificial epitaxial nanosheet layers **304** are removed by, for example, a reactive ion etch.

[0037] FIG. **8**A is a cross sectional view across the gate line direction of a GAA semiconductor device **300** at a sixth stage of processing depicted in accordance with an illustrative embodiment. FIG. **8**B is a cross sectional view along the gate line direction of a GAA semiconductor device **300** at a sixth stage of processing depicted in accordance with an illustrative embodiment.

[0038] In the sixth stage, the semiconductor channel nanosheet layers **306** and the dummy nanosheet layer **308** have been coated with a high dielectric constant (high-k) material layer **814** and the spaces formed by removing the sacrificial epitaxial nanosheet layers **304** have been symmetrically filled with a WF metal A **802**. In an embodiment, the thickness of the WF metal A **802** is between 1 nm and 10 nm. A gate **820** is formed in the space formed by removing the dummy gate **310**. Thus, there is a single gate **820** controlling each of the semiconductor channel nanosheet layers **306**. The gate **820** includes the gate fill metal **804** surrounded by WF metal B **806** and WF metal A **802**. The gate **820** is separated from the spacers **402** by an interlevel (IL) high-k (HK) dielectric material **810**. In an embodiment, the gate fill metal **804** is one of tungsten (W) or cobalt (Co). In an embodiment, the top surface is planarized and polished with, for example, chemical mechanical polishing (CMP).

[0039] FIG. **9**A is a cross-sectional view of a prior art conventional GAA nanosheet structure **900**. FIG. **9**B is a cross-section view of an illustrative embodiment of a GAA nanosheet structure **950** with a top dummy sheet. A comparison of the conventional GAA nanosheet structure **900** with the disclosed GAA nanosheet structure **950** shows that while both structures **900**, **950** include a plurality of semiconductor channel nanosheet layers **910** surrounded by WF metal A **906** and WF metal B **908**, formed over a silicon substrate **902**, the disclosed structure **950** also includes a dummy nanosheet **912** over the top semiconductor channel nanosheet layer **910**. Thus, the suspension thickness for the top, t_t (i.e., top thickness of metal A **906**), and the suspension thickness for the bottom t_b (i.e., bottom thickness of metal A **906**), are not equal ($t_t \neq t_b$) for the conventional structure **900**, but are equal ($t_t = t_b$) for the disclosed structure **950**. Thus, the disclosed structure **950** controls the effective WF of the top nanosheet, and the control of V_{th} uniformity of the top sheet is achieved. Additionally, the disclosed nanosheet structure **950** provides better control of multi-V_{th} with changing the metal thickness than is provided by prior art structures.

[0040] The disclosed method and nanosheet structures can be implemented to provide devices with multiple or different threshold voltages.

[0041] FIG. **10**A is a cross sectional view across the gate line direction of a GAA semiconductor device **1000** constructed with a first threshold voltage, V_{th1}, depicted in accordance with an illustrative embodiment. FIG. **10**B is a cross sectional view along the gate line direction of the GAA semiconductor device **1000** depicted in accordance with an illustrative embodiment. GAA semiconductor device **1000** is similar to GAA semiconductor device **300** illustrated in FIGS. **8**A & **8**B. GAA semiconductor device **1000** includes a silicon substrate **1002** and a plurality of semiconductor channel nanosheet layers **1006** surrounded by high-k dielectric material **1018**. The semiconductor channel nanosheet layers **1006** are separated from each other by layers of WF metal A **1004** and WF metal B **1010**. A dummy nitride layer **1008** is formed over the top semiconductor channel nanosheet layer **1006** and is surrounded by a high-k dielectric material **1018**. The dummy nitride layer **1008** is separated from the top semiconductor nanosheet layer **1006** by layers of WF metal A **1004** and WF metal B **1010**. The GAA semiconductor device **1000** also includes S/D epitaxy and junctions **1014** that is fabricated in a similar fashion to S/D epitaxy and junctions **602**, an IL HK layer **1022** that is fabricated in a similar fashion to IL HK layer **702**, spacers **1020** that is fabricated in a similar fashion to spacers **702**, and a gate **1050** that is fabricated in a similar fashion to the gate **820** described above with reference to FIGS. **8**A-**8**B and that includes a high-k dielectric material **1018**, the WF metal A **1004**, the WF metal B **1010**, and the gate fill metal **1012**.

[0042] FIG. **11**A is a cross sectional view across the gate line direction of a GAA semiconductor device **1100** constructed with a second threshold voltage, V_{th2}, depicted in accordance with an illustrative embodiment. FIG. **11**B is a cross sectional view along the gate line direction of the GAA semiconductor device **1100** depicted in accordance with an illustrative embodiment. GAA semiconductor device **1100** is similar to GAA semiconductor device **300** illustrated in FIGS. **8**A & **8**B. GAA semiconductor device **1100** includes a silicon substrate **1102** and a plurality of semiconductor channel nanosheet layers **1106** surrounded by high-k dielectric material **1118**. The semiconductor channel nanosheet layers **1106** are separated from each other by layers of WF metal A **1104** and WF metal B **1110**. A dummy nitride layer **1108** is formed over the top semiconductor channel nanosheet layer **1106** and is surrounded by a high-k dielectric material **1118**. The dummy nitride layer **1108** is separated from the top semiconductor nanosheet layer **1106** by layers of WF metal A **1104** and WF metal B **1110**. The GAA semiconductor device **1100** also includes S/D epitaxy and junctions **1114** that is fabricated in a similar fashion to S/D epitaxy and junctions **602**, an IL HK layer **1122** that is fabricated in a similar fashion to IL HK layer **702**, spacers **1120** that is fabricated in a similar fashion to spacers **702**, and a gate **1150** that is fabricated in a similar fashion to the gate **820** described above with reference to FIGS. **8**A-**8**B and that includes a high-k dielectric material **1118**, the WF metal A **1104**, the WF metal B **1110**, and the gate fill metal **1112**.

[0043] The GAA semiconductor device **1100** has a thicker suspension thickness for the WF metal A **1104** than the suspension thickness for the WF metal A **1004** for GAA semiconductor device **1000**. Thus, the WF metal A **1104** only partially fills the gaps between adjacent ones of the semiconductor channel nanosheet layers **1106** and the gap between the top semiconductor channel nanosheet layer **1106** and the dummy nitride nanosheet layer **1108**. However, the WF metal A **1104** completely fills the gaps between adjacent ones of the semiconductor channel nanosheet layers **1106** and the gap between the top semiconductor channel nanosheet layer **1106** and the dummy nitride nanosheet layer **1108**. This results in GAA semiconductor device **1100**

having a different threshold voltage, V_{th2}, than the threshold voltage, V_{th1}, of GAA semiconductor device **1000**.

[0044] Turning next to FIG. **12**, a flowchart of a process for fabricating a GAA semiconductor device with stacked nanosheets and a dummy nitride layer is depicted in accordance with an illustrative embodiment. The process illustrated in FIG. **12** can be implemented to perform the steps described for fabricating a stacked nanosheet structure depicted in FIGS. **3**A&B-**8**A&B.

[0045] The process begins by forming a dummy gate and a dummy nanosheet over stacked nanosheets (step **1200**). Next a gate spacer is formed by the dummy gate and the fins are chopped from the device (step **1202**). Inner spacers are then formed (step **1204**) after which, source/drain epitaxial layers and junctions are formed (step **1206**). Next, an IL HK dielectric is formed over the top of the device and the dummy gate and sacrificial layers are removed (step **1208**). Next, the voids created by removing the sacrificial layers and the dummy gate are filled with HK dielectric material, work function metals A and B, and gate fill materials, after which CMP is performed as described above with reference to FIGS. **8**A & **8**B.

[0046] In some alternative implementations of an illustrative embodiment, the function or functions noted in the blocks may occur out of the order noted in the figure. For example, in some cases, two blocks shown in succession may be performed substantially concurrently, or the blocks may sometimes be performed in the reverse order, depending upon the functionality involved. Also, other blocks may be added in addition to the illustrated blocks in a flowchart or block diagram.

[0047] For example, additional steps showing forming semiconductor channel or other materials for forming metal or dielectric layers may be present although not described in the flowcharts. In yet another illustrative example, one or more additional logic devices may be fabricated along with stacked nanosheet structure.

[0048] The process utilized to create the structure, results in stacked nanosheet structures, such as stacked nanosheet MOSFETs with more uniform work function of the work function metals as compared with prior art devices. Also, the disclosed processes result in stacked nanosheet structures with better V_{th} control.

[0049] The methods and structures that have been described above with reference to figures in the different examples, may be employed in any electrical device including integrated circuit chips. The integrated circuit chips including the disclosed structures and formed using the disclosed methods may be integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either an intermediate product, such as a motherboard, or an end product. The end product can be any product that includes integrated circuit chips, including computer products or devices having a display, a keyboard or other input device, and a processor unit.

[0050] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiment. The terminology used herein was chosen to best explain the principles of the embodiment, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed here.

[0051] The flowchart and block diagrams in the Figures illustrate the architecture, functionality, and operation of possible implementations of systems, methods and computer program products according to various embodiments of the present invention. In this regard, each block in the flowchart or block diagrams may represent a module, segment, or portion of code, which comprises one or more executable instructions for implementing the specified logical function (s). It should also be noted that, in some alternative implementations, the functions noted in the block may occur out of the order noted in the figures. For example, two blocks shown in succession may, in fact, be executed substantially concurrently, or the blocks may sometimes be executed in the reverse order, depending upon the functionality involved. It will also be noted that each block of the block diagrams and/or flowchart illustration, and combinations of blocks in the block diagrams and/or flowchart illustration, can be implemented by special purpose hardware-based systems that perform the specified functions or acts, or combinations of special purpose hardware and computer instructions.

What is claimed is:

1. A gate all around (GAA) stacked nanosheet field effect transistor (FET), comprising:

a plurality of stacked semiconductor channel nanosheet layers;

a dummy nanosheet layer formed above a top one of the stacked semiconductor channel nanosheet layers, the dummy nanosheet layer formed from a dielectric material;

a high dielectric constant (high-k) material formed around each of the plurality of stacked semiconductor channel nanosheet layers and around the dummy nanosheet layer; and

a first work function (WF) metal formed around the plurality of stacked semiconductor channel nanosheet layers and the dummy nanosheet layer.

2. The GAA stacked nanosheet FET of claim **1**, wherein a top thickness of the first WF metal above the top one of the stacked semiconductor channel nanosheet layers is equal to a bottom thickness of the first WF metal below the top one of the stacked semiconductor channel nanosheet layers.

3. The GAA stacked nanosheet FET of claim **1**, further comprising a second WF metal formed around the first WF metal.

4. The GAA stacked nanosheet FET of claim **1**, wherein the first WF metal only partially fills first gaps between adjacent ones of the plurality of stacked semiconductor channel nanosheet layers and wherein the first WF metal only partially fills a second gap between the top one of the plurality of stacked semiconductor channel nanosheet layers and the dummy nanosheet layer.

5. The GAA stacked nanosheet FET of claim **1**, wherein the first WF metal completely fills first gaps between adjacent ones of the plurality of stacked semiconductor channel nanosheet layers and wherein the first WF metal completely fills a second gap between the top one of the plurality of stacked semiconductor channel nanosheet layers and the dummy nanosheet layer.

6. The GAA stacked nanosheet FET of claim **1**, wherein a thickness of each of the plurality of stacked semiconductor channel nanosheet layers is between 6 nanometers (nm) and 20 nm.

7. The GAA stacked nanosheet FET of claim **1**, wherein a thickness of the first WF metal around each of the plurality of stacked semiconductor channel nanosheet layers is between 1 nanometer (nm) and 10 nm.

8. The GAA stacked nanosheet FET of claim **1**, further comprising a single gate for all of the plurality of stacked semiconductor channel nanosheet layers.

9. The GAA stacked nanosheet FET of claim **1**, wherein each of the plurality of stacked semiconductor channel nanosheet layers comprises silicon.

10. The GAA stacked nanosheet FET of claim **1**, wherein the dummy nanosheet layer comprises silicon nitride.

11. The GAA stacked nanosheet FET of claim **1**, wherein the first WF metal comprises one of tungsten and cobalt.

12. A method for forming a gate all around (GAA) stacked nanosheet field effect transistor (FET), comprising:

forming alternating layers of sacrificial epitaxial nanosheet layers and semiconductor channel nanosheet layers; and

forming a dummy nanosheet layer over the top of a top sacrificial epitaxial nanosheet layer, the dummy nanosheet layer comprising a dielectric material.

13. The method of claim **12**, further comprising:

removing the sacrificial epitaxial nanosheet layers;

forming a high dielectric constant material layer around each of the semiconductor channel nanosheet layers and the dummy nanosheet layer; and

forming a first work function (WF) metal around the high dielectric constant material layer.

14. The method of claim **13**, further comprising:

forming a second WF metal around the first WF metal.

15. The method of claim **13**, wherein the first WF metal only partially fills first gaps between adjacent ones of the plurality of stacked semiconductor channel nanosheet layers and wherein the first WF metal only partially fills a second gap between the top one of the plurality of stacked semiconductor channel nanosheet layers and the dummy nanosheet layer.

16. The method of claim **13**, wherein the first WF metal completely fills first gaps between adjacent ones of the plurality of stacked semiconductor channel nanosheet layers and wherein the first WF metal completely fills a second gap between the top one of the plurality of stacked semiconductor channel nanosheet layers and the dummy nanosheet layer.

17. The method of claim **13**, wherein a thickness of each of the plurality of stacked semiconductor channel nanosheet layers is between 6 nanometers (nm) and 20 nm.

18. The method of claim **13**, wherein a thickness of the first WF metal around each of the plurality of stacked semiconductor channel nanosheet layers is between 1 nanometer (nm) and 10 nm.

19. The method of claim **13**, wherein the dummy nano sheet layer comprises silicon nitride.

20. The method of claim **13**, wherein the first WF metal comprises one of tungsten and cobalt.

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