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(54) **INTEGRATED FREEWHEELING DIODE AND EXTRACTION DEVICE**

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(52) **U.S. Cl.**

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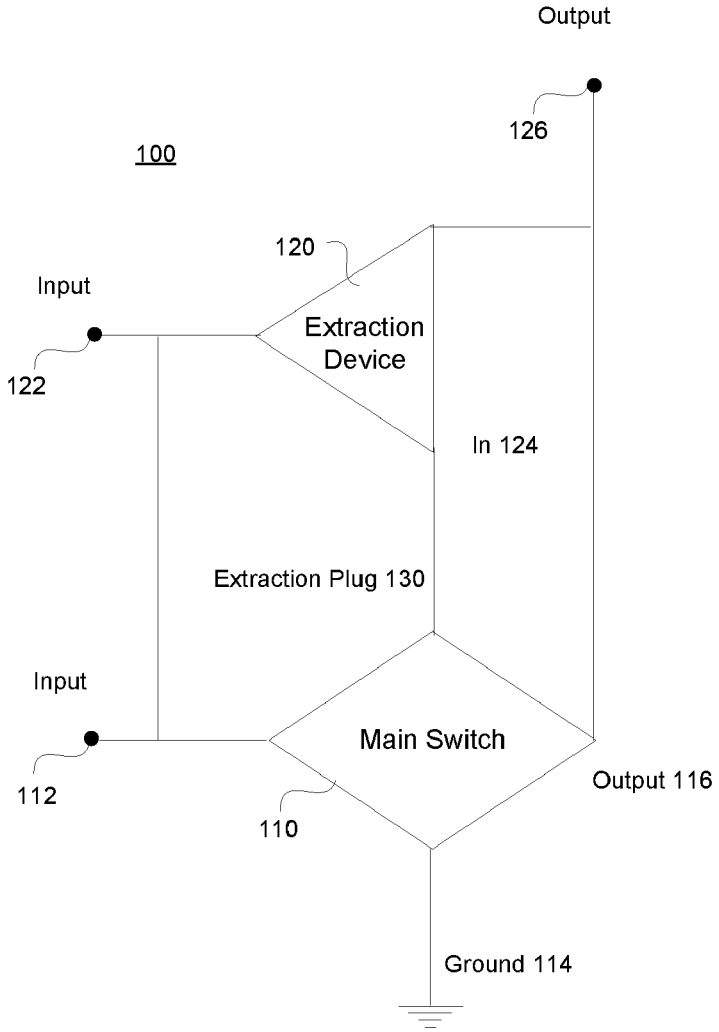
(57) **ABSTRACT**

A Freewheeling Diode of any kind (Fast Recovery Diode, Schottky Barrier Diode or other variants) is integrated with a Forced Extraction Device and in this way two entirely different functions—the Free-Wheeling function and the Forced Extraction function are combined in one device, simplifying the circuit and reducing the number of components. The FWD part of the integrated device is standard in the industry, but the Forced Extraction Device is made using a lateral or vertical PMOS with a votage capability between a control input and the output terminals that is as high or higher than the rating voltage of the Main Switch that will be used together with the FWD.



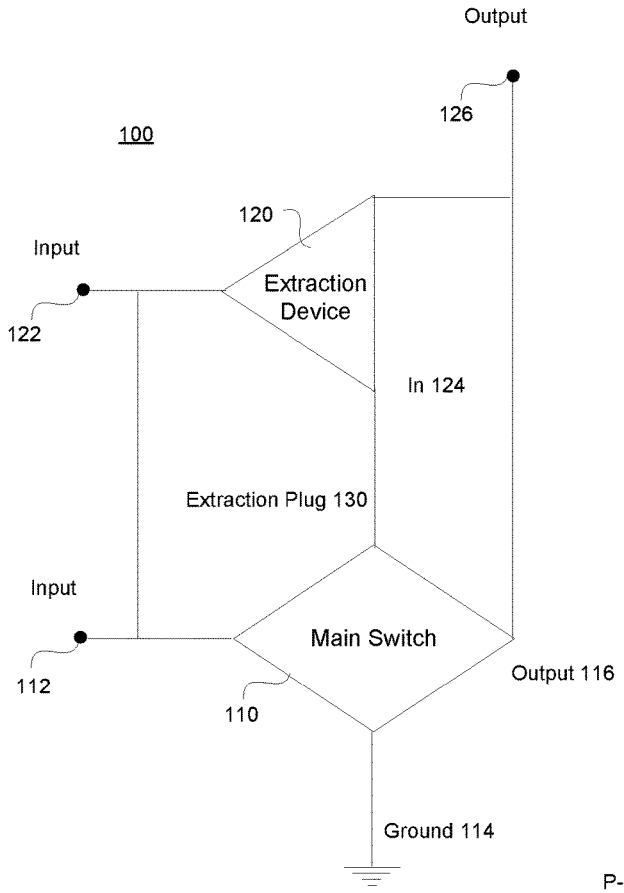

Output
126
100
120
Input
Extraction Device
122
In 124
Extraction Plug 130
Input
Main Switch
Output 116
112
110
Ground 114

FIG. 1

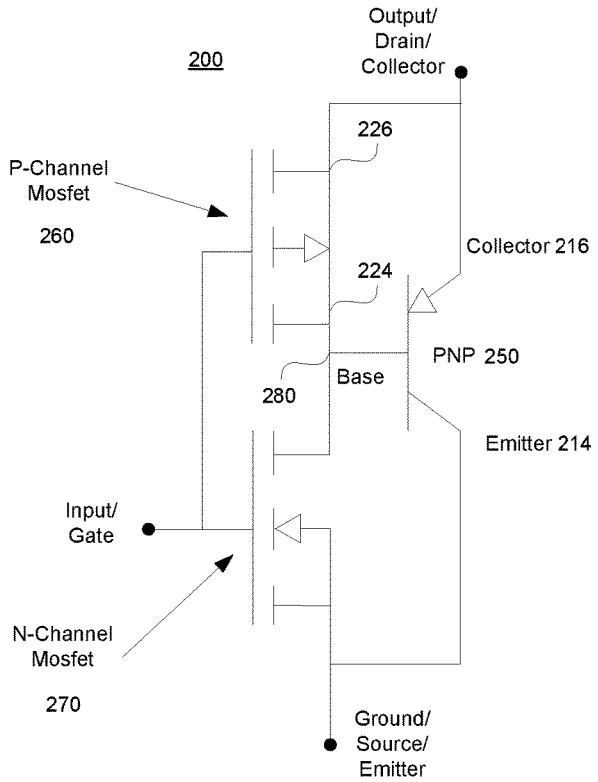

200
Output/ Drain/ Collector
226
P-Channel Mosfet
260
Collector 216
224
PNP 250
Base
280
Emitter 214
Input/ Gate
N-Channel Mosfet
270
Ground/ Source/ Emitter

FIG. 2

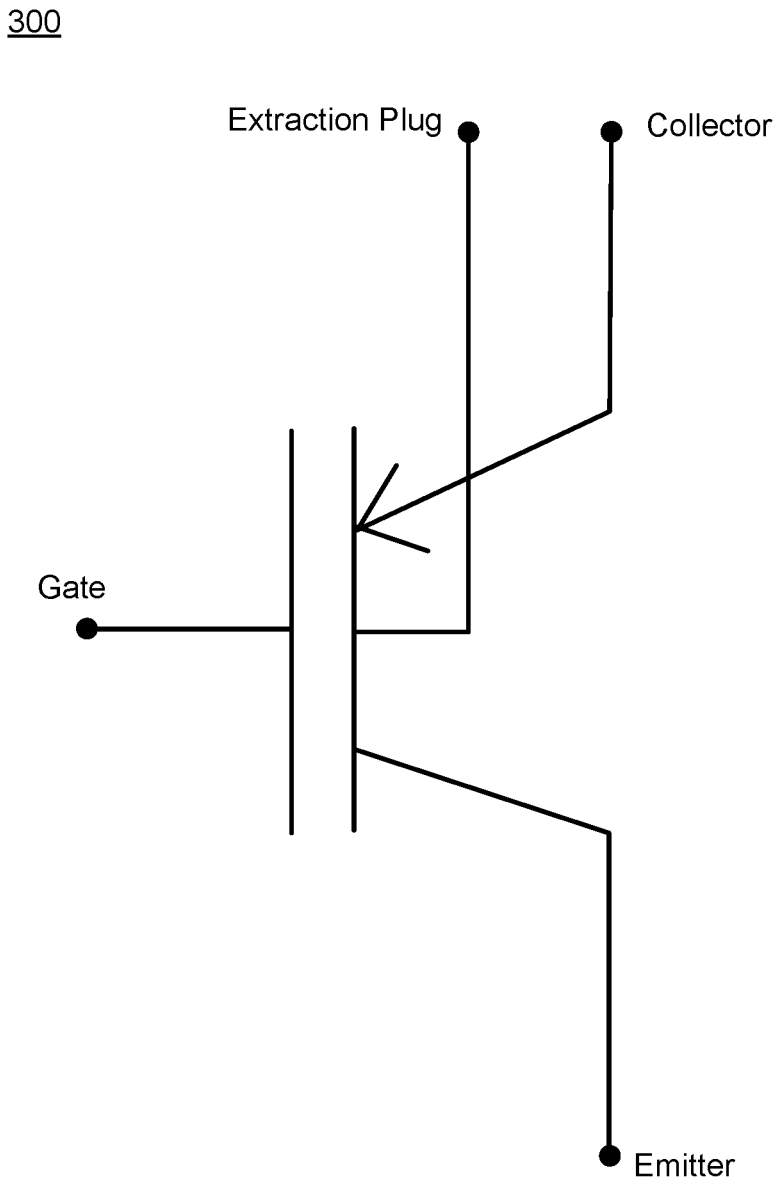


FIG. 3

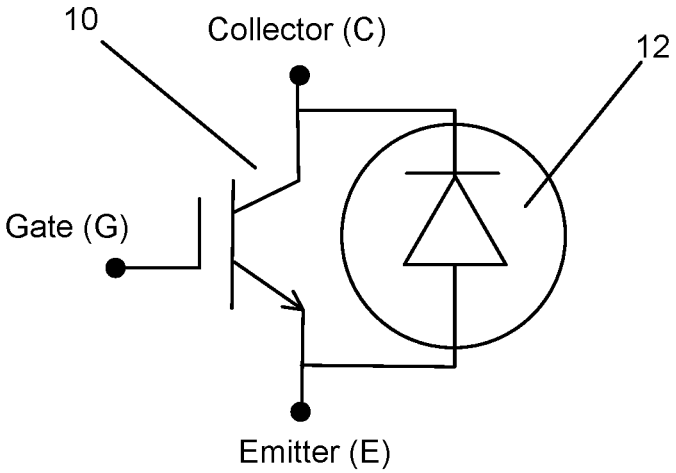


FIG. 4
(prior art)

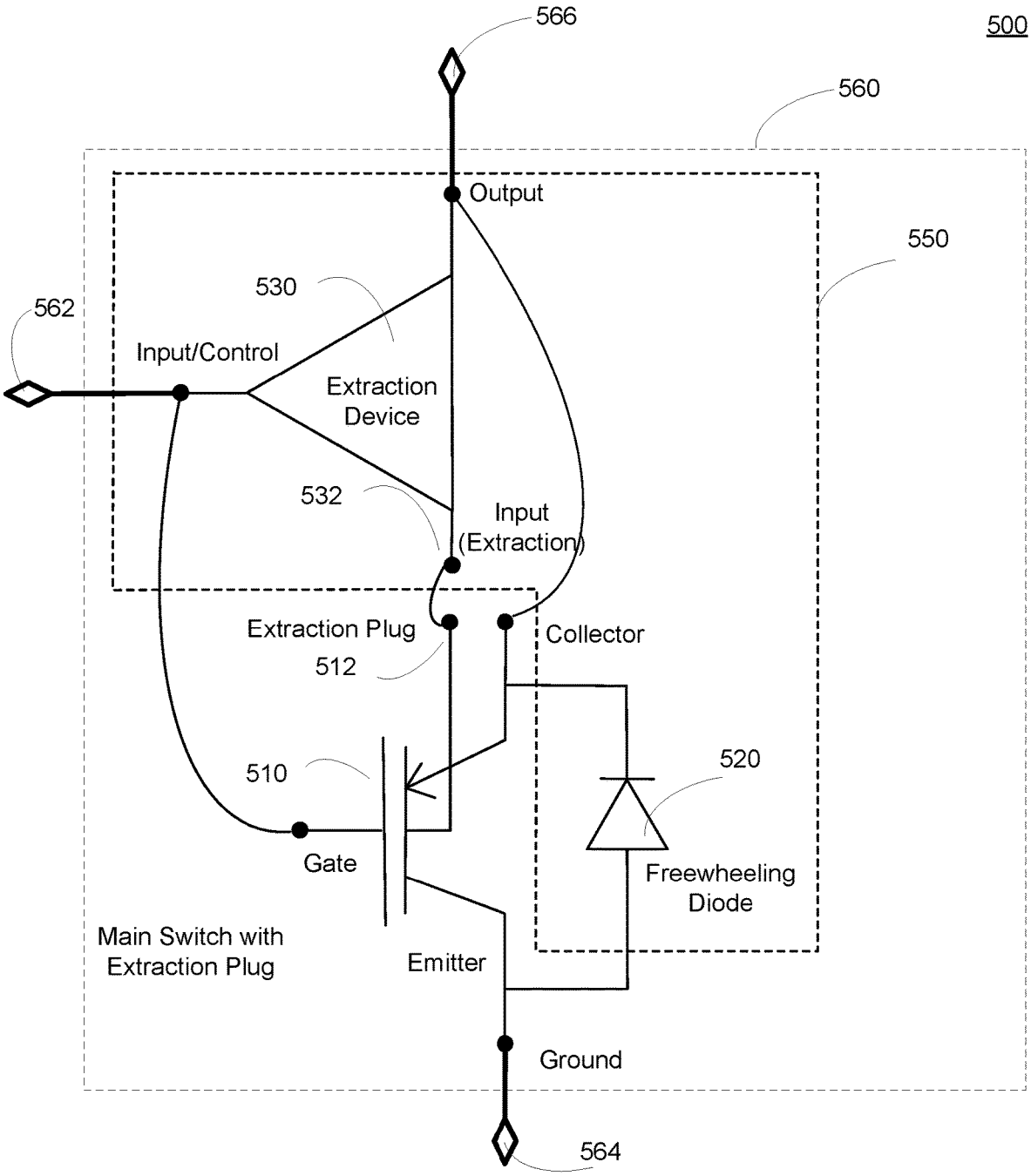

566
500
560
Output
550
530
562
Input/Control
Extraction
Device
532
Input
(Extraction)
Extraction Plug
512
Collector
510
520
Gate
Freewheeling
Diode
Main Switch with
Extraction Plug
Emitter
Ground
564

FIG. 5

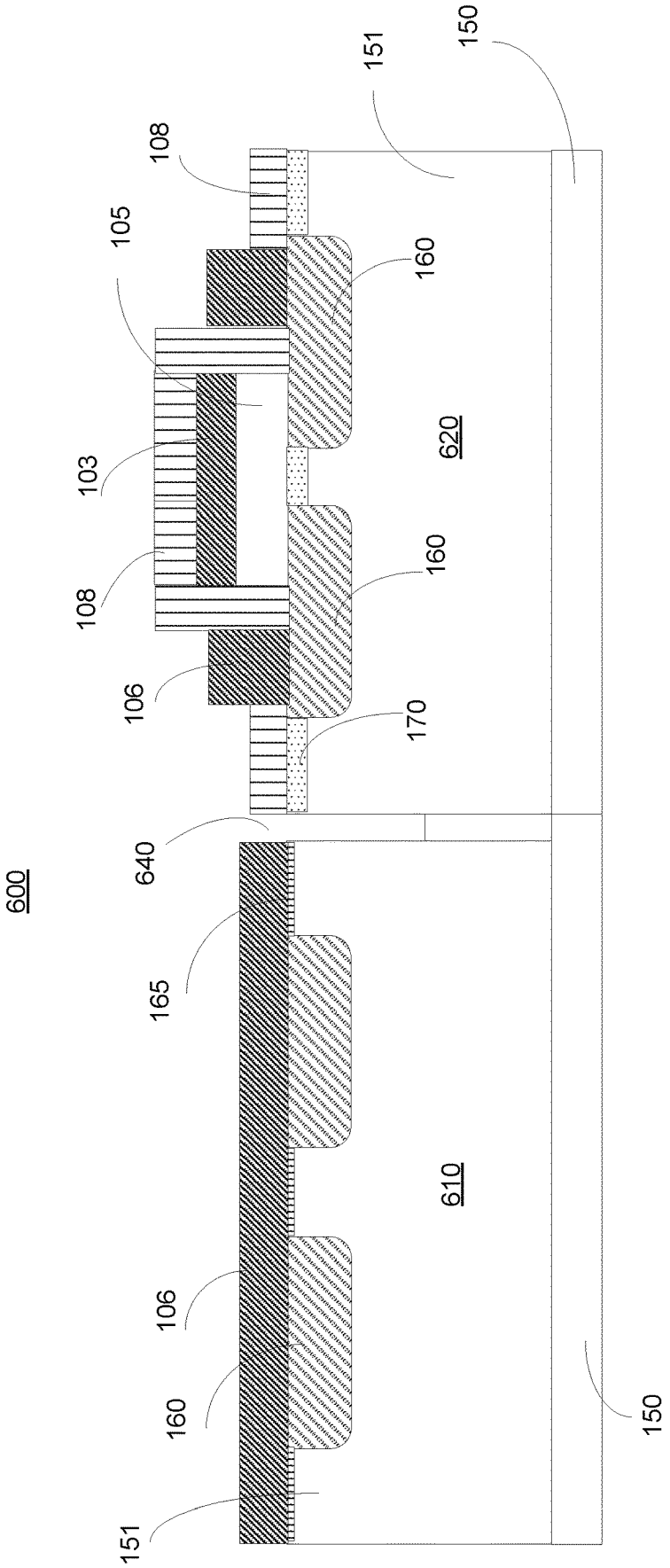


FIG. 6

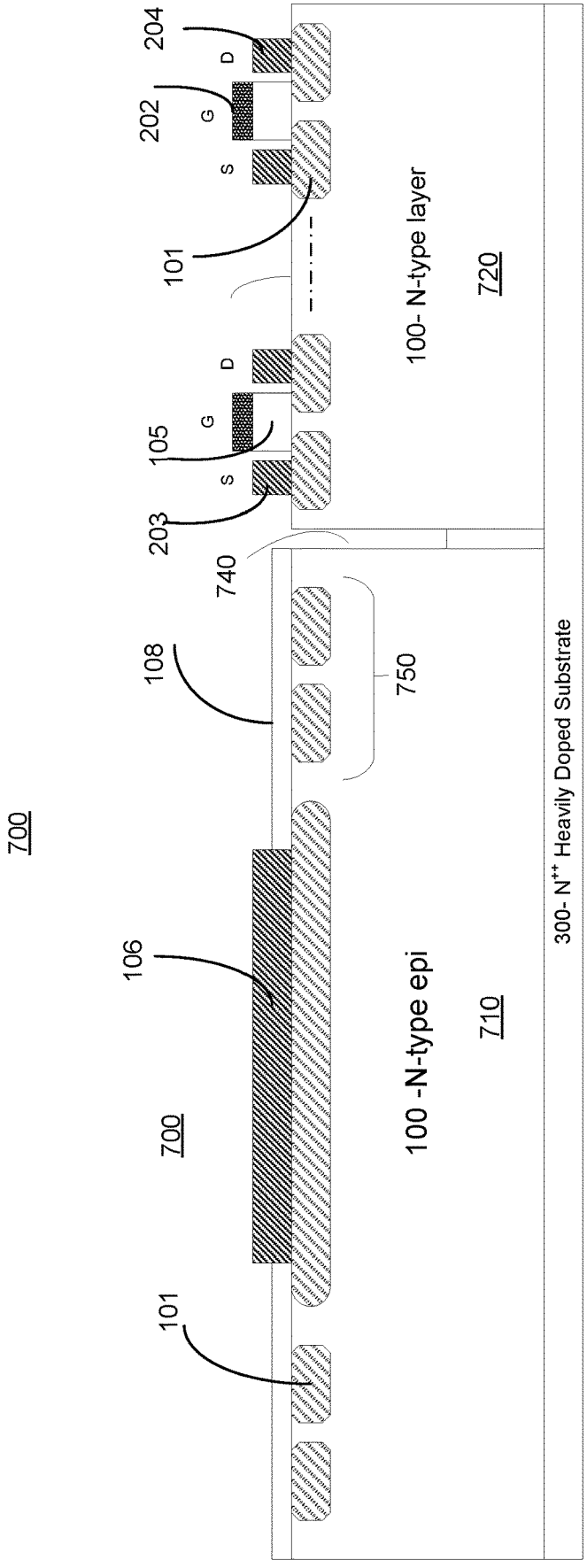

700
204
202
101
105
203
740
108
750
106
101
D
G
S
D
G
S
100- N-type layer
720
100 -N-type epi
710
300- N++ Heavily Doped Substrate

FIG. 7

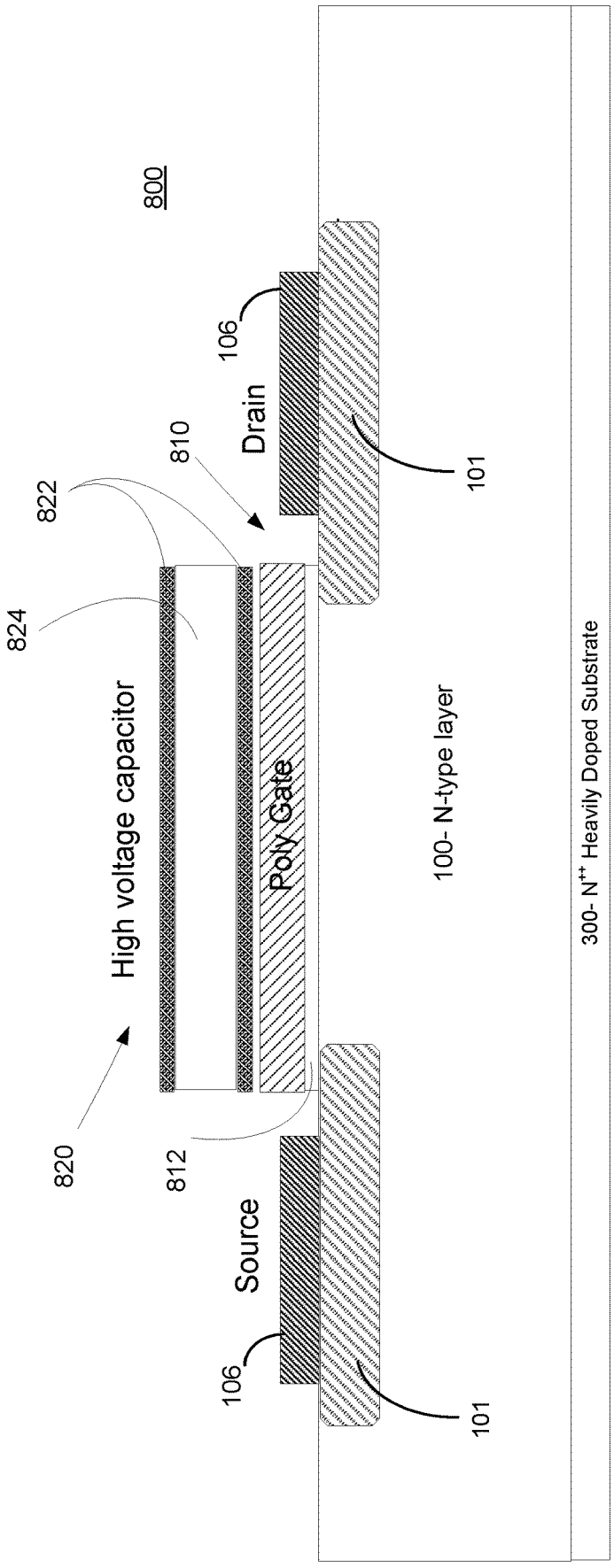

800
106
Drain
810
822
824
High voltage capacitor
Poly Gate
820
812
Source
106
101
101
100- N-type layer
300- N++ Heavily Doped Substrate

FIG. 8

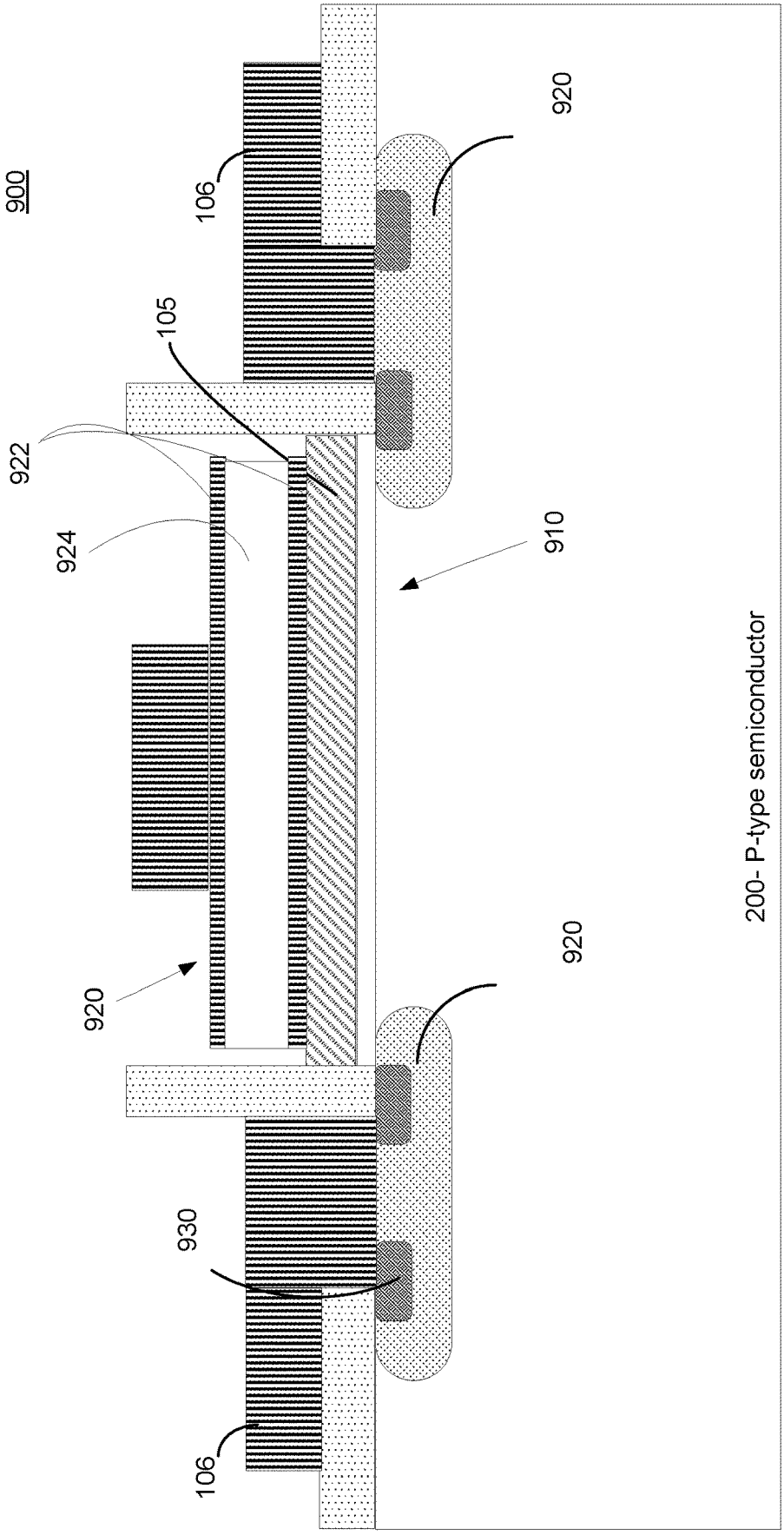

900
106
920
105
922
924
910
920
920
930
106
200- P-type semiconductor

FIG. 9

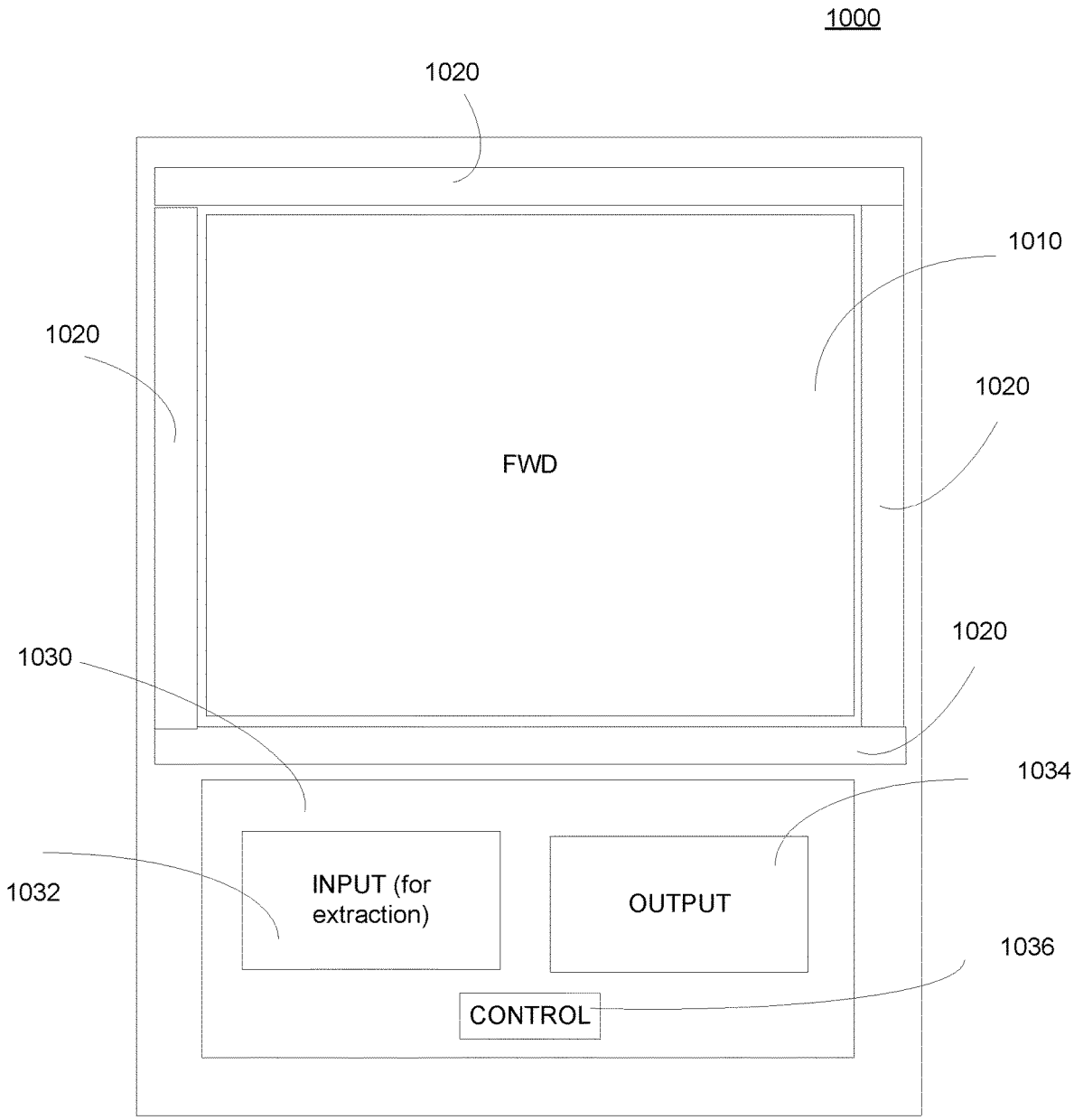

1000
1020
1010
1020
FWD
1020
1020
1030
1034
1032
INPUT (for extraction)
OUTPUT
1036
CONTROL

FIG. 10

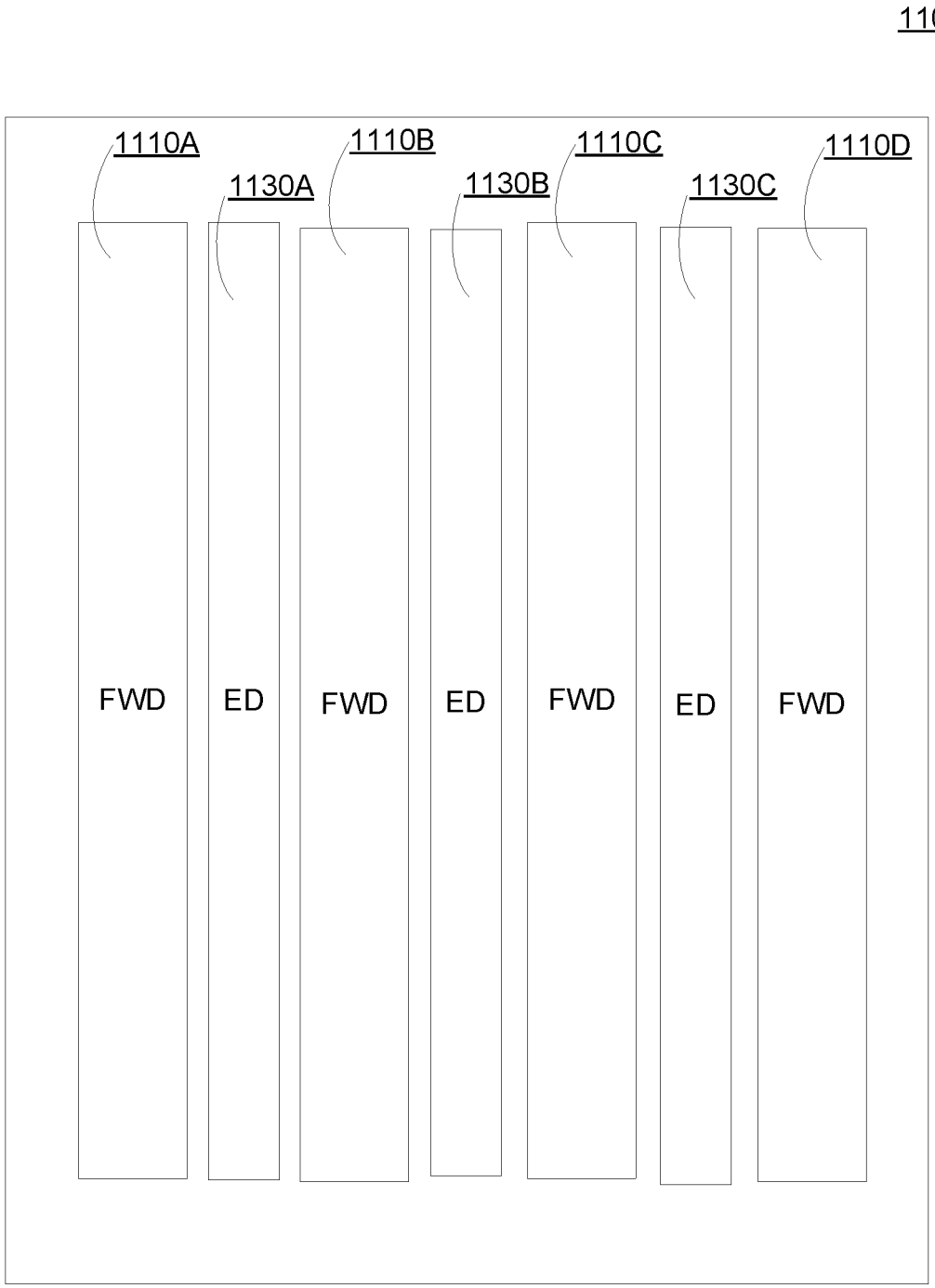

1100
1110A
1110B
1110C
1110D
1130A
1130B
1130C
FWD
ED
FWD
ED
FWD
ED
FWD

FIG. 11

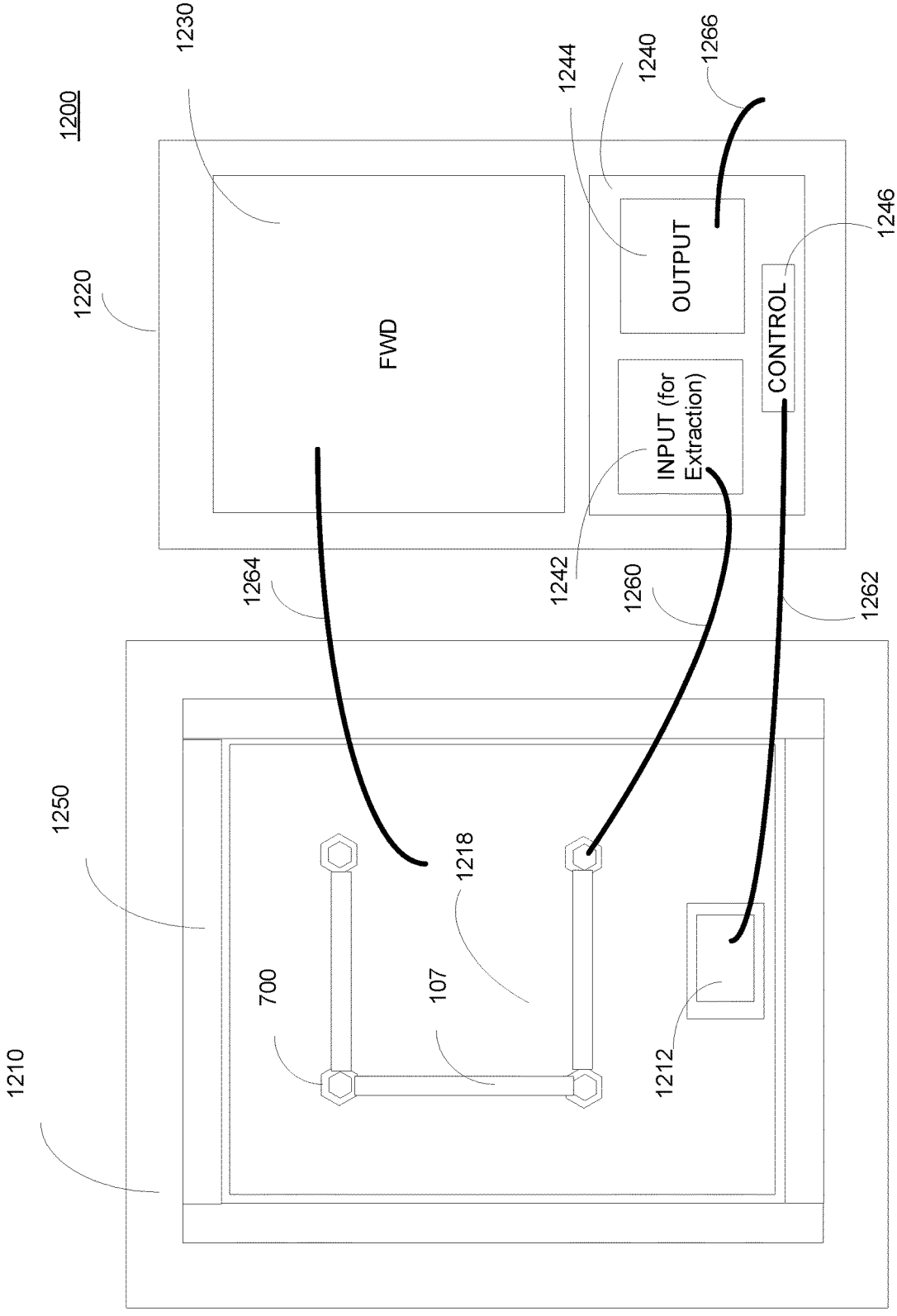

1200
1230
1244
1240
1266
1246
1220
FWD
OUTPUT
CONTROL
INPUT (for Extraction)
1264
1242
1260
1262
1250
1218
700
107
1212
1210

FIG. 12

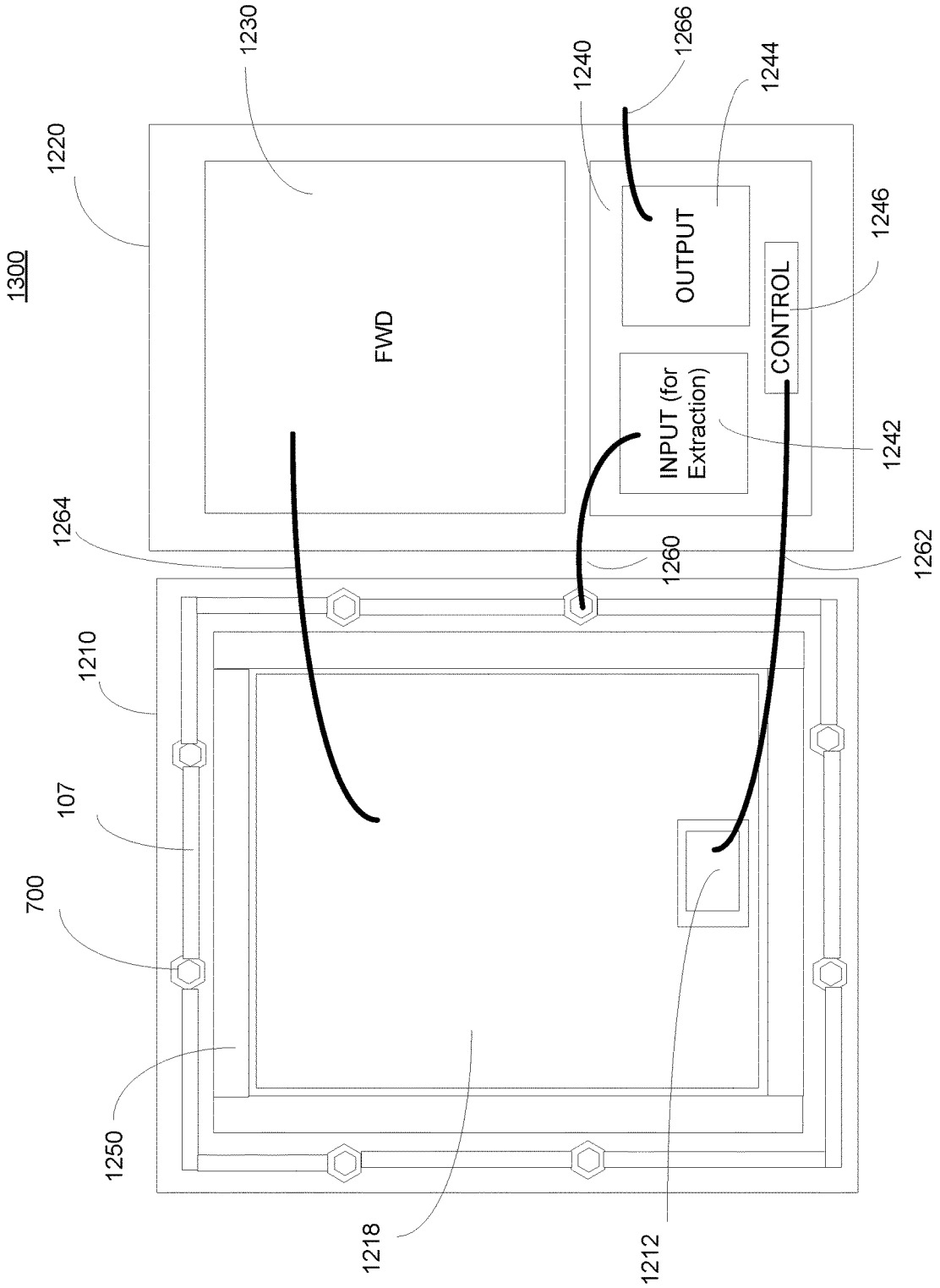

1300
1220
1230
1240
1266
1244
1246
FWD
OUTPUT
CONTROL
INPUT (for Extraction)
1242
1264
1260
1262
1210
107
700
1250
1218
1212

FIG. 13

INTEGRATED FREEWHEELING DIODE AND EXTRACTION DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application Ser. No. 17/496,658, filed Oct. 7, 2021, which is a non-provisional of and claims benefit to U.S. provisional patent application No. 63/093,701, filed Oct. 19, 2020, entitled SEMICONDUCTOR STRUCTURE HAVING A FORCED EXTRACTION DEVICE, the disclosure of which is incorporated herein by reference in its entirety. This application is also related to U.S. patent application Ser. No. 17/339,832, filed Jun. 4, 2021, entitled POWER SEMICONDUCTOR DEVICE WITH FORCED CARRIER EXTRACTION AND METHOD OF MANUFACTURE, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] This disclosure relates to semiconductor devices, and, more particularly, to a semiconductor structure that includes a Freewheeling Diode coupled to a forced carrier Extraction Device that improves the switching speed of a Main Switch for which the turn-off process depends on the recombination speed of charge carriers.

BACKGROUND

[0003] The previously incorporated U.S. patent application Ser. No. 17/339,832 describes problems with long turn-off times in power semiconductor switches and a solution that uses a forced carrier Extraction Device. Some power semiconductor devices that carry relatively large amounts of current include a Freewheeling Diode (FWD), especially those that operate on inductive loads. In power circuits like push-pull, half-bridge or full-bridge modules, the Freewheeling Diode is connected in parallel to the main semiconductor switch. Some power switches, like Mosfets, have a "built in" diode, which can be used as a Freewheeling Diode. In such cases, special process steps are used to shorten the reverse recovery time and lower the reverse recovery charge of the FWD, as this charge contributes to the turn-on switching energy of the Main Switch.

[0004] Insulated Gate Bi-Polar Transistors (IGBTs) are widely used for a broad range of power semiconductors since their features are well suited for such roles. IGBTs include a built-in diode, but the built-in diode cannot be used as a FWD because of the P-type injector layer, which causes the built-in diode of the IGBT on the backside of the IGBT to have an orientation opposite that of a Mosfet. The diode in an IGBT is formed at the intersection of the P-wells and N-type drift layer, for instance, or at the intersection of an N-well for a P-type IGBT. The injector layer of the IGBT provides the conductivity modulation of the drift region while the IGBT is conducting, which makes the IGBT such a well-performing device from an on-conduction point of view. But this same injector layer prevents the built-in diode in an IGBT from acting as an FWD, which is why nearly all IGBTs are equipped with a separate FWD in most power applications.

[0005] Recently, Silicon Carbide Schottky Barrier Diodes (SiC SBDs) have been replacing Silicon FWDs in commercial products. An SBD formed on SiC has a lower forward voltage and no reverse recovery charge, and therefore its contribution to the turn-on energy loss of the Main Switch, such as when an IGBT is used for the Main Switch, is due only to the charge stored in the depletion region of the SBD.

[0006] Another effect of the existence of the injector layer opposite to the Mosfet makes the turn-off process of a Main Switch that employs conductivity modulation, such as an IGBT, very slow, due to the need of the injected carriers to "disappear" through recombination when the IGBT turns off.

[0007] Special process steps that control the level of injection or the recombination rate are widely used to speed up the turn-off time of power semiconductors that use conductivity modulation. Providing such a switch, such as an IGBT, with an ability or structure to remove excess charge in the drift region and therefore lower the turn-off energy of the power semiconductor, is a worthwhile goal.

[0008] State-of-the-art IGBTs lack the means to access the region where the carriers contributing to the conductivity modulation recombine. Extraction Plugs, which are described in detail in the incorporated '832 application, may be formed or placed inside the Main Switch, such as an IGBT, such that the electrical performance of the Main Switch is not degraded in any way. Although such Extraction Plugs may speed up a power semiconductor switch when coupled to an Extraction Device to remove charge in the drift region during the turn-off process of the switch, forming the Extraction Device itself may involve extra process steps compared to forming the IGBT itself.

[0009] Embodiments of the disclosure address these and other limitations of the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. **1** is a conceptual schematic diagram of a switch having an Extraction terminal, connected to a voltage-controlled Extraction Device, according to embodiments of this disclosure.

[0011] FIG. **2** is a schematic diagram of a complementary IGBT having an injecting PNP transistor, as well as a P-channel MOSFET, and an N-channel MOSFET coupled in series, according to embodiments of the disclosure.

[0012] FIG. **3** is a simplified schematic diagram illustrating an IGBT switching device, having emitter, collector, and gate terminals, and further illustrating an Extraction Plug connection, to which an Extraction Device may be connected, according to embodiments of the disclosure.

[0013] FIG. **4** is a schematic of a known voltage-controlled Main Switch, such as an IGBT, having a freewheeling diode connected in parallel to the switch.

[0014] FIG. **5** is a schematic diagram illustrating a Main Switch, a Freewheeling Diode, and an Extraction Device, according to embodiments of the invention.

[0015] FIG. **6** is a cross-sectional diagram of a Freewheeling Diode and an Extraction Device, according to embodiments of the invention.

[0016] FIG. **7** is a cross-sectional diagram illustrating a Freewheeling Diode, high-voltage termination, and a multicell PMOS formed on a semiconductor substrate, according to embodiments of the invention.

[0017] FIG. **8** is a cross-sectional diagram of a lateral PMOS Extraction Device and a high voltage capacitor according to embodiments of the invention.

[0018] FIG. **9** is a cross-sectional diagram of a vertical PMOS Extraction Device and a high voltage capacitor according to embodiments of the invention.

[0019] FIG. **10** is a top layout view of an integrated FWD with an Extraction Device, placed outside of the high voltage termination of the FWD, according to embodiments of the invention.

[0020] FIG. **11** is a top layout view of an integrated FWD with an Extraction Device, interspaced in the active area of the die, according to embodiments of the invention.

[0021] FIG. **12** is a top layout view of a voltage controlled Main Switch having an output on the backside of the die, according to embodiments of the invention.

[0022] FIG. **13** is a top assembly view of a voltage controlled Main Switch having Extraction Plugs formed around an edge of the die, according to embodiments of the invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0023] The present disclosure relates to the field of power semiconductors with conductivity modulation, like IGBTs and its variants, which are structured or used to switch inductive loads. When switching inductive loads, a Free-wheeling Diode is commonly used when the switching device, like the IGBT, has to commutate On and Off current through an inductance. Thus, although IGBTs remain an excellent choice for those semiconductor devices carrying relatively large amounts of current, so called power devices, the slow switching speeds caused by the slow recombination of minority carriers in conductivity-modulation bipolar devices after switching off continues to inhibit their performance. Including Extraction Plugs and an Extraction Device in a three terminal device that uses conductivity modulation can greatly improve its switching speed, as described below.

[0024] Benefits of including an Extraction Device in conjunction with a power semiconductor device are described with reference to FIGS. **1-3**. Benefits of including FWDs with power semiconductor devices that also include an Extraction Device are described with reference to FIGS. **4-13**.

[0025] FIG. **1** is a conceptual schematic diagram of a combined device **100** that generally includes a Main Switch **110** coupled to an Extraction Device **120**. The device **100** further includes one or more Extraction Plugs **130** formed in the drift layer of the Main Switch **110**. Extraction Plugs are fully described in the previously incorporated U.S. patent application Ser. No. 17/339,832. In general, Extraction Plugs may be formed in devices that use conductivity modulation to provide access to a drift layer of the device. The Extraction Plugs **130** are formed and placed so that they do not degrade, in any way, the performance of the structure **100**, especially its blocking voltage. An Extraction Device **120**, also described in the '832 application, turns on when the Main Switch **110** turns off. If the Main Switch is embodied by a device that uses conductivity modulation, such as an IGBT, the Extraction Device **120** works to remove charge carriers left over in the bulk region when the Main Switch **110** turns off through the Extraction Plug **130** of the Main Switch. The forced Extraction Device **120** is preferably voltage controlled, and its blocking voltage between terminals is generally the same or higher than the blocking voltage of the Main Switch **110**.

[0026] The structure **100** of FIG. **1** may be structured as a three-terminal device. The structure **100** includes an input terminal coupled to an input **112** of the Main Switch **110** and to an input **122** of the Extraction Device **120**, and an output terminal **126** coupled to an output of the Extraction Device **120**. The structure **100** further includes a ground terminal **114** coupled to the Main Switch **110**. Because the inputs **112**, **122** of the Main Switch **110** and Extraction Device **120** are tied together, the input signal driving the input **112** of the Main Switch **110** also drives the input **122** of the Extraction Device **120**.

[0027] The Extraction Device **120** may be integrated on the same die as the Main Switch **110**, or it may be a discrete device formed on a separate semiconductor substrate that is electrically coupled to the Main Switch. In some embodiments the semiconductor substrate for the Main Switch and a semiconductor substrate for the Extraction Device **120** may be separate substrates but assembled together in a single module or even in a single package.

[0028] The structure **100** of FIG. **1** conceptually operates as indicated as in Table 1:

TABLE 1

Operational States of Main Device and Extraction Device

Device/State	Turn On	Turn Off	Input-Ground Voltage	Output-Ground Voltage
Main Device	On	Off	Low	High
Extraction Device	OFF	On	High	Low

[0029] In operation, when the Main Switch **110** is ON, the Extraction Device **120** is OFF, and vice-versa. In device operation, i.e., when the Main Switch **110** is conducting, the Extraction Device **120** does not interfere or affect the operation of the Main Switch **110**. In other words, the operating parameters of a Main Switch **110** coupled to the Extraction Device **120** are the same or similar as a Main Switch that is not coupled to an Extraction Device. The Main Switch **110** has a low breakdown voltage between the input and ground terminals, but a relatively high breakdown voltage between the output and ground terminals. Conversely, the Extraction Device **120** has a high breakdown voltage between its input and ground terminals, and a relatively low breakdown voltage between the ground and the output terminals.

[0030] FIG. **2** is a schematic diagram of a circuit **200** including components that may be used to form an example embodiment **200** that functions as the structure **100** of FIG. **1**. The circuit **200** includes an IGBT Main Switch, which is formed of a PNP transistor **250** as an injector and an N-channel Mosfet **270** that drives the PNP transistor. A P-channel Mosfet **260** functions as the Extraction Device **120** of FIG. **1**. The Mosfets **260** and **270** are coupled in series. The device **200** may be integrated on a single semiconductor die. In other embodiments, as described above, the P-Channel Mosfet **260** may be formed on a separate semiconductor die and electrically connected to the N-Channel Mosfet **270**. Internal components of the IGBT Main Switch further include a collector **216**, and an emitter **214**. The P-Channel Mosfet **260**, which operates as the Extraction Device, includes a source **224** and a drain **226**. Since the output terminal of the device **200**, in this configuration, is coupled to both the collector **216** of the IGBT and the drain **226** of the P-Channel Mosfet **260**, it is labeled as Output/Drain/Collector. Similarly, the ground terminal is coupled to the emitter **214** of the IGBT and the source of the N-Channel Mosfet **270**, the ground terminal is labeled Ground/Source/Emitter. Finally, since the input terminal of

the device **200** is coupled to the gates of both the N-Channel Mosfet **270** and the P-Channel Mosfet **260**, the input terminal is labeled Input/Gate. Although it is not separately shown on the schematic diagram of the circuit **200**, an Extraction Plug for the IGBT would be coupled to the base of the PNP transistor **250**, which is in the drift region of the IGBT, and is labeled as reference **280**. Importantly, the Extraction Plug, or reference **280**, is electrically coupled to a source of the P-Channel Mosfet **260**.

[0031] In operation of the device **200**, when the Input/gate voltage is HIGH, the base of the PNP **250** transistor is connected to a ground at the source of the MOSFET **270**, while the device **200** is conducting. Then, when the Input/gate voltage goes LOW, to turn off the device **200**, the N-channel MOSFET **270** turns OFF, while the P-channel MOSFET **260** turns ON. The P-Channel MOSFET **260** turning ON provides a path for excess charge to be removed from the drift region **280** from the source of the P-Channel Mosfet **260** to the drain of the P-Channel Mosfet, which is coupled to the output of the device **200**. The P-Channel MOSFET **260** is formed so that, when the gate voltage is HIGH, the P-Channel MOSFET **260** is OFF, and turns on when the gate voltage goes LOW. At low Vgs voltages of the N-Channel Mosfet **270**, when the Main Switch (IGBT) turns OFF, the P-Channel MOSFET **260** operates similar to that of a resistor, with its drain coupled to the positively bias on the collector **216** of the PNP **250**. Therefore, electrons are pulled toward the positively biased drain electrode of the P-Channel MOSFET **260**, and charge is removed from the drift region **280** at a relatively constant rate. The P-Channel MOSFET **260** provides a path for the charge, carried by electrons, to be removed from the drift layer **280** through the positively charged drain. Recall that one of the main problems for conventional IGBT devices to switch off quickly is that there is no access to the drain of the Mosfet. Instead, the Extraction Device, which here is the P-channel MOSFET **260**, extracts excess carriers relatively quickly from the bulk drift area **280** of the IGBT by conducting them to the collector through the P-channel MOSFET **260**. This action of removing the excess charge carriers when the IGBT turns off significantly decreases the turn-off time of the IGBT.

[0032] The aforementioned Extraction Plugs, or merely plugs, are used to provide access to areas of the bulk semiconductor in conductivity modulation devices. These Extraction Plugs, in turn, may be coupled to the source (i.e, the input or extraction terminal) of an Extraction Device to remove the excess carriers from the conductivity modulation device when the conductivity modulation device is being turned off. This greatly reduces the turn-off time of the conductivity modulation device. Further details of the structure of the Extraction Plugs may be obtained from the '832 application, although embodiments of the invention are applicable to other forms of Extraction Plugs providing the same function as that described herein.

[0033] FIG. **3** is a simple schematic diagram illustrating an IGBT switching device **300**, having emitter, collector, and gate terminals, and further illustrating an Extraction Plug terminal, also called an Extraction Terminal, to which an Extraction Device may be connected. This schematic diagram neatly illustrates the concepts of including one or more Extraction Plugs in the drift region of an IGBT, which, as described above, facilitates the removal of carriers during forced carrier extraction from the drift region through the Extraction Plugs and further through the Extraction Device during turn-off of the Main Switch. The Extraction Plug terminal is electrically connected to the Extraction Plug or Plugs in the IGBT. In application, the Extraction Plug terminal of the IGBT switching device **300** may be further coupled to an Extraction Device, as detailed below. In embodiments where the Extraction Plug and Extraction Device are formed on the same semiconductor substrate, it is not strictly necessary that the Extraction Plug be coupled to an output terminal. In other embodiments, where the Extraction Plug and Extraction Device are formed on different substrates, the Extraction Plug may be coupled to an Extraction Plug Terminal, which, in turn, may be coupled to an Extraction Device located on a different substrate. In this way, the process steps for forming an IGBT having an Extraction Plugs may be optimized separately from the process steps for forming an IGBT.

[0034] Further, recall from above that power switching devices that drive inductive loads nearly always include a Freewheeling Diode (FWD) to protect the switch from over voltage as the switch turns off and the magnetic field around the inductive load collapses. To protect against damage caused by the inductor, a protective FWD is coupled in parallel to the switch. FIG. **4** is a schematic of a known voltage-controlled Main Switch **10**, such as an IGBT, having an FWD **12** connected in parallel to the switch. As described above, some power semiconductor devices that carry relatively large amounts of current include an FWD, especially those that operate on inductive loads. In power circuits like push pull, half-bridge or full-bridge modules, the FWD is connected in parallel to the main semiconductor switch. With reference to FIG. **4**, the IGBT **10** is a bipolar semiconductor device used for carrying relatively large current loads. The IGBT **10** includes emitter, collector, and gate terminals, which function as the input, output, and gate terminals of the switch. The FWD **12** is coupled in parallel to the IGBT, with one terminal of the FWD coupled to the collector and the other terminal coupled to the emitter. In circuits that drive inductive loads, the FWD **12** shunts current from the inductive load across the IGBT **10** as the IGBT turns off, and also limits voltage across the IGBT. Otherwise, the current generated by the collapse of the magnetic field around the inductor would be applied directly to the IGBT **10**, which would likely cause damage. In this way the FWD **12** acts as a protection device for the switch **10**. Also, the FWD **12** is designed and fabricated to withstand the full rated voltage of the Main Switch **10**, including the avalanche rating, or it has to be implemented with a higher blocking voltage than the Main Switch.

[0035] FIG. **5** is a schematic diagram illustrating a system **500** that includes a Main Switch **510** having an Extraction Plug electrode **512**, an FWD **520**, and an Extraction Device **530**, according to embodiments of the invention. Although all of the components illustrated in FIG. **5** may be integrated on a single die, it is possible, and perhaps preferable, that the FWD **520** and an Extraction Device **530** are packaged in a separate device **550**, which is electrically connected to the Main Switch **510**. Also, the Main Switch **510** may be a one semiconductor die, and the separate device **550**, including the FWD **520** and an Extraction Device **530**, is formed on another semiconductor die, but both the semiconductor dies are together in a single semiconductor module or package. More details and discussion of possible layouts is given below.

[0036] System **500** illustrates a three-terminal device capable of driving inductive loads, since the IGBT Main Switch **510** is electrically coupled to the FWD **520**, even though the diode **520** may be formed on a substrate separate from the IGBT Main Switch **510**. Further, since the turn-off time of an IGBT is shortened by coupling an Extraction Device **530** to the Extraction Plug **512** of the IGBT **510**, including an Extraction Device **530** in the system **500** provides the extraction function when the IGBT **510** turns off. Therefore, it may be convenient to produce the IGBT Main Switch **510** with an Extraction Plug terminal **512** separately from a device that includes both an FWD as well as an Extraction Device, such as the device **530**. Thus the system **500** may form a single package or module including one component having the IGBT Main Switch **510** and having another component **550**, which includes the FWD **520** and the Extraction Device **530**. Electrical connections are made within the system **500** as illustrated in FIG. **5**. For instance, a gate of the IGBT Main Switch **510** is electrically coupled to an input of the Extraction Device **530**. The Extraction Plug terminal **512** of the IGBT Main Switch **510** is electrically coupled to an extraction input **532** of the Extraction Device **530**. A collector of the IGBT Main Switch **510** is coupled to an output of the Extraction Device **530**. To finish the connections, a cathode of the FWD **520** is coupled to a collector of the IGBT Main Switch **510**, and the anode of the FWD **520** is coupled to an emitter of the IGBT Main Switch **510**.

[0037] If the system **500** is created in a discrete package **560**, it could be a three-terminal device with an input control terminal **562**, a ground terminal **564**, and an output terminal **566**. Such a package **560** includes an IGBT **510** or Main Switch having an Extraction Plug terminal **512** that is coupled to a component **550**. The component **550** includes an FWD **520** and an Extraction Device **530**. This package **560** includes all of the components for a power device for driving an inductive load having a shortened turn-off time compared to typical IGBTs. In detail, the FWD **520** is effectively mandatory for any power switch operating with an inductive load. Embodiments of the invention further include the Extraction Device **530** to shorten the turn-off time of the voltage-controlled switch device with conductivity modulation **510**. Although the Main Switch **510** is illustrated as being an IGBT, embodiments of the invention extend to any voltage-controlled switch device with conductivity modulation.

[0038] FIG. **6** is a cross-sectional diagram of an integrated device **600** including an FWD **610** and an Extraction Device **620** produced on a same semiconductor substrate, according to embodiments of the invention. In this example, the FWD **610** is a merged PN-Schottky structure. But, the FWD **610** may be any of several different types of FWDs. For example, the FWD **610** may be a PIN (p-type and n-type materials separated by an insulator) diode, and may or may not include materials for shortening carrier lifetimes, such as gold or platinum diffusions, electron or proton irradiations, etc. The FWD **610** may also be a Fast Recovery Diode, for example. Although the FWD **610** and the Extraction Device **620** of the integrated device **600** are formed on the same semiconductor die, they may be separated by a deep trench **640**, which may be formed using standard fabrication techniques. The deep trench **640** separates the cathode of the FWD **520** (FIG. **5**) from the substrate of the lateral PMOS in the Extraction Device **530**. Such separation allows each device to operate virtually independent from one another. It is not necessary that the FWD **610** and the Extraction Device **620** be formed on the same die. In other embodiments the FWD **610** and the Extraction Device **620** may be electrically coupled to one another but formed on separate semiconductor dies. In the illustrated embodiment, the lateral PMOS Extraction Device **620** includes a thick gate oxide **105**. The Extraction Device **620** is also "counter doped" at the surface of the semiconductor to create conditions for a suitable turn-on voltage, Vth. As represented in this cross section of FIG. **6**, the FWD **610** and the PMOS Extraction Device **620** structures could be formed and interspaced in the active area of the die. The device **600** is an example of the type of structure that could make the component **550** part of the device **500** of FIG. **5**.

[0039] Other structures in the integrated device **600** are conventional, such as a polysilicon gate **103**, front metal **106**, passivation layer **108**, substrate **150**, such as SiC or other wide bandgap material, N-type drift region **151**, P-Wells **160**, Schottky Metal **165**, and counter-doped region **170**.

[0040] FIG. **7** is a cross-sectional diagram of a device **700** illustrating an FWD **710**, high-voltage termination **750**, and a multi-cell PMOS Extraction Device **720** formed on any type of semiconductor, such as Silicon, SiC, wide-bandgap material, etc., according to embodiments of the invention. The placement of the Extraction Device **720** in the illustrated embodiment of FIG. **7** is outside of the High Voltage Termination **750** of the FWD **710**, but this placement is not mandatory. The P-Wells **101** of the FWD **710** and Extraction Device **720** can very well operate together to provide a blocking voltage needed for the FWD. Other conventional components of the device **700** not referred to above include a gate **202**, source **203**, and drain **204** of the PMOS transistors in the Extraction Device **720**.

[0041] FIG. **8** is a cross-sectional diagram of a lateral PMOS Extraction Device **800** that includes a PMOS transistor **810** coupled to a high voltage capacitor **820**, according to embodiments of the invention. The capacitor **820** includes electrodes **822** separated by an insulating or dielectric layer **824**. The PMOS transistor **810** includes a thin gate oxide **812**. In some instances the thin gate oxide **812** is easier to produce than a thick gate oxide, used in previous examples, so the thin gate oxide may be preferable. The high voltage capacitor **820** is series coupled to the built-in capacitance of the thin gate oxide **812**. As described above, when a PMOS transistor is used as the Extraction Device, the Extraction Device does not have any substantive function during the DC operation of the Main Switch, i.e., while the Main Switch is fully off or fully on. This means the Extraction Device **800** is OFF when the Main Switch is turned ON and it is ON when the Main Switch gets turned OFF. Given these characteristics, it is possible for an external capacitor with a relatively high voltage rating to be used to seamlessly protect the gate oxide of the PMOS Extraction Device, even when, such as in the Extraction Device **800**, it has a thin gate oxide. This series circuit configuration is possible because the PMOS Extraction Device **800** operates only during the switching on and off of the Main Device (not illustrated in FIG. **8**) to which it is coupled, and the switching control signals also cause the turn-on and turn-off of the PMOS transistor **810** in a seamless way. Further, by using a high-voltage external capacitor **820** in series with the capacitor formed by a polysilicon gate and the gate oxide **812** of the lateral PMOS **810**, the total capacitance of the series con-

nection of these two capacitances can be tailored to adjust the voltage spikes of the gate signal. This protection is important, especially in the case when the Main Switch is made on wide bandgap semiconductors, for which the gate oxides are very thin and therefore very sensitive to voltage spikes. The capacitance of the series connection of the capacitance of the gate oxide **812** of the PMOS **810** and the capacitor **820** itself may range from 1 pF to 800 pF, and more preferably from 1 pF to 100 pF. Of course, the specific values of the capacitance of the series connection will be implementation specific. The Extraction Device **800** is an example type of device that may be present in the device **550** and used for the Extraction Device **530** of FIG. **5**.

[0042] FIG. **9** is a cross-sectional diagram of a vertical PMOS Extraction Device **900**, including a vertical PMOS transistor **910**. The PMOS transistor **910** may be made on any type of semiconductor material. The PMOS transistor **910** in this embodiment has a thick gate oxide **105**, which provides a high voltage rating for the PMOS transistor **910**, exceeding that of a Main Switch to which it is connected. Also, the Extraction Device **900** includes a high-voltage rated capacitor **920** that is connected in series with the Gate-Drain capacitance of the vertical PMOS transistor **910**. The capacitor **920** is formed of conductive plates **922** separated by an insulator **924**. Even though in this illustration the high voltage capacitor **920** has similar dimensions as does the PMOS transistor **910**, such as the Poly Gate Width of the vertical PMOS **910**, in actuality, the high voltage capacitor **920** can be placed anywhere on the top of the PMOS die, or outside of it and properly wire-bonded to the control electrode of the Extraction Device.

[0043] Thus, the embodiments of the Extraction Devices illustrated in FIGS. **8** and **9** illustrate various options that may be used in implementing the Extraction Device, such as the Extraction Device **530** of FIG. **5**.

[0044] FIG. **10** is a top layout view of a device **1000** that includes an FWD **1010** integrated with an Extraction Device **1030** on a single semiconductor substrate. The FWD **1010** may be one of the FWDs described above. The FWD **1010** is surrounded by a high voltage termination **1020**. An Extraction Device **1030** is placed outside the high voltage termination **1020** of the FWD **1010**. The Extraction Device **1030** includes an input electrode **1032** for extraction, an output electrode **1034**, and a control electrode **1036**. This device **1030** is an example layout of the device **550** of FIG. **5**. If the device **1000** were coupled to a Main Switch, such as an IGBT having an Extraction Plug terminal, the control electrode **1036** would be coupled to a gate of the IGBT, the input (for extraction) electrode **1032** would be coupled to the Extraction Plug terminal of the IGBT, and the output electrode **1034** would be coupled to both a collector of the IGBT and to a cathode (not illustrated) of the FWD **1010**. Finally, the anode (not illustrated) of the FWD **1010** would be coupled to the emitter of the IGBT. When so connected, the FWD **1010** of the device **1000** provides high voltage protection to the IGBT during turn-off while the Extraction Device **1030** substantially increases the turn-off speed of the IGBT.

[0045] FIG. **11** is a top layout view of a device **1100** including one or more FWDs **1110** and one or more Extraction Devices **1130** as described above. In this layout, the FWDs **1110** are interleaved with the Extraction Devices **1130** in the active area of the die. The electrodes of the Extraction Devices **1130** are not illustrated as they may be implementation specific, and may be placed as the design dictates. Also, the FWDs **1110** illustrated in the device **1100** may be coupled together to make one or more FWDs. In other words, FWDs **1110**A and **1110**B may be coupled to one another to make a single, larger FWD. In another embodiment, all of the FWDs **1110**A, **1110**B, **1110**C, and **1110**D, maybe be coupled together to make a single FWD for the entire device **1100**. The same is true for the Extraction Devices **1130**A, **1130**B, and **1130**C, which may be variously connected to one another to make one, two, or three separate Extraction Devices **1130**. FIG. **11** illustrates the cellular or tessellated nature of the design in which multiple FWDs **1110** and Extraction Devices **1130** may be produced without affecting the functionality of the device. Further, the FWD **1110** and Extraction Device **1130** may be coupled to a one or more IGBTs as described above with reference to FIG. **10**.

[0046] FIG. **12** is a top layout view of a complete device **1200** that includes a voltage controlled Main Switch **1210** formed on a first semiconductor die coupled to an assisting device **1220** formed on a second semiconductor die. The Main Switch **1210** includes Extraction Plugs **700** placed inside an active area **1250**. The active area **1250** of a semiconductor device is the area within which the main electrical function of the power semiconductor device is performed. Metallizations **107** connect the Extraction Plugs **700** to each other. A gate terminal **1212** of the Main Switch **1210** is also illustrated within the active area **1250**. The Main Switch **1210** has its output on the backside of the die. The assisting device **1220** includes an FWD **1230** and a PMOS transistor **1240**, which functions as an Extraction Device, as described above. The Extraction Device **1240** includes an input terminal **1242** for extraction, an output terminal **1244**, and a control terminal **1246**.

[0047] The Extraction Plugs **700** of the Main Switch **1210** are connected to one another through the metalizations **107** and also to the extraction input **1242** of the Extraction Device **1240** through a wire bond **1260**. A wire bond electrically connects devices that are produced on two different substrates, where die metallizations cannot be used. Another wire bond **1282** couples the gate terminal **1212** of the Main Switch **1210** to the control electrode **1246** of the Extraction Device **1240**. With reference to FIG. **5**, the FWD **1230** has its anode coupled to an emitter of the Main Switch **1210** through a wire bond **1264**. The output of the Extraction Device **1240** is coupled by a wire bond **1266** to a collector of the Main Switch **1210**, which, as described above, is located on the back side of the Main Switch **1210**, and is therefore not visible in FIG. **12**. The output of the Extraction Device **1240** is also coupled to the cathode of the FWD **1230**. This connection between the output of the Extraction Device **1240** and the cathode of the FWD **1230** may be an internal metallization within the assisting device **1220**, and is therefore not separately illustrated in FIG. **12**. Thus, FIG. **12** is an example of a physical manifestation of the device **560** described above with reference to FIG. **5**, which includes both a Main Switch **510** and assisting device **550**. If the complete device **1200** is a three terminal device, then the wire bond **1264** would be coupled to the ground terminal of the device, the wire bond **1266** would be coupled to the output terminal of the device, and the wire bond **1262** would be coupled to the control input terminal of the device. The wire bond **1260** would not need to be connected to a terminal of the complete device **1200** because the connection between the Extraction Plug terminal of the Main Switch

1210 and the input terminal **1242** of the Extraction Device **1240** need only be an internal connection.

[0048] FIG. **13** is a top assembly view of a device **1300** that is similar to the device **1200** of FIG. **12**. The same or similar features that were described with reference to FIG. **12** will not be repeated in the description of FIG. **13**, for brevity. The main difference between devices **1200** and **1300** is that the extraction plugs **700** of the device **1300** are formed outside of the high voltage termination **1250**, whereas the Extraction Plugs **700** of the device **1300** are formed within the high voltage termination **1250**. As described above, location of the Extraction Plugs **700** has little or no effect on their function to provide an access to the drift area of the semiconductor Main Switch through which the Extraction Device **1240** can expediently remove charge from while the Main Switch is turning off.

[0049] Power semiconductor switches having Extraction Plugs may be developed as a hybrid of the devices **1200** and **1300**, with some Extraction Plugs **700** located inside the high voltage termination area **1250** and some Extraction Plugs **700** located outside the high voltage termination area within the same device itself.

Example Embodiments

[0050] In accordance to the present disclosure, an IGBT or other semiconductor device may take the following forms, along with their equivalents.

[0051] Example 1 is a Freewheeling diode integrated with a Forced Extraction Device. The Freewheeling diode may be of any kind, such as PIN, Schottky, etc.

[0052] Example 2 is a Freewheeling Diode coupled to an Extraction Device, which, in turn, is connected to a Main Switch that includes an Extraction Electrode or Extraction Plugs.

[0053] Example 3 is a Freewheeling Diode integrated with an Extraction Device, in which both the Diode and Extraction Device are made on Silicon.

[0054] Example 4 is a Freewheeling Diode integrated with an Extraction Device, in which both the Diode and Extraction Device are made on Wide Bandgap semiconductors.

[0055] Example 5 is a Freewheeling Diode integrated with a lateral PMOS Extraction Device, which, in turn, is connected to a Main Switch. The lateral PMOS Extraction Device has a thick gate oxide that withstands at least the blocking voltage of the Main Switch (IGBT).

[0056] Example 6 is a Freewheeling Diode integrated with a lateral PMOS Extraction Device. The lateral PMOS has a thin gate oxide and a high voltage rating capacitor that is connected in series with the capacitor of the controlling electrode of the Extraction Device.

[0057] Example 7 is a Freewheeling Diode integrated with a vertical PMOS Extraction Device which, in turn, is connected to a Main Switch. The vertical PMOS Extraction Device has a thick gate oxide that withstands at least the blocking voltage of the Main Switch (IGBT).

[0058] Example 8 is a Freewheeling Diode integrated with a vertical PMOS Extraction Device. The vertical PMOS has a thin gate oxide and a high voltage rating capacitor that is connected in series with the capacitor of the controlling electrode of the Extraction Device

[0059] Example 9 is a High Voltage Capacitor connected in series with the capacitor of the controlling electrode of the Extraction Device.

[0060] The above description of illustrated implementations of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

[0061] These modifications may be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

What is claimed is:

1. A semiconductor device formed on a semiconductor substrate, the semiconductor having a first, second, third, and fourth terminals, the semiconductor device comprising:

a freewheeling diode coupled between the first and second terminals; and

an Extraction Device structured to be coupled to a conductivity modulation switch device through the third terminal, the Extraction Device further coupled to the second terminal and the fourth terminal.

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