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(54) **SEMICONDUCTOR DEVICE PACKAGES AND METHODS OF MANUFACTURING THE SAME**

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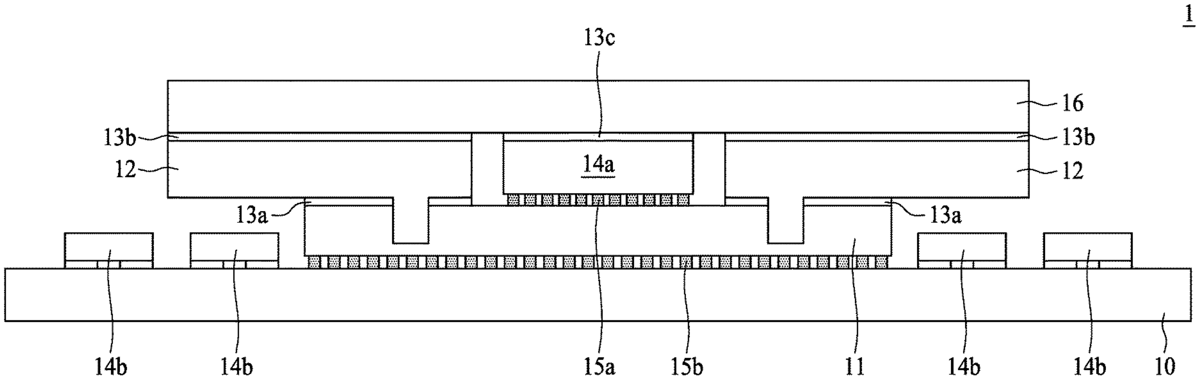
(57) **ABSTRACT**

A semiconductor device package includes a substrate, an electronic component disposed on the substrate, a supporting structure disposed on the substrate and surrounding the electronic component, and a heat spreading structure disposed on the supporting structure. A length of the supporting structure and a length of the heat spreading structure are greater than a length of the substrate.



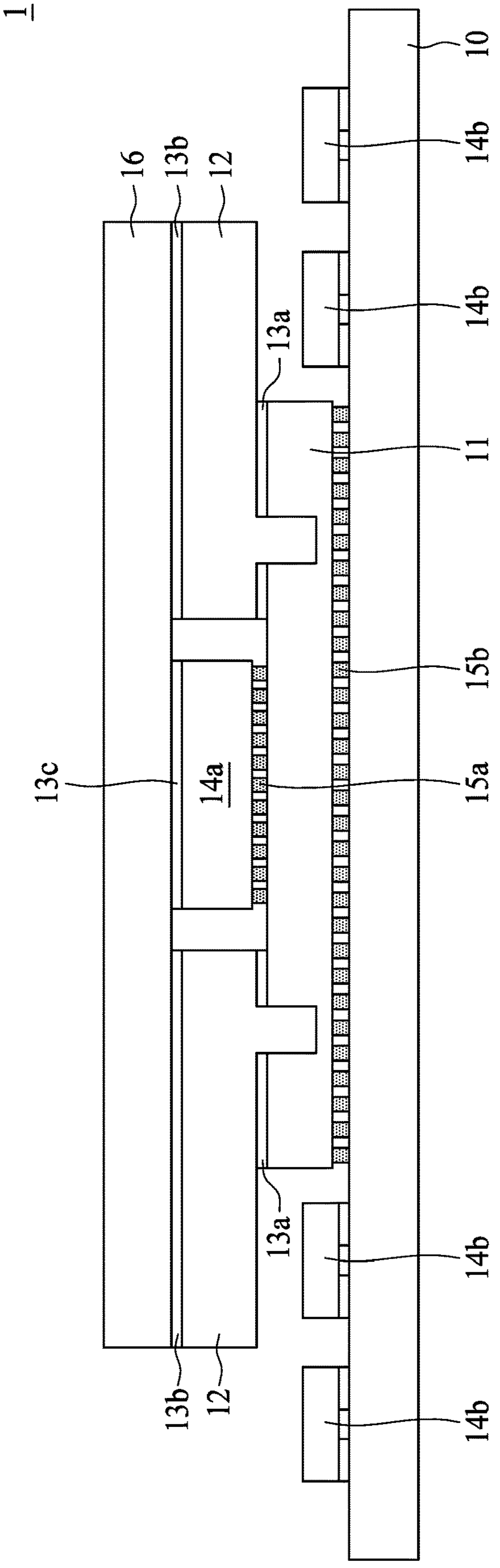


FIG. 1A

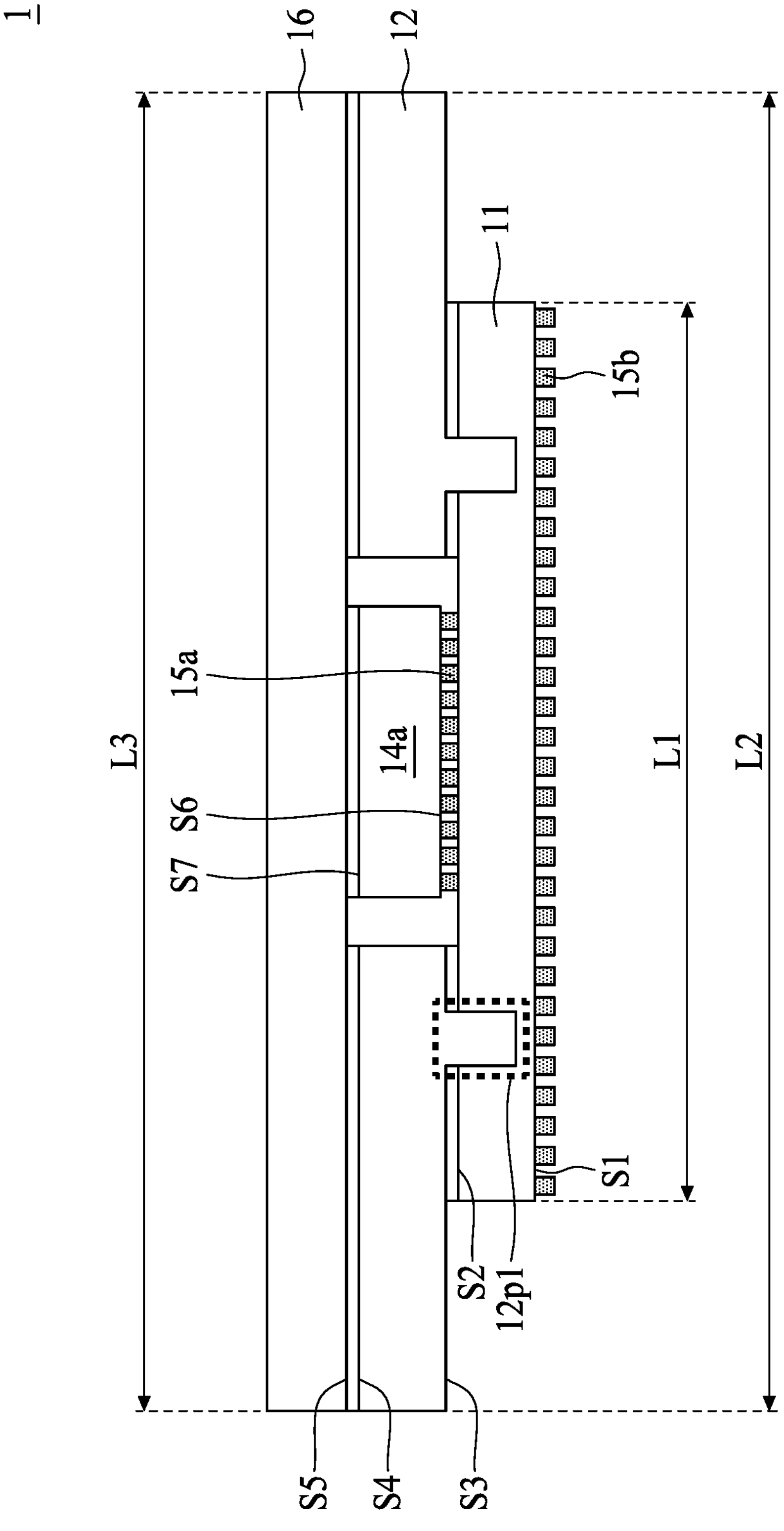


FIG. 1B

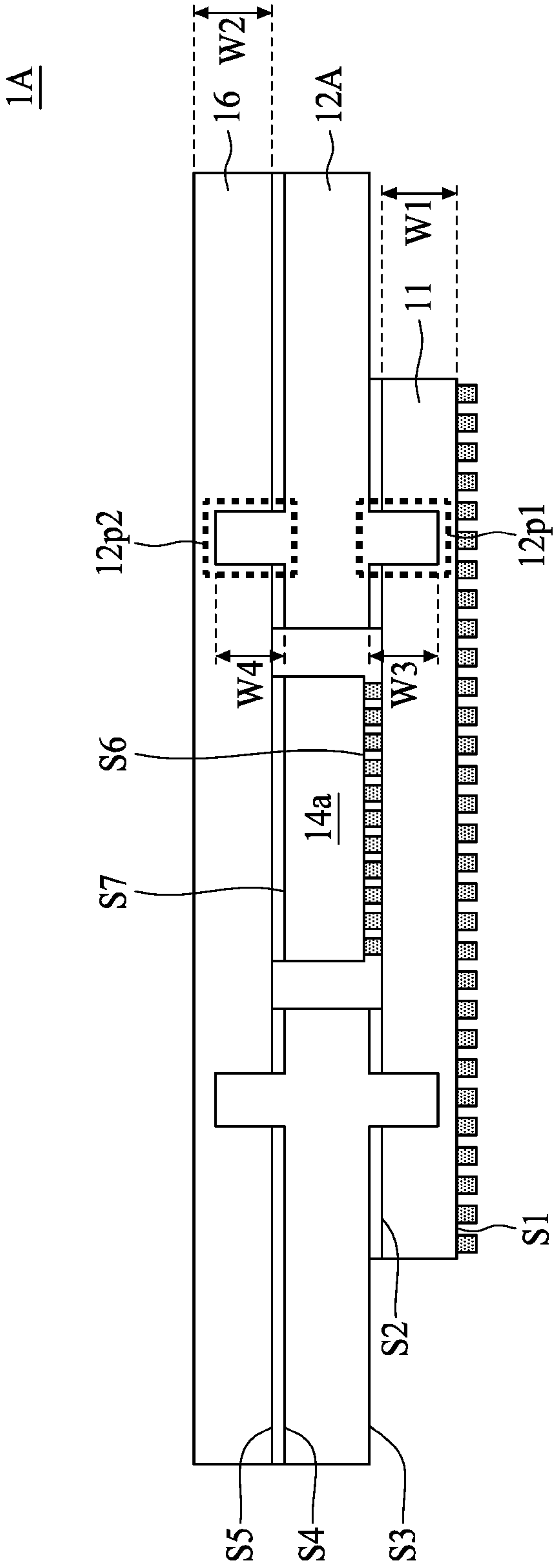


FIG. 1C

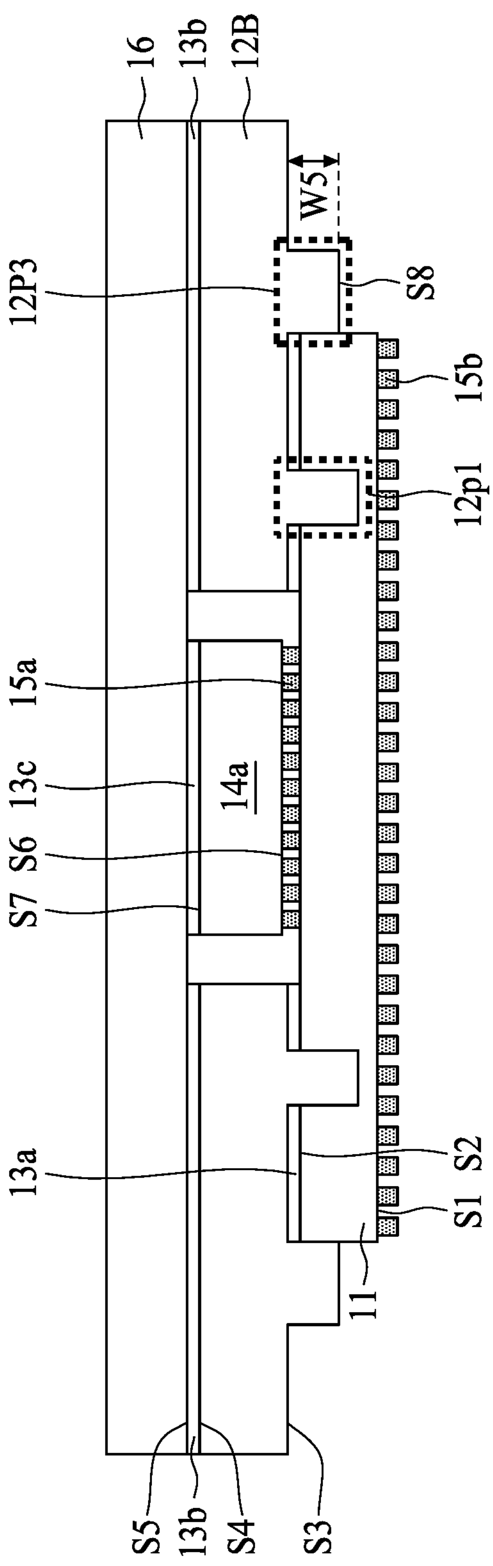

1B
16
13b
12B
W5
12P3
S8
15b
12p1
15a
13c
14a
S6
S7
13a
S2
S1
11
S5
13b
S4
S3

FIG. 1D

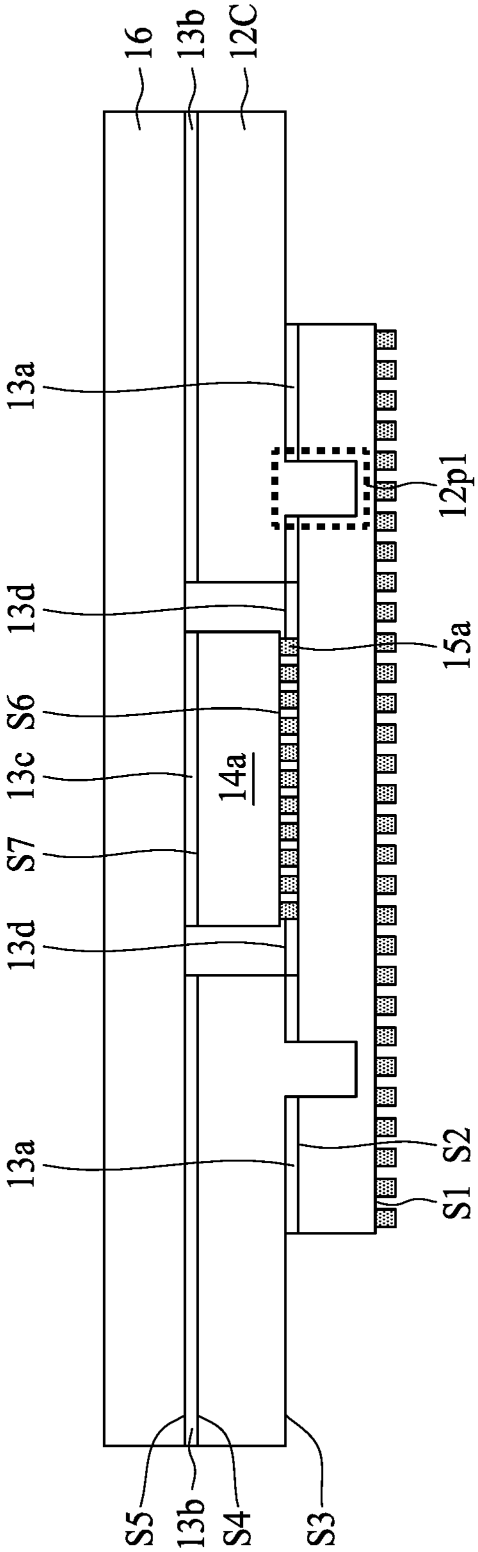

1C
16
13b
12C
13a
12p1
13d
15a
S6
13c
14a
S7
13d
13a
S2
S1
S5
13b
S4
S3

FIG. 1E

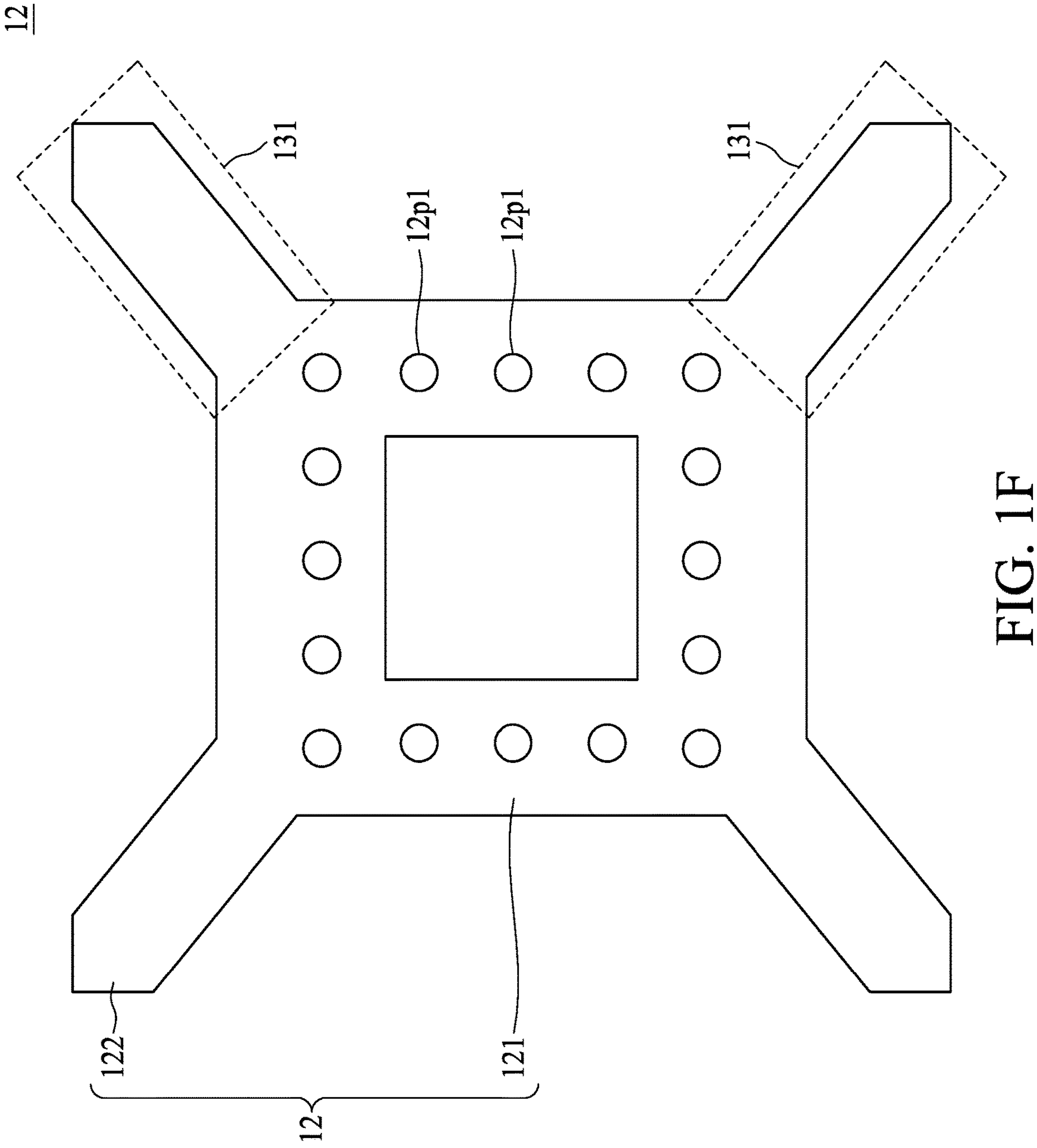


FIG. 1F

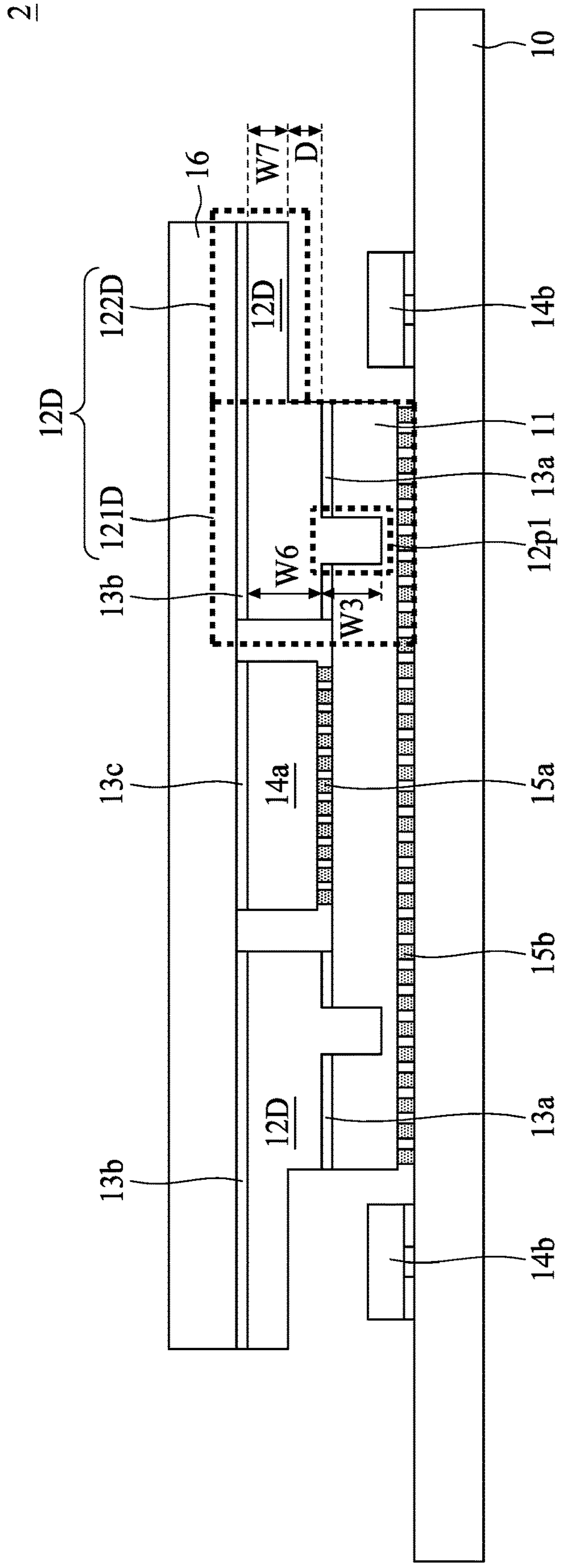

2
10
16
W7
D
12D
122D
12D
121D
14b
11
13a
12p1
13b
W6
W3
13c
14a
15a
15b
13a
12D
13b
14b

FIG. 2A

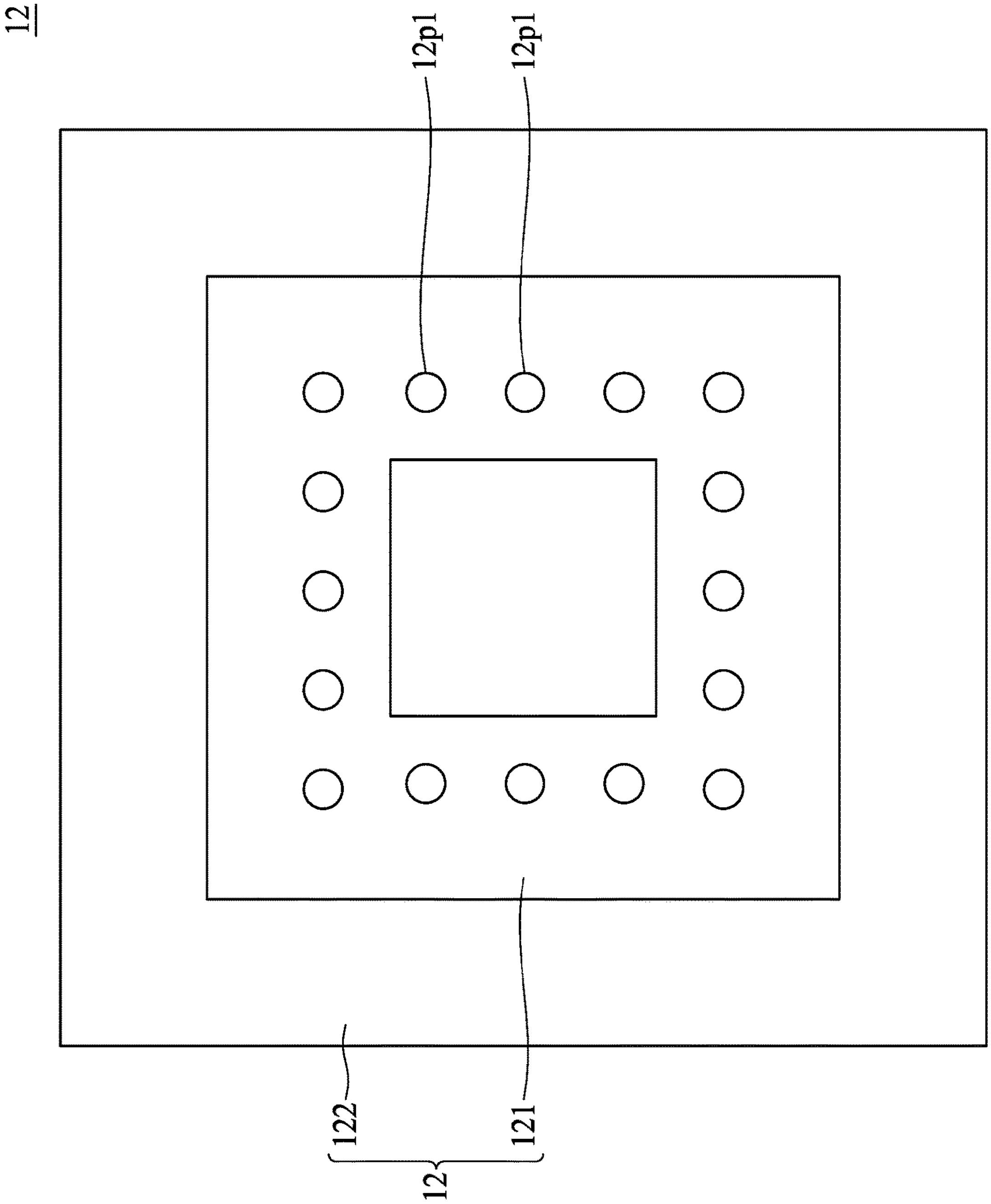


FIG. 2B

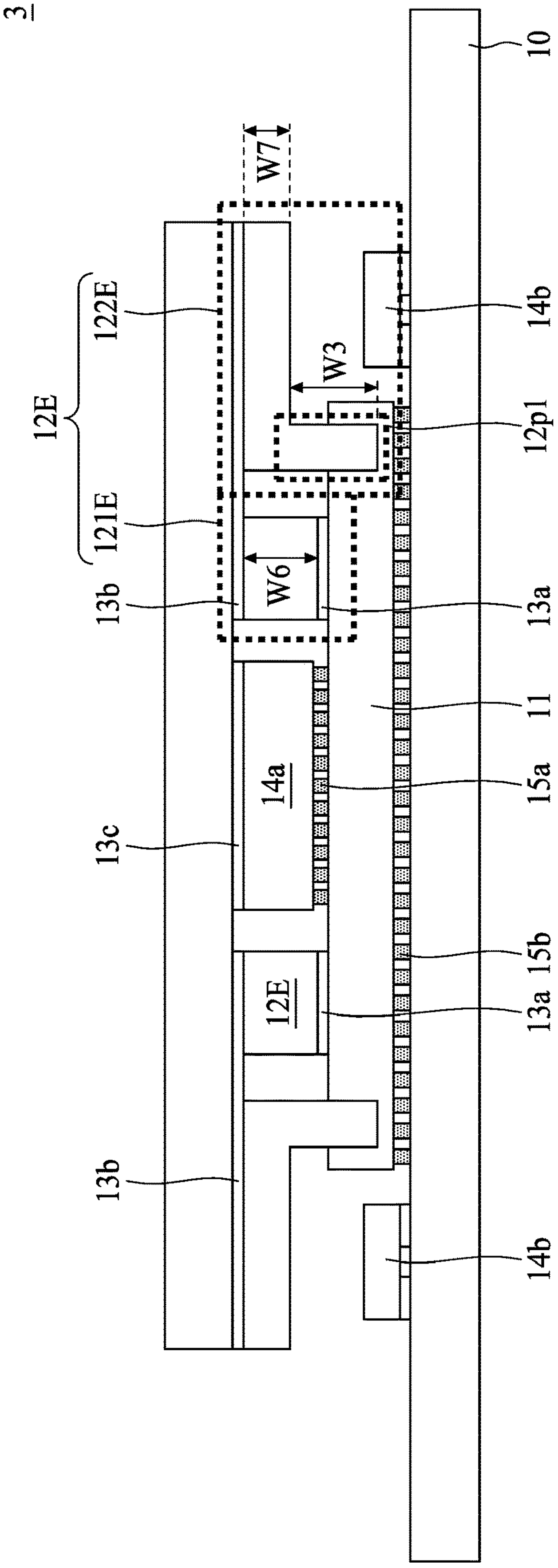

3
12E
122E
121E
13b
13c
13b
W7
W3
W6
14a
12E
10
14b
12p1
13a
11
15a
15b
13a
14b

FIG. 3A

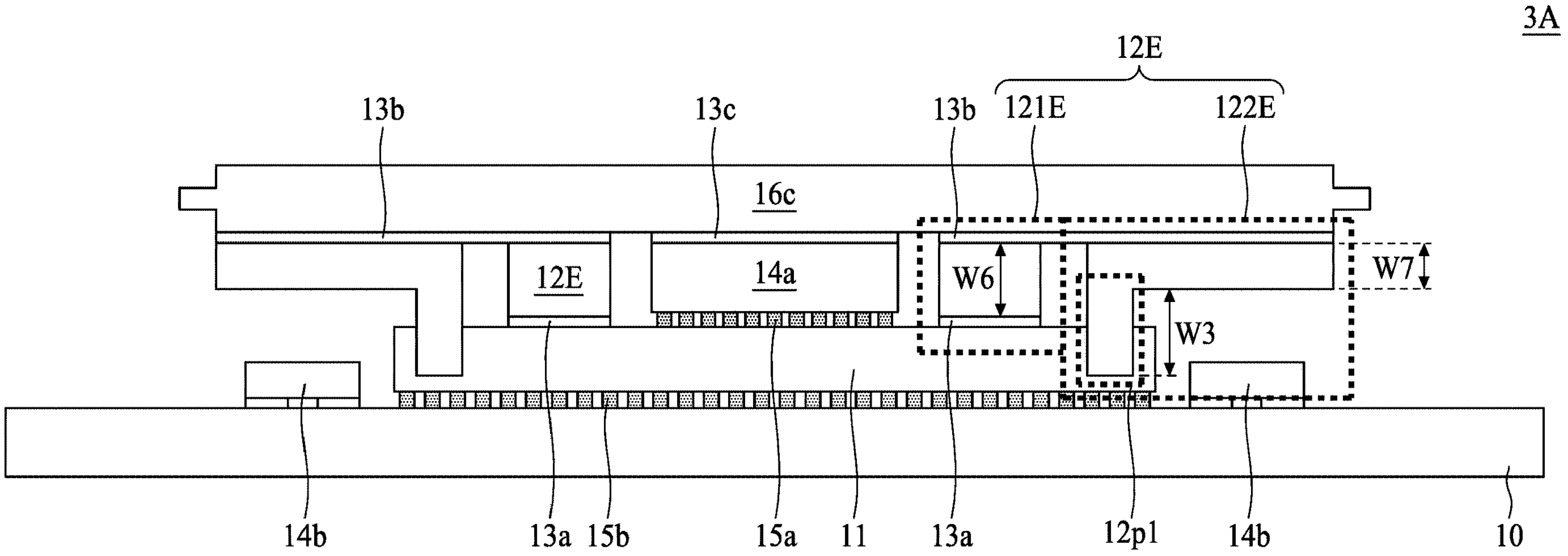

3A
12E
13b
13c
13b
121E
122E
16c
12E
14a
W6
W7
W3
14b
13a
15b
15a
11
13a
12p1
14b
10

FIG. 3B

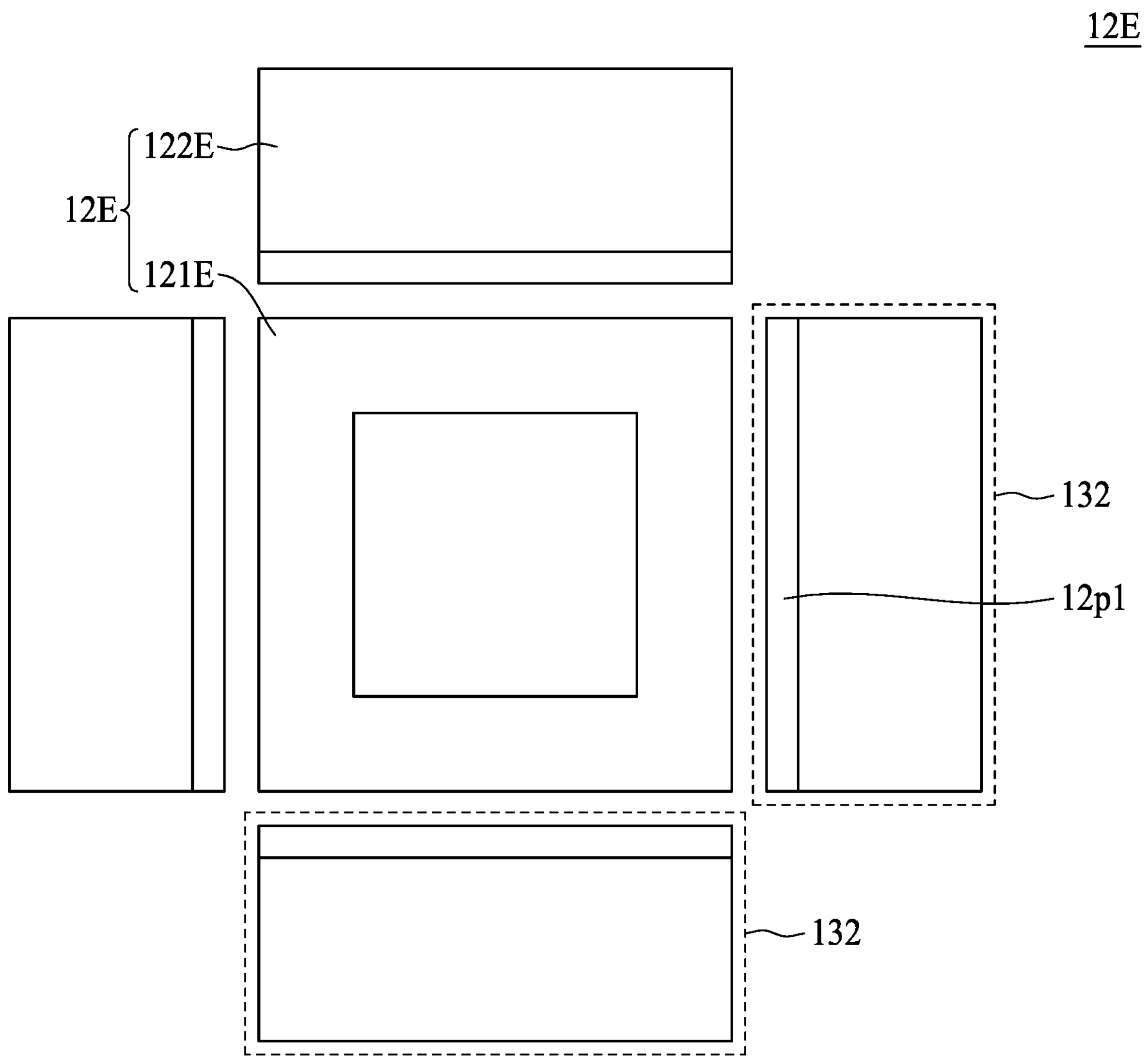


FIG. 3C

SEMICONDUCTOR DEVICE PACKAGES AND METHODS OF MANUFACTURING THE SAME

BACKGROUND

1. Field of the Disclosure

[0001] The present disclosure relates to semiconductor device packages and methods of manufacturing the same.

2. Description of Related Art

[0002] A semiconductor device package may include some semiconductor devices stacked atop one another. However, as the functionality of the semiconductor device improves, more heat may be generated. The overall device package should have a large heat dispersion area to achieve more efficient heat dissipation. Although increasing the size of the device package contributes to heat dissipation, it will inevitably increase the cost of the process and sacrifice the PCB area usage.

SUMMARY

[0003] According to some example embodiments of the instant disclosure, a semiconductor device package includes a substrate, an electronic component disposed on the substrate, a supporting structure disposed on the substrate and surrounding the electronic component, and a heat spreading structure disposed on the supporting structure. A length of the supporting structure and a length of the heat spreading structure are greater than a length of the substrate.

[0004] According to some example embodiments of the instant disclosure, a semiconductor device package includes a substrate, a first electronic component disposed on the substrate, a supporting structure surrounding the first electronic component, and a heat spreading structure covering the first electronic component and the supporting structure. The supporting structure has a first portion over the substrate and a second portion extending laterally beyond a lateral surface of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Aspects of the present disclosure are readily understood from the following detailed description when read with the accompanying figures. It should be noted that various features may not be drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0006] FIG. **1**A, FIG. **1**B, FIG. **1**C, FIG. **1**D and FIG. **1**E are cross-sectional views of a semiconductor device package in accordance with some embodiments of the present disclosure.

[0007] FIG. **1**F is a top view of a supporting structure of the semiconductor device package in accordance with some embodiments of the present disclosure.

[0008] FIG. **2**A is a cross-sectional view of another semiconductor device package in accordance with some embodiments of the present disclosure.

[0009] FIG. **2**B is a top view of a supporting structure of the semiconductor device package in accordance with some embodiments of the present disclosure.

[0010] FIG. **3**A and FIG. **3**B are cross-sectional views of a semiconductor device package in accordance with some embodiments of the present disclosure.

[0011] FIG. **3**C is a top view of a supporting structure of the semiconductor device package in accordance with some embodiments of the present disclosure.

[0012] Common reference numerals are used throughout the drawings and the detailed description to indicate the same or similar elements. The present disclosure will be more apparent from the following detailed description taken in conjunction with the accompanying drawings.

DETAILED DESCRIPTION

[0013] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below. These are, of course, merely examples and are not intended to be limiting. In the present disclosure, reference to the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0014] Embodiments of the present disclosure are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable concepts that may be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative and do not limit the scope of the disclosure.

[0015] FIG. **1**A is a cross-sectional view of a semiconductor device package **1** in accordance with some embodiments of the present disclosure. The semiconductor device package **1** includes a carrier **10**, a substrate **11**, a supporting structure **12**, electronic components **14***a* and **14***b*, and a heat spreading structure **16**.

[0016] The carrier **10** may be, for example, a printed circuit board, such as a paper-based copper foil laminate, a composite copper foil laminate, or a polymer-impregnated glass-fiber-based copper foil laminate. The carrier **10** has an interconnection structure and/or a grounding element.

[0017] The substrate **11** is formed or disposed on the carrier **10**. The substrate **11** may be connected to the carrier **10** by the electrical contacts **15***b*. The substrate **11** may be, for example, a printed circuit board, such as a paper-based copper foil laminate, a composite copper foil laminate, or a polymer-impregnated glass-fiber-based copper foil laminate. The substrate **11** may include an interconnection structure, such as a redistribution layer (RDL) or a grounding element.

[0018] Each of the electronic components **14***a* and **14***b* include a plurality of semiconductor devices, such as, but not limited to, transistors, capacitors and resistors interconnected together by a die interconnection structure into functional circuits to thereby form an integrated circuit. As will be understood to those skilled in the art, the device side of the semiconductor die includes an active portion including integrated circuitry and interconnection. The electronic components **14***a* and **14***b* may be any suitable integrated circuit device including, but not limited to, a microprocessor (e.g., single or multi-core), a memory device, a chipset, a graphics device, a high bandwidth memory (HBM), or an application-specific integrated circuit (ASIC) according to several different embodiments.

[0019] The electronic component **14***a* is formed or disposed on the substrate **11**. A plurality of electrical contacts **15***a* are disposed on an active surface of the electronic component **14***a* to provide electrical connection between the electronic component **14***a* and the substrate **11**. The electronic components **14***b* are formed or disposed on the carrier **10**. The electronic components **14***b* are disposed adjacent to the substrate **11**. Some of the electronic components **14***b* may be arranged below the supporting structure **12**. For example, some of the electronic component **14** are disposed within a projection of the supporting structure **12** on the carrier **10**. For example, some of the electronic component **14** are fully covered by the supporting structure **12** from a top view of the semiconductor device package **1**.

[0020] The supporting structure **12** is disposed on the substrate **11**. The supporting structure **12** may be connected to the substrate **11** through an adhesive layer **13***a*. In some embodiments, the supporting structure **12** laterally extends beyond a lateral surface of the substrate **11**. In some embodiments, the supporting structure **12** laterally extends beyond a lateral surface of some of the electronic component **14***b*. In some embodiments, a portion of the supporting structure **12** extends within the substrate **11** and is in contact with the substrate **11**. A portion of the supporting structure **12** is surrounded by or embedded within the substrate **11**. A portion of the supporting structure **12** is spaced apart from the substrate **11** by the adhesive layer **13***a*.

[0021] The supporting structure **12** may be or include aluminum (Al), copper (Cu), titanium (Ti), tungsten (W) or other suitable material(s) (e.g., metal, alloy or non-metal conductive material(s)). The supporting structure **12** may also include epoxy resin, a polyimide, a phenolic compound, a silicone dispersed therein, or a combination thereof.

[0022] The adhesive layer **13***a* is formed between the substrate **11** and the supporting structure **12**. The supporting structure **12** may be connected to the substrate by utilizing the adhesive layer **13***a*. In some embodiments, the adhesive layer **13***a* may include a gel type or film type adhesive layer. The adhesive layer **13***a* may include a thermoset resin. The adhesive layer **13***a* may include a thermoplastic resin. The adhesive layer **13***a* may include one or more of the following: a resin, a polyester resin, a polyether resin, an epoxy resin and/or a polyolefin composition. In some embodiments, the adhesive layer **13***a* may include a thermal interface material (TIM) or a thermal paste layer.

[0023] The heat spreading structure **16** is formed or disposed on the supporting structure **12** and the electronic component **14***a*. The heat spreading structure **16** may be supported or sustained by the supporting structure **12**. The heat spreading structure **16** is thermally connected to the electronic component **14***a* (e.g., to a backside surface of the electronic component **14***a*). When heat is generated by the electronic component **14***a*, the heat dissipation may be achieved by the heat spreading structure **16**.

[0024] The heat spreading structure **16** may include a heat sink, cold plate, or other suitable cooling means, or a lid, or heat pipe, or another intermediate structure which is in contact with the electronic component **14***a*. The heat spreading structure **16** is envisioned to be constructed using heat-conducting material including copper and/or aluminum. The heat spreading structure **16** may dissipate heat generated by circuitry present on, for example, the electronic component **14***a*.

[0025] The adhesive layer **13***c* is disposed between the heat spreading structure **16** and the supporting structure **12**. The heat spreading structure **16** may be secured or connected to the supporting structure **12** by utilizing the adhesive layer **13***c*. Therefore, an efficient heat transfer path may be provided from the electronic component **14***a* via the adhesive layer **13***c* to the heat spreading structure **16**.

[0026] In some embodiments, the adhesive layer **13***c* may include a gel type or film type adhesive layer, a thermoset resin, or a thermoplastic resin. The adhesive layer **13***c* may also include one or more of the following: a resin, a polyester resin, a polyether resin, an epoxy resin and/or a polyolefin composition. In some embodiments, the adhesive layer **13***c* may include a thermal interface material (TIM) or a thermal paste layer.

[0027] The adhesive layer **13***b* is formed between the heat spreading structure **16** and the supporting structure **12**. The heat spreading structure **16** may be connected to the supporting structure **12** by utilizing the adhesive layer **13***b*. In some embodiments, the adhesive layer **13***b* may include one or more of the following: a resin, a polyester resin, a polyether resin, an epoxy resin and/or a polyolefin composition. In some embodiments, the adhesive layer **13***b* may include a thermal interface material (TIM) or a thermal paste layer.

[0028] In some embodiments, a material of the adhesive layer **13***b* is the same as a material of the adhesive layer **13***a*. A material of the adhesive layer **13***c* is the same as the material of the adhesive layer **13***b* and the adhesive layer **13***a*. In other embodiments, a material of the adhesive layer **13***c* is different from the material of the adhesive layer **13***b* and the adhesive layer **13***a*.

[0029] FIG. **1**B is a cross-sectional view of a portion of the semiconductor device package **1** in accordance with some embodiments of the present disclosure. In FIG. **1**B, the carrier **10** and the electronic components **14***b* may be omitted. The supporting structure **12** includes a pin portion **12***p***1**. The pin portion **12***p***1** may have a rectangle or a rectangle-like profile, a round or a round-like profile, a horn or a horn-like profile, or a cone or a cone-like profile.

[0030] The pin portion **12***p***1** extends from a bottom surface S3 of the supporting structure **12** into the substrate **11**. The pin portion **12***p***1** is surrounded by the adhesive layer **13***a* and covered by the substrate **11**. The pin portion **12***p***1** is in contact with the substrate **11**. Since the pin portion **12***p***1** is extended or stuck into the substrate **11**, the sustaining and linkage between the substrate **11** and the supporting structure **12** may be improved.

[0031] In some embodiments, a length L2 of the supporting structure **12** is greater than a length L1 of the substrate **11**. In some embodiments, a length L3 of the heat spreading structure **16** is greater than a length L1 of the substrate. The length L2 of the supporting structure **12** is substantially the same to the length L3 of the heat spreading structure **16**. Therefore, heat resistance may be reduced by arranging the long heat spreading structure **16** with a large heat transference area to achieve efficient heat dissipation.

[0032] In some embodiments, the length L3 of the heat spreading structure **16** is smaller than three times of the length L1 of the substrate **11**. The length L2 of the supporting structure **12** is smaller than three times of the length L1 of the substrate **11**. The above size constraint may prevent the heat spreading structure **16** from dropping or falling.

[0033] FIG. **1**C is a cross-sectional view of the semiconductor device package **1**A in accordance with some embodiments of the present disclosure. The semiconductor device package **1**A is similar to the semiconductor device package **1**, and the differences therebetween are described below.

[0034] In some embodiments, the supporting structure **12**A laterally extends beyond a lateral surface of the substrate **11**. In some embodiments, the supporting structure **12**A laterally extends beyond a lateral surface of some of the electronic component **14***b*. In some embodiments, a portion of the supporting structure **12** extends within the substrate **11** and is in contact with the substrate **11**. The supporting structure **12**A further includes the pin portion **12***p***2**. The pin portion **12***p***2** may have a rectangle or a rectangle-like profile, a round or a round-like profile, a horn or a horn-like profile, or a cone or a cone-like profile.

[0035] The pin portion **12***p***2** extends from a top surface S**4** of the supporting structure **12** into the heat spreading structure **16**. The pin portion **12***p***2** is surrounded by the adhesive layer **13***b* and covered by the heat spreading structure **16**. The pin portion **12***p***2** is extended or stuck into the heat spreading structure **16**. Therefore, the sustaining and linkage between the heat spreading structure **16** and the supporting structure **12**A may be improved by arranging the pin portion **12***p***2**.

[0036] A width W**4** of the pin portion **12***p***2** is smaller than a thickness W2 of the heat spreading structure **16**. The width W**4** of the pin portion **12***p***2** is greater than half of the thickness W**2** of the heat spreading structure **16**. For example, the width W**4** of the pin portion **12***p***2** is about 50% to 90% of the thickness W**2** of the heat spreading structure **16**. A width W**3** of the pin portion **12***p***1** is smaller than a thickness W1 of the substrate **11**. The width W**3** of the pin portion **12***p***1** is greater than half of the thickness W**1** of the substrate **11**. For example, the width W**3** of the pin portion **12***p***1** is about 50% to 90% of the thickness W**1** of the substrate **11**.

[0037] FIG. **1**D is another cross-sectional view of the semiconductor device package **1**B in accordance with some embodiments of the present disclosure. The semiconductor device package **1**B is similar to the semiconductor device package **1**, and the differences therebetween are described below.

[0038] The supporting structure **12**B includes a pin portion **12***p***3**. The pin portion **12***p***3** is disposed within a projection of the supporting structure **12**B. For example, the pin portion **12***p***3** may be fully covered by the supporting structure **12**B from a top view of the semiconductor device package **1**B. The pin portion **12***p***3** may have a rectangle or a rectangle-like profile, a round or a round-like profile, a horn or a horn-like profile, or a cone or a cone-like profile.

[0039] The pin portion **12***p***3** extends from a bottom surface S**3** of the supporting structure **12**B. The pin portion **12***p***3** is adjacent to or in direct contact with the lateral surface S**8** the substrate **11**. A width W**5** of the pin portion **12***p***3** is smaller than a thickness W1 of the substrate **11**. The width W**5** of the pin portion **12***p***3** is greater than half of the thickness W1 of the substrate **11**. For example, the width W**5** of the pin portion **12***p***3** is about 50% to 90% of the thickness W1 of the substrate **11**. The pin portion **12***p***3** upholds the substrate **11** to improve the sustaining and linkage between the substrate **11** and the supporting structure **12**B.

[0040] FIG. **1**E is another cross-sectional view of the semiconductor device package **1**C in accordance with some embodiments of the present disclosure. The semiconductor device package **1**B is similar to the semiconductor device package **1**, and the differences therebetween are described below. The electronic component **14***a* is separated apart from the supporting structure **12**C. An air gap is formed between the electronic component **14***a* and the supporting structure **12**C to achieve heat spreading.

[0041] An adhesive layer **13***d* is formed or disposed on the substrate **11**. The adhesive layer **13***d* is formed between the electronic component **14***a* and the supporting structure **12**C. The adhesive layer **13***d* may be in direct contact with the adhesive layer **13***a* and the electrical contacts **15***a*. A heat transfer path may be provided accordingly from the electronic component **14***a* via the electrical contacts **15***a* to the adhesive layer **13***d*.

[0042] FIG. **1**F is a top view of the supporting structure **12** of the semiconductor device package **1** in accordance with some embodiments of the present disclosure. The supporting structure **12** includes two portions **121** and **122**. The portion **121** may have a rectangle or a rectangle-like profile or a square ring. The electronic component **14***a* may be located at the central region encircled by the portion **121**.

[0043] The pin portions **12***p***1** are formed within the portion **121**. The positions of the pin portions **12***p***1** are arranged in a rectangle or a rectangle-like profile. The pin portions **12***p***1** encircle or surround the electronic component **14***a*. The portion **122** includes several prolonging portions **131**. The prolonging portions **131** extend from four corners of the region **121**. A thickness of the portion **121** is substantially the same as a thickness of the portion **122**. In other embodiments, A thickness of the portion **121** is greater than a thickness of the portion **122**.

[0044] FIG. **2**A is a cross-sectional view of another semiconductor device package **2** in accordance with some embodiments of the present disclosure. The semiconductor device package **2** is similar to the semiconductor device package **1**, and the differences therebetween are described below.

[0045] The supporting structure **12**D includes two portions **121**D and **122**D. The portion **121**D includes the pin portion **12***p***1**. The thickness W**6** of the portion **121**D may be different from the thickness W**7** of the portion **122**D. The thickness W**7** of the portion **122**D may be smaller than the thickness W**6** of the portion **121**D. The length of the supporting structure **12**D is greater than the length of the substrate **11**. Therefore, a large space under the portion **122**D may be provided to accommodate the electronic components **14***b* on the carrier **10**. Furthermore, the weight of the supporting structure **12**D may be reduced.

[0046] The length L**3** of the heat spreading structure **16** is greater than the length L1 of the substrate **11** but smaller than three times of the length L1 of the substrate **11**. The length L2 of the supporting structure **12**D is smaller than three times of the length L1 of the substrate **11**. The thickness W**2** of the heat spreading structure **16** may be arranged at a range of 0.5 mm to 3 mm. There is a distance D to illustrate the difference between the thickness W6 of the portion **121**D and the thickness W7 of the portion **122**D. The length L3 of the heat spreading structure **16** may be smaller than 100 times of the difference between the distance D and thickness W**2** of the heat spreading structure **16**.

[0047] FIG. **2**B is a top view of the supporting structure **12**D of the semiconductor device package in accordance with some embodiments of the present disclosure. The supporting structure **12**D includes two portions **121**D and **122**D. The portion **121**D is surrounded or encircled by the portion **122**D. The portion **121**D may have a rectangle or a rectangle-like profile or a square ring. The portion **122**D may have a rectangle or a rectangle-like profile or a square ring.

[0048] The electronic component **14***a* may be located at the central region encircled by the portion **121**D. The electronic component **14***b* may be located under the region **122**D. The pin portions **12***p***1** are formed within the portion **121**D. The positions of the pin portions **12***p***1** are arranged in a rectangle or a rectangle-like profile. The pin portions **12***p***1** encircle or surround the electronic component **14***a*. A thickness of the portion **121**D is greater than a thickness of the portion **122**D.

[0049] FIG. **3**A is a cross-sectional view of a semiconductor device package **3** in accordance with some embodiments of the present disclosure. The semiconductor device package **3** is similar to the semiconductor device package **2**, and the differences therebetween are described below. The portion **121**E is connected to the substrate **11** by the adhesive layer **13***a*. The portion **122**E includes a pin portion **12***p***1**. The portion **122**E is connected to the substrate **11** by the pin portion **12***p***1** without forming an adhesive layer. The portion **121**E is separated apart from the portion **122**E. An air gap may be formed between the portions **121**E and **122**E to achieve heat spreading.

[0050] The thickness W**6** of the portion **121**E is different from the thickness W**7** of the portion **122**E. The thickness W**7** of the portion **122**E may be smaller than the thickness W**6** of the portion **121**E. Therefore, a large space under the portion **122**E may be provided to accommodate the electronic components **14***b* on the carrier **10**. Furthermore, the weight of the supporting structure **12**E may be reduced.

[0051] FIG. **3**B is another cross-sectional view of the semiconductor device package **3**A in accordance with some embodiments of the present disclosure. The semiconductor device package **3**A is similar to the semiconductor device package **3**, and the differences therebetween are described below.

[0052] The heat spreading structure **16** further includes a vapor chamber **16**C. The heat spreading structure **16** is envisioned to be constructed using heat-conducting material with vapor chambers or heat pipes, for example, inside of the base, and the like. Therefore, the heat spreading structure **16** may spread or dissipate heat generated by the electronic components **14***a* and **14***b*.

[0053] FIG. **3**C is a top view of the supporting structure **12**E of the semiconductor device package **1** in accordance with some embodiments of the present disclosure. The supporting structure **12**E includes two portions **121**E and **122**E. The portion **121**E may have a rectangle or a rectangle-like profile or a square ring. The electronic component **14***a* may be located at the central region encircled by the portion **121**E.

[0054] The pin portions **12***p***1** are formed within the portion **122**E rather than the portion **121**E. The pin portions **12***p***1** may have a strip or a strip-like profile. The pin portions **12***p***1** encircle or surround the electronic component **14***a*. The portion **122**E includes several auxiliary portions **132**. The auxiliary portions **132** extend from four sides of the region **121**E. The portion **121**E is separated apart from the portion **122**E. A thickness of the portion **121**E is greater than a thickness of the portion **122**E.

[0055] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper," "lower," "left," "right" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly. It should be understood that when an element is referred to as being "connected to" or "coupled to" another element, it may be directly connected to or coupled to the other element, or intervening elements may be present.

[0056] The terms "approximately," "substantially," "substantial" and "about" are used herein to describe and account for small variations. When used in conjunction with an event or circumstance, the terms may refer to instances in which the event or circumstance occurs precisely, as well as instances in which the event or circumstance occurs to a close approximation. As used herein with respect to a given value or range, the term "about" generally means within ±10%, ±5%, ±1%, or ±0.5% of the given value or range. Ranges may be expressed herein as being from one endpoint to another endpoint or between two endpoints. All ranges disclosed herein are inclusive of the endpoints, unless specified otherwise. The term "substantially coplanar" may refer to two surfaces within micrometers (μm) of lying along a same plane, such as within 10 μm, within 5 μm, within 1 μm, or within 0.5 μm of lying along the same plane. When referring to numerical values or characteristics as "substantially" the same, the term may refer to the values lying within ±10%, ±5%, ±1%, or ±0.5% of an average of the values.

[0057] The foregoing outlines the features of several embodiments and detailed aspects of the present disclosure. The embodiments described in the present disclosure may be readily used as a basis for designing or modifying other processes and structures for carrying out the same or similar purposes and/or achieving the same or similar advantages of the embodiments introduced herein. Such equivalent constructions do not depart from the spirit and scope of the present disclosure, and various changes, substitutions, and alterations may be made without departing from the spirit and scope of the present disclosure.

1. A semiconductor device package, comprising:

a substrate;

an electronic component disposed on the substrate;

a supporting structure disposed on the substrate and surrounding the electronic component; and

a heat spreading structure disposed on the supporting structure, wherein a length of the supporting structure and a length of the heat spreading structure are greater than a length of the substrate.

2. The semiconductor device package as claimed in claim **1**, wherein the length of the heat spreading structure is smaller than three times of the length of the substrate.

3. The semiconductor device package as claimed in claim **1**, wherein the supporting structure further comprises a first pin portion extending from a bottom surface of the supporting structure into the substrate.

4. The semiconductor device package as claimed in claim **3**, wherein the supporting structure further comprises a second pin portion extending from a top surface of the supporting structure into the heat spreading structure.

5. The semiconductor device package as claimed in claim **3**, wherein a depth of the first pin portion is greater than half of a thickness of the substrate.

6. The semiconductor device package as claimed in claim **1**, wherein the heat spreading structure is connected to a top surface of the supporting structure by a first adhesive layer; the substrate is connected to a bottom surface of the supporting structure by a second adhesive layer, and a material of the first adhesive layer is the same as a material of the second adhesive layer.

7. The semiconductor device package as claimed in claim **6**, wherein the heat spreading structure is connected to a backside surface of the electronic component by a third adhesive layer, and a material of the third adhesive layer is the same as the material of the first adhesive layer and the second adhesive layer.

8. The semiconductor device package as claimed in claim **6**, wherein the heat spreading structure is connected to a backside surface of the electronic component by a third adhesive layer, and a material of the third adhesive layer is different from the material of the first adhesive layer and the second adhesive layer.

9. The semiconductor device package as claimed in claim **1**, wherein the supporting structure further comprises a third pin portion extending from a bottom surface of the supporting structure and contacting a lateral surface of the substrate.

10. The semiconductor device package as claimed in claim **1**, wherein the supporting structure has a rectangular profile to encircle the electronic component.

11. The semiconductor device package as claimed in claim **10**, wherein the supporting structure has a first portion and a second portion surrounding the first portion, the first portion and the second portion have rectangular profiles, and a thickness of the second portion is smaller than a thickness of the first portion.

12. The semiconductor device package as claimed in claim **10**, wherein the supporting structure has a first portion and a second portion surrounding the first portion; the first portion has a rectangular profile, and the second portion comprises four prolonging portions extending from four corners of the first portion.

13. The semiconductor device package as claimed in claim **10**, wherein the supporting structure has a first portion and a second portion separated apart from the first portion; the first portion has a rectangular profile, and the second portion comprises four auxiliary portions separated from each other and extending from four sides of first portion.

14. The semiconductor device package as claimed in claim **1**, wherein the heat spreading structure has a vapor chamber.

15. A semiconductor device package, comprising:

a substrate;

a first electronic component disposed on the substrate;

a supporting structure surrounding the first electronic component, the supporting structure having a first portion over the substrate and a second portion extending laterally beyond a lateral surface of the substrate; and

a heat spreading structure covering the first electronic component and the supporting structure.

16. The semiconductor device package as claimed in claim **15**, wherein a length of the supporting structure and a length of the heat spreading structure are greater than a length of the substrate.

17. The semiconductor device package as claimed in claim **15**, wherein a thickness of the first portion of the supporting structure is greater than a thickness of the second portion of the supporting structure.

18. The semiconductor device package as claimed in claim **15**, further comprising a second electronic component disposed adjacent to the substrate and below the second portion of the supporting structure.

19. The semiconductor device package as claimed in claim **15**, wherein the first portion of the supporting structure has a rectangular profile, and the second portion of the supporting structure comprises four prolonging portions extending from four corners of the first portion.

20. The semiconductor device package as claimed in claim **15**, wherein the first portion of the supporting structure is separated apart from the second portion of the supporting structure.

21. The semiconductor device package as claimed in claim **15**, wherein the supporting structure further comprises a first pin portion extending from a bottom surface of the first portion into the substrate.

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