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(54) Title: STRUCTURE COMPRISING TUNABLE ANTI-REFLECTIVE COATING AND METHOD OF FORMING THEREOF

(57) Abstract: An interconnect structure in back end of line (BEOL) applications comprising a tunable etch resistant anti-reflective (TERA) coating is described. The TERA coating can, for example, be incorporated within a single damascene structure, or a dual damascene structure. The TERA coating can serve as part of a lithographic mask for forming the interconnect structure, or it may serve as a hard mask, a chemical mechanical polishing (CMP) stop layer, or a sacrificial layer during CMP.

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STRUCTURE COMPRISING TUNABLE ANTI-REFLECTIVE COATING AND METHOD OF FORMING THEREOF

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a structure comprising a tunable anti-reflective coating (ARC) and a method of forming the structure and, more particularly, to a back-end of line (BEOL) structure comprising a tunable ARC layer and a method of forming the structure.

Description of Related Art

[0002] In material processing methodologies, pattern etching comprises the application of a patterned mask of radiation-sensitive material, such as photoresist, to a thin film on an upper surface of a substrate, and transferring the mask pattern to the underlying thin film by etching. The patterning of the radiation-sensitive material generally involves coating an upper surface of the substrate with a thin film of radiation-sensitive material and then exposing the thin film of radiation-sensitive material to a radiation source through a reticle (and associated optics) using, for example, a photolithography system. Then a developing process is performed, during which the removal of the irradiated regions of the radiation-sensitive material occurs (as in the case of positive photoresist), or the removal of non-irradiated regions occurs (as in the case of negative resist) using a base developing solution, or solvent. The remaining radiation-sensitive material exposes the underlying substrate surface in a pattern that is ready to be etched into the surface. Photolithographic systems for performing the above-described material processing methodologies have become a mainstay of semiconductor device patterning for the last three decades, and are expected to continue in that role down to 65 nm resolution, and less.

[0003] The resolution (r_o) of a photolithographic system determines the minimum size of devices that can be made using the system. Having a given lithographic constant k_1, the resolution is given by the equation

$$r_o = k_1 \lambda / NA, \qquad (1)$$

[0004] where λ is the operational wavelength, and NA is the numerical aperture given by the equation

$$NA = n \cdot \sin \theta_o . \qquad (2)$$

[0005] Angle θ_o is the angular semi-aperture of the system, and n is the index of refraction of the material filling the space between the system and the substrate to be patterned.

[0006] Therefore, current lithographic trends involve increasing the numerical aperture (NA) in order to print smaller and smaller structures. However, although the increased NA permits greater resolution, the depth of focus for the images projected into the light-sensitive material is reduced, leading to thinner mask layers. As the light-sensitive layer thickness decreases, the patterned light-sensitive layer becomes less effective as a mask for pattern etching, i.e., most of the (light-sensitive) mask layer is consumed during etching. Without a dramatic improvement in etch selectivity, single layer masks have become deficient in providing the necessary lithographic and etch characteristics suitable for high resolution lithography.

[0007] An additional shortcoming of single layer masks is the control of critical dimension (CD). Substrate reflections at ultraviolet (UV) and deep ultraviolet (DUV) wavelengths are known to cause standing waves in the light-sensitive layer due to thin film interference. This interference manifests as periodic variations in light intensity in the light-sensitive layer during exposure resulting in vertically spaced striations in the light-sensitive layer and loss of CD.

[0008] In order to counter the effects of standing waves in the light-sensitive layer as well as provide a thicker mask for subsequent pattern etch transfer, a bilayer or multilayer mask can be formed that incorporates a bottom anti-reflective coating (BARC). The BARC layer comprises a thin absorbing film to reduce thin film interference; however, the BARC layer can still suffer from several limitations including poor thickness uniformity due in part to spin-on deposition techniques.

[0009] Alternatively, vapor deposited thin film ARC layers that offer the ability to tune the optical properties of the film have been proposed to alleviate many of the above identified problems. Known as tunable etch resistant ARC (TERA) layers, TERA films can be produced having a tunable index of refraction and extinction

coefficient which can be optionally graded along the film thickness to match the optical properties of the substrate with the imaging light-sensitive layer; see US Patent No. 6,316,167, assigned to International Business Machines Corporation. As described in this patent, TERA films are used in lithographic structures for front end of line (FEOL) operations, such as gate formation, where control of the critical dimension is very important. However, the present inventors have recognized that TERA films have not been used in back end of line (BEOL) operations, such as metal interconnect, perhaps due to the lesser importance of critical dimension to these operations.

Summary of the Invention

[0010] One aspect of the present invention is to reduce or eliminate any or all of the above-described problems.

[0011] Another object of the present invention is to provide a structure incorporating a tunable anti-reflective coating, and a method of forming the same.

[0012] According to another aspect, a semiconductor device is described comprising: a semiconductor substrate; a film stack formed on the semiconductor substrate and including a tunable anti-reflective coating formed within the film stack having a structural formula R:C:H:X, wherein R is selected from the group consisting of Si, Ge, B, Sn, Fe, Ti, and combinations thereof, and wherein X is not present or is selected from the group consisting of one or more of O, N, S, and F; and a damascene structure for a metal interconnect formed in the film stack.

[0013] According to another aspect, a process for forming an integrated circuit structure is described comprising: forming a layer of dielectric material on a substrate; forming a layer of tunable etch resistant anti-reflective (TERA) material on the layer of dielectric material; and forming a damascene structure for a metal interconnect by using the layer of TERA material as at least one of a lithographic structure for the formation of the interconnect structure, a hard mask, an anti-reflective coating, and a chemical mechanical polishing (CMP) stop layer.

[0014] According to another aspect, a semiconductor device is described comprising: a semiconductor substrate; a film stack formed on the semiconductor substrate; and means for integrating a tunable anti-reflective coating with a damascene structure for a metal interconnect formed in the film stack.

Brief Description of the Drawings

[0015] In the accompanying drawings:

[0016] FIGs. 1A through 1H present a simplified schematic representation of a method of forming an interconnect structure in accordance with an embodiment of the present invention;

[0017] FIGs. 2A through 2F present a simplified schematic representation of a method of forming an interconnect structure in accordance with another embodiment of the present invention;

[0018] FIGs. 3A through 3F present a simplified schematic representation of a method of forming an interconnect structure in accordance with another embodiment of the present invention;

[0019] FIGs. 4A through 4J present a simplified schematic representation of a method of forming an interconnect structure in accordance with another embodiment of the present invention;

[0020] FIGs. 5A through 5D present a simplified schematic representation of a method of forming an interconnect structure in accordance with another embodiment of the present invention; and

[0021] FIGs. 6A through 6I present a simplified schematic representation of a method of forming an interconnect structure in accordance with another embodiment of the present invention.

Detailed Description of Exemplary Embodiments

[0022] As described above, a tunable etch resistant anti-reflective (TERA) coating can be integrated in front end of line (FEOL) applications, such as the formation of a gate for transistor devices, wherein the TERA coating provides substantial improvement to a lithographic structure for forming gate devices at the 65 nm device node and smaller. However, these films have not been used in back end of line (BEOL) operations, such as metal interconnect, perhaps due to the lesser importance of critical dimension to these operations. The present inventors have recognized that use of TERA films as a tunable ARC layer as well as a removable etch hard mask, a sacrificial layer, or chemical-mechanical polishing (CMP) stop

layer provides useful properties for back end of line (BEOL) operations, such as metal interconnect. According to the present invention, at least one TERA coating is integrated with a back end of line (BEOL) application, such as within a single damascene or dual damascene metal interconnect structure formed in a film stack, wherein at least one TERA coating provides at least one of a lithographic structure for the formation of the interconnect structure, a hard mask, an anti-reflective coating, a sacrificial layer, or a chemical mechanical polishing (CMP) stop layer.

[0023] Referring now to the drawings, wherein like reference numerals designate identical or corresponding parts throughout the several views, FIGs. 1A through 1H present a schematic representation of a method of forming an interconnect structure in a film stack according to one embodiment. The method can be characterized as the integration of a TERA coating into a multiple hard mask via first dual damascene structure. The term "via-first", as used herein, refers to a process wherein an etch relating to formation of the via occurs before an etch relating to the formation of another feature such as a trench.

[0024] As shown in FIG. 1A, the method begins with preparing a film stack 100 comprising a substrate 110 having a metal line 112 formed therein, a metal cap layer 115 formed on the substrate 110, a first dielectric layer 120 formed on the metal cap layer 115, an etch stop layer 125 formed on the first dielectric layer 120, a second dielectric layer 130 formed on the etch stop layer 125, a hard mask layer 135 formed on the second dielectric layer 130, a tunable etch resistant anti-reflective (TERA) coating 140 formed on the hard mask layer 135, and a layer of light-sensitive material 145 formed on the TERA coating 140.

[0025] The film stack 100 may or may not include the hard mask layer 135. When film stack 100 includes hard mask layer 135, hard mask layer 135 can provide at least one of a hard mask, or a CMP stop layer, and TERA coating 140 can provide at least one of a top hard mask, a tunable ARC layer, a CMP stop layer, and a sacrificial layer when the hard mask layer 135 is utilized as CMP stop layer in a dual damascene structure. When film stack 100 does not include hard mask layer 135, TERA coating 140 provides at least one of a single hard mask, a tunable ARC layer, and a CMP stop layer. The utilization of the TERA coating 140 as the layer in contact with the light-sensitive material 145 of the film stack 100 can facilitate control of the critical dimension (CD) of the interconnect structure, or

control of CD variation within the interconnect structure (due to, for example, line edge roughness in the layer of light-sensitive layer 145). The formation of the film stack 100 can comprise steps, and utilize techniques known to those skilled in the art of preparing such (insulating) film stacks for inter-level, and intra-level, (metal) interconnect structures, such as single damascene and dual damascene structures.

[0026] For example, the metal line 112 can comprise tungsten, aluminum, or copper. Additionally, for example, the metal cap layer 115 can comprise a nitride or carbide material, such as silicon nitride (Si_3N_4) or silicon carbide (SiC) or silicon carbonitride (SiCN) or silicon oxycarbonitride (SiCON), or combinations thereof, or other films suitable as a metal diffusion barrier. This layer can be formed using methods including but not limited to chemical vapor deposition (CVD), or plasma enhanced CVD (PECVD). Additionally, for example, the etch stop layer 125, which can be an optional layer (as will be described later), can comprise a nitride material, such as silicon nitride (Si_3N_4), a carbide material, such as silicon carbide (SiC) or silicon oxycarbide (SiCO), or an oxide material such as silicon dioxide (SiO_2), or combinations thereof. This layer can be formed using methods including but not limited to chemical vapor deposition (CVD), or plasma enhanced CVD (PECVD).

[0027] The first dielectric layer 120 and the second dielectric layer 130 can comprise the same material composition, or different material composition. Each dielectric layer can, for example, comprise silicon dioxide, or a dielectric material having a nominal dielectric constant value less than the dielectric constant of SiO_2, which is approximately 4 (e.g., the dielectric constant for thermal silicon dioxide can range from 3.8 to 3.9). More specifically, the first and second dielectric layers 120, 130 may have a dielectric constant of less than 3.7, or a dielectric constant ranging from 1.6 to 3.7.

[0028] Each dielectric layer 120, 130 can be formed using chemical vapor deposition (CVD) or plasma enhanced chemical vapor deposition (PECVD) techniques, or spin-on dielectric (SOD) techniques such as those offered in the Clean Track ACT 8 SOD and ACT 12 SOD coating systems commercially available from Tokyo Electron Limited (TEL). The Clean Track ACT 8 (200 mm) and ACT 12 (300 mm) coating systems provide coat, bake, and cure tools for SOD materials. The track system can be configured for processing substrate

sizes of 100 mm, 200 mm, 300 mm, and greater. Other systems and methods for forming a dielectric film on a substrate are well known to those skilled in the art of both spin-on dielectric technology and CVD dielectric technology.

[0029] Furthermore, the first and second dielectric layers 120, 130 may, for example, be characterized as low dielectric constant (or low-k) dielectric films. These dielectric layers may include at least one of an organic, inorganic, and inorganic-organic hybrid material. Additionally, these dielectric layers may be porous or non-porous. For example, these dielectric layers may include an inorganic, silicate-based material, such as carbon doped silicon oxide (or organo siloxane), deposited using CVD techniques. Examples of such films include Black Diamond™ CVD organosilicate glass (OSG) films commercially available from Applied Materials, Inc., or Coral™ CVD films commercially available from Novellus Systems. Alternatively, these dielectric layers may include porous inorganic-organic hybrid films comprised of a single-phase, such as a silicon oxide-based matrix having CH_3 bonds that hinder full densification of the film during a curing or deposition process to create small voids (or pores). Still alternatively, these dielectric layers may include porous inorganic-organic hybrid films comprised of at least two phases, such as a carbon-doped silicon oxide-based matrix having pores of organic material (e.g., porogen) that is decomposed and evaporated during a curing process. Still alternatively, these dielectric layers may include an inorganic, silicate-based material, such as hydrogen silsesquioxane (HSQ) or methyl silsesquioxane (MSQ), deposited using SOD techniques. Examples of such films include FOx HSQ commercially available from Dow Corning, XLK porous HSQ commercially available from Dow Corning, and JSR LKD-5109 commercially available from JSR Microelectronics. Still alternatively, these dielectric layers can comprise an organic material deposited using SOD techniques. Examples of such films include SiLK-I, SiLK-J, SiLK-H, SiLK-D, and porous SiLK semiconductor dielectric resins commercially available from Dow Chemical, and GX-3™, and GX-3P™ semiconductor dielectric resins commercially available from Honeywell.

[0030] Additionally, for example, the (optional) hard mask layer 135 can comprise a nitride, such as silicon nitride (Si_3N_4), a carbide, such as silicon carbide (SiC) or silicon oxycarbide (SiCO), or a refractory metal or refractory metal nitride such as tantalum nitride (TaN), or combinations thereof. This layer may be formed

employing methods including but not limited to chemical vapor deposition (CVD) methods, plasma enhanced chemical vapor deposition (PECVD) methods and physical vapor deposition (PVD) sputtering methods.

[0031] The TERA coating 140 comprises a structural formula R:C:H:X, wherein R is selected from the group consisting of Si, Ge, B, Sn, Fe, Ti, and combinations thereof, and wherein X is not present or is selected from the group consisting of one or more of O, N, S, and F. The TERA coating 140 can be fabricated to demonstrate an optical range for index of refraction of approximately $1.40 < n < 2.60$, and for extinction coefficient of approximately $0.01 < k < 0.78$. Alternately, at least one of the index of refraction and the extinction can be graded (or varied) along a thickness of the TERA coating 140. Additional details are provided in US Patent No. 6,316,167, entitled "Tunable vapor deposited materials as antireflective coatings, hardmasks and as combined antireflective coating/hardmasks and methods of fabrication thereof and application thereof, assigned to International Business Machines Corporation; the entire contents of which are incorporated herein in their entirety. Furthermore, the TERA coating 140 can be formed using PECVD, as described in greater detail in pending US Patent Application, entitled "Method and apparatus for depositing materials with tunable optical properties and etching characteristics", filed on August 21, 2003; the entire contents of which are incorporated herein in their entirety. The optical properties of the TERA coating 140, such as the index of refraction, can be selected so as to substantially match the optical properties of the underlying layer, or layers. For example, underlying layers such as non-porous dielectric films can require achieving an index of refraction in the range of $1.4<n<2.6$; and underlying layers such as porous dielectric films can require achieving an index of refraction in the range of $1.2<n<2.6$.

[0032] Additionally, for example, the layer of light-sensitive material 145 can comprise photoresist, wherein a pattern can be formed therein using micro-lithography, followed by the removal of the irradiated regions of the light-sensitive material (as in the case of positive photoresist), or non-irradiated regions (as in the case of negative resist) using a developing solvent. For example, the layer (or layers) of light-sensitive material 145 can be formed using a track system. The track system can be configured for processing 248 nm resists, 193 nm resists, 157 nm resists, EUV resists, (top/bottom) anti-reflective coatings (TARC/BARC),

and top coats. For example, the track system can comprise a Clean Track ACT 8, or ACT 12 resist coating and developing system commercially available from Tokyo Electron Limited (TEL). Other systems and methods for forming a photoresist film on a substrate are well known to those skilled in the art of spin-on resist technology. Additionally, for example, the mask pattern can be formed using any suitable conventional stepping lithographic system, or scanning lithographic system.

[0033] Once the layer of light-sensitive material 145 is formed on film stack 100, it can be patterned with a first pattern 180 using micro-lithography, as described above. The first pattern 180 can, for example, comprise a pattern for a via, or contact. As shown in FIG. 1B, the first pattern 180 can be transferred to the TERA coating using, for example, dry plasma etching. The dry plasma etch process can comprise a plasma chemistry containing at least one of the species selected from the group consisting of oxygen, fluorine, chlorine, bromine, hydrogen, and combinations thereof. Alternatively, the plasma chemistry can further comprise nitrogen or an inert gas, such as a Noble gas (i.e., helium, neon, argon, xenon, krypton, radon). Still alternatively, the plasma chemistry is chosen to exhibit high etch selectivity between the etch rate of the TERA coating and the etch rate of the overlying patterned layer of light-sensitive material. Still alternatively, the plasma chemistry is chosen to exhibit high etch selectivity between the etch rate of the TERA coating and the etch rate of the underlying hard mask layer. Once the first pattern 180 is transferred to the TERA coating 140, the patterned TERA coating 140 can be utilized as a single hard mask, or a top hard mask, when utilized with the hard mask stop layer 135, for etching the underlying film stack. The remaining light-sensitive material 145 is then removed using plasma or other chemical techniques known to those skilled in the art.

[0034] Referring now to FIG. 1C, another layer of light-sensitive material 146 is formed on film stack 100 using techniques described above. Therein, a second pattern 190 is formed using micro-lithography. The second pattern 190 can, for example, comprise a trench pattern. Once the second pattern 190 is formed in the layer of light-sensitive material 146, the second pattern 190 is transferred to the TERA coating 140, and the first pattern 180 is transferred to the hard mask layer 135, as shown in FIG. 1D. For example, the transfer of the second pattern

and the first pattern to the TERA coating and the hard mask layer, respectively, can be performed simultaneously.

[0035] Following the pattern transfers to the TERA coating 140 and the hard mask layer 135, FIG. 1E illustrates the transfer of the first pattern 180 to the second dielectric layer 130. Because the intermediate via etch step of FIG. 1E is stopped at the etch stop layer 125, the structure of FIG. 1E is referred to herein as a partial via structure. The transfer of the first pattern 180 to the second dielectric layer 130 can comprise dry plasma etching, wherein the process is designed to stop on the underlying etch stop layer 125.

[0036] For instance, when etching oxide dielectric films such as silicon oxide, silicon dioxide, etc., or when etching inorganic low-k dielectric films such as carbon doped silicon oxide materials, the etch gas composition generally includes a fluorocarbon-based chemistry such as at least one of C_4F_8, C_5F_8, C_3F_6, C_4F_6, CF_4, etc., and at least one of an inert gas, oxygen, or CO. Additionally, for example, when etching organic low-k dielectric films, the etch gas composition may include at least one of a fluorocarbon gas, a nitrogen-containing gas, a hydrogen-containing gas, or an oxygen-containing gas. The techniques for selectively etching a dielectric film, such as those described earlier, are well known to those skilled in the art of dielectric etch processes. The plasma chemistry can be chosen to exhibit a high selectivity for etching the second dielectric layer 130 relative to the etch stop layer 125. The etching processes can be chosen to exhibit any one of profile and critical dimension (CD) control, etch uniformity (across the substrate), a flat etch front in order to avoid micro-trenching, etch selectivity to the layer of light-sensitive material, and etch selectivity to the CMP stop layer and the etch stop layer.

[0037] Referring now to FIG. 1F, the first pattern 180 is transferred to the etch stop layer 125, and the second pattern 190 is transferred to the hard mask layer 135. For example, the transfer of the first pattern and the second pattern to the etch stop layer and the hard mask layer, respectively, can be performed simultaneously. The pattern transfer can utilize dry plasma etching, wherein the plasma chemistry comprises at least one of NF_3, SF_6, HBr, a fluorocarbon gas, a hydrofluorocarbon gas, or an oxygen-containing gas. The etching processes can be chosen to exhibit any one of profile and critical dimension (CD) control, etch

selectivity to the layer of light-sensitive material, etch uniformity (across the substrate), and complete hard mask layer and etch stop layer removal.

[0038] In FIG. 1G, the second pattern 190 is transferred to the second dielectric layer 130, and the first pattern 180 is transferred to the first dielectric layer 120. For example, the transfer of the second pattern and the first pattern to the second dielectric layer and the first dielectric layer, respectively, can be performed simultaneously, wherein the etching process for the second dielectric layer stops on the etch stop layer 125, and the etching process for the first dielectric layer stops on the metal cap layer 115. The etching processes can comprise dry plasma etching, utilizing plasma chemistries such as those described above for dielectric layers. The etching processes can be chosen to exhibit any one of profile and critical dimension (CD) control, etch uniformity (across the substrate), a flat etch front in order to avoid micro-trenching, and first pattern/second pattern corner selectivity. Any remaining light-sensitive material 146 may then be removed using plasma or other chemical techniques known to those skilled in the art.

[0039] Thereafter, as shown in FIG. 1H, the first pattern 180 is transferred to the metal cap layer 115, hence, completing the formation of, for example, a via structure 155 and a trench structure 150.

[0040] According to another embodiment, FIGs. 2A through 2F present a schematic representation of a method of forming an interconnect structure in a film stack 200. The method can be characterized as the integration of a TERA coating into a full via first dual damascene structure. As used herein, the term "full-via-first" refers to a process wherein an etch relating to full formation of the via occurs before an etch relating to the formation of another feature such as a trench. The film stack 200 comprises a substrate 210 having a metal line 212 formed therein, a metal cap layer 215 formed on the substrate 210, a first dielectric layer 220 formed on the metal cap layer 215, an etch stop layer 225 formed on the first dielectric layer 220, a second dielectric layer 230 formed on the etch stop layer 225, a hard mask layer 235 formed on the second dielectric layer 230, a tunable etch resistant anti-reflective (TERA) coating 240 formed on the hard mask layer 235, and a layer of light-sensitive material 245 formed on the TERA coating 240, and it can be prepared in much the same manner as the film stack 100 described in FIG. 1A. The film stack 200 may or may not include the

hard mask layer 235. When film stack 200 includes hard mask layer 235, hard mask layer 235 can provide at least one of a hard mask, or a CMP stop layer, and the TERA coating 240 can provide at least one of a top hard mask, a tunable ARC layer, a CMP stop layer, and a sacrificial layer when the hard mask layer 235 is utilized as CMP stop layer in a dual damascene structure. When film stack 200 does not include hard mask layer 235, TERA coating 240 provides at least one of a single hard mask, a tunable ARC layer, and a CMP stop layer.

[0041] Once the layer of light-sensitive material 245 is formed on film stack 200, it can be patterned with a first pattern 280 using micro-lithography, as described above. The first pattern 280 can, for example, comprise a pattern for a via, or contact. As shown in FIG. 2B, the first pattern 280 can be transferred to the TERA coating 240, the (optional) hard mask layer 235, the second dielectric layer 230, the etch stop layer 225, and the first dielectric layer 220 using, for example, dry plasma etching. The etching process for each layer can comprise steps, and chemistries similar to those described above. Because the intermediate via etch step of FIG. 2B is stopped at the metal cap layer 215, the structure of FIG. 2B is referred to herein as a full via structure. Any remaining light-sensitive material 245 is then removed using plasma or other chemical techniques known to those skilled in the art.

[0042] Referring now to FIG. 2C, another layer of light-sensitive material 246 is formed on film stack 200 using techniques described above. Therein, a second pattern 290 is formed using micro-lithography. The second pattern 290 can, for example, comprise a trench pattern. Once the second pattern 290 is formed in the layer of light-sensitive material 246, the second pattern 290 is transferred to the TERA coating 240, the hard mask layer 235, and the second dielectric layer 230. Any remaining light-sensitive material 246 is then removed using plasma or other chemical techniques known to those skilled in the art. Thereafter, as shown in FIG. 2D, the first pattern 280 is transferred to the metal cap layer 215, hence, completing the formation of, for example, a via structure 250 and a trench structure 255.

[0043] It is possible that during the removal of the light-sensitive layer 245 following the pattern transfer of the first pattern 280, the ashing (or stripping) process can affect the properties of TERA coating 240. Therefore, in one embodiment of the present invention, the TERA coating 240 can be removed and

re-deposited as shown in FIG. 2E. Thereafter, the pattern transfer of the second pattern 290 can be performed as shown in FIGs. 2C and 2D. However, during this etching process, the TERA coating 240 may or may not be entirely removed from the exposed sidewalls of the first dielectric film 220. Therefore, in an alternate embodiment, as shown in FIG. 2F, the TERA coating 240 is removed following the first pattern transfer, and a BARC layer material 270 is applied using, for example, spin coating techniques. The BARC layer material 270 filling via structure 250 may then be partially removed or recessed using a dry plasma etch. The etch gas composition may include at least one of a fluorocarbon gas, a nitrogen-containing gas, a hydrogen-containing gas, or an oxygen-containing gas. Thereafter, the pattern transfer of the second pattern 290 can be performed using standard techniques known to those skilled in the art.

[0044] According to another embodiment, FIGs. 3A through 3F present a schematic representation of a method of forming an interconnect structure in a film stack 300. The method can be characterized as the integration of a TERA coating into a full via first dual damascene structure without a stop layer. The film stack 300 comprises a substrate 310 having a metal line 312 formed therein, a metal cap layer 315 formed on the substrate 310, a dielectric layer 320 formed on the metal cap layer 315, a tunable etch resistant anti-reflective (TERA) coating 340 formed on the dielectric layer 320, and a layer of light-sensitive material 345 formed on the TERA coating 340, and each layer in film stack 300 can be prepared in much the same manner as the film stack 100 described in FIG. 1A. Herein, the TERA coating 340 can provide a CMP stop layer and a tunable ARC layer.

[0045] Once the layer of light-sensitive material 345 is formed on film stack 300, it can be patterned with a first pattern 380 using micro-lithography, as described above. The first pattern 380 can, for example, comprise a pattern for a via, or contact. As shown in FIG. 3B, the first pattern 380 can be transferred to the TERA coating 340, and the dielectric layer 320 using, for example, dry plasma etching. The etching process for each layer can comprise steps, and chemistries similar to those described above. Any remaining light-sensitive material 345 is then removed using plasma or other chemical techniques known to those skilled in the art.

[0046] Referring now to FIG. 3C, another layer of light-sensitive material 346 is formed on film stack 300 using techniques described above. Therein, a second pattern 390 is formed using micro-lithography. The second pattern 390 can, for example, comprise a trench pattern. Once the second pattern 390 is formed in the layer of light-sensitive material 346, the second pattern 390 is transferred to the TERA coating 340, and an upper portion of the dielectric layer 320. The depth to which the second pattern 390 is transferred into the dielectric layer 320 can be adjusted by decreasing, or increasing, the etch time during the etching process. Any remaining light-sensitive material 346 is then removed using plasma or other chemical techniques known to those skilled in the art. Thereafter, as shown in FIG. 3D, the first pattern 380 is transferred to the metal cap layer 315, hence, completing the formation of, for example, a via structure 350 and a trench structure 355.

[0047] As described above, it is possible that during the removal of the light-sensitive layer 345 following the pattern transfer of the first pattern 380, the ashing (or stripping) process can affect the properties of TERA coating 340. Therefore, in one embodiment, the TERA coating 340 can be removed and re-deposited as shown in FIG. 3E. Thereafter, the pattern transfer of the second pattern 390 can be performed as shown in FIGs. 3C and 3D. During this etching process, however, the TERA coating 340 may or may not be entirely removed from the exposed sidewalls of the dielectric layer 320. In an alternate embodiment, as shown in FIG. 3F, the TERA coating 340 is removed following the first pattern transfer, and a BARC layer 370 is applied using, for example, spin coating techniques. The BARC layer material 370 filling via structure 350 may then be partially removed or recessed using a dry plasma etch. The etch gas composition may include at least one of a fluorocarbon gas, a nitrogen-containing gas, a hydrogen-containing gas, or an oxygen-containing gas. Thereafter, the pattern transfer of the second pattern 390 can be performed using standard techniques known to those skilled in the art.

[0048] According to yet another embodiment, FIGs. 4A through 4K present a schematic representation of a method of forming an interconnect structure in a film stack 400. The method can be characterized as the integration of a TERA coating into a multiple hard mask trench first dual damascene structure. The film stack 400 comprises a substrate 410 having a metal line 412 formed therein, a

metal cap layer 415 formed on the substrate 410, a first dielectric layer 420 formed on the metal cap layer 415, an (optional) etch stop layer 425 formed on the first dielectric layer 420, a second dielectric layer 430 formed on the (optional) etch stop layer 425, an (optional) hard mask layer 435 formed on the second dielectric layer 430, a tunable etch resistant anti-reflective (TERA) coating 440 formed on the (optional) hard mask layer 435, a second TERA coating 441 formed on the first TERA coating 440, and a layer of light-sensitive material 445 formed on the TERA coating 441, and it can be prepared in much the same manner as the film stack 100 described in FIG. 1A. The film stack 400 may or may not include the hard mask layer 435. When film stack 400 includes hard mask layer 435, hard mask layer 435 can provide at least one of a hard mask, or a CMP stop layer, and the second TERA coating 441 can provide at least one of a top hard mask, a tunable ARC layer, a CMP stop layer, and a sacrificial layer when the hard mask layer 435 is utilized as CMP stop layer in a dual damascene structure. When film stack 400 does not include hard mask layer 435, the second TERA coating 441 provides at least one of a single hard mask, a tunable ARC layer, and a CMP stop layer.

[0049] Once the layer of light-sensitive material 445 is formed on film stack 400, it can be patterned with a first pattern 480 using micro-lithography, as described above. The first pattern 480 can, for example, include a pattern for a trench. As shown in FIG. 4B, the first pattern 480 can be transferred to the second TERA coating 441 using, for example, dry plasma etching. The etching process can comprise steps, and chemistries similar to those described above. Any remaining light-sensitive material 445 may then removed using plasma or other chemical techniques known to those skilled in the art.

[0050] Referring now to FIG. 4C, another layer of light-sensitive material 446 is formed on film stack 400 using techniques described above. Therein, a second pattern 490 is formed using micro-lithography. The second pattern 490 can, for example, comprise a via pattern. As shown in FIG. 4D, once the second pattern 490 is formed in the layer of light-sensitive material 445, the second pattern 490 is transferred to the first TERA coating 440, and the (optional) hard mask layer 435.

[0051] Thereafter, as shown in FIG. 4E, the second pattern 490 is transferred to the second dielectric layer 430. Referring now to FIG 4F, any remaining light-

sensitive material 446 is then removed using plasma or other chemical techniques known to those skilled in the art.

[0052] In FIG. 4G, the first pattern 480 is transferred to the first TERA coating and the second pattern 490 is transferred to the (optional) etch stop layer 425. The transfer of the first pattern and the second pattern to the first TERA coating and the (optional) etch stop layer, respectively, can be performed simultaneously, wherein the etching process for the first TERA coating stops on the hard mask layer 435, and the etching process for the (optional) etch stop layer stops on the first dielectric layer 420. The etching processes can comprise dry plasma etching, utilizing plasma chemistries such as those described above for dielectric layers. The etching processes can be chosen to exhibit any one of profile and critical dimension (CD) control, etch uniformity (across the substrate), a flat etch front in order to avoid micro-trenching, and first pattern/second pattern corner selectivity.

[0053] Referring now to FIG. 4H, the first pattern 480 is transferred to the hard mask layer 435 and the second pattern 490 is partially transferred to the first dielectric layer 420. Thereafter, as shown in FIG. 4I, the first pattern 480 is transferred to the second dielectric layer 430 and the second pattern 490 is transferred to the first dielectric layer 420. The transfer of the first pattern and the second pattern to the second dielectric layer and the first dielectric layer, respectively, can be performed simultaneously, wherein the etching process for the second dielectric layer stops on the etch stop layer 425, and the etching process for the first dielectric layer stops on the metal cap layer 415. The etching processes can comprise dry plasma etching, utilizing plasma chemistries such as those described above for dielectric layers. The etching processes can be chosen to exhibit any one of profile and critical dimension (CD) control, etch uniformity (across the substrate), a flat etch front in order to avoid micro-trenching, and first pattern/second pattern corner selectivity.

[0054] Thereafter, as shown in FIG. 4J, the second pattern 490 is transferred to the metal cap layer 415, hence, completing the formation of, for example, a via structure 455 and a trench structure 450.

[0055] According to another embodiment, FIGs. 5A through 5D present a schematic representation of a method of forming an interconnect structure in a film stack 500. The method can be characterized as the integration of a TERA coating with a buried via mask dual damascene structure. The film stack 500

comprises a substrate 510 having a metal line 512 formed therein, a metal cap layer 515 formed on the substrate 510, a first dielectric layer 520 formed on the metal cap layer 515, a first tunable etch resistant anti-reflective (TERA) coating 540 formed on the first dielectric layer 520, and a layer of light-sensitive material 545 formed on the first TERA coating 540. Each layer can be prepared in much the same manner as the film stack 100 described in FIG. 1A.

[0056] Once the layer of light-sensitive material 545 is formed on film stack 500, it can be patterned with a first pattern 580 using micro-lithography, as described above. The first pattern 580 can, for example, comprise a pattern for a via, or contact. As shown in FIG. 5B, the first pattern 580 can be transferred to the first TERA coating 540 using, for example, dry plasma etching. The etching process for the first TERA layer can comprise steps, and chemistries similar to those described above. Following the etching process, the remaining layer of light-sensitive material 545 is removed using plasma or other chemical techniques known to those skilled in the art.

[0057] Now referring to FIG. 5C, a second dielectric layer 530 is formed on the patterned first TERA coating 540, a hard mask layer 535 is formed on the second dielectric layer 530, a second TERA coating 542 is formed on the hard mask layer 535, and another layer of light-sensitive material 546 is formed on the second TERA coating 542. Each layer can be prepared in much the same manner as the film stack 100 described in FIG. 1A. The film stack 500 may or may not include the hard mask layer 535. When film stack 500 includes hard mask layer 535, hard mask layer 535 can provide at least one of a hard mask, or a CMP stop layer, and TERA coating 540 can provide at least one of a top hard mask, a tunable ARC layer, a CMP stop layer, and a sacrificial layer when the hard mask layer 535 is utilized as CMP stop layer in a dual damascene structure. When film stack 500 does not include hard mask layer 535, TERA coating 540 provides at least one of a single hard mask, a tunable ARC layer, and a CMP stop layer.

[0058] Once the additional layer of light-sensitive material 546 is formed on film stack 500, a second pattern 590 is formed using micro-lithography. The second pattern 590 can, for example, comprise a pattern for a trench. As shown in FIG. 5D, once the second pattern 590 is formed in the layer of light-sensitive material 546, the second pattern 590 is transferred to the second TERA coating 542, the (optional) hard mask layer 535, and the second dielectric layer 530 using, for

example, dry plasma etching. While the first TERA coating 540 serves as an etch stop layer, the first pattern 580 is transferred to the first dielectric layer 520 using, for example, dry plasma etching. Any remaining light-sensitive material 546 may then removed using plasma or other chemical techniques known to those skilled in the art. Thereafter, the metal cap layer 515 can be removed, hence, completing the formation of, for example, a via structure 550 and a trench structure 555. The etching processes for each layer can comprise steps, and chemistries similar to those described above.

[0059] According to another embodiment, FIGs. 6A through 6I present a schematic representation of a method of forming an interconnect structure in a film stack 600. The method can be characterized as the integration of a TERA coating with single damascene structure. The film stack 600 comprises a substrate 610 having a metal line 612 formed therein, a metal cap layer 615 formed on the substrate 610, a first dielectric layer 620 formed on the metal cap layer 615, an (optional) first hard mask 625 formed on the first dielectric layer 620, a first TERA coating 640 formed on the first (optional) hard mask 625, and a layer of light-sensitive material 645 formed on the first TERA coating 640. Each layer can be prepared in much the same manner as the film stack 100 described in FIG. 1A.

[0060] The film stack 600 may or may not include the hard mask layer 625. When film stack 600 includes hard mask layer 625, hard mask layer 625 can provide at least one of a hard mask, or a CMP stop layer, and TERA coating 640 can provide at least one of a top hard mask, a tunable ARC layer, and a CMP stop layer. When film stack 600 does not include hard mask layer 625, TERA coating 640 provides at least one of a single hard mask, a tunable ARC layer, and a CMP stop layer.

[0061] Once the layer of light-sensitive material 645 is formed on film stack 600, it can be patterned with a first pattern 680 using micro-lithography, as described above. The first pattern 680 can, for example, comprise a pattern for a via, or contact. As shown in FIG. 6B, the first pattern 680 can be transferred to the first TERA coating 640 and the (optional) first hard mask 625 using, for example, dry plasma etching. The etching process(es) can comprise steps, and chemistries similar to those described above. Thereafter, as shown in FIG. 6C, the first pattern 680 is transferred to the first dielectric layer 620 using, for example, dry

plasma etching. The etching process can comprise steps, and chemistries similar to those described above. Following the etching process, as illustrated in FIG. 6D, the remaining layer of light-sensitive material 645 is removed using plasma or other chemical techniques known to those skilled in the art.

[0062] Referring now to FIG. 6E, the first pattern 680 is transferred to the metal cap layer 615 using, for example, dry plasma etching. The etching process can comprise steps, and chemistries similar to those described above.

[0063] Now referring to FIG. 6F, metal, such as aluminum or copper, is deposited on film stack 600 to fill the first pattern (or via) in the first dielectric layer 620 using at least one of physical vapor deposition (PVD), CVD, PECVD, electro-plating, or any combination thereof. Once the metal deposition is complete, the metal is polished, using, for example, CMP, to the first hard mask layer 625. Thereafter, a second metal cap layer 626 is formed on the first (optional) hard mask layer 625 and metal-filled first pattern (or via) 613, a second dielectric layer 630 is formed on the second metal cap layer 626, a second (optional) hard mask layer 635 is formed on the second dielectric layer 630, a second TERA coating 641 is formed on the second (optional) hard mask layer 635, and another layer of light-sensitive material 646 is formed on the second TERA coating 641. Each layer can be prepared in much the same manner as the film stack 100 described in FIG. 1A. The film stack 600 may or may not include the second hard mask layer 635. When film stack 600 includes hard mask layer 635, hard mask layer 635 can provide at least one of a hard mask, or a CMP stop layer, and TERA coating 641 can provide at least one of a top hard mask, a tunable ARC layer, and a CMP stop layer. When film stack 600 does not include hard mask layer 635, TERA coating 640 provides at least one of a single hard mask, a tunable ARC layer, and a CMP stop layer.

[0064] Once the additional layer of light-sensitive material 646 is formed on film stack 600, a second pattern 690 is formed using micro-lithography. The second pattern 690 can, for example, comprise a pattern for a trench. As shown in FIG. 6G, once the second pattern 690 is formed in the layer of light-sensitive material 646, the second pattern 690 is transferred to the second TERA coating 641, the second (optional) hard mask layer 635, and the second dielectric layer 630 using, for example, dry plasma etching. As illustrated in FIG. 6H, any remaining light-sensitive material 646 may then removed using plasma or other chemical

techniques known to those skilled in the art. Thereafter, the second metal cap layer 626 can be removed, hence, completing the formation of, for example, a via structure 650 (filled with metal) and a trench structure 655 (prepared for metal fill). The etching processes for each layer can comprise steps, and chemistries similar to those described above.

[0065] Although only certain exemplary embodiments of this invention have been described in detail above, those skilled in the art will readily appreciate that many modifications are possible in the exemplary embodiments without materially departing from the novel teachings and advantages of this invention. Accordingly, all such modifications are intended to be included within the scope of this invention.

CLAIMS:

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a film stack formed on the semiconductor substrate and including a tunable anti-reflective coating formed within said film stack having a structural formula R:C:H:X, wherein R is selected from the group consisting of Si, Ge, B, Sn, Fe, Ti, and combinations thereof, and wherein X is not present or is selected from the group consisting of one or more of O, N, S, and F; and

a damascene structure for a metal interconnect formed in the film stack.

2. The device of claim 1, wherein said tunable anti-reflective coating comprises a part of a lithographic structure during the formation of said metal interconnect in said film stack.

3. The device of claim 1, wherein said tunable anti-reflective coating comprises a chemical mechanical polishing (CMP) stop layer for said damascene structure.

4. The device of claim 1, wherein said tunable anti-reflective coating comprises at least one of a single hard mask, a top layer in a multiple layer hard mask, and an anti-reflective coating.

5. The device of claim 1, wherein said tunable anti-reflective coating is configured to have optical properties that substantially match the optical properties of said film stack.

6. The device of claim 5, wherein said optical properties comprise at least one of an index of refraction, and an extinction coefficient.

7. The device of claim 6, wherein said index of refraction comprises a value ranging from 1.4 to 2.6.

8. The device of claim 6, wherein said extinction coefficient comprises a value ranging from 0.01 to 0.78.

9. The device of claim 6, wherein at least one of said index of refraction and said extinction coefficient is graded along a thickness of said tunable anti-reflective coating.

10. The device of claim 6, wherein said index of refraction comprises a value ranging from 1.2 to 2.6.

11. The device of claim 1, wherein said tunable anti-reflective coating comprises at least one of chemical vapor deposition (CVD) coating, and plasma enhanced CVD coating.

12. The device of claim 1, wherein said tunable anti-reflective coating is configured to provide at least one of control of a critical dimension of said single damascene structure, and control of a critical dimension variation of said damascene structure.

13. The semiconductor device of claim 1, wherein said damascene structure is a single damascene structure.

14. The semiconductor device of claim 1, wherein said damascene structure is a dual damascene structure.

15. The semiconductor device of Claim 1, wherein said film stack further comprises a low-k dielectric layer.

16. A process for forming an integrated circuit structure comprising:

forming a layer of dielectric material on a substrate;

forming a layer of tunable etch resistant anti-reflective (TERA) material on said layer of dielectric material; and

forming a damascene structure for a metal interconnect by using said layer of TERA material as at least one of a lithographic structure for the formation

of the interconnect structure, a hard mask, an anti-reflective coating, and a chemical mechanical polishing (CMP) stop layer.

17. The process of Claim 16, further comprising:

forming a layer of light-sensitive material on said layer of TERA material, wherein the optical properties of said light-sensitive layer and said TERA layer are substantially the same;

and

exposing said layer of light-sensitive material to a pattern of radiation,

wherein said forming said layer of TERA material facilitates producing a pattern in said layer of light-sensitive material substantially the same as said pattern of radiation.

18. The process of claim 17, wherein said forming said layer of TERA material comprises providing a part of the lithographic structure for the formation of a metal interconnect for said device structure.

19. The process of claim 17, wherein said forming said layer of TERA material comprises depositing said layer of TERA material using at least one of chemical vapor deposition (CVD), and plasma enhanced CVD.

20. The process of Claim 16, wherein said forming a damascene structure comprises integrating a tunable anti-reflective coating with a single damascene structure.

21. The process of Claim 16, wherein said forming a damascene structure comprises integrating a tunable anti-reflective coating with a dual damascene structure.

22. The process of Claim 21, wherein said forming a damascene structure comprises integrating a tunable anti-reflective coating with a dual damascene structure formed using a method comprising at least one a via-first method, a full-via-first method, a full-via with no stop layer method, a trench-first method, and a buried via mask method.

23. A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a second dielectric layer formed on said first dielectic layer, a hard mask layer formed on said dielectric layer, a tunable etch resistant anti-reflective (TERA) coating formed on said hard mask layer, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said TERA coating;

forming a second layer of light-sensitive material on said TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said TERA coating;

transferring said first pattern to said hard mask layer;

transferring said first pattern to said second dielectric layer;

transferring said second pattern to said hard mask layer;

transferring said second pattern to said second dielectric layer;

transferring said first pattern to said first dielectric layer; and

transferring said first pattern to said metal cap layer.

24. The method of claim 23, further comprising:

removing said first layer of light-sensitive material.

25. The method of claim 23, further comprising:

removing said second layer of light-sensitive material.

26. The method of claim 23, further comprising:

preparing said film stack with an etch stop layer formed on said first dielectric layer prior to said second dielectric layer formed on said etch stop layer; and

transferring said first pattern to said etch stop layer.

27. The method of claim 23, further comprising:

forming a layer of bottom anti-reflective coating (BARC) on said TERA coating; and

removing said BARC layer.

28. A semiconductor device comprising:

a semiconductor substrate;

a film stack formed on the semiconductor substrate; and

means for integrating a tunable anti-reflective coating with a damascene structure for a metal interconnect formed in the film stack.

29. A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a second dielectric layer formed on said first dielectric layer, a hard mask layer formed on said dielectric layer, a first tunable etch resistant anti-reflective (TERA) coating formed on said hard mask layer, a second TERA coating formed on said first TERA coating, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said second TERA coating;

forming a second layer of light-sensitive material on said TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said first TERA coating;

transferring said second pattern to said hard mask layer;

transferring said second pattern to said second dielectric layer;

transferring said second pattern to said first dielectric layer;

transferring said first pattern to said first TERA coating;

transferring said first pattern to said hard mask layer;

transferring said first pattern to said second dielectric layer; and

transferring said second pattern to said metal cap layer.

30. The method of claim 29, further comprising:

removing said first layer of light-sensitive material following said transferring said first pattern to said second TERA coating.

31. The method of claims 29, or 30, further comprising:

removing said second layer of light-sensitive material following said transferring said second pattern to said second dielectric layer.

32. The method of claims 29, 30, or 31, further comprising:

preparing said film stack with an etch stop layer formed on said first dielectric layer prior to said second dielectric layer formed on said etch stop layer; and

transferring said second pattern to said etch stop layer.

33. A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a tunable etch resistant anti-reflective (TERA) coating formed on said first dielectric layer, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said TERA coating;

forming a second dielectric layer on said TERA coating;

forming a second TERA coating on said film stack;

forming a second layer of light-sensitive material on said second TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said second TERA coating;

transferring said second pattern to said second dielectric layer;

transferring said first pattern to said first dielectric layer; and

transferring said first pattern to said metal cap layer.

34. The method of claim 33, further comprising:

forming a hard mask layer on said second dielectric layer; and

forming said second TERA coating on said hard mask layer; and

transferring said second pattern to said hard mask layer.

35. A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a hard mask formed on said first dielectric layer, a tunable etch resistant anti-reflective (TERA) coating formed on said hard mask layer, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said TERA coating;

transferring said first pattern to said hard mask layer;

transferring said first pattern to said first dielectric layer;

transferring said first pattern to said metal cap layer;

removing said TERA coating;

filling said first pattern in said first dielectric layer and said metal cap layer with metal;

forming a second metal cap layer on said film stack;

forming a second dielectric layer on said second metal cap layer;

forming a second hard mask layer on said second dielectric layer;

forming a second TERA coating on said second hard mask layer;

forming a second layer of light-sensitive material on said second TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said second TERA coating;

transferring said second pattern to said second hard mask layer;

transferring said second pattern to said second dielectric layer; and

transferring said second pattern to said second metal cap layer.

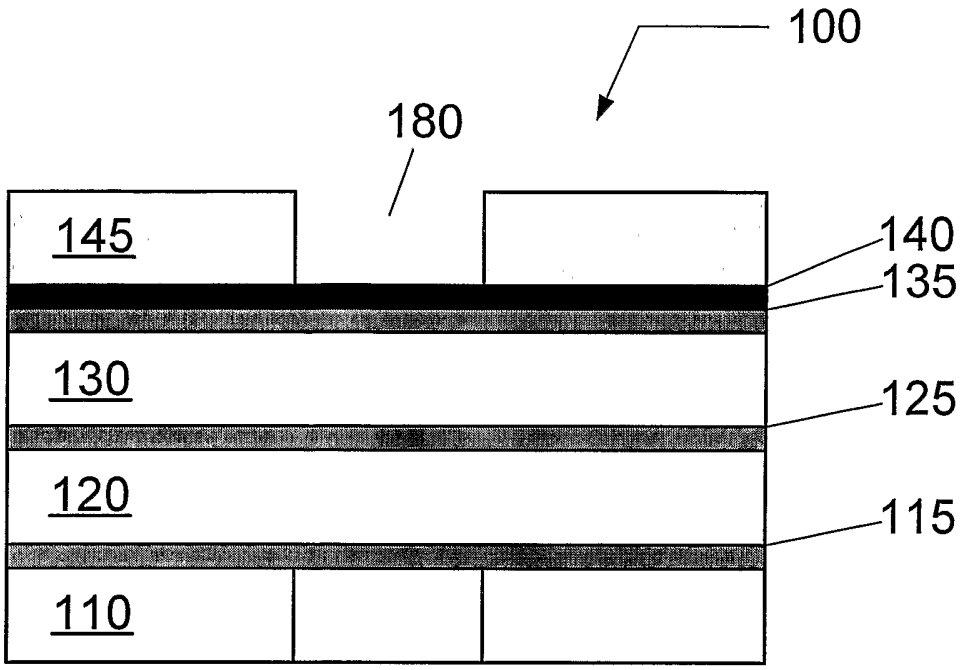
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FIG. 1A

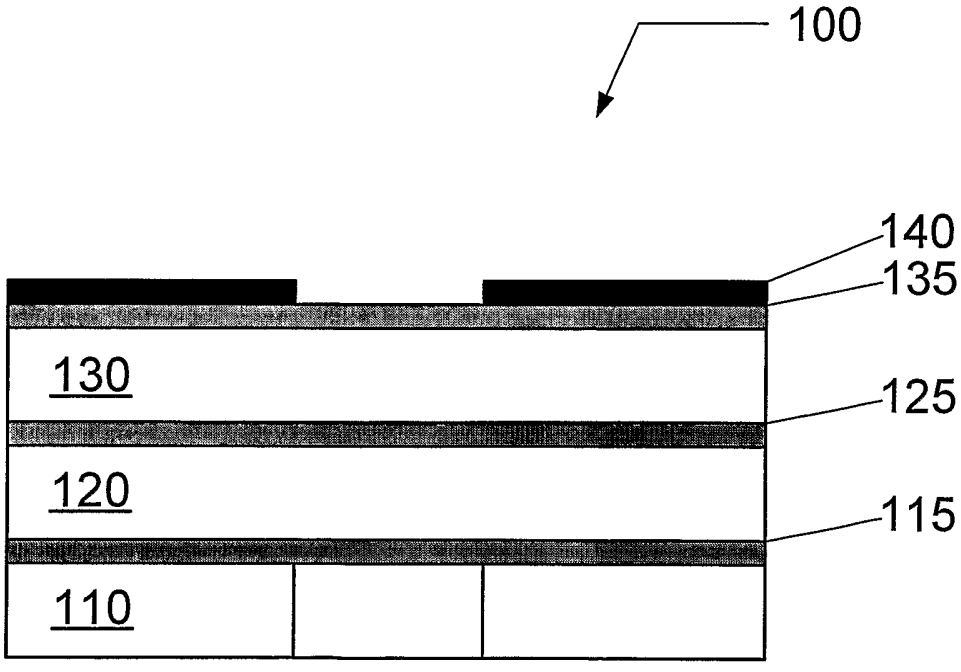
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FIG. 1B

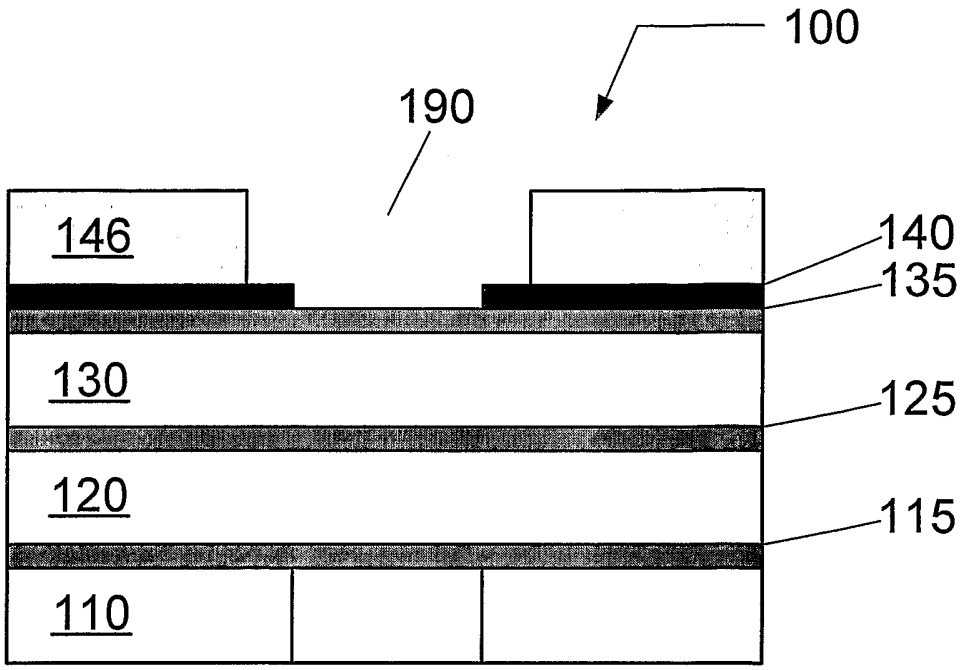
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FIG. 1C

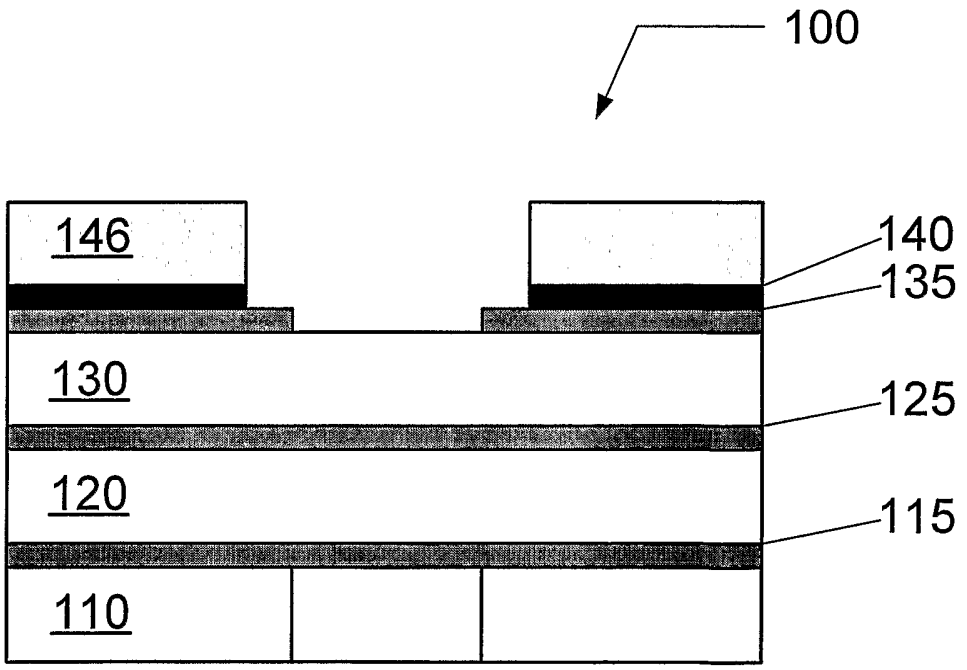
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FIG. 1D

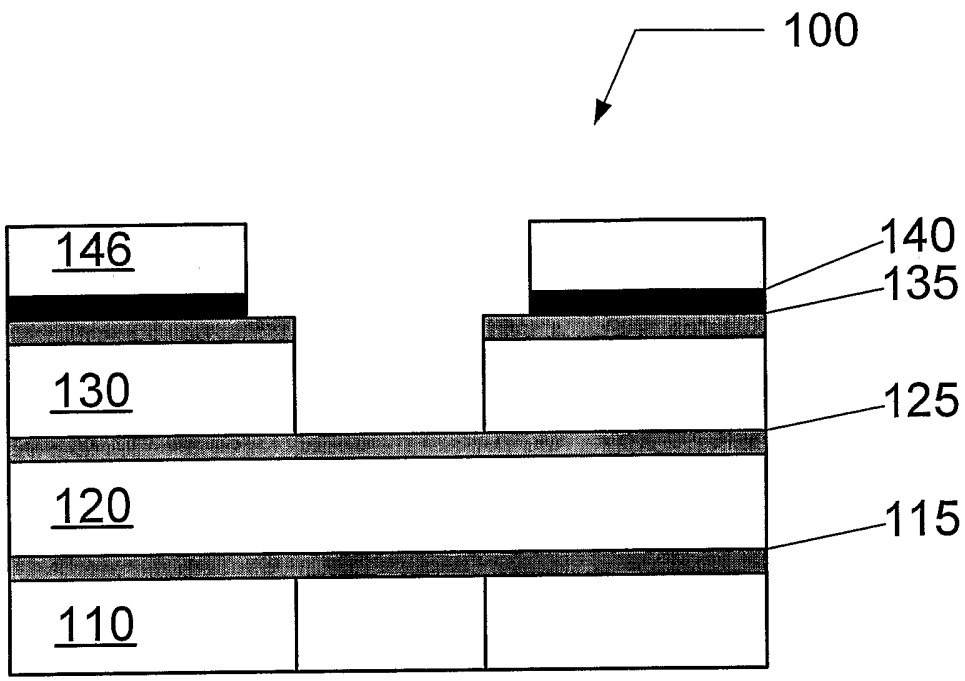
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FIG. 1E

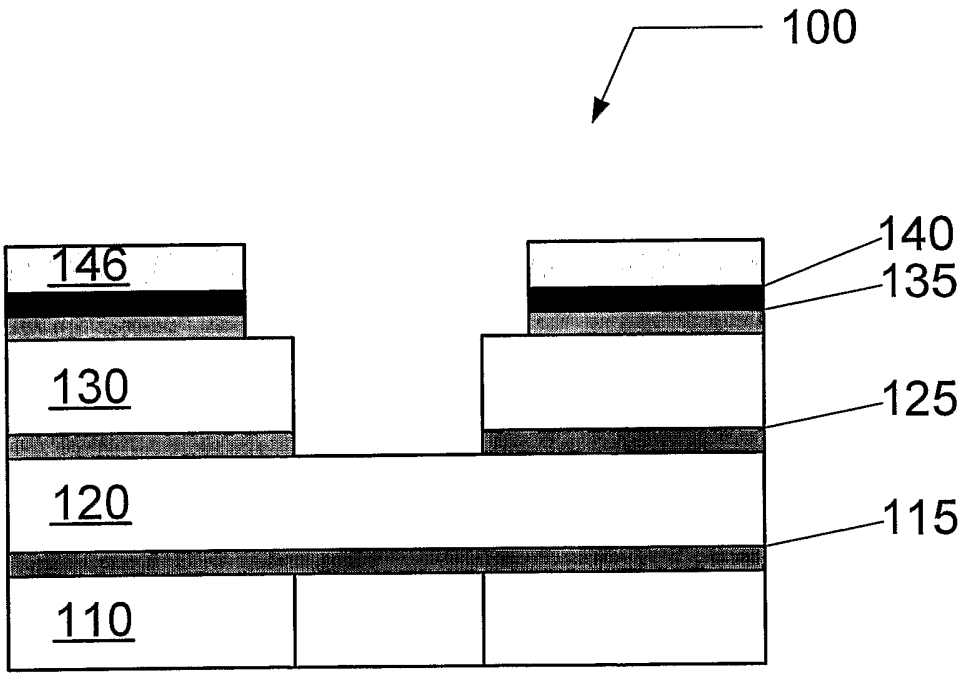
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FIG. 1F

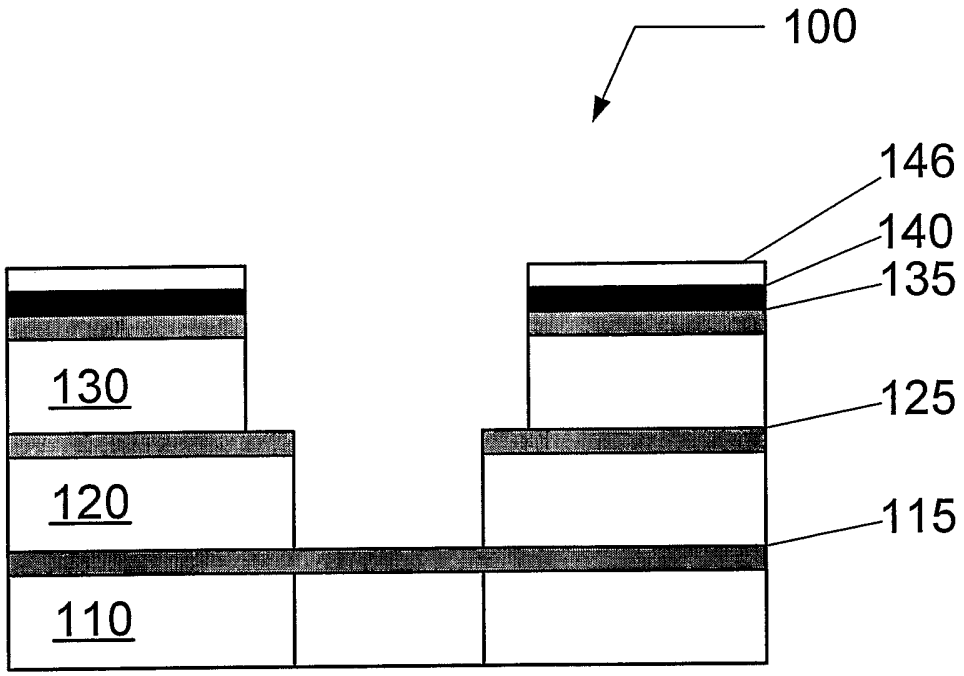
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FIG. 1G

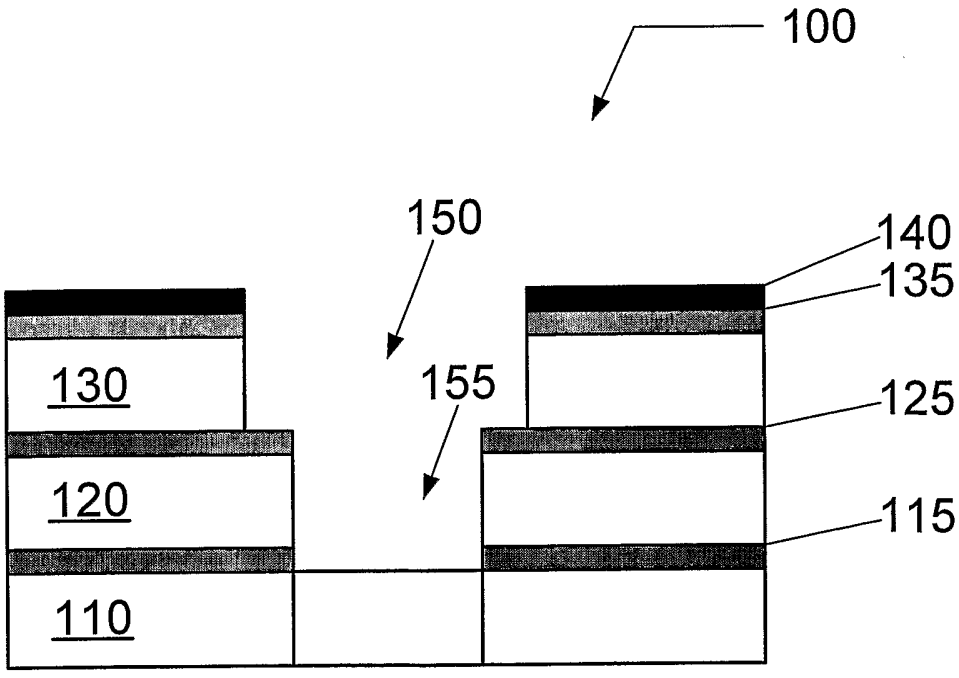
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FIG. 1H

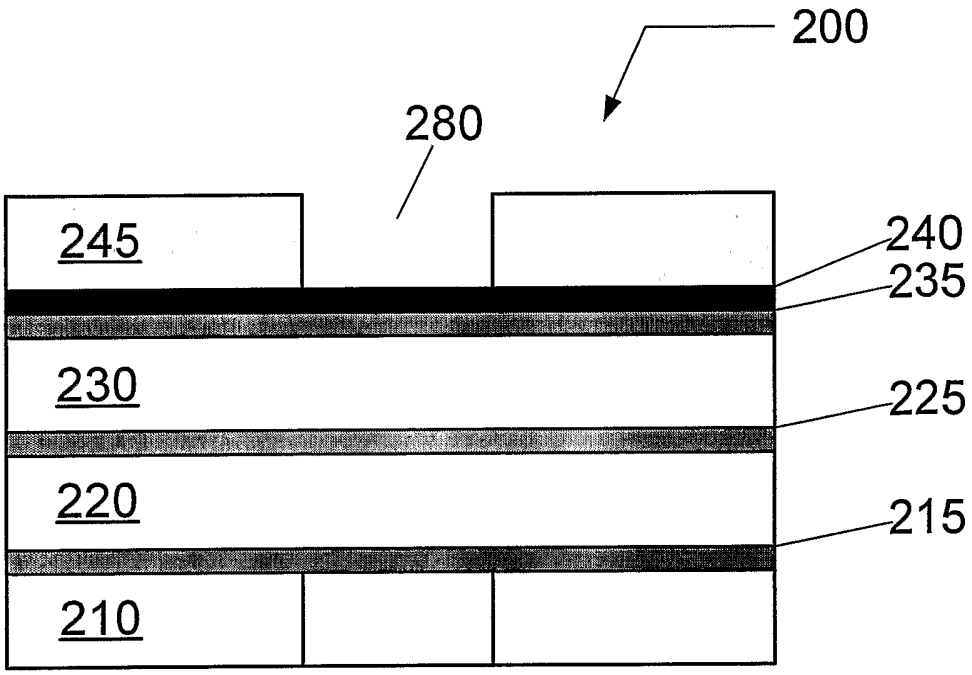
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FIG. 2A

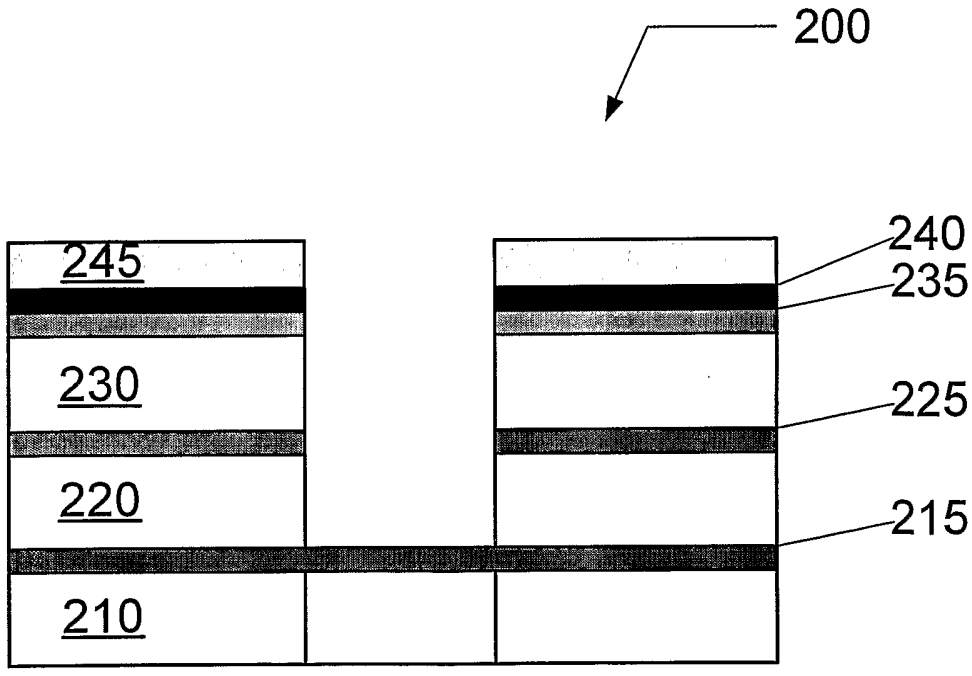
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FIG. 2B

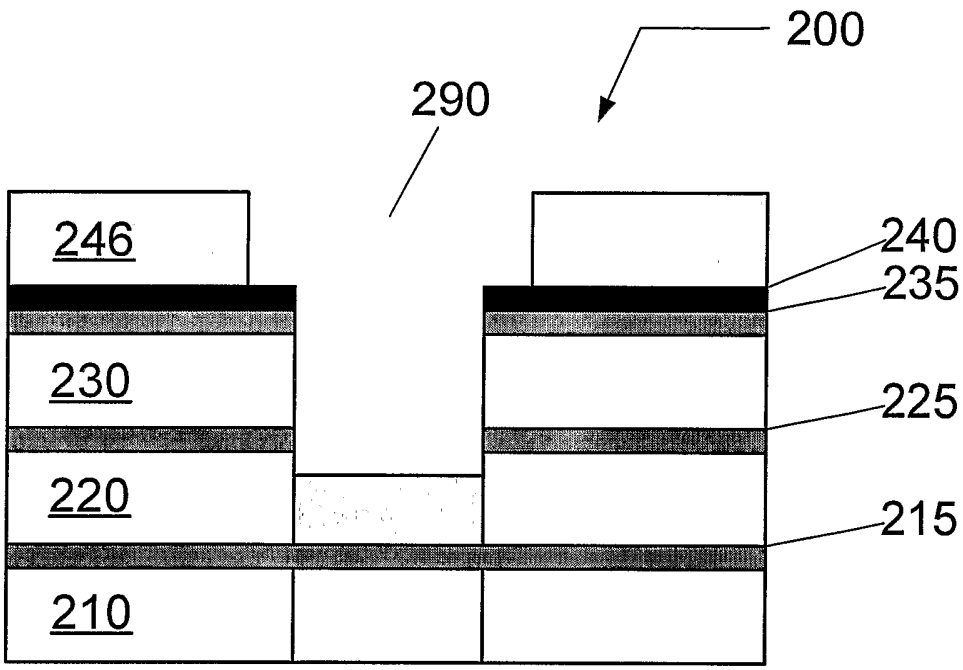
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FIG. 2C

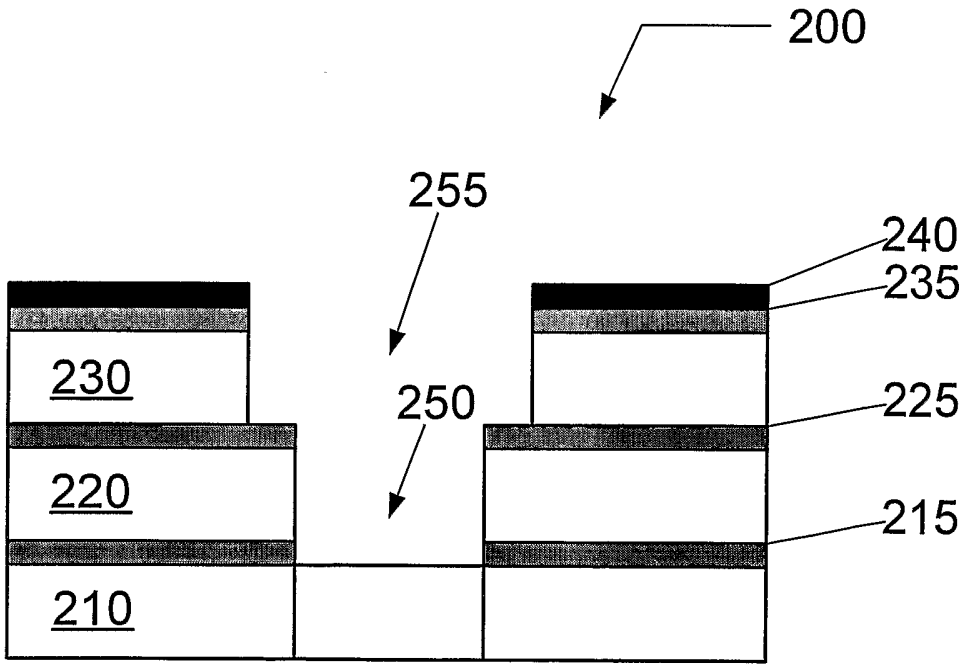
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FIG. 2D

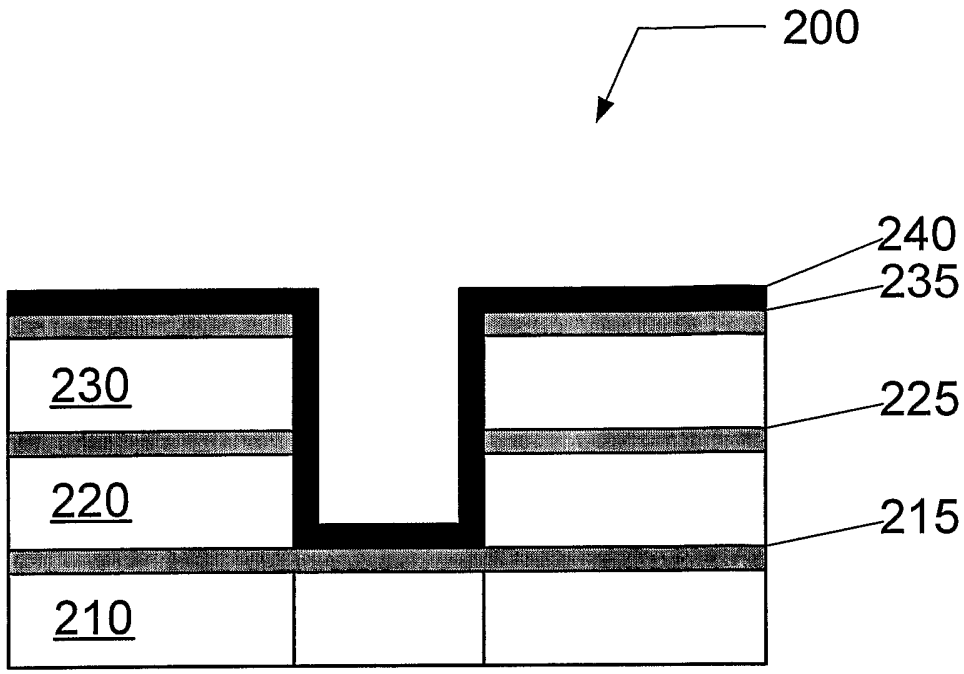

FIG. 2E

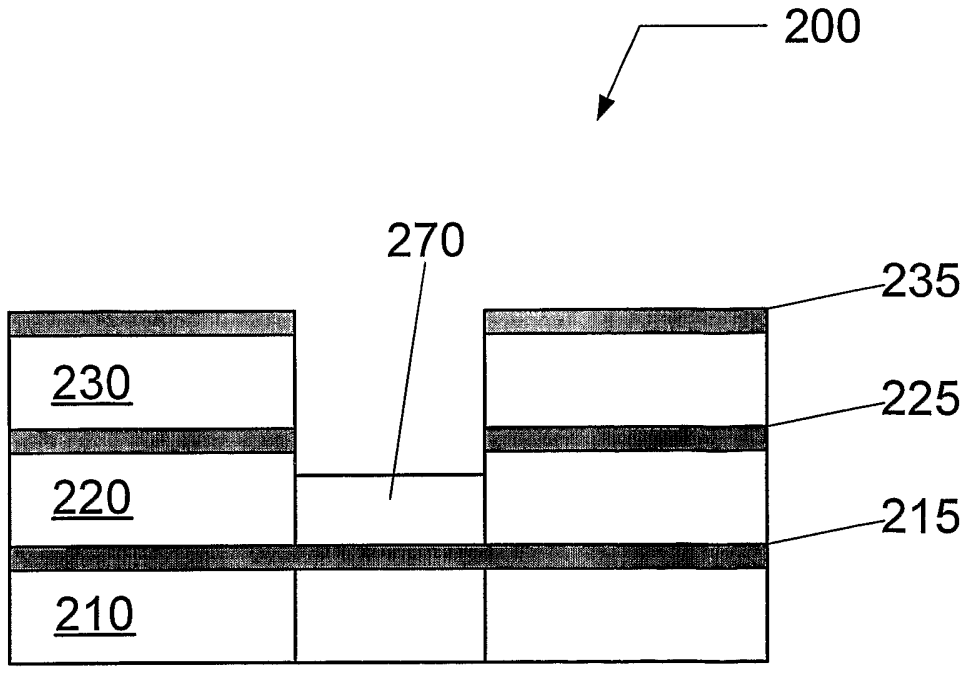

FIG. 2F

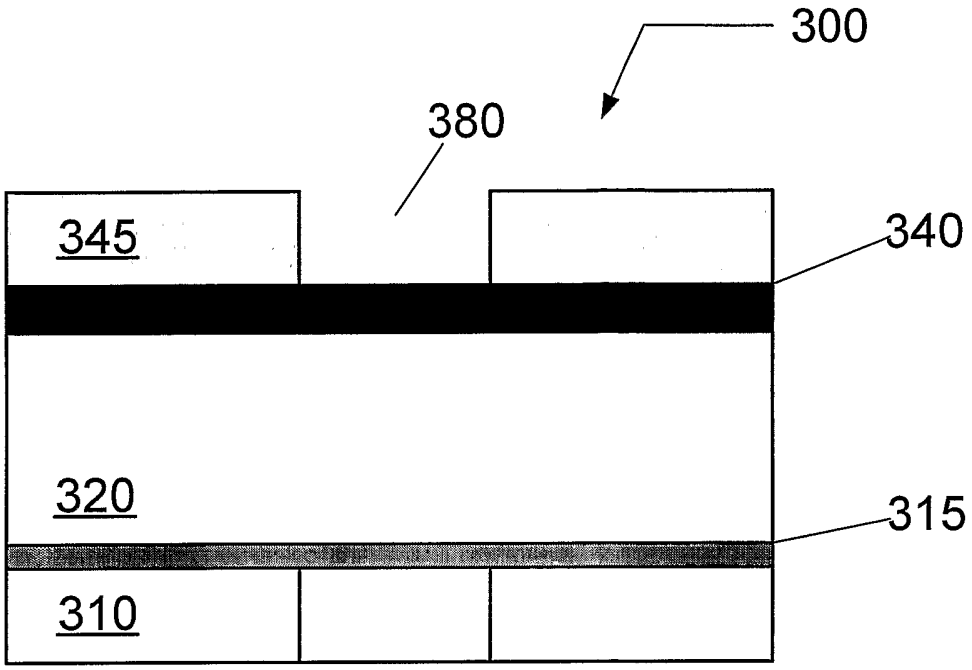

FIG. 3A

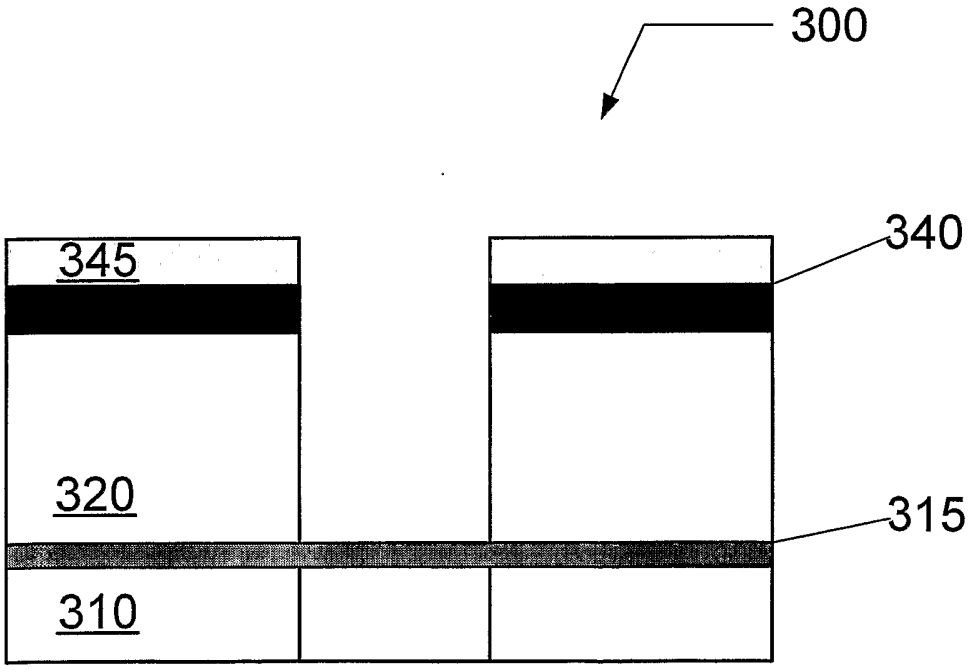

FIG. 3B

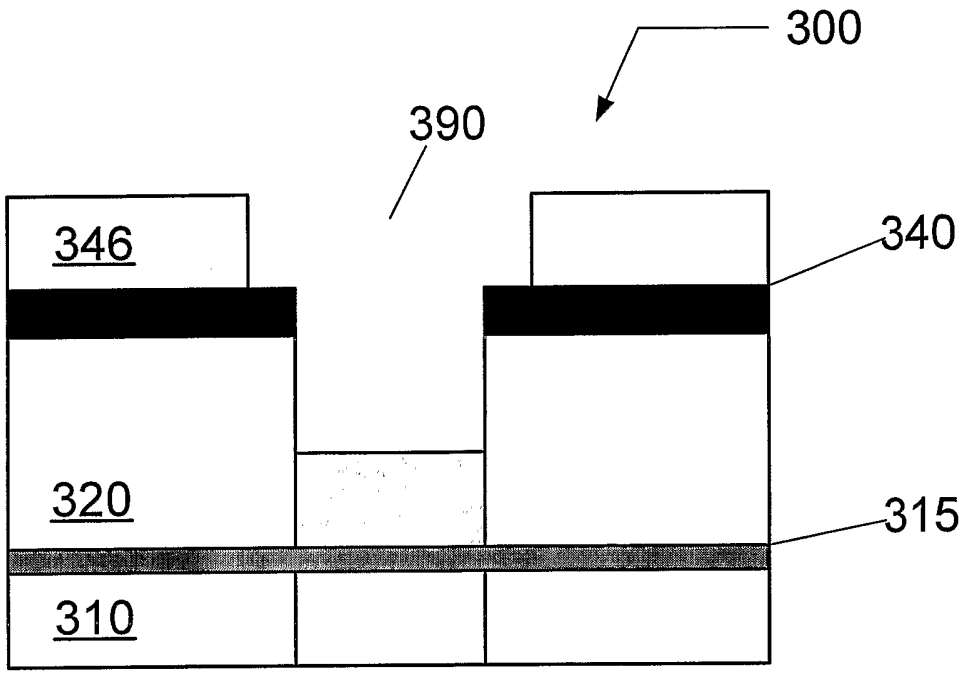

FIG. 3C

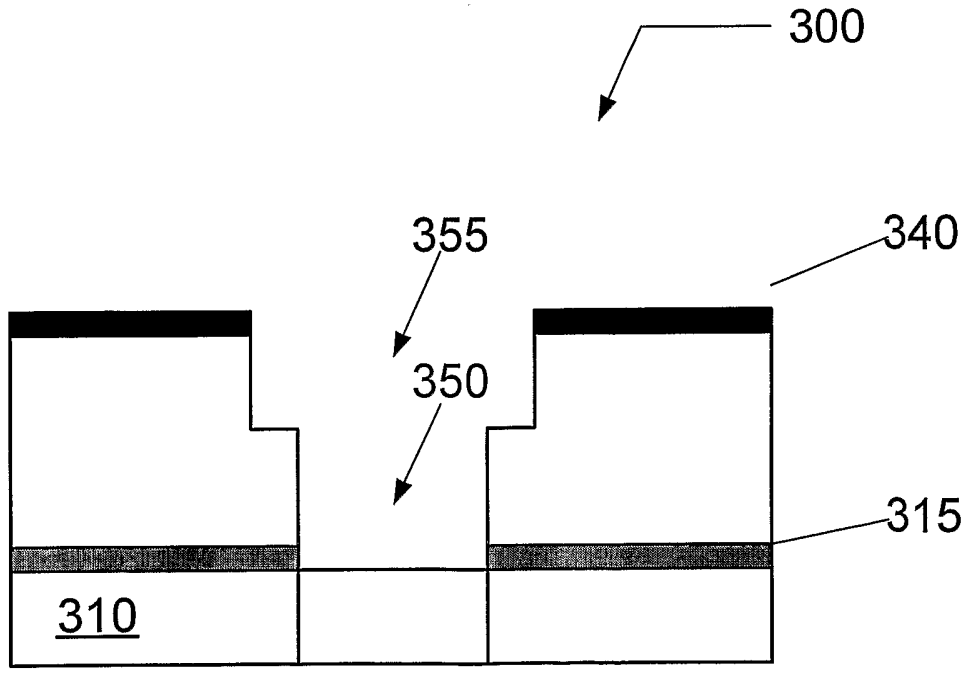

FIG. 3D

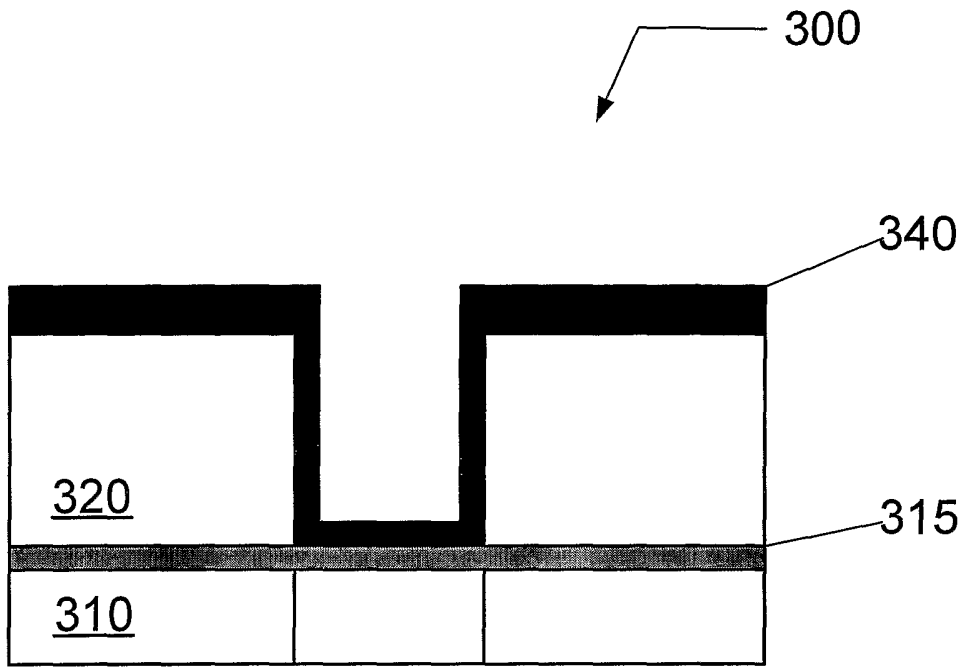

FIG. 3E

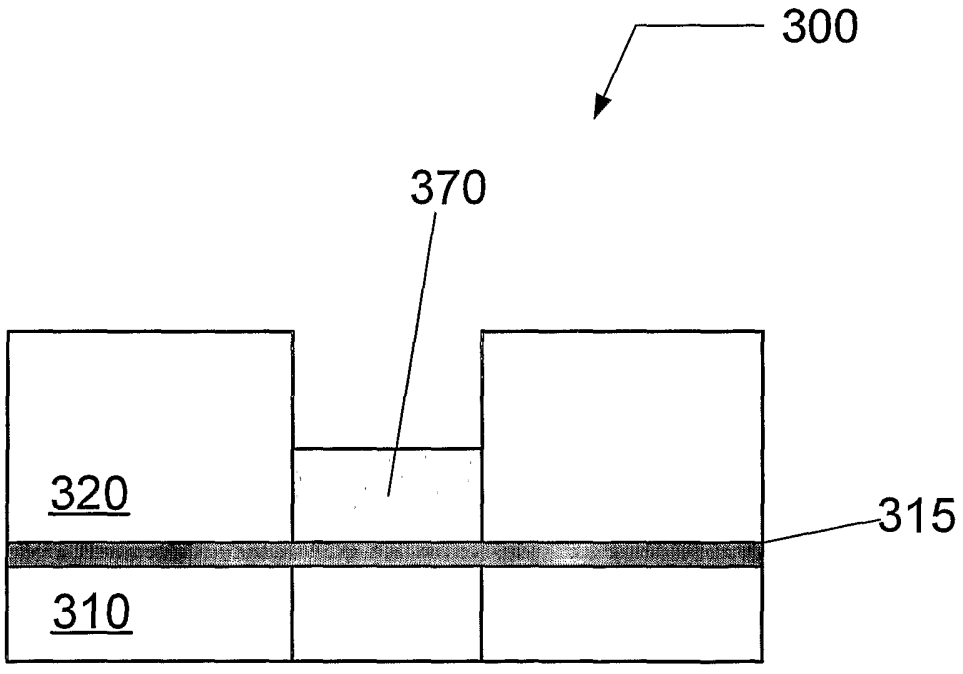

FIG. 3F

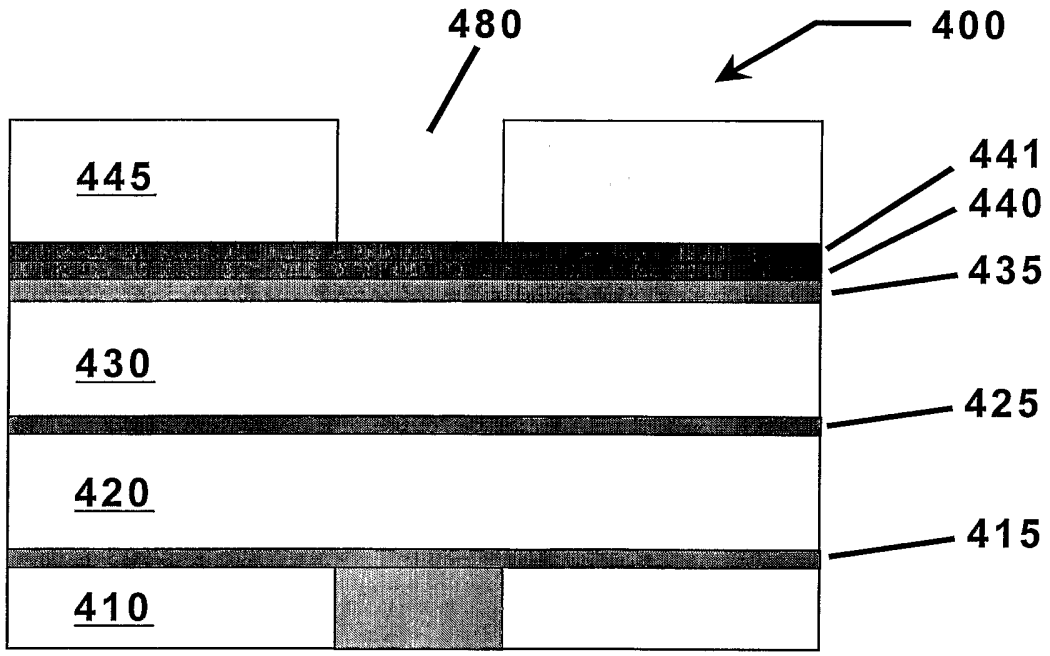
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FIG. 4A

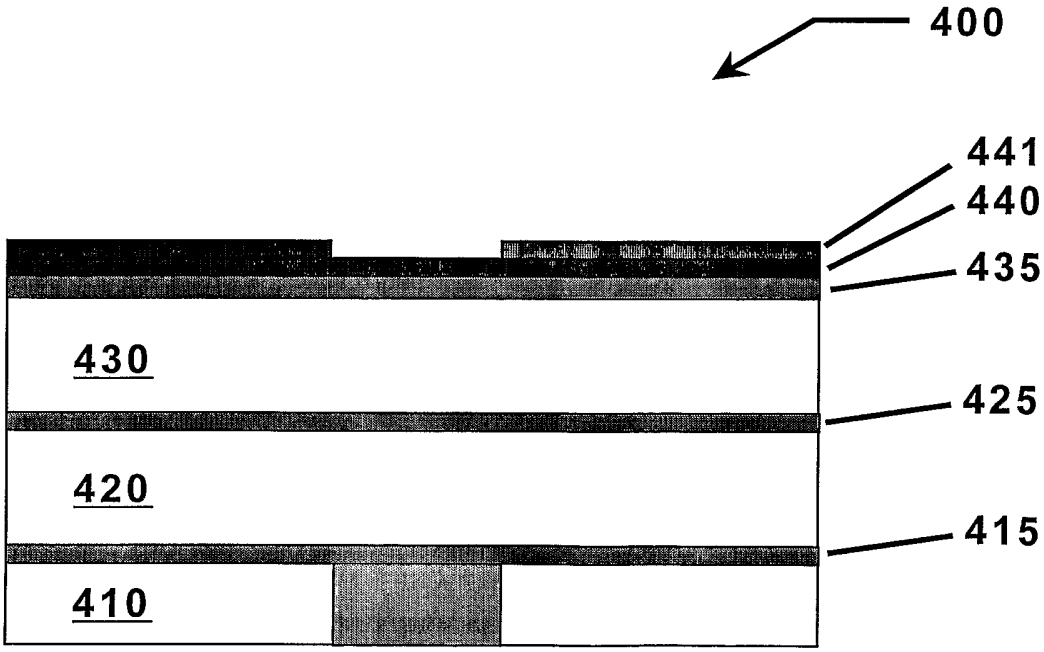
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FIG. 4B

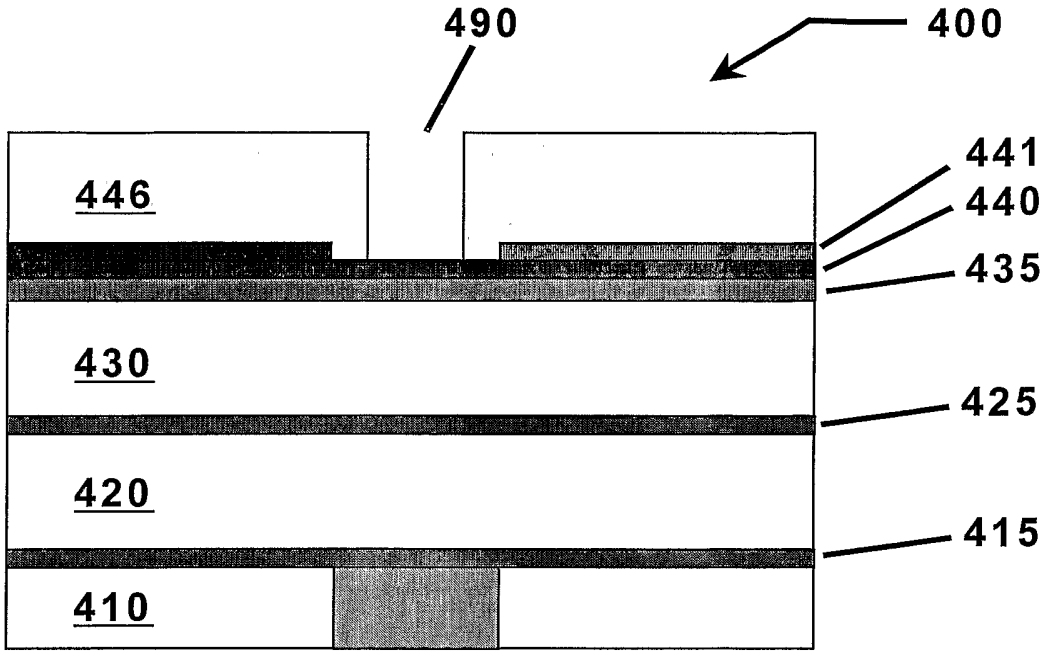
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FIG. 4C

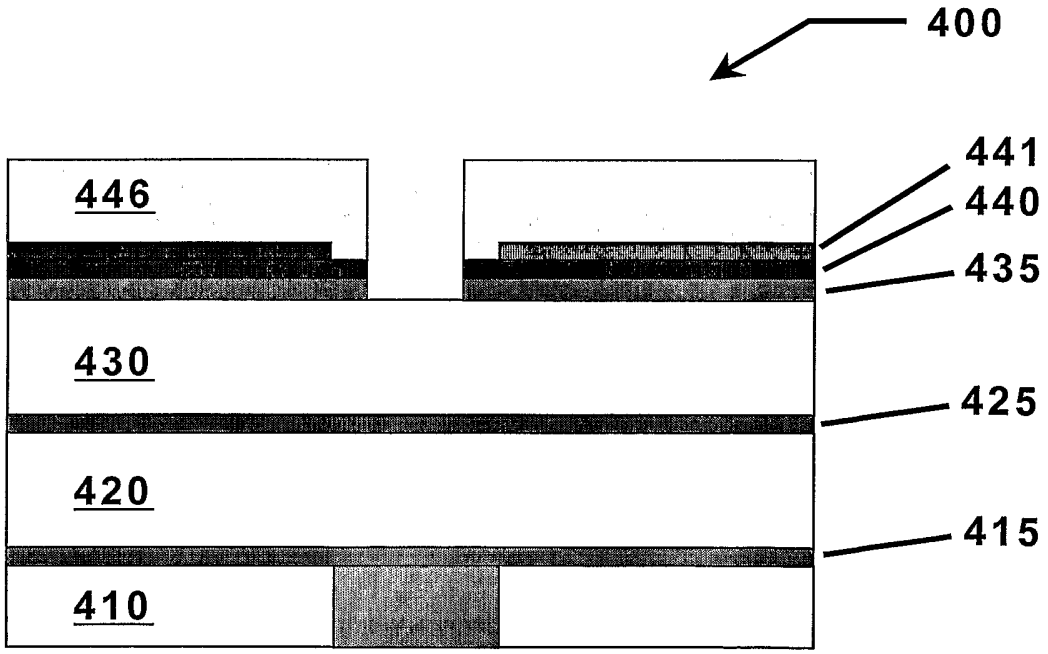
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FIG. 4D

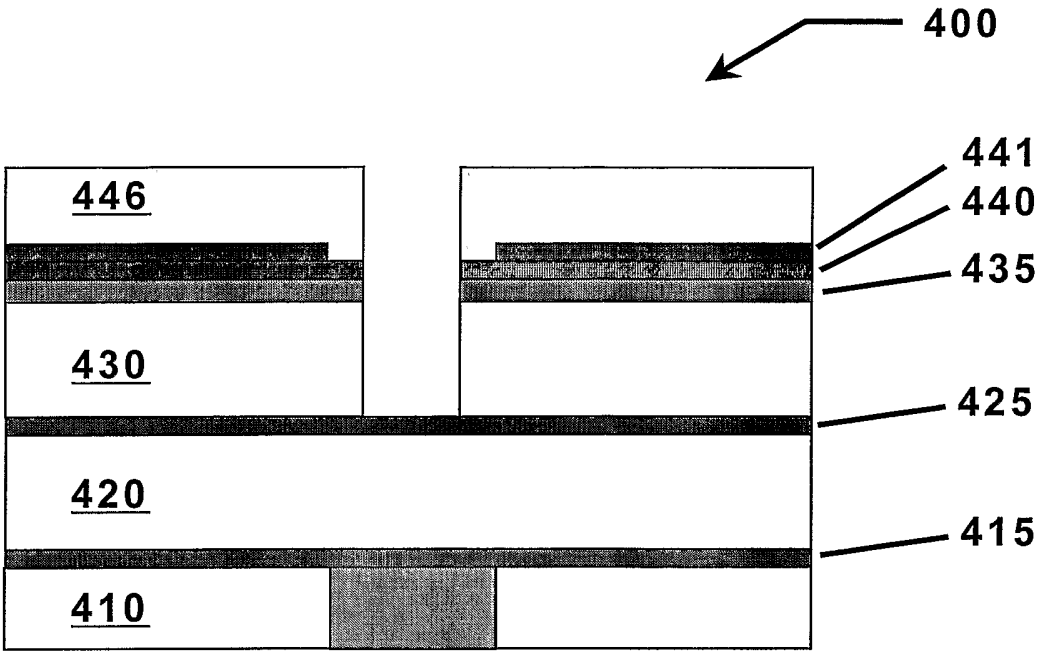
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FIG. 4E

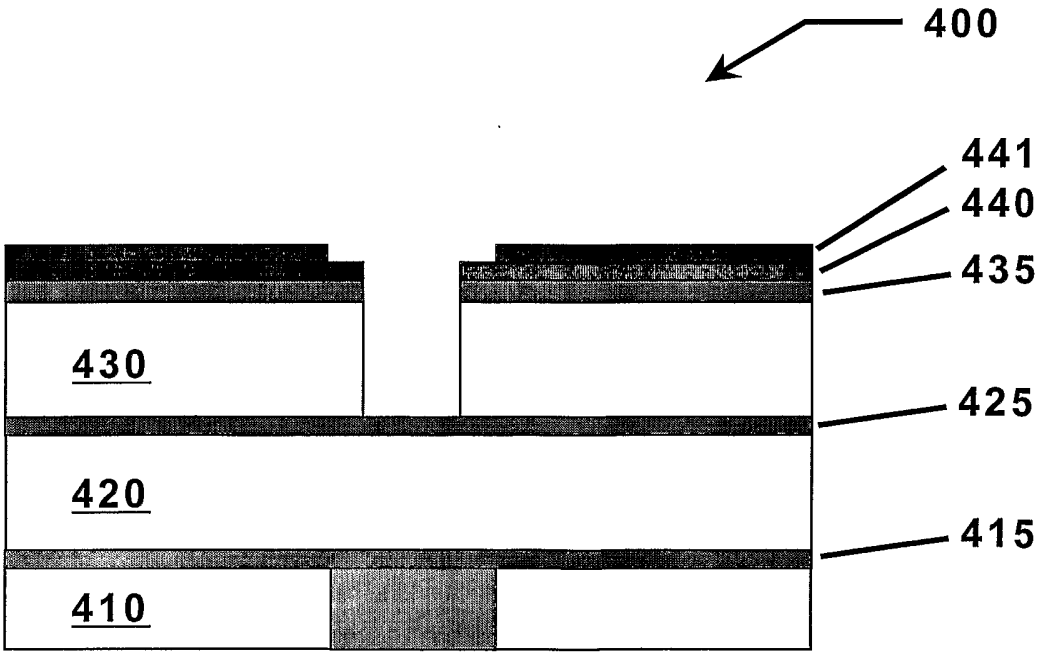
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FIG. 4F

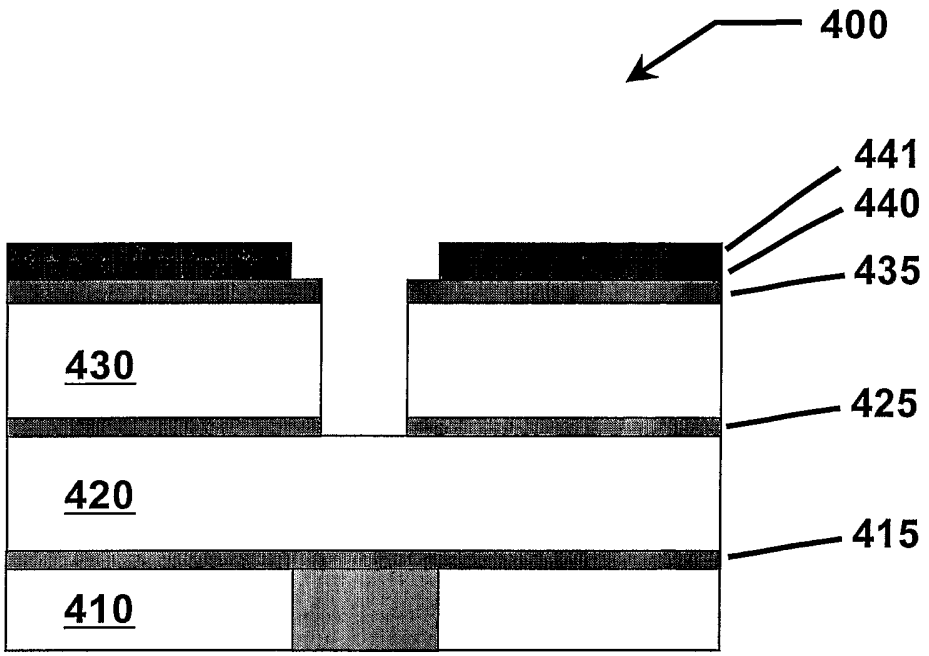
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FIG. 4G

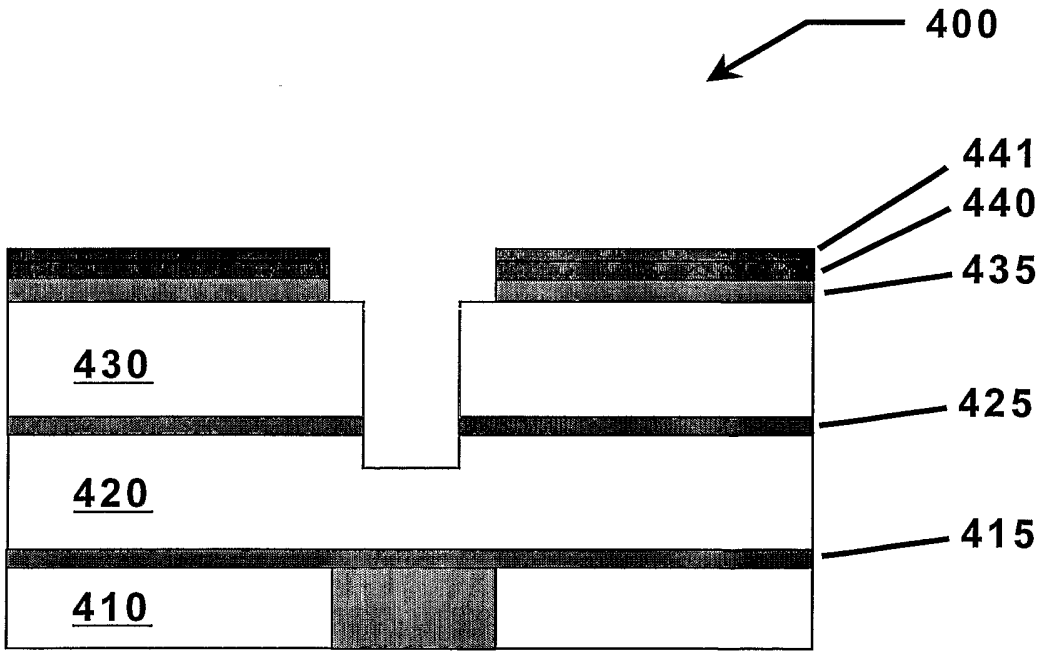
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FIG. 4H

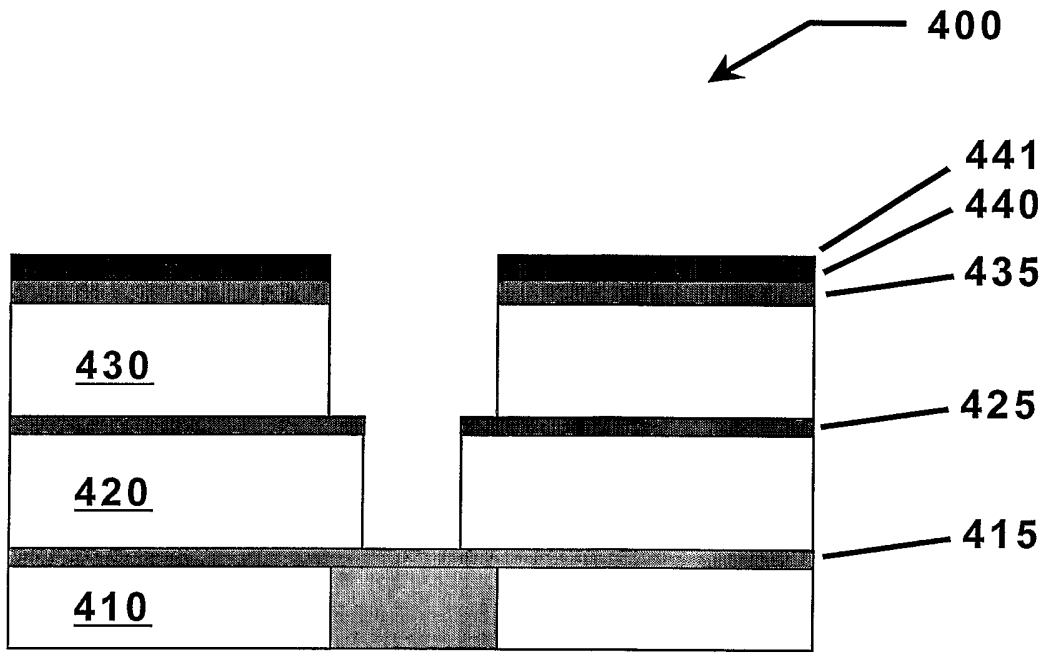
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FIG. 4I

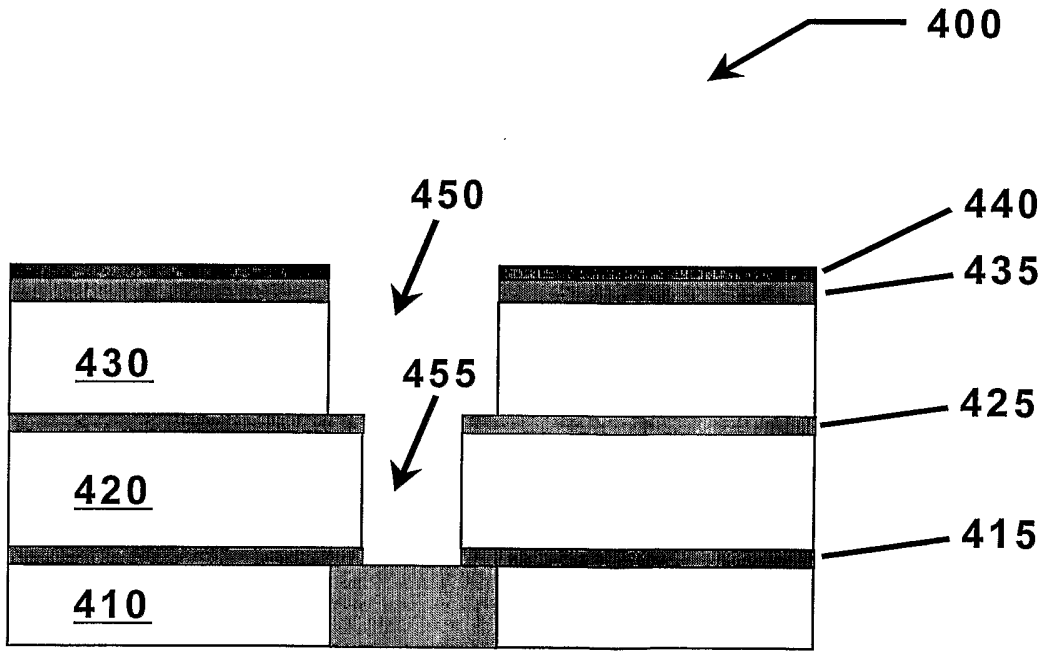
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FIG. 4J

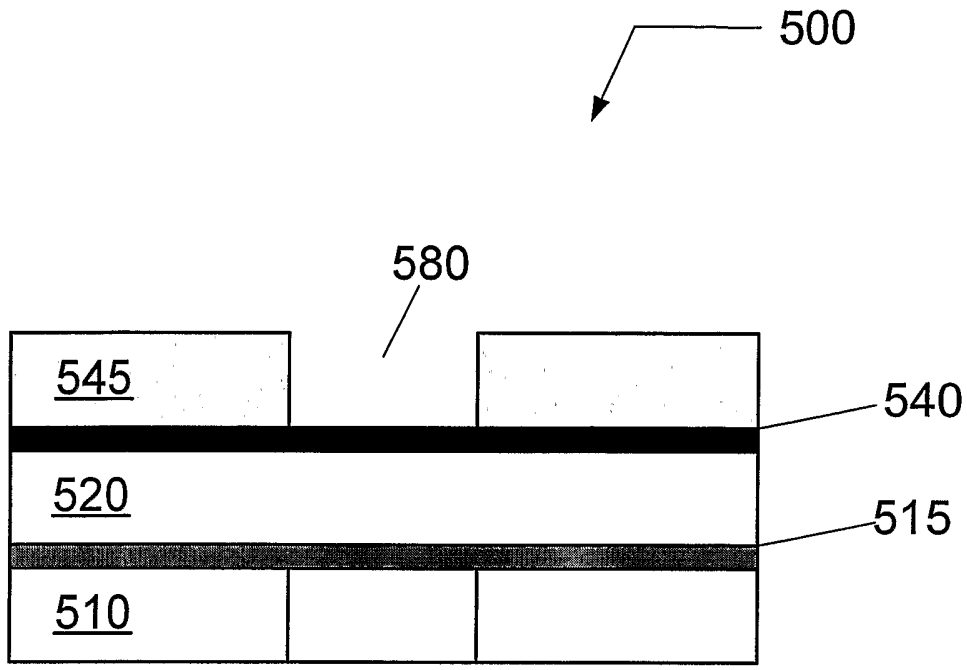

FIG. 5A

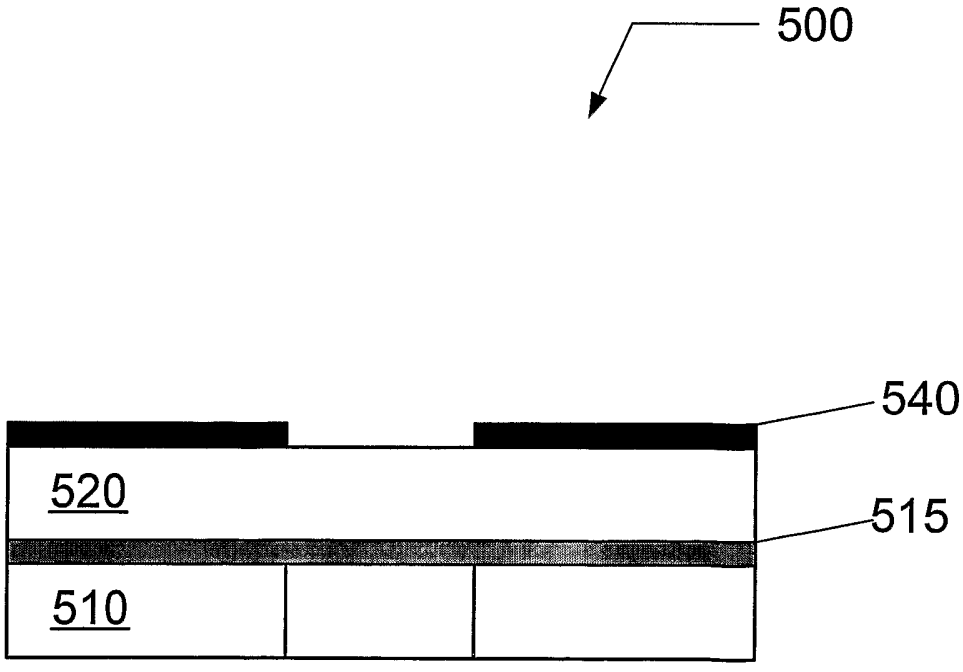

FIG. 5B

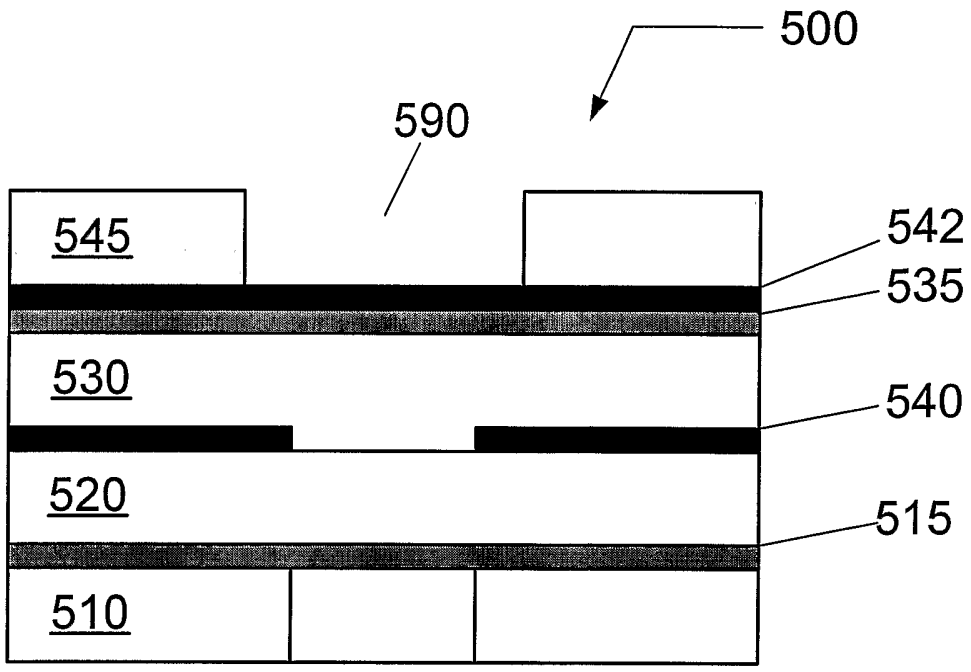
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FIG. 5C

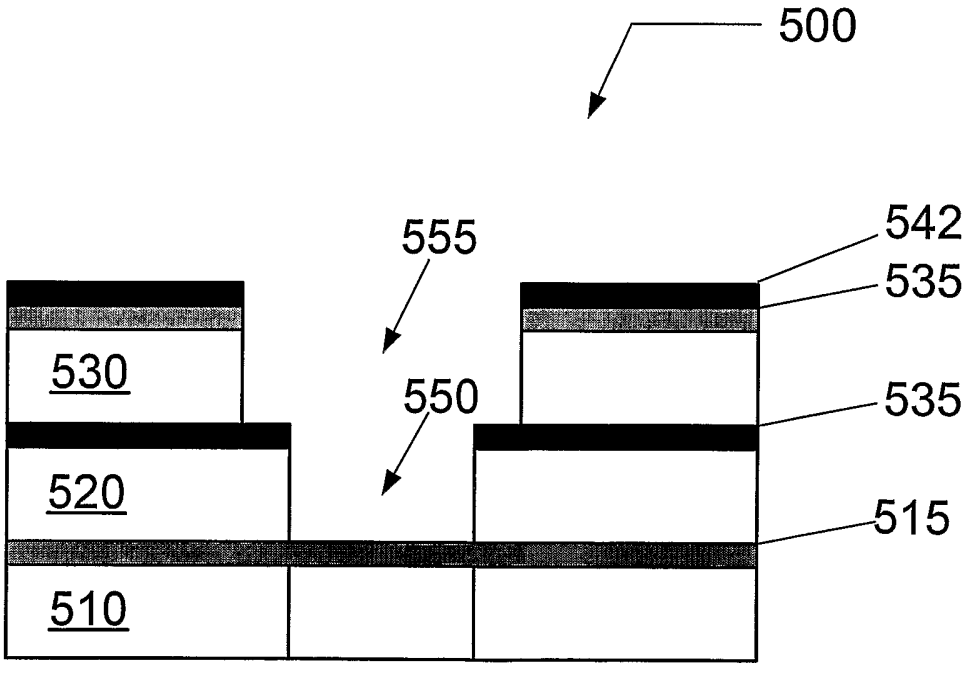
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FIG. 5D

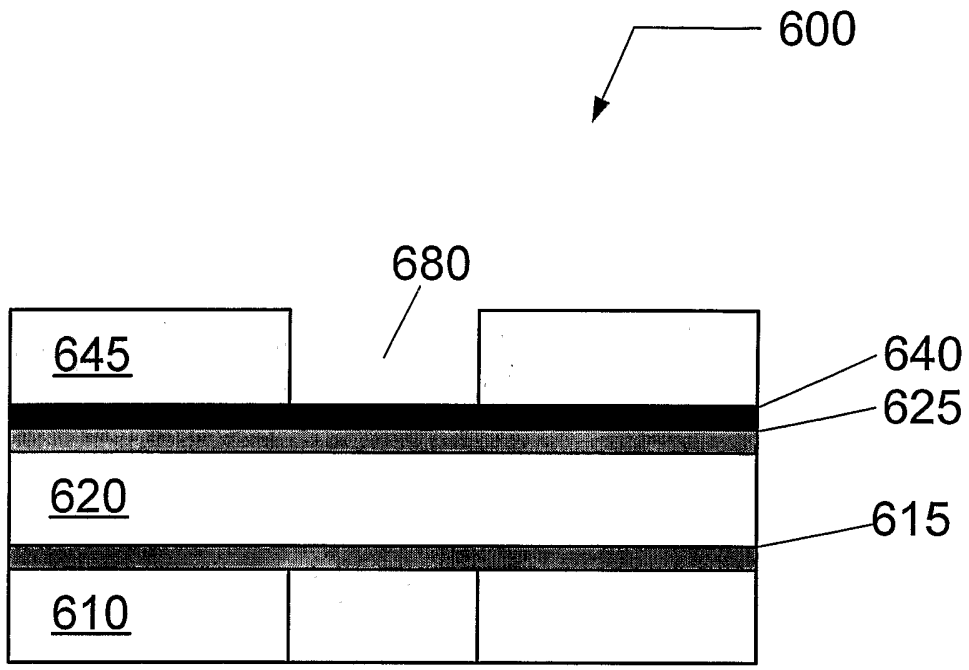

FIG. 6A

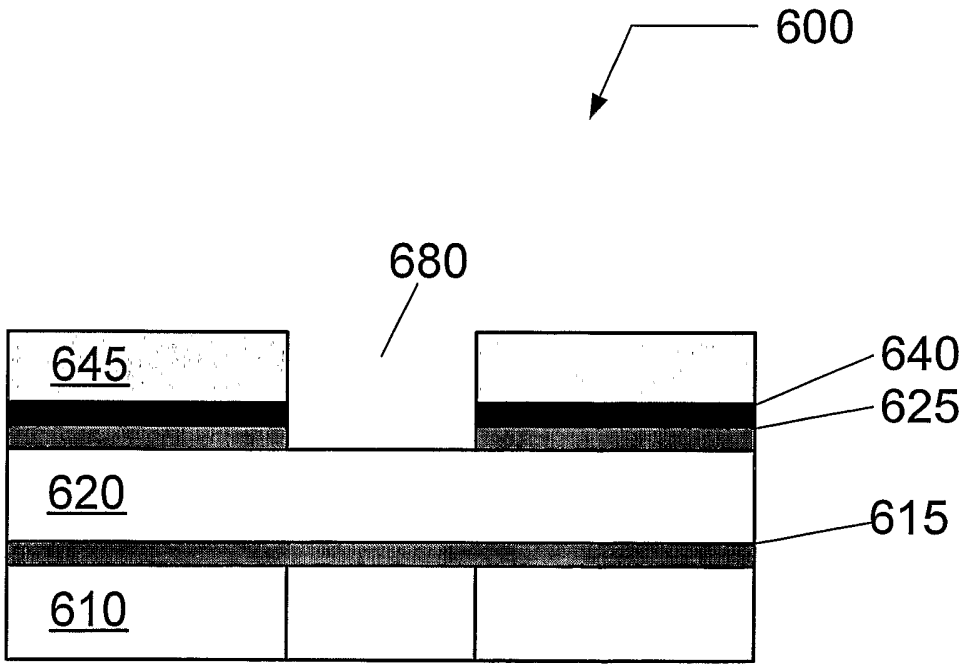

FIG. 6B

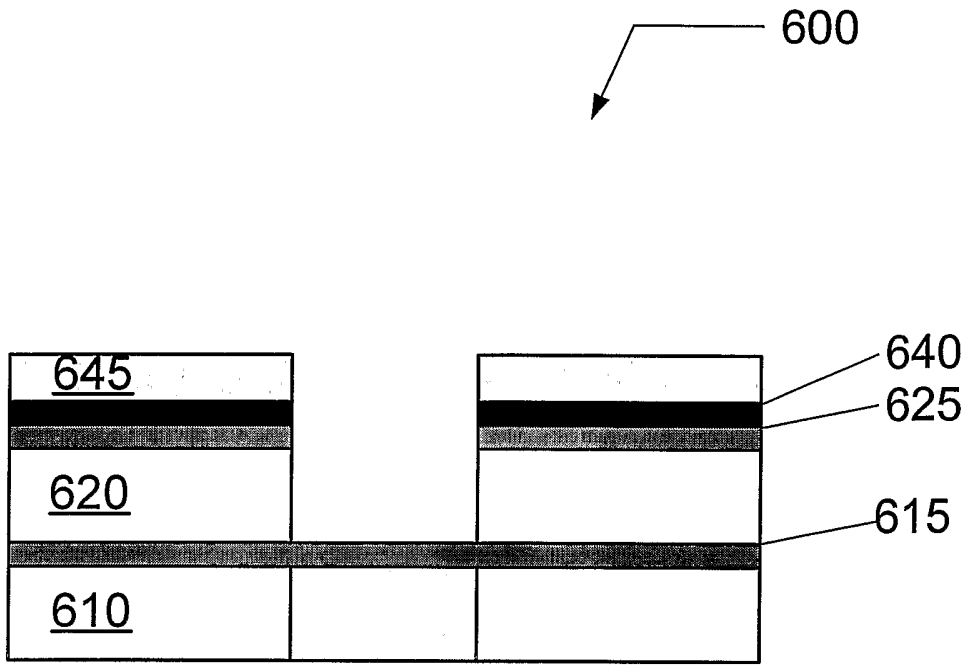

FIG. 6C

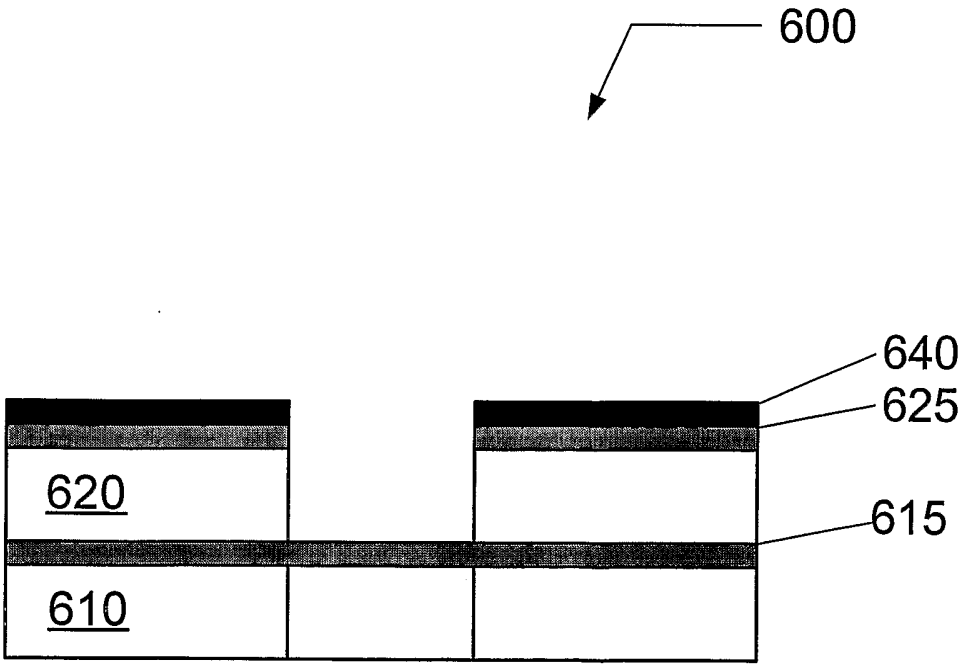

FIG. 6D

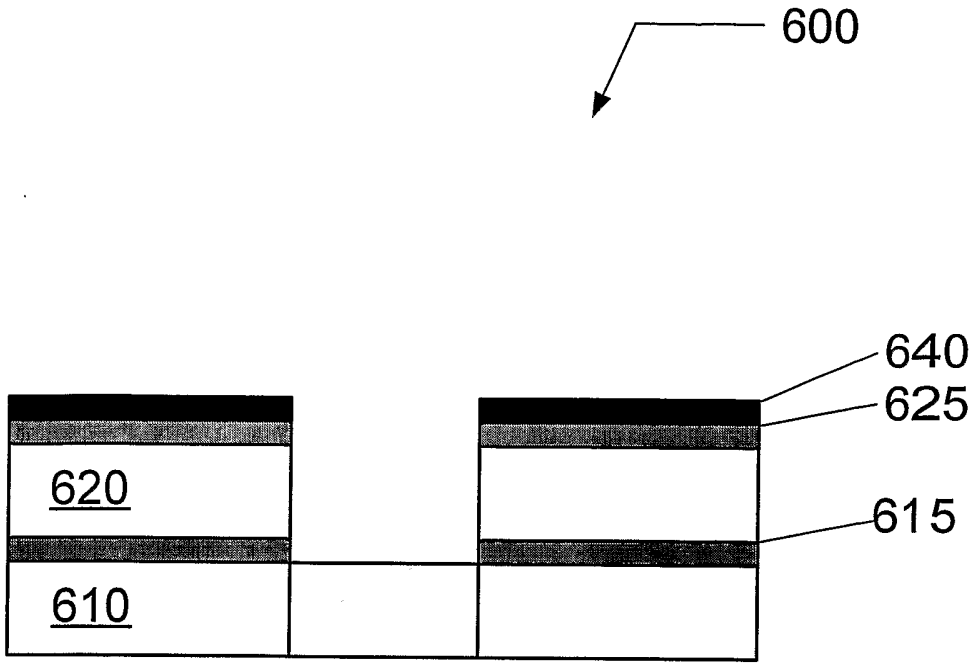
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FIG. 6E

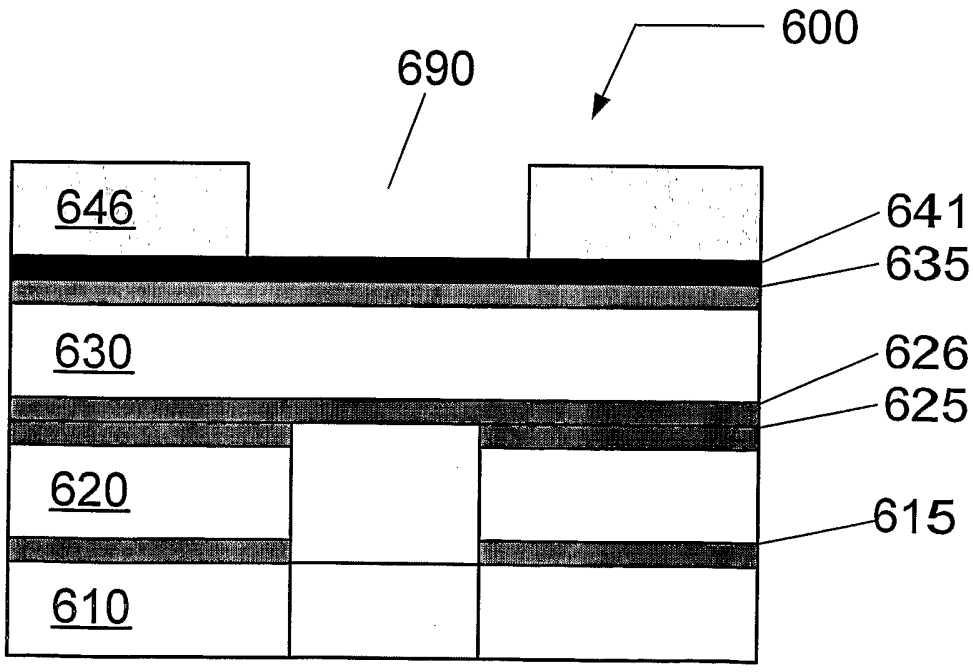
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FIG. 6F

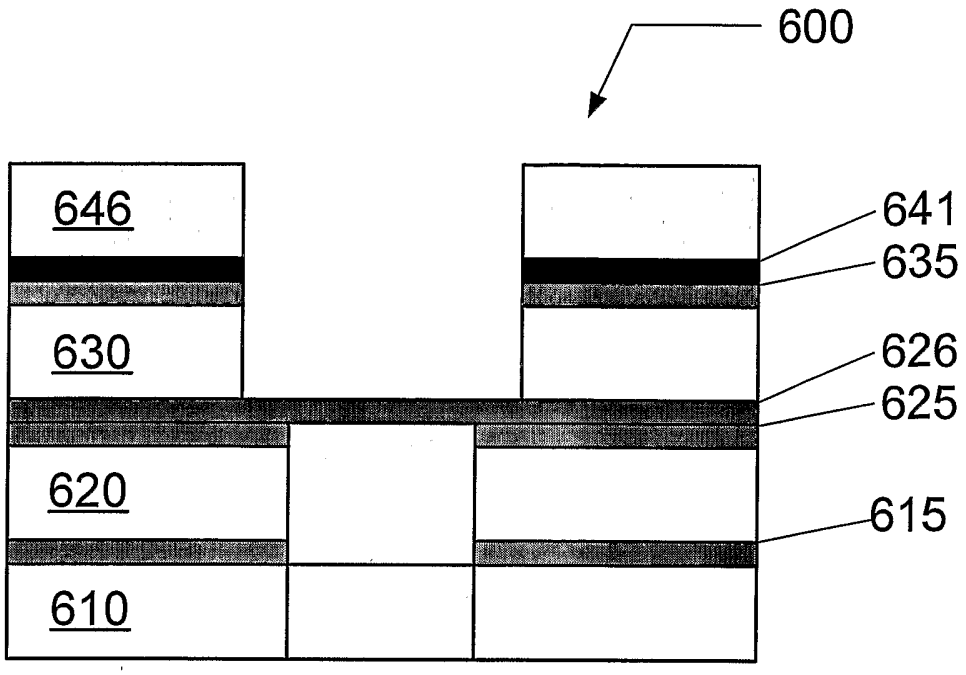
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FIG. 6G

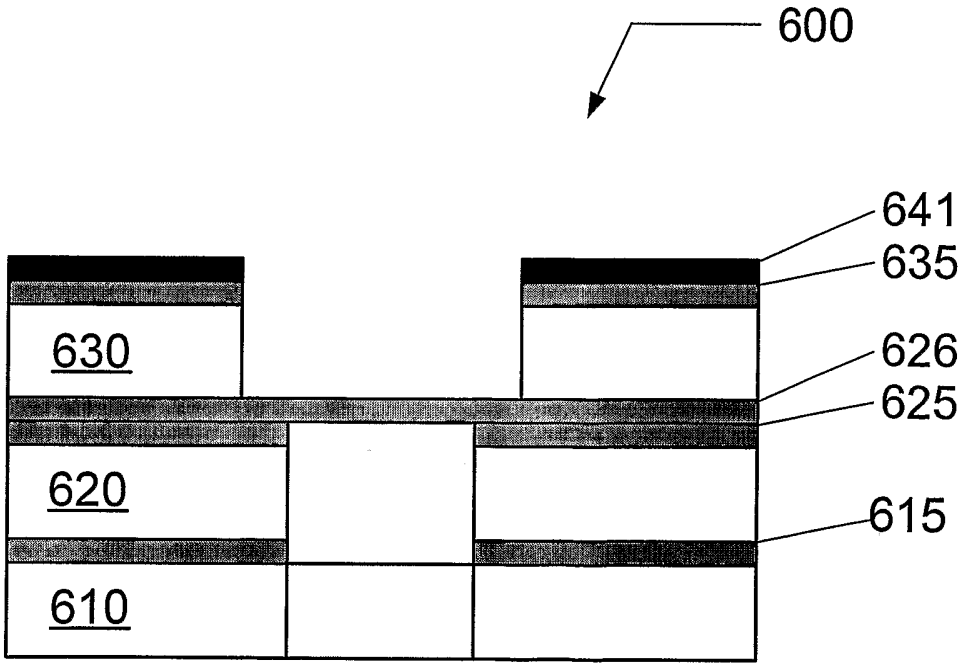
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FIG. 6H

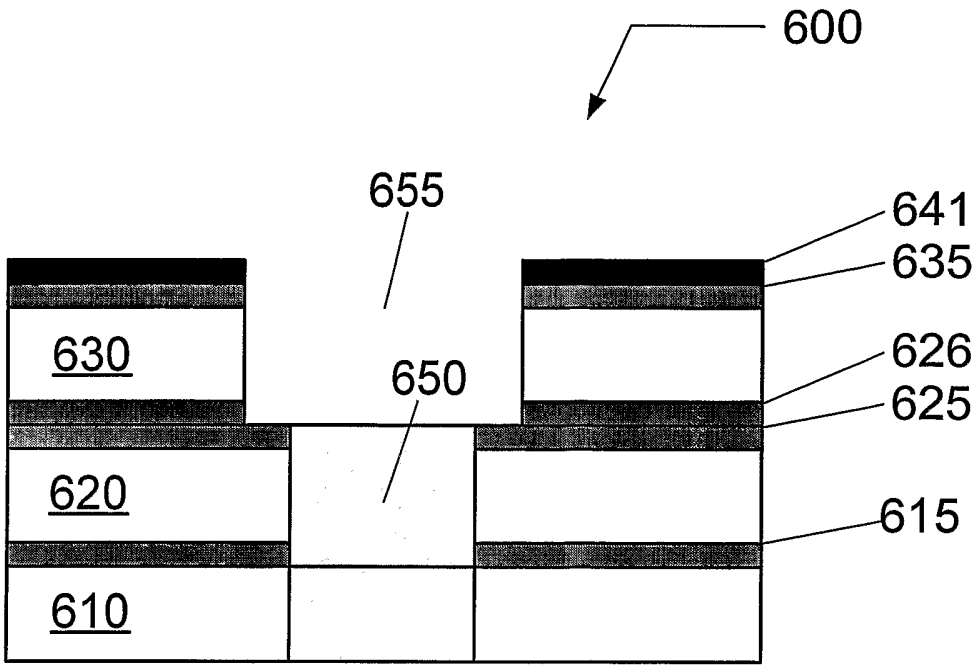

FIG. 6I

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US04/30915

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 21/4763
US CL : 438/638

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 438/638

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,316,167 B1 (ANGELOPOULOS ET AL.) 13 NOVEMBER 2001, SEE COLUMN 4, LINES 33-67; COLUMN 5, LINES 1-57; COLUMN 7, LINES 29-67; COLUMN 8, LINES 1-67; COLUMN 10, LINES 1-64 AND COLUMN 12, LINES 4-67. FIGS. 10-11 .	1-15 --- 16-35
Y	US 6,620,727 B2 (BRENNAN) 16 SEPTEMBER 2003, SEE COLUMN 2, LINES 17-67 AND COLUMN 3, LINES 1-54. FIGS. 2A-2F.	16-35

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 January 2005 (14.01.2005)	31 MAR 2005
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer Theresa Doan Telephone No. (571) 272-1704

Form PCT/ISA/210 (second sheet) (July 1998)