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(54) METHOD OF FORMING SEMICONDUCTOR STRUCTURES

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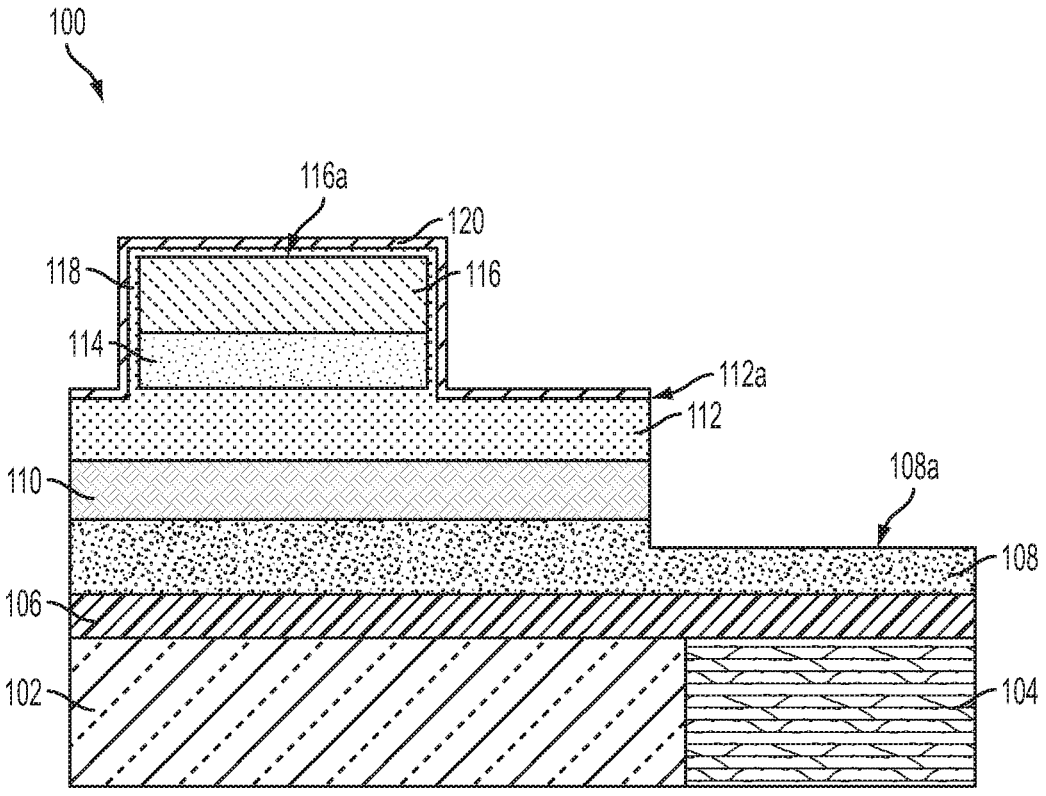
(52) **U.S. Cl.**

CPC ***H01L 28/60*** (2013.01); ***H01L 23/5223*** (2013.01); ***H01L 28/65*** (2013.01)

(57) **ABSTRACT**

A method of making a metal insulator metal (MIM) capacitor includes forming a copper bulk layer in a base layer, wherein the copper bulk layer includes a hillock extending from a top surface thereof. The method further includes depositing an etch stop layer over the base layer and the copper bulk layer. The method further includes depositing an oxide-based dielectric layer over the etch stop layer. The method further includes forming a capacitor over the oxide-based dielectric layer. The method further includes forming a contact extending through the oxide-based dielectric layer and the etch stop layer to contact the copper bulk layer, wherein the forming of the contact removes the hillock.



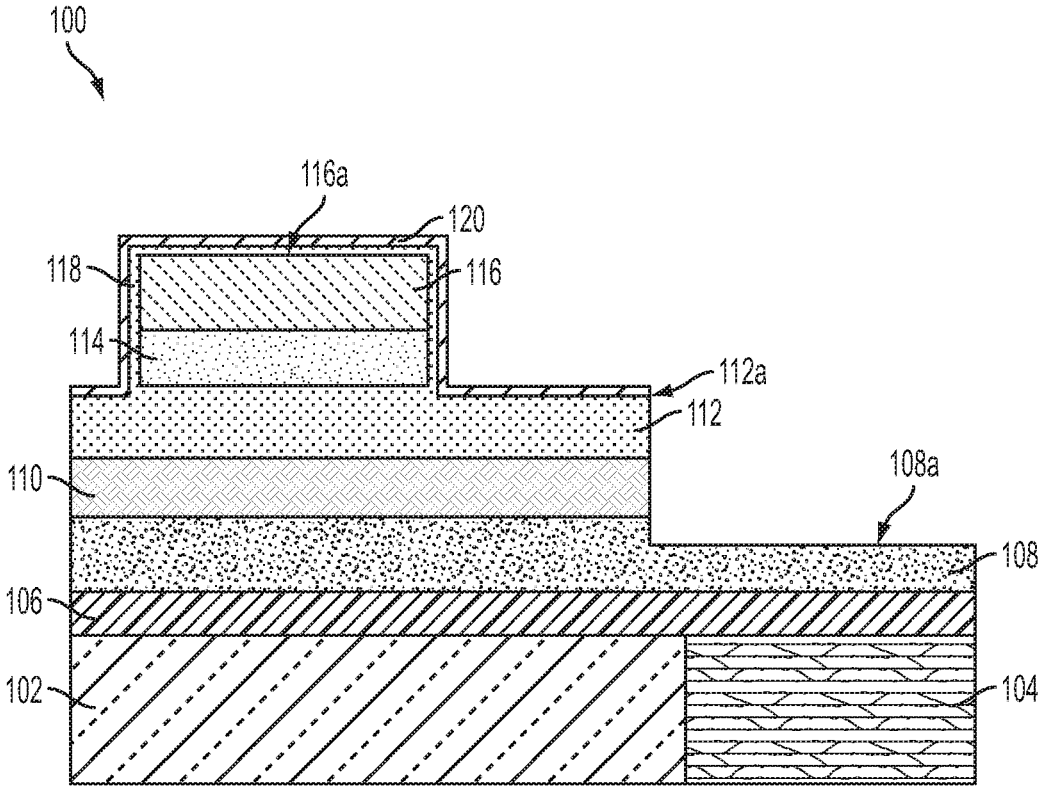


FIG. 1

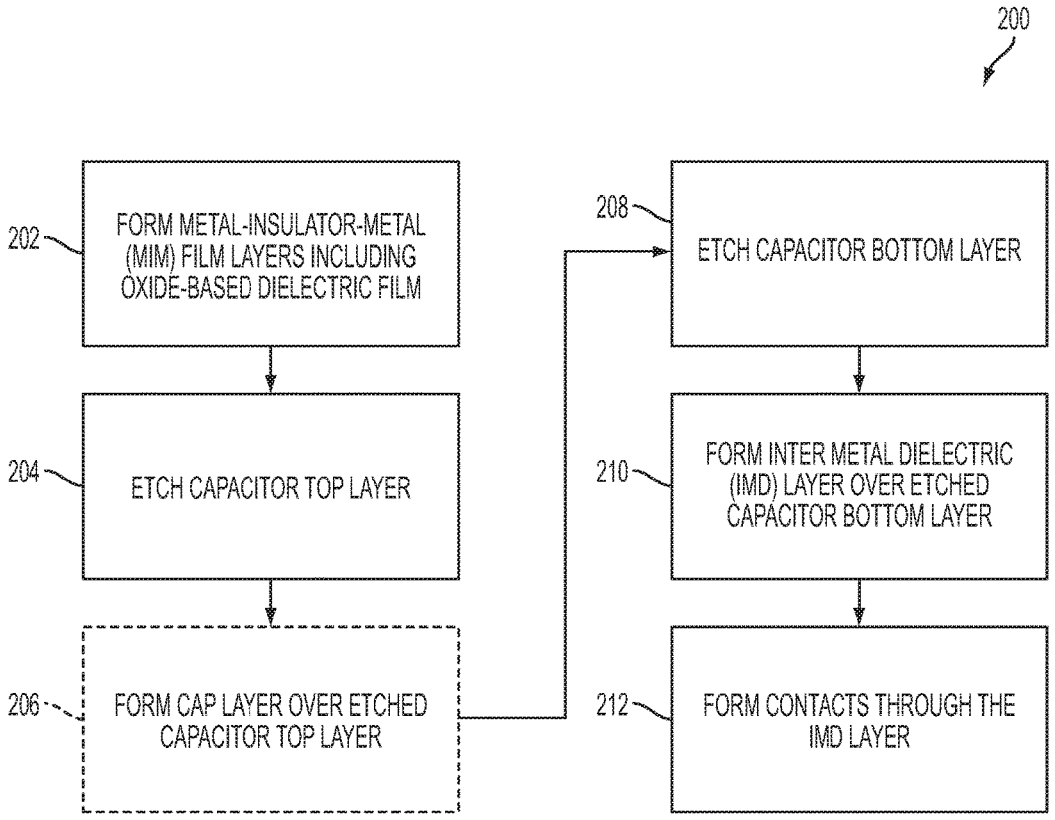

200
202
FORM METAL-INSULATOR-METAL (MIM) FILM LAYERS INCLUDING OXIDE-BASED DIELECTRIC FILM
204
ETCH CAPACITOR TOP LAYER
206
FORM CAP LAYER OVER ETCHED CAPACITOR TOP LAYER
208
ETCH CAPACITOR BOTTOM LAYER
210
FORM INTER METAL DIELECTRIC (IMD) LAYER OVER ETCHED CAPACITOR BOTTOM LAYER
212
FORM CONTACTS THROUGH THE IMD LAYER

FIG. 2

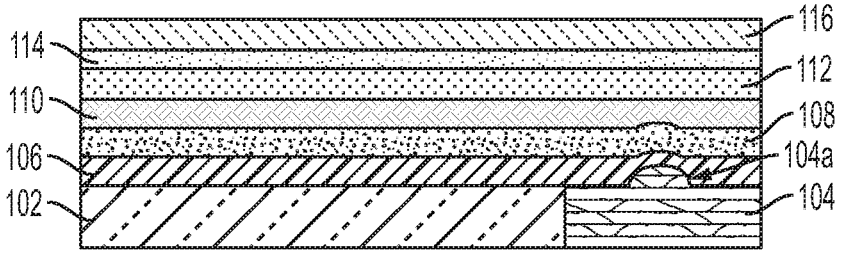

116
114
112
110
108
106
104a
102
104

FIG. 3A

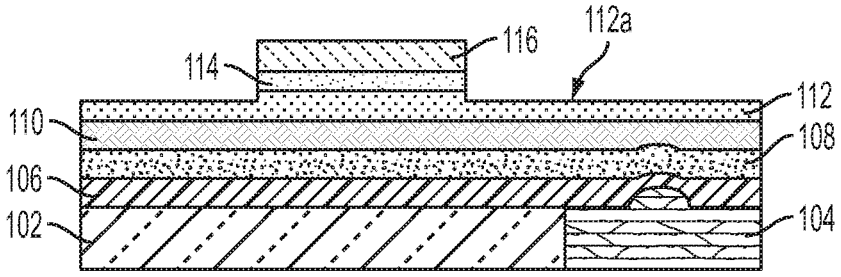

112a
116
114
112
110
108
106
102
104

FIG. 3B

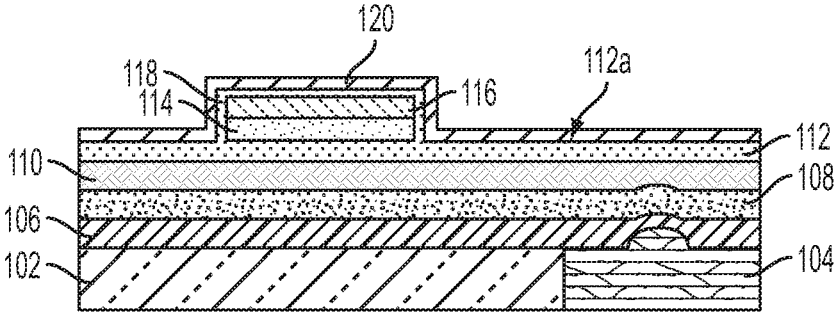

120
118
114
116
112a
112
110
108
106
102
104

FIG. 3C

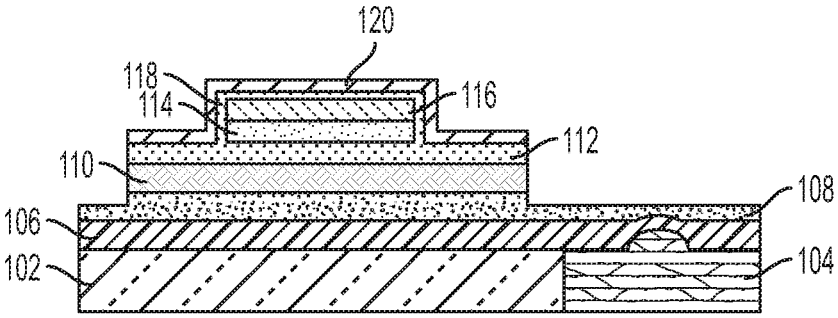

120
118
114
116
112
110
108
106
102
104

FIG. 3D

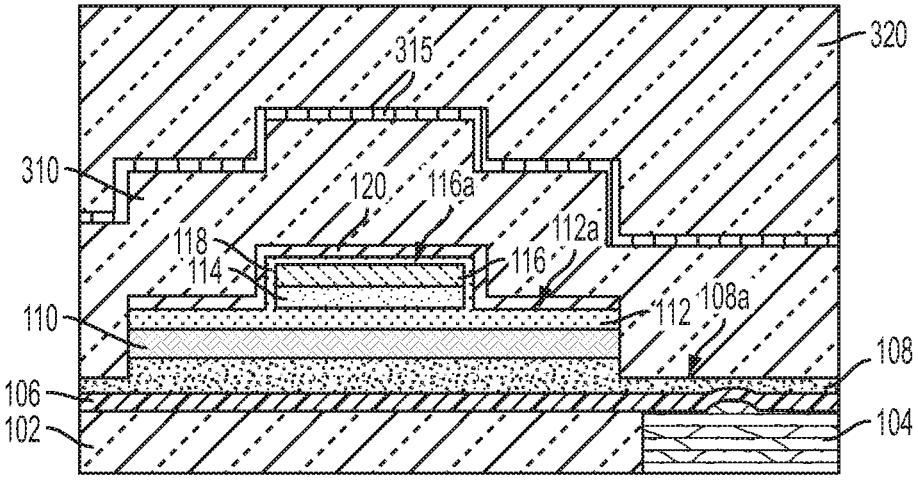

315
320
310
120
116a
112a
118
114
116
110
112
108a
108
106
102
104

FIG. 3E

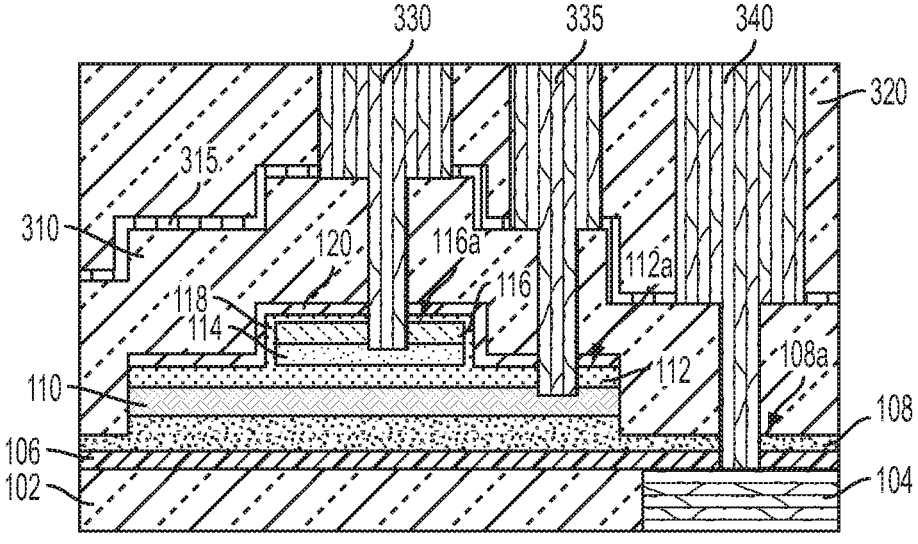

330
335
340
320
315
310
120
116a
112a
118
114
116
110
112
108a
108
106
102
104

FIG. 3F

METHOD OF FORMING SEMICONDUCTOR STRUCTURES

PRIORITY CLAIM

[0001] The present application is a divisional of U.S. application Ser. No. 13/969,356, filed Aug. 16, 2013, which is incorporated herein by reference in its entirety.

RELATED APPLICATION

[0002] This application is related to U.S. application Ser. No. 13/161,076, filed Jun. 15, 2011, now U.S. Pat. No. 8,552,485, issued Oct. 8, 2013, the entirety of which is hereby incorporated by reference.

BACKGROUND OF THE DISCLOSURE

[0003] In general, a capacitor includes two conductive electrodes on opposing sides of a dielectric or other insulating layer, and may be categorized based on the materials employed to form the electrodes. For example, in a metal-insulator-metal (MIM) capacitor, the electrodes substantially comprise metallic materials. MIM capacitors offer the advantage of a relatively constant value of capacitance over a relatively wide range of voltages applied thereto. MIM capacitors also exhibit a relatively small parasitic resistance.

[0004] In integrated circuit designs, on-chip capacitors are used in various applications including dynamic random access memories (DRAM), voltage controlled oscillators (VCO), phase-lock loops, operational amplifiers and other circuit designs. On-chip capacitors are also used to decouple circuits from noise in a separate portion of an electrical system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0006] FIG. **1** is a cross-sectional view of metal insulator metal (MIM) capacitor in accordance with one or more embodiments;

[0007] FIG. **2** is a flowchart of a method of forming an MIM capacitor in accordance with one or more embodiments; and

[0008] FIGS. **3**A-**3**F are cross-sectional views of an MIM capacitor during various fabrication stages in accordance with one or more embodiments.

DETAILED DESCRIPTION

[0009] The following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are examples and are not intended to be limiting.

[0010] Three-dimensional integrated circuits (3D IC) have been proposed to integrate more transistors and circuits in a given area. In a process of forming a 3D IC, two dies, each including respective integrated circuits, are disposed to opposing surfaces of an interposer. Through-substrate-via (TSV) structures, also referred to as through-wafer-via structures, are formed in the interposer, providing electrical connection between the dies.

[0011] An interposer includes a substrate through which a TSV structure is formed. A dielectric layer is formed over the TSV structure. A copper bulk which is wider than the TSV structure is formed in the dielectric layer and in contact with the TSV structure. An etch stop layer is then formed on the dielectric layer.

[0012] To provide a charge storage, a MIM capacitor is formed on the etch stop layer. A method of forming the MIM capacitor that is known to the applicants includes forming capacitor plate/capacitor dielectric/capacitor plate layers on the etch stop layer. A removal process using chemicals removes portions of the layers to pattern the MIM capacitor. The applicants find that the removal process over removes the etch stop layer that is directly under the layers in some instances, attacking hillocks of the copper bulk. The chemicals of the removal process result in the corrosion at the top surface of the copper bulk. If a via plug is formed over and in contact with the corroded copper bulk, an open electrical connection between the via plug and the corroded copper bulk occurs, in some instances.

[0013] FIG. **1** is a cross-sectional view of a metal insulator metal (MIM) capacitor **100** in accordance with one or more embodiments. MIM capacitor **100** includes a base layer **102** and a copper bulk layer **104** in the base layer. An etch stop layer **106** is over base layer **102** and copper bulk layer **104**. An oxide-based dielectric layer **108** is over etch stop layer **106**. A top surface **108***a* of oxide-based dielectric layer **108** is a location for forming a contact with copper bulk layer **104**. A capacitor bottom layer **110** is over oxide-based dielectric layer **108**. An insulator layer **112** is over capacitor bottom layer **110**. A top surface **112***a* of insulator layer **112** is a location for forming a contact with capacitor bottom layer **110**. A capacitor top layer **114** is over insulator layer **112**. A protection layer **116** is over capacitor top layer **114**. A top surface **116***a* of protection layer **116** is a location for forming a contact with capacitor top layer **114**. A top dielectric layer **118** is over top surface **116***a* and top surface **112***a*. Top dielectric layer **118** also covers sidewalls of capacitor top layer **114** and protection layer **116**. A cap layer **120** is over top dielectric layer **118**.

[0014] Base layer **102** is part of a support structure. In some embodiments, base layer **102** is part of an interposer. In some embodiments, the interposer is configured to provide electrical connection in a 3-dimensional (3-D) integrated circuit package system. In some embodiments, the interposer includes at least one passive device, e.g., a capacitor, a resistor, and/or an inductor. In some embodiments, the interposer is substantially free from including any active device, e.g., metal-oxide-semiconductor (MOS) transistors, bipolar junction transistors (BJTs), complementary MOS (CMOS) transistors, etc. In some embodiments, the interposer can be referred to as a passive interposer.

[0015] In some embodiments, MIM capacitor **100** includes various passive and active microelectronic devices, such as resistors, capacitors, inductors, diodes, metal-oxide-semiconductor field effect transistors (MOSFETs), complementary MOS (CMOS) transistors, bipolar junction transistors (BJTs), laterally diffused MOS (LDMOS) transistors, high power MOS transistors, FinFET transistors, other types of transistors, devices, circuits, and/or any combinations thereof.

[0016] In some embodiments, base layer **102** is a substrate. In some embodiments, the substrate includes an elementary semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenide, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and/or GaInAsP; any other suitable material; or combinations thereof. In at least one embodiment, the alloy semiconductor substrate may have a gradient SiGe feature in which the Si and Ge composition change from one ratio at one location to another ratio at another location of the gradient SiGe feature. In another embodiment, the alloy SiGe is formed over a silicon substrate. In another embodiment, a SiGe substrate is strained. Furthermore, the semiconductor substrate may be a semiconductor on insulator, such as a silicon on insulator (SOI), or a thin film transistor (TFT). In some examples, the semiconductor substrate may include a doped epi layer or a buried layer. In other examples, the compound semiconductor substrate may have a multilayer structure, or the substrate may include a multilayer compound semiconductor structure.

[0017] Copper bulk layer **104** is in base layer **102** to provide electrical connection between various circuitry in the base layer or another portion of a 3D IC. In some embodiments, copper bulk layer **104** continuously extends through base layer **102**. In some embodiments, copper bulk layer **104** includes at least one barrier material and at least one conductive material. The at least one barrier material includes, for example, titanium, titanium-nitride, tantalum, tantalum-nitride, other barrier materials, and/or combinations thereof. The at least one conductive material includes, for example, aluminum, copper, aluminum-copper, polysilicon, other suitable conductive materials, and/or combinations thereof.

[0018] Etch stop layer **106** is disposed over base layer **102** and copper bulk layer **104**. Etch stop layer **106** helps to reduce a risk of an etching process etching through the etch stop layer and removing material from base layer **102** or copper bulk layer **104**. In some embodiments, etch stop layer **106** is made of at least one material, such as silicon nitride, silicon oxynitride, silicon carbide, silicon oxycarbide, silicon carbon nitride, other suitable dielectric materials, and/or any combinations thereof.

[0019] Oxide-based dielectric layer **108** is disposed over etch stop layer **106**. Oxide-based dielectric layer **108** provides a buffer between the etch stop layer **106** and a later formed inter metal dielectric (IMD) layer, which further reduces the risk of an etching process etching through the etch stop layer and removing material from base layer **102** or copper bulk layer **104**. During formation of copper bulk layer **104** and etch stop layer **106**, hillocks or bumps in a top surface of the copper bulk layer are common. A hillock in copper bulk layer **104** will impact a surface profile of etch stop layer **106** resulting in a corresponding hillock in the etch stop layer. Sidewalls and corners of a hillock in etch stop layer **106** are thinner than other portions of the etch stop layer. During an etching process, such as that used to form a contact, the thinner portions of etch stop layer **106** are insufficient to prevent etching through the etch stop layer, in some instances. As a result, copper bulk layer **104** or base layer **102** are damaged by the etching process. In some instances where the damage is significant, a later formed contact will not electrically connect to copper bulk layer **104** and will be incapable of transferring electrical signals to the copper bulk layer, resulting in a non-functional device.

[0020] Oxide-based dielectric layer **108** has a thickness ranging from about **50** angstroms (Å) to about 2000 Å. If a thickness of oxide-based dielectric layer **108** is too thin, the oxide-based dielectric layer will not provide adequate protection of etch stop layer **106**, in some instances. If a thickness of oxide-based dielectric layer **108** is too great, etching and processing times for forming a contact with copper bulk layer **104** are increased, which increases a risk of damage to capacitor top layer **114**.

[0021] A material of oxide-based dielectric layer **108** is selected to have similar etch characteristics, e.g., etch rates in common etchants, as a later formed IMD layer, so that etch stop layer **106** is able to continue functioning as an etch stop layer during a contact formation process. If a material of oxide-based dielectric layer **108** as a sufficiently dissimilar etch characteristics, etching time during contact formation will be increased, which will increase a risk of damage to top capacitor layer **114**. In some embodiments, oxide-based dielectric layer **108** includes silicon oxide, TEOS (tetraethoxysilane; tetraethylorthosilicate; tetraethelorthosilicate; tetrethoxysilicide) oxide, a silicon-rich silicon oxide, or another suitable oxide-based dielectric material. A silicon-rich silicon oxide is a silicon oxide which includes more than 50% silicon.

[0022] Top surface **108***a* is not covered by capacitor bottom layer **110** and provides a location for forming a contact to electrically connect to copper bulk layer **104**. In some instances, top surface **108***a* includes at least one hillock corresponding to a hillock in copper bulk layer **104**. Despite the presence of a hillock in top surface **108***a*, additional thickness provided by oxide-based dielectric layer **108** reduces the risk of etch through to copper bulk layer **104** during contact formation.

[0023] Capacitor bottom layer **110** is over oxide-based dielectric layer **108**. Capacitor bottom layer **110** includes a conductive material used to form part of an MIM capacitor. In some embodiments, capacitor bottom layer **110** includes a metallic material. In some embodiments, the metallic material includes aluminum, copper, aluminum copper, tantalum, tantalum nitride, titanium, titanium nitride, tantalum silicon nitride, tungsten, tungsten nitride, other metallic materials, and/or any combinations thereof.

[0024] Insulator layer **112** is over capacitor bottom layer **110**. Insulator layer **112** includes an insulator material used to form an MIM capacitor. In some embodiments, insulator layer **112** has a dielectric constant that is equal to or higher than that of a silicon dioxide, e.g., about 3.9. To increase a capacitance of MIM capacitor **100**, a thickness of insulator layer **112** is reduced and/or a high dielectric constant (high-k) material is used as the insulator layer, in some embodiments. For example, insulator layer **112** includes silicon oxynitride, silicon nitride, hafnium oxide (HfO_2), hafnium silicon oxide (HfSiO), hafnium silicon oxynitride (HfSiON), hafnium tantalum oxide (HMO), hafnium titanium oxide (HfTiO), hafnium zirconium oxide (HfZrO), other dielectric materials, and/or any combinations thereof.

[0025] Top surface **112***a* is not covered by capacitor top layer **114** and provides a location for forming a contact to electrically connect to capacitor bottom layer **110**.

[0026] Capacitor top layer **114** is over insulator layer **112**. Capacitor top layer **114** includes a conductive material used

to form part of an MIM capacitor. In some embodiments, capacitor top layer **114** includes a metallic material. In some embodiments, the metallic material includes aluminum, copper, aluminum copper, tantalum, tantalum nitride, titanium, titanium nitride, tantalum silicon nitride, tungsten, tungsten nitride, other metallic materials, and/or any combinations thereof. In some embodiments, capacitor top layer **114** includes a same material as capacitor bottom layer **110**. In some embodiments, capacitor top layer **114** includes a different material from capacitor bottom layer **110**.

[0027] Protection layer **116** is over capacitor top layer **114**. Protection layer **116** helps to protect capacitor top layer **114** during a contact formation process. Protection layer **116** includes a different material from the later formed IMD layer and has different etching characteristics from the later formed IMD layer. A thickness of protection layer **116** is sufficient to prevent etching through capacitor top layer **114** during the contact formation processes. In some embodiments, protection layer **116** includes silicon oxynitride, silicon nitride, silicon carbide, or another suitable material.

[0028] Top dielectric layer **118** that is over protection layer **116**. Top dielectric layer **118** provides extra protection for capacitor top layer **114** during contact formation processes by protecting both the top surface of capacitor top layer **114** and sidewalls of the capacitor top layer. In some embodiments, top dielectric layer **118** is a single layer. In some embodiments, top dielectric layer **118** is a multi-layer structure. In some embodiments, top dielectric layer **118** includes silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, silicon oxycarbide, silicon carbon nitride, other dielectric materials, and/or any combinations thereof. In some embodiments, top dielectric layer **118** is a dual-layer structure including a silicon oxide layer and a silicon nitride layer formed thereon. In some embodiments where cap layer **120** and protection layer **116** provide sufficient protection for capacitor top layer **114**, top dielectric layer **118** is omitted.

[0029] Cap layer **120** that is over top dielectric layer **118**. Cap layer **120** provides extra protection for capacitor top layer **114** during contact formation processes by protecting both the top surface of capacitor top layer **114** and sidewalls of the capacitor top layer. In some embodiments, cap layer **120** is a single layer. In some embodiments, cap layer **120** is a multi-layer structure. In some embodiments, cap layer **120** includes silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, silicon oxycarbide, silicon carbon nitride, other dielectric materials, and/or any combinations thereof. In some embodiments, cap layer **120** is a dual-layer structure including a silicon oxide layer and a silicon nitride layer formed thereon. In some embodiments where top dielectric layer **118** and protection layer **116** provide sufficient protection for capacitor top layer **114**, cap layer **120** is omitted.

[0030] FIG. **2** is a flow chart of a method **200** of forming an MIM capacitor in accordance with one or more embodiments. Method **200** begins with operation **202** in which MIM film layers, including an oxide-based dielectric film, are formed. In some embodiments, the MIM film layers include an etch stop layer; the oxide-based dielectric layer over the etch stop layer; a capacitor bottom layer over the oxide-based dielectric layer; an insulator layer over the capacitor bottom layer; a capacitor top layer over the insulator layer; and a protection layer over the capacitor top layer.

[0031] In some embodiments, the MIM film layers are blanket deposited over a base layer including a copper bulk layer in the base layer. In some embodiments, the MIM film layers are selectively deposited using a mask. In some embodiments, at least one of the MIM film layers is deposited in a separate chamber. In some embodiments, the MIM film layers are deposited in a same chamber using different materials.

[0032] In some embodiments, dielectric layers of the MIM film layers are formed by a chemical vapor deposition (CVD) process, a plasma-enhanced CVD (PECVD) process, a physical vapor deposition (PVD) process, an atomic layer deposition (ALD), other suitable process, or any combinations thereof. In some embodiments, metallic layers of the MIM film layers are formed by a CVD process, a PVD process, an ALD process, an electroplating process, another process, or any combinations thereof. In some embodiments, a removal process, e.g., a chemical mechanical polish (CMP) process, is performed between formations of subsequent layers in the MIM film layers.

[0033] FIG. **3**A is a cross-sectional view of an MIM capacitor following operation **202** in accordance with one or more embodiments. The arrangement of FIG. **3**A includes etch stop layer **106**, oxide-based dielectric layer **108**, capacitor bottom layer **110**, insulator layer **112**, capacitor top layer **114**, and protection layer **116** blanket deposited over base layer **102** including copper bulk layer **104**. The arrangement of FIG. **3**A includes a hillock **104***a* in copper bulk layer **104**. Hillock **104***a* impacts a profile of etch stop layer **106** and oxide-base layer **108**.

[0034] Returning to FIG. **2**, method **200** continues with etching the capacitor top layer in operation **204**. In some embodiments, etching the capacitor top layer also includes etching the protection layer. The capacitor top layer is etched in order to expose a portion of the insulator layer to enable formation of a contact with the capacitor bottom layer.

[0035] In some embodiments, the capacitor top layer is etched using a photolithographic process. The photo lithographic process includes depositing a mask layer over the capacitor top layer, developing and patterning the mask layer to form openings in the mask layer. The capacitor top layer is then etched through the openings in the mask layer. In some embodiments, the etching process includes a dry etching process, a wet etching process, another suitable material removal process or a combination thereof.

[0036] FIG. **3**B is a cross-sectional view of an MIM capacitor following operation **204** in accordance with one or more embodiments. In comparison with the arrangement of FIG. **3**A, the arrangement of FIG. **3**B includes a capacitor top layer **114** and protection layer **116** which have a reduced size and expose top surface **112***a*. The arrangement of FIG. **3**B includes a remaining portion of capacitor top layer **114** offset from a center of the MIM capacitor. In some embodiments, the remaining portion of capacitor top layer **114** is aligned with an edge of the MIM capacitor. In some embodiments, the remaining portion of capacitor top layer **114** is centered in the MIM capacitor.

[0037] Returning to FIG. **2**, method **200** continues with optional operation **206** in which a cap layer is formed over the etched capacitor top layer. In some embodiments, forming the cap layer includes forming a separate top dielectric layer over the etched capacitor top layer prior to forming the cap layer. In some embodiments, forming the cap layer includes forming a single layer. In some embodiments, forming the cap layer includes forming a multi-layered structure.

[0038] In some embodiments, the cap layer is formed using a CVD process, a PECVD process, a PVD process, an ALD, another suitable process, or any combinations thereof. In some embodiments, the cap layer is selectively formed over the etched capacitor top layer. In some embodiments, the cap layer is blanket deposited over the etched capacitor top layer and the top surface of the insulator layer exposed during operation **204**.

[0039] In some embodiments, operation **206** is omitted. Operation **206** is omitted if the protection layer provides sufficient protection of the capacitor top layer during subsequent contact formation processes.

[0040] FIG. **3**C is a cross-sectional view of an MIM capacitor following operation **206** in accordance with one or more embodiments. In comparison with the arrangement of FIG. **3**B, the arrangement of FIG. **3**C includes top dielectric layer **118** and cap layer **120** over protection layer **116**, capacitor top layer **114** and top surface **112***a*.

[0041] Returning to FIG. **2**, method **200** continues with etching the capacitor bottom layer in operation **208**. In some embodiments, etching the capacitor bottom layer also includes etching the insulator layer. The capacitor bottom layer is etched in order to expose a portion of the oxide-based dielectric layer to enable formation of a contact with the copper bulk layer.

[0042] In some embodiments, the capacitor bottom layer is etched using a photolithographic process. The photo lithographic process includes depositing a mask layer over the capacitor bottom layer, developing and patterning the mask layer to form openings in the mask layer. The capacitor bottom layer is then etched through the openings in the mask layer. In some embodiments, the etching process includes a dry etching process, a wet etching process, another suitable material removal process or a combination thereof.

[0043] FIG. **3**D is a cross-sectional view of an MIM capacitor following operation **208** in accordance with one or more embodiments. In comparison with the arrangement of FIG. **3**C, the arrangement of FIG. **3**D includes capacitor bottom layer **110** and insulator layer **112** which have a reduced size and expose top surface **108***a*. The arrangement of FIG. **3**D includes a remaining portion of capacitor bottom layer **110** offset from a center of the MIM capacitor. In some embodiments, the remaining portion of capacitor bottom layer **110** is aligned with an edge of the MIM capacitor. In some embodiments, the remaining portion of capacitor bottom layer **110** is centered in the MIM capacitor.

[0044] Returning to FIG. **2**, method **200** continues with operation **210** in which an inter metal dielectric (IMD) layer is formed over the etched capacitor bottom layer. In some embodiments, more than one IMD layer is formed over the etched capacitor bottom layer. In some embodiments, the more than one IMD layers are separated by an etch stop layer. In some embodiments, the IMD layer includes silicon oxide, e.g., undoped silicate glass (USG), boron-doped silicate glass (BSG), phosphor-doped silicate glass (PSG), boron-phosphor-doped silicate glass (BPSG), or the like, silicon oxy-nitride, silicon nitride, a low dielectric constant (low-k) material, an ultra-low-k dielectric material, and/or any combinations thereof.

[0045] FIG. **3**E is a cross-sectional view of an MIM capacitor following operation **210** in accordance with one or more embodiments. In comparison with the arrangement of FIG. **3**D, the arrangement of FIG. **3**E includes a first IMD layer **310** over etched capacitor bottom layer **110**. The arrangement of FIG. **3**E further includes an etch stop layer **315** over first IMD layer **310** and a second IMD layer **320** over the etch stop layer.

[0046] In some embodiments, first IMD layer **310** and second IMD layer **320** include a same material. In some embodiments, first IMD layer **310** and second IMD layer **320** include different materials. In some embodiments, etch stop layer **320** includes a same material as etch stop layer **106**. In some embodiments, etch stop layer **320** includes a different material from etch stop layer **106**.

[0047] First IMD layer **310** is conformal with remaining portions of the MIM film layers. A thickness of first IMD layer **310** over top surface **108***a* is substantially equal to a thickness of the first IMD layer over top surface **112***a* and top surface **116***a*. Due to the substantially equal thicknesses, an etching time to form an opening in first IMD layer **310** for a contact is substantially equal for capacitor top layer **114**, capacitor bottom layer **110** and copper bulk layer **104**. The substantially equal etching time for each of the contact openings helps to reduce the risk of over etching and damaging of capacitor top layer **114**, capacitor bottom layer **110** or copper bulk layer **104**.

[0048] Etch stop layer **315** is conformal with first IMD layer **310**. Etch stop layer **315** provides an etch stop so that etching second IMD layer **320** to form openings for an interconnect structure does not damage first IMD layer **310**.

[0049] Second IMD layer **320** is conformal with etch stop layer **315**. In some embodiments, second IMD layer **320** is part of an interconnect structure.

[0050] Returning to FIG. **2**, method **200** continues with operation **212** in which contacts are formed through the IMD layer. A first contact is formed to electrically connect to the capacitor top layer. A second contact is formed to electrically connect to the capacitor bottom layer. A third contact is formed to electrically connect to the copper bulk layer. In some embodiments, the contacts include at least one barrier material and at least one conductive material. In some embodiments, the at least one barrier material includes titanium, titanium-nitride, tantalum, tantalum-nitride, other barrier materials, or combinations thereof. In some embodiments, the at least one conductive material includes aluminum, copper, aluminum-copper, polysilicon, other conductive materials, or combinations thereof. In some embodiments, the contacts are via plug structures, single damascene structures, conductive bulks, conductive slats, conductive lines, or any other conductive structure shape. In some other embodiments, the contacts are part of a dual damascene structure.

[0051] In some embodiments, the contacts are formed using a photolithography/etching process to form an opening in the IMD layer. The opening is then filled with the contact, e.g., the at least one barrier layer and the at least one conductive layer. In some embodiments, a CMP process is then used to remove excess contact material from a top surface of the IMD layer. In some embodiments, at least one contact is formed separately. In some embodiments, all contacts are formed simultaneously. In some embodiments, the openings for each contact are formed separately and each opening is filled simultaneously.

[0052] FIG. **3**F is a cross-sectional view of an MIM capacitor following operation **212** in accordance with one or more embodiments. In comparison with the arrangement of FIG. **3**E, the arrangement of FIG. **3**F includes a first contact **330** electrically connected to capacitor top layer **114**; a

second contact **335** electrically connected to capacitor bottom layer **110**; and a third contact **340** electrically connected to copper bulk layer **104**. In the arrangement of FIG. **3**F, second contact **335** is positioned between first contact **330** and third contact **340**. In some embodiments, first contact **330** is positioned between second contact **335** and third contact **340**.

[0053] First contact **330** extends through second IMD layer **320**; etch stop layer **315**, first IMD layer **310**, cap layer **120**, top dielectric layer **118** and protection layer **116** in order to electrically connect to capacitor top layer **114**.

[0054] Second contact **335** extends through second IMD layer **320**; etch stop layer **315**, first IMD layer **310**, and insulator layer **112** in order to electrically connect to capacitor bottom layer **110**.

[0055] Third contact **340** extends through second IMD layer **320**, etch stop layer **315**, first IMD layer **310**, oxide-based dielectric layer **108** and etch stop layer **106** in order to electrically connect to copper bulk layer **104**. The inclusion of oxide-based dielectric layer **108** helps to ensure that third contact **340** is electrically connected to copper bulk layer **104** by preventing damage to the copper bulk layer during the etching process used to form the opening for the third contact. As a result, electrical signals are able to be transmitted from copper bulk layer **104** to third contact **340**.

[0056] One of ordinary skill in the art would recognize that additional operations are able to be added to method **200** in order to form a finished device. One of ordinary skill in the art would also recognize that an order of operations is able to be changed and operations are able to be combined or separated.

[0057] One aspect of this description relates to a method of making a metal insulator metal (MIM) capacitor. The method includes forming a copper bulk layer in a base layer, wherein the copper bulk layer includes a hillock extending from a top surface thereof. The method further includes depositing an etch stop layer over the base layer and the copper bulk layer. The method further includes depositing an oxide-based dielectric layer over the etch stop layer. The method further includes forming a capacitor over the oxide-based dielectric layer. The method further includes forming a contact extending through the oxide-based dielectric layer and the etch stop layer to contact the copper bulk layer, wherein the forming of the contact removes the hillock. In some embodiments, the forming of the oxide-based dielectric layer includes forming the oxide-based dielectric layer comprising at least one of a silicon oxide, a silicon-rich silicon oxide, or a TEOS (tetraethoxysilane; tetraethylorthosilicate; tetraethelorthosilicate; tetrethoxysilicide) oxide. In some embodiments, the forming of the oxide-based dielectric layer includes forming the oxide-based dielectric layer having a thickness ranging from about 50 angstroms (Å) to about 2000 Å. In some embodiments, wherein the forming of the contact includes etching a capacitor bottom layer of the capacitor to expose a portion of a top surface of the oxide-based dielectric layer; and forming a contact hole through the exposed portion of the top surface of the oxide-based dielectric layer to expose the copper bulk layer. In some embodiments, the method further includes depositing a conformal inter metal dielectric (IMD) layer over the capacitor and the oxide-based dielectric layer, wherein the forming of the contact includes forming the contact extending through the IMD layer. In some embodiments, the method further includes depositing a cap layer over the capacitor. In some embodiments, the depositing of the cap layer includes depositing the cap layer over a protection layer, wherein the protection layer separates a top conductive layer of the capacitor from the cap layer. In some embodiments, the method further includes etching a bottom conductive layer of the capacitor to expose a portion of oxide-based dielectric layer. In some embodiments, etching the bottom conductive layer of the capacitor includes recessing a top surface of the oxide-based dielectric layer.

[0058] Another aspect of this description relates to a method of making a metal insulator metal (MIM) capacitor. The method includes forming a copper bulk layer in a base layer, wherein the copper bulk layer includes a hillock extending from a top surface thereof. The method further includes depositing an oxide-based dielectric layer over the copper bulk layer, wherein the deposited oxide-based dielectric layer includes a protrusion corresponding to the hillock. The method further includes forming a capacitor over the oxide-based dielectric layer, wherein the capacitor includes a top conductive layer, a bottom conductive layer and a capacitor dielectric layer between the top conductive layer and the bottom conductive layer. The method further includes etching the bottom conductive layer to expose a portion of the oxide-based dielectric layer, wherein the etching of the bottom conductive layer further includes recessing a top surface of the oxide-based dielectric layer to remove the protrusion. In some embodiments, the method further includes forming a contact extending through the oxide-based dielectric layer to contact the copper bulk layer, wherein the forming of the contact removes the hillock. In some embodiments, the method further includes depositing an etch stop layer over the copper bulk layer, wherein the etch stop layer is between the oxide-based dielectric layer and the copper bulk layer, and the etch stop layer includes a bump corresponding to the hillock. In some embodiments, the forming of the contact includes removing the bump in the etch stop layer. In some embodiments, the method further includes forming a top dielectric layer over a top surface and sidewalls of the top conductive layer. In some embodiments, the method further includes depositing a cap layer over a top surface and sidewalls of the top dielectric layer. In some embodiments, the etching of the bottom conductive layer further includes etching the cap layer.

[0059] Still another aspect of this description relates to a method of making a semiconductor device. The method includes forming a copper bulk layer in a base layer, wherein the copper bulk layer includes a hillock extending from a top surface thereof. The method further includes depositing an etch stop layer over the copper bulk layer, wherein the etch stop layer includes a bump corresponding to the hillock. The method further includes depositing an oxide-based dielectric layer over the etch stop layer, wherein the deposited oxide-based dielectric layer includes a protrusion corresponding to the hillock. The method further includes recessing a top surface of the oxide-based dielectric layer to remove the protrusion. The method further includes forming a contact extending through the oxide-based dielectric layer and the etch stop layer to contact the copper bulk layer, wherein the forming of the contact removes the hillock. In some embodiments, the method further includes forming a capacitor over the oxide-based dielectric layer, wherein the capacitor includes a top conductive layer, a bottom conductive layer and a capacitor dielectric layer between the top conductive layer and the bottom conductive layer. In some embodi-

ments, the method further includes depositing a conformal inter metal dielectric (IMD) layer over the recessed top surface of the oxide-based dielectric layer. In some embodiments, the forming of the contact includes forming the contact through the IMD layer.

[0060] It will be readily seen by one of ordinary skill in the art that the disclosed embodiments fulfill one or more of the advantages set forth above. After reading the foregoing specification, one of ordinary skill will be able to affect various changes, substitutions of equivalents and various other embodiments as broadly disclosed herein. It is therefore intended that the protection granted hereon be limited only by the definition contained in the appended claims and equivalents thereof.

What is claimed is:

1. A method of making a metal insulator metal (MIM) capacitor, the method comprising:

forming a copper bulk layer in a base layer, wherein the copper bulk layer comprises a hillock extending from a top surface thereof;

depositing an etch stop layer over the base layer and the copper bulk layer;

depositing an oxide-based dielectric layer over the etch stop layer;

forming a capacitor over the oxide-based dielectric layer; and

forming a contact extending through the oxide-based dielectric layer and the etch stop layer to contact the copper bulk layer, wherein the forming of the contact removes the hillock.

2. The method of claim **1**, wherein the forming of the oxide-based dielectric layer comprises forming the oxide-based dielectric layer comprising at least one of a silicon oxide, a silicon-rich silicon oxide, or a TEOS (tetraethoxysilane; tetraethylorthosilicate;

tetraethelorthosilicate; tetrethoxysilicide) oxide.

3. The method of claim **1**, wherein the forming of the oxide-based dielectric layer comprises forming the oxide-based dielectric layer having a thickness ranging from about 50 angstroms (Å) to about 2000 Å.

4. The method of claim **1**, wherein the forming of the contact comprises:

etching a capacitor bottom layer of the capacitor to expose a portion of a top surface of the oxide-based dielectric layer; and

forming a contact hole through the exposed portion of the top surface of the oxide-based dielectric layer to expose the copper bulk layer.

5. The method of claim **1**, further comprising depositing a conformal inter metal dielectric (IMD) layer over the capacitor and the oxide-based dielectric layer, wherein the forming the of the contact comprises forming the contact extending through the IMD layer.

6. The method of claim **1**, further comprising depositing a cap layer over the capacitor.

7. The method of claim **6**, wherein the depositing of the cap layer comprises depositing the cap layer over a protection layer, wherein the protection layer separates a top conductive layer of the capacitor from the cap layer.

8. The method of claim **1**, further comprising etching a bottom conductive layer of the capacitor to expose a portion of the oxide-based dielectric layer.

9. The method of claim **8**, wherein etching the bottom conductive layer of the capacitor comprises recessing a top surface of the oxide-based dielectric layer.

10. A method of making a metal insulator metal (MIM) capacitor, the method comprising:

forming a copper bulk layer in a base layer, wherein the copper bulk layer comprises a hillock extending from a top surface thereof;

depositing an oxide-based dielectric layer over the copper bulk layer, wherein the deposited oxide-based dielectric layer includes a protrusion corresponding to the hillock;

forming a capacitor over the oxide-based dielectric layer, wherein the capacitor includes a top conductive layer, a bottom conductive layer and a capacitor dielectric layer between the top conductive layer and the bottom conductive layer; and

etching the bottom conductive layer to expose a portion of the oxide-based dielectric layer, wherein the etching of the bottom conductive layer further comprises recessing a top surface of the oxide-based dielectric layer to remove the protrusion.

11. The method of claim **10**, further comprising forming a contact extending through the oxide-based dielectric layer to contact the copper bulk layer, wherein the forming of the contact removes the hillock.

12. The method of claim **11**, further comprising depositing an etch stop layer over the copper bulk layer, wherein the etch stop layer is between the oxide-based dielectric layer and the copper bulk layer, and the etch stop layer includes a bump corresponding to the hillock.

13. The method of claim **12**, wherein the forming of the contact comprises removing the bump in the etch stop layer.

14. The method of claim **10**, further comprising forming a top dielectric layer over a top surface and sidewalls of the top conductive layer.

15. The method of claim **14**, further comprising depositing a cap layer over a top surface and sidewalls of the top dielectric layer.

16. The method of claim **15**, wherein the etching of the bottom conductive layer further comprises etching the cap layer.

17. A method of making a semiconductor device, the method comprising:

forming a copper bulk layer in a base layer, wherein the copper bulk layer comprises a hillock extending from a top surface thereof;

depositing an etch stop layer over the copper bulk layer, wherein the etch stop layer includes a bump corresponding to the hillock;

depositing an oxide-based dielectric layer over the etch stop layer, wherein the deposited oxide-based dielectric layer includes a protrusion corresponding to the hillock;

recessing a top surface of the oxide-based dielectric layer to remove the protrusion; and

forming a contact extending through the oxide-based dielectric layer and the etch stop layer to contact the copper bulk layer, wherein the forming of the contact removes the hillock.

18. The method of claim **17**, further comprising forming a capacitor over the oxide-based dielectric layer, wherein the capacitor includes a top conductive layer, a bottom conduc-

tive layer and a capacitor dielectric layer between the top conductive layer and the bottom conductive layer.

19. The method of claim **17**, further comprising depositing a conformal inter metal dielectric (IMD) layer over the recessed top surface of the oxide-based dielectric layer.

20. The method of claim **19**, wherein the forming of the contact comprises forming the contact through the IMD layer.

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