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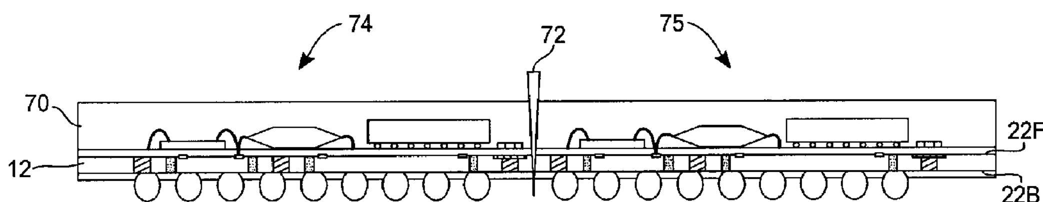
(54) Title: MULTI-COMPONENT ELECTRONIC PACKAGE WITH PLANARIZED EMBEDDED-COMPONENTS SUBSTRATE



(57) Abstract: An electronic multi -component package (74, 75) is assembled by placing multiple electronic components (30) within multiple openings (16) of a package substrate (12), then depositing and curing adhesive filler (34) in gaps between the components and the inner peripheries of the openings. Circuit features (38, 42), including conductive interconnects, are formed by thin-film photolithography over both front and back surfaces (22F, 22B) of the package substrate. Preformed conductive vias (18) through the package substrate provide electrical connection between circuit features on opposite substrate surfaces. Additional electronic components (50, 54, 58) may be attached (52, 56, 60) to conductive lands on at least one side of the package. The circuit features also include contact pads (66) for external package connections, such as in a ball-grid-array or equivalent structure.

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Description

MULTI-COMPONENT ELECTRONIC PACKAGE WITH PLANARIZED EMBEDDED-COMPONENTS SUBSTRATE

TECHNICAL FIELD

The present invention relates to integrated circuit (IC) chip packages and the mounting of one or more IC dice to a support substrate and/or frame together with associated circuit components and interconnects.

BACKGROUND ART

Multi-component electronic packages and system-in-package (SIP) packages that are employed in the electronics industry today all utilize substrates for device inter-connection and attachment. Typical organic substrate materials are epoxy-glass, polyimide, and fluoropolymer laminates. Typical inorganic substrate materials are ceramics, low-temperature co-fire ceramics (LTCC) and silicon. The interconnect circuitry and component attach features are fabricated onto the substrates prior to components assembly.

With the exception of a silicon substrate, which employs thin-film metal deposition processes for the circuitry fabrication to yield line geometries on the order of one micrometer, all of the other substrate materials yield line geometries that are 50 micrometers or larger. A silicon substrate can only be used in single-sided applications and is often fragile in the final package form. The larger line geometries of the other substrates necessitate a larger final package size. The resultant longer interconnect lengths can also compromise package performance. Package designs with smaller package footprints and lower profiles, along with higher performance and yields, are ever being sought in

the electronics industry.

SUMMARY DISCLOSURE

The present invention is method of assembling a multi-component electronic package and the package so formed in which microelectronic integrated circuit (IC) dice and/or discrete active/passive components are embedded into a "windowed" substrate carrier, planarized on both top and bottom surfaces. Electrically conductive interconnects and dielectric layers are deposited, or otherwise formed, on the top and bottom surfaces to electrically connect the embedded components.

In particular, a package substrate is provided, having defined front and back surfaces, with conductive vias through the package substrate. Multiple openings in the package substrate are sized to receive electronic components. After securing the package substrate on a vacuum support, multiple electronic components are placed within those openings and secured in place by the vacuum support. Adhesive filler material is deposited within a gap between the components and the inner peripheries of the corresponding openings, and then the filler is cured so as to permanently secure the embedded electronic components within the package substrate.

Circuit features are then formed in one or more layers over both front and back surfaces of the package substrate, for example, by thin-film photolithography. Features on opposite surfaces are electrically connected to each other by means of the conductive vias through package substrate. The circuit features include conductive interconnects that are electrically connected to the multiple electronic components embedded within the substrate. Integrated passive features, such as inductors, can also be formed during the circuitry fabrication process. Additional electronic components

can be attached to resulting structure, e.g., at metal lands. A land-grid array, ball-grid array or pin-grid array can be formed on a back surface of the package substrate.

5 Package components are thus assembled onto the substrate to form an extremely compact, highly integrated, multi-component package or system-in-package (SIP) that provides an extremely small footprint and low profile. The electrical performance of the package is 10 improved due to the ability to place the IC dice and other components in close proximity. The thin-film conductive interconnects formed on the planarized surfaces allow a much finer line width and spacing geometry in comparison with even the most advanced 15 printed circuit board technologies. It also allows precise, high Q, integrated passive inductors to be formed in close proximity to the IC dice. With the interconnect layers deposited directly above and below the IC dice, a more efficient use is made of the 20 package's footprint area, resulting in a smaller package size. The standard die-attach, wire bond or flip-chip attach processes can be eliminated by using this embedded components method.

25 BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B are respective top plan and side sectional views (the latter taken through the line 1B-1B in Fig. 1A) of a wafer substrate serving as a starting point for assembly of a multi-component 30 electronic package in accord with the present invention.

Figs. 2A through 2H are respective side sectional views, analogous to Fig. 1B, at various stages in a process of assembling an electronic package in accord with the present invention.

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DETAILED DESCRIPTION

With reference to Figs. 1A and 1B, a wafer 10 forms a substrate 12 for one or more IC chip packages. When cut into sections, e.g., 14_1, 14_2, 14_3, 14_4, each of those sections of the wafer 10 will define a separate package. The substrate 12 is typically composed of a dielectric material, such ceramics, glass, or plastics (e.g., epoxy, polyimide, or fluoropolymers). The substrate 12 has open cavities 16 into which IC die and other discrete electronic components will be placed. The width and length dimensions of the open cavities 16 are normally slightly larger than the components that will be inserted to allow tolerance for variations in the individual component size and room for adding an adhesive compound between the components and the inner periphery of the cavities 16.

Conductive vias 18 through the substrate 12 provide electrical pathways between the designated front and back surfaces 22F and 22B of the substrate 12 upon which electrical interconnects and other circuit elements (inductors, etc.) will be formed. Component lands 20, also conductive, may serve as attachment pads for discrete components, and also as land-grid, ball-grid or pin-grid pads for electrically connecting the resultant IC package to a printed circuit board or other system-level circuit structure.

With reference to Fig. 2A, a method of assembling the package begins with the aforementioned substrate 12 being mounted front-side down onto a die alignment vacuum plate 24. Various IC dice and discrete electrical components (active or passive) to be embedded in the substrate 12 are placed within the cavities 16. Preferably, IC dice will be place active side 32 down, so that the active side 32 will be generally coplanar with the front surface 22F of the substrate. In this way, we

don't need to use a substrate having the same thickness as the IC dice, and the various IC dice being embedded need not all have the same thickness. Vacuum openings 26 in the vacuum plate 24 will hold the substrate 12, and the IC dice and other discrete components 30 in a fixed position.

With reference to Fig. 2B, normally the components 30 will be somewhat smaller in length and width dimensions than the cavities 16 in which they are place. The gaps between the components 30 and the inner peripheries of the cavities 16 are filled with an adhesive compound 34. After curing of the adhesive compound 34, the substrate 12 with its embedded components 30 is released by the vacuum plate 24. The cured adhesive compound 34 now holds the embedded components 30 in place. Depending on the adhesive compound being used to fill the gaps, the curing can be performed by application of heat (e.g., in a furnace) or by ultraviolet light. A self-curing adhesive (e.g., an epoxy resin with catalyst) could be also be used.

The designated back side of the package (opposite from that containing the active surfaces on the die) may be kept relatively planar by controlling the thicknesses of the die and discrete components, or may be made planar, if needed, by performing a post-embedding grind process, with a liquid dielectric coating added to facilitate the planarizing.

With reference to Figs. 2D through 2F, thin-film deposition and photolithographic etching processes are used to build-up one or more layers circuit features over both surfaces 22B and 22F of the substrate assembly 12. On each side, there can be either a single layer of interconnects and other integrated circuit features, or, more usually, multiple layers of interconnects and

features separated by dielectric material layers and connected where needed by vias.

For example, as seen in Fig. 2D, a thin-film metallic layer 38 may be deposited over the front surface 22F of the substrate assembly 12, followed by a photolithographic mask layer 40. After patterning and etching of the thin-film metallic layer 38, removal of the mask layer 40, and possible repeating of the deposition and patterning of additional layers, such as a dielectric layer, integrated circuit features result. These circuit features may include metal lands for and interconnects between the embedded IC dice and other embedded components 30, as well as integrated passive elements, such as thin-film inductors.

Likewise, further integrated circuit features are also formed on the back surface 22B, including metallic lands, by means of successive deposition, patterning and etching using one or more thin-film and mask layers 42 and 44, as seen in Fig. 2E.

The result is a substrate assembly 12 with patterned circuitry 38 and 42 on both front and back sides, 22F and 22B, of the substrate. As already noted with reference to Figs. 1A and 1B, the circuitry on opposite sides of the substrate assembly 12 in Fig. 2F are connected to each other by means of the vias 18 that were pre-formed in the starting substrate.

With reference to Fig. 2G, additional electronic components can be attached to the resulting structure at metal lands on one of the surfaces, for example, above the front surface 22F. This may include die 50 attached with wire bonds 52, leaded packages 54 attached with their leads 56, ball-grid-array (BGA) packages 58 attached with solder balls 60, and discrete components 62. The opposite side of the assembly 12, for example, back side 22F, may have contact pads formed

thereon, such as a BGA structure of solder balls 66. Alternatively, pins could be attached at metal lands on the back surface to form a pin-grid-array (PGA) package structure. Or, the lands themselves, formed on the back
5 surface's thin film layer 42 in Figs. 2E and 2F, could define a land-grid-array.

With reference to Fig. 2H, the electronic components 50, 54, 58, etc. above the front surface 22F may optionally be covered by an epoxy over-mold 70,
10 coating or lid cover to protect them from damage during handling of the assembled package. Finally, the wafer 10 seen in Fig. 1A, now a completed package assembly, undergoes saw singulation into individual packages 74, 75, etc., with the cuts made along the dashed lines
15 indicated in Fig. 1A that demarcate the various segments.

Claims

1. A method of assembling a multi-component electronic package, comprising:

providing a package substrate having defined front and back surfaces, with conductive vias through the package substrate providing electrical connections between the front and back surfaces, and with multiple openings in the package substrate adapted to receive electronic components;

securing the package substrate on a vacuum support;

placing multiple electronic components within the multiple openings of the package substrate, the electronic components being secured in place by the vacuum support, each electronic component being spaced from an inner periphery of its corresponding opening of the package substrate by a gap;

depositing an adhesive filler material within the gap and then curing the adhesive filler material, such that the electronic components within the openings are permanently secured to the package substrate; and

forming circuit features in one or more layers on both front and back surfaces of the package substrate, circuit features on opposite surfaces of the package substrate being electrically connected to each other by means of the conductive vias through the package substrate, the circuit features including conductive interconnects that are electrically connected to the multiple electronic components, the circuit features on at least one surface of the package substrate including a set of contact pads defining external connection locations for the assembled multi-component electronic package.

2. The method as in claim 1, wherein the package substrate comprises a dielectric material with metallic vias therethrough.

5 3. The method as in claim 1, wherein at least one of the multiple electronic components placed within the openings of the package substrate is an integrated circuit (IC) die.

10 4. The method as in claim 3, wherein the IC die has an active surface and the IC die is placed in an opening of the package substrate with its active surface coinciding with designated front surface of the package substrate.

15 5. The method as in claim 1, wherein the circuit features are formed by photolithography, with deposition a thin-film feature layer and a mask layer over the feature layer, patterning and etching of the feature layer using the mask layer, removal of the mask layer,
20 and repeating to pattern additional feature layers.

6. The method as in claim 1, wherein the circuit features include integrated passive circuit elements.

25 7. The method as in claim 1, wherein the circuit features are successive formed first on one surface of the package substrate and then on the other surface of the package substrate.

30 8. The method as in claim 1, wherein the circuit features formed on the package substrate include conductive lands and the method further comprises attaching additional electronic components onto the designated front surface of the package substrate with
35 electrical connections to the conductive lands.

9. The method as in claim 8, further comprising providing a protective covering over the additional electronic components.

5 10. The method as in claim 1, wherein the set of contact pads are formed as circuit features on a designated back surface of the package substrate.

11. The method as in claim 10, wherein the set of contact pads form a package contact structure selected from the group consisting of a land-grid-array, ball-grid-array and pin-grid-array.

12. The method as in claim 1, wherein the package substrate is a wafer for assembling multiple packages, and the method, after forming the circuit features, further includes segmenting the wafer into individual assembled packages.

20 13. A multi-component electronic package, comprising:

a package substrate having designated front and back surfaces with conductive vias through the substrate;

multiple electronic components embedded within the package substrate and secured thereto by a cured adhesive material; and

one or more layers of circuit features on both front and back surfaces of the package substrate, circuit features on opposite surfaces of the package substrate being electrically connected to each other by means of the conductive vias through the package substrate, the circuit features including conductive interconnects that are electrically connected to the multiple electronic components, the circuit features on at least one surface of the package substrate including a set of contact pads

defining external connection locations for the electronic multi-component package.

14. The package as in claim 13, wherein the package substrate comprises a dielectric material with metallic vias therethrough.

15. The package as in claim 13, wherein at least one of the multiple electronic components embedded within the package substrate is an integrated circuit (IC) die.

16. The package as in claim 13, wherein the circuit features include integrated passive circuit elements.

17. The package as in claim 13, wherein the circuit features formed on the package substrate include conductive lands and the package further comprises additional electronic components attached to the designated front surface of the package substrate with electrical connections to the conductive lands.

18. The package as in claim 17, further comprising a protective covering over the additional electronic components.

19. The package as in claim 13, wherein the set of contact pads form a package contact structure selected from the group consisting of a land-grid-array, ball-grid-array and pin-grid-array.

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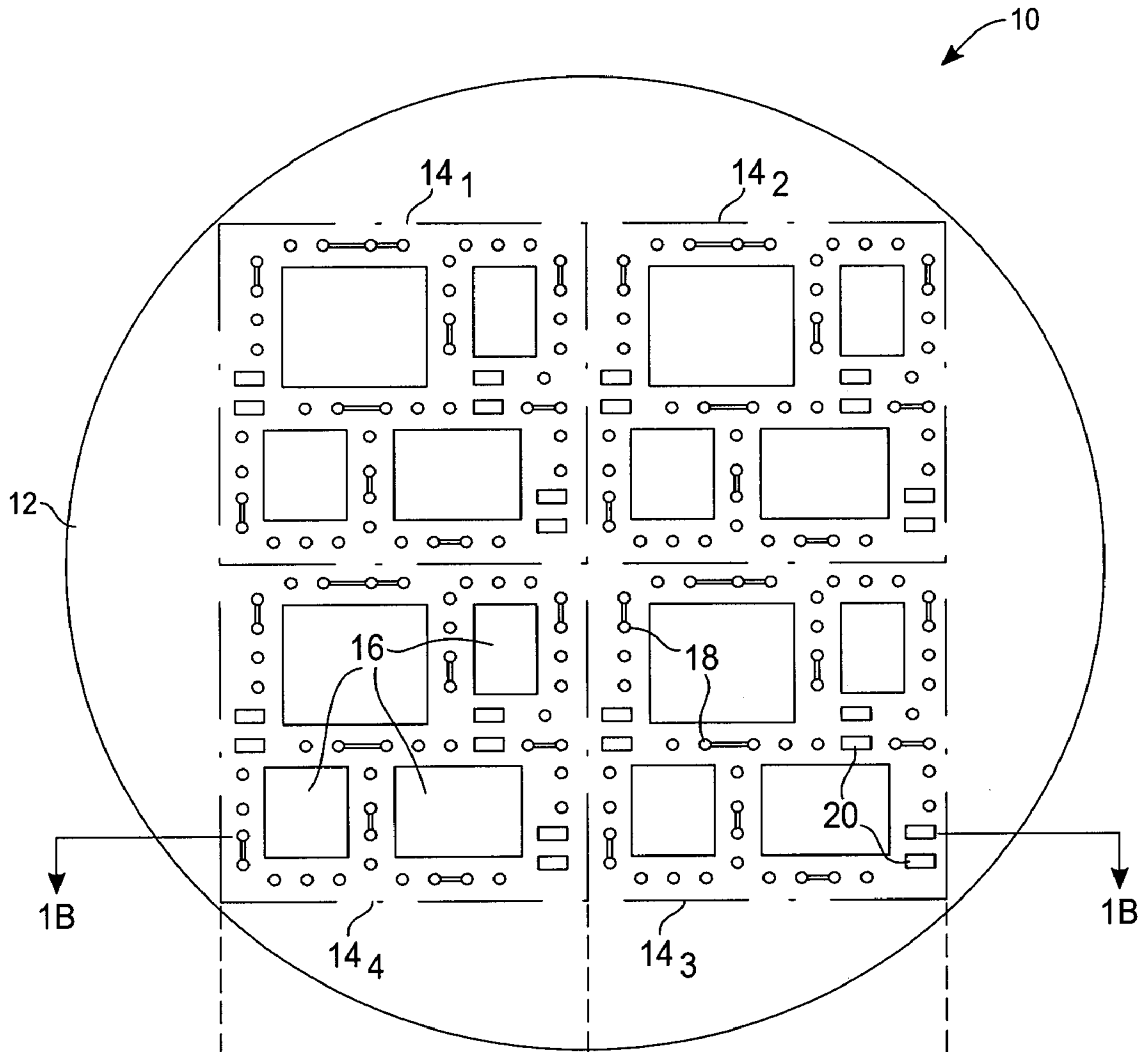

Fig._1A

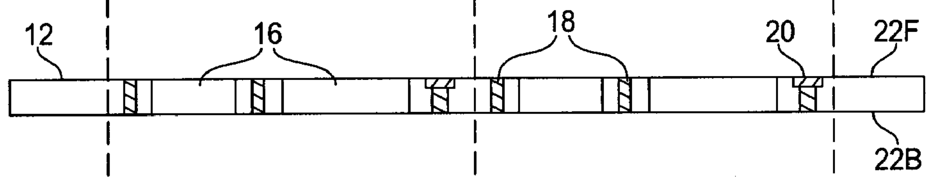

Fig._1B

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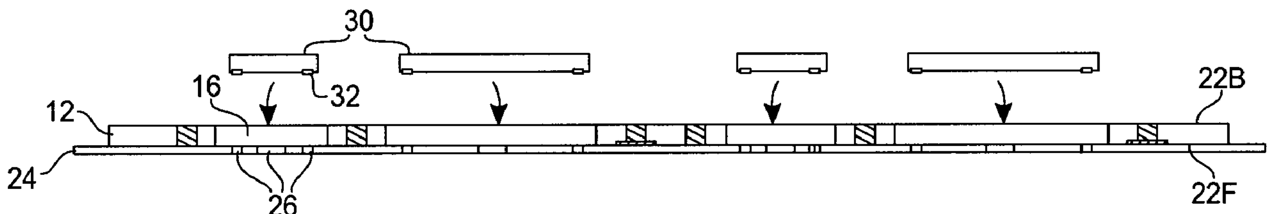

Fig._ 2A

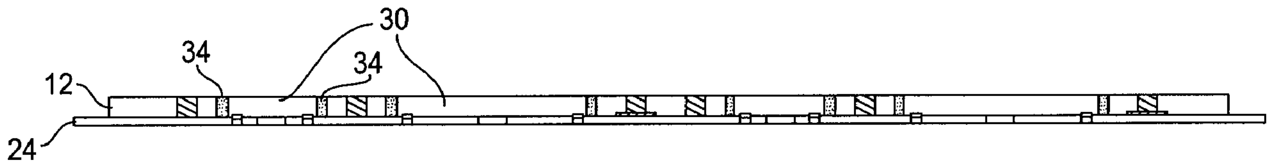

Fig._ 2B

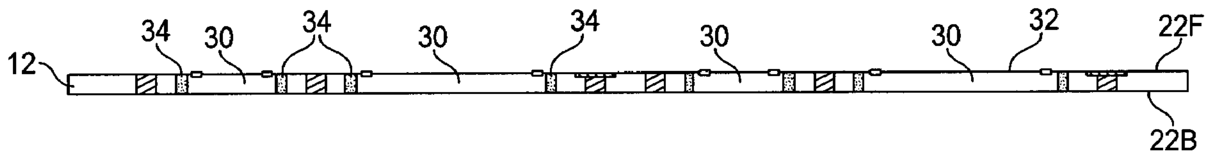

Fig._ 2C

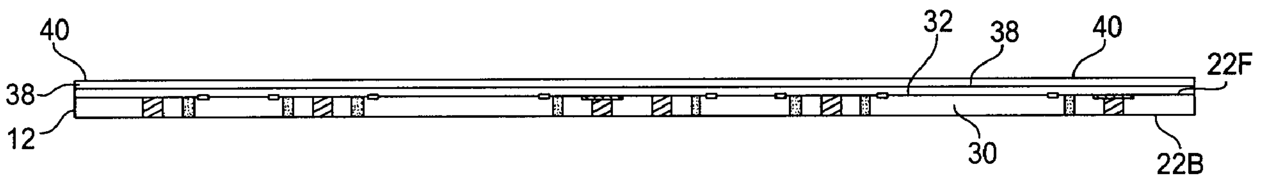

Fig._ 2D

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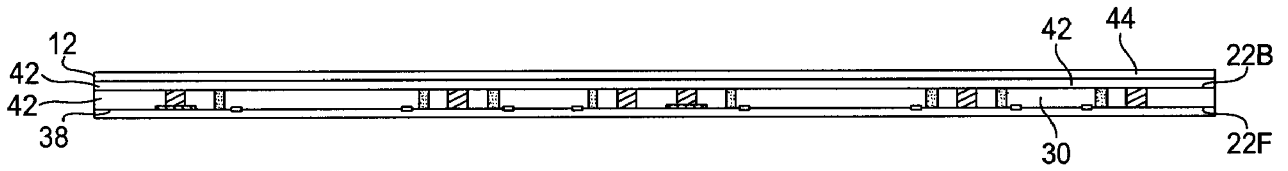

Fig._ 2E

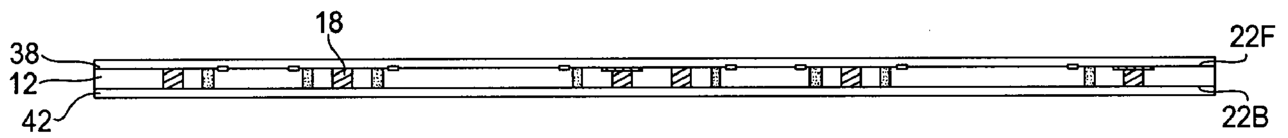

Fig._ 2F

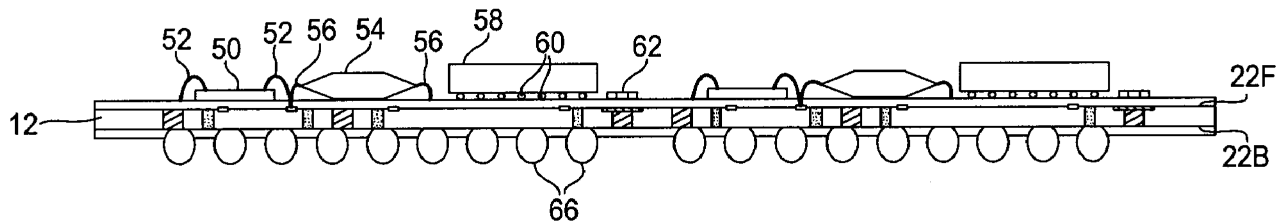

Fig._ 2G

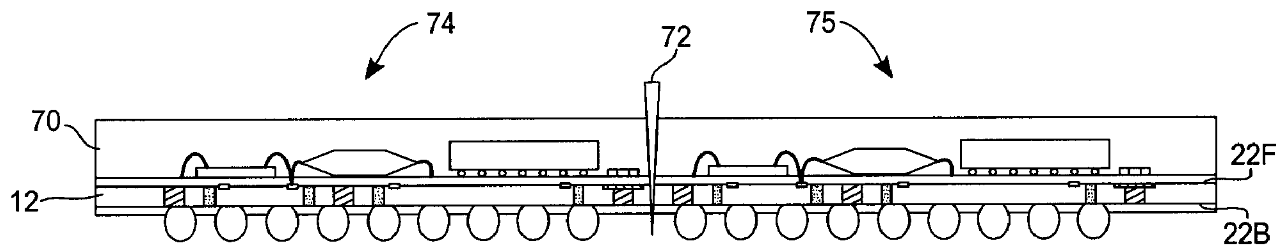

Fig._ 2H