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(54) SPLIT-GATE FLASH MEMORY CELL WITH VARYING INSULATION GATE OXIDES, AND METHOD OF FORMING SAME

FLASH-SPEICHERZELLE MIT GETEILTEM GATE UND VERFAHREN ZUR HERSTELLUNG DERSELBEN

CELLULE DE MÉMOIRE FLASH À GRILLE DIVISÉE, À OXYDES DE GRILLE D'ISOLATION VARIABLES, ET SON PROCÉDÉ DE FORMATION

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EP 3 815 149 B1

Description

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 62/669,263 filed on May 9, 2018, and U.S. Patent Application No. 16/057,750 filed on August 7, 2018.

FIELD OF THE INVENTION

[0002] The present invention relates to split gate non-volatile memory cells

BACKGROUND OF THE INVENTION

[0003] Split gate non-volatile memory cells with three gates are known. See for example U.S. Patent 7,315,056, which discloses split gate memory cells each having source and drain regions in a semiconductor substrate with a channel region extending there between, a floating gate over a first portion of the channel region, a control gate (also called a word line gate) over a second portion of the channel region, and a PIE gate over the source region.

[0004] Fabrication method improvements are needed to better control the formation of various elements of the memory cells.

[0005] Document US 2016/336415 A1 refers to a split-gate flash memory cell. An erase gate and a floating gate are laterally spaced over a semiconductor substrate. The floating gate has a height increasing towards the erase gate, a concave sidewall surface neighboring the erase gate, and a tip defined an interface of the concave sidewall surface and an upper surface of the floating gate. A control gate and a sidewall spacer are arranged over the upper surface of the floating gate. The control gate is laterally offset from the tip of the floating gate, and the sidewall spacer is laterally arranged between the control gate and the tip. A method for manufacturing the split-gate flash memory cell is also provided.

BRIEF SUMMARY OF THE INVENTION

[0006] The present invention is set out in the appended claims.

[0007] A method of forming a memory device according to the invention is presented in claim 1. Embodiments of the invention are presented in the dependent claims.

[0008] Other objects and features of the present invention will become apparent by a review of the specification, claims and appended figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figs. 1-17 are side cross sectional views showing the steps in forming the memory cells.

DETAILED DESCRIPTION OF THE INVENTION

[0010] The present invention is an improved method of forming non-volatile split gate memory cells having three gates per memory cell. While the figures show only a pair of memory cells being formed, it should be appreciated that an array of memory cells are formed during the process. The process begins by forming an silicon dioxide layer (oxide) 12 on the upper surface of a semiconductor substrate 10, and a polysilicon layer (poly) 14 on the oxide layer 12, as shown in Fig. 1. To dope the poly, a poly implant can be performed at this time. A silicon nitride layer (nitride) 16 is formed as a hard mask on the poly layer 12, as shown in Fig. 2. Photo resist 18 is formed over the structure and patterned using a photolithography process (i.e., photo resist formation, selective exposure of the photo resist, removal of selective portions of the photoresist leaving portions of the underlying material exposed). Here, portions of the nitride layer 16 are left exposed. A nitride etch is then used to remove the exposed portions of the nitride layer 16 not protected by the patterned photoresist 18, leaving a block of the nitride 16 on the poly layer 14. A polysilicon sloped etch is then used to etch the upper surface of poly layer 14, creating a sloped upper surface for the poly layer where the upper surface slopes upwardly as it approaches the block of nitride 16. To control the floating gate threshold voltage, an implantation is then performed on the exposed portions of the poly layer 14, as shown in Fig. 3.

[0011] After photo resist removal, oxide spacers 20 are formed on the poly layer 14. Formation of spacers is well known, and involves the deposition of material followed by an anisotropic etch of the material, whereby the material is removed except for portions thereof abutting vertically oriented structures. The upper surface of the spacer is typically rounded. In this case, oxide is deposited, followed by an anisotropic oxide etch leaving oxide spacers 20 abutting the side walls of nitride block 16, as shown in Fig. 4. A poly etch is performed to remove the portions of the poly layer 14 not protected by the oxide spacers 20, as shown in Fig. 5. To control the word line threshold voltage, an implant into the portions of the substrate also not protected by the nitride block 16 and oxide spacers 20 can be performed at this time (using oxide layer 12 on the substrate surface as a buffer layer). An oxide spacer 22 is formed on the exposed ends of the poly layer 14 to form the main isolation between poly 14 and the word line gate to be formed later by performing oxide deposition (e.g., high temperature oxide HTO deposition), and an anisotropic oxide etch, which leaves oxide spacer 22 on the ends (along the side surfaces) of the poly layer 14, as shown in Fig. 6. Another oxide layer 24 is then deposited on the structure (as the main portion of the gate oxide for high-voltage peripheral devices to be formed later), for example by high temperature oxide deposition, as shown in Fig. 7.

[0012] The structure is covered with photoresist 26, which is patterned to remove the portion of the photore-

sist over the nitride block 16. Oxide, nitride and poly etches are performed to remove oxide layer 24 on the nitride block 16, the nitride block 16, and the portion of the poly layer 14 exposed by the removal of the nitride block 16, leaving poly blocks 14a having an upwardly sloping upper surface that terminates in a sharp edge 14b. An implant process follows for forming the source region 28 in the substrate 10 between the oxide spacers 20 and poly blocks 14a (i.e., the source region is formed under a gap that exists between the oxide spacers 20 and a gap that exists between the poly blocks 14a). The resulting structure is shown in Fig. 8.

[0013] A tunnel oxide layer 30 is then formed on the exposed ends of the poly blocks 14a including the sharp edges 14b, as shown in Fig. 9. Specifically, the tunnel oxide layer 30 is formed by first performing an oxide etch (e.g., wet etch) to laterally recess the sidewall of each spacer 20 away from the respective ends of the poly blocks 14a, exposing the sharp edges 14b. The tunnel oxide layer 30 is then formed by high temperature oxide HTO deposition. The tunnel oxide layer 30 extends along the exposed sidewalls of poly layer blocks 14a, and wraps around the sharp edges 14b. However, the HTO deposition does not consume the polysilicon sharp edges 14b, thus maintaining their shape.

[0014] A wet oxidation is then used to thicken the oxide 32 over the source region 28 and the tunnel oxide layer 30 wrapping around the sharp edges 14b, as shown in Fig. 10. Photoresist 34 is then formed between the oxide spacers 20, and an oxide etch is used to remove the oxide layer on the substrate outside of the pair of spacers, leaving the substrate surface exposed, as shown in Fig. 11. Then, a thin oxide layer (WL oxide) 36 is formed on the substrate outside of the pair of spacers, as shown in Fig. 12 (after photo resist removal).

[0015] A layer of polysilicon 38 is then formed over the structure. This poly layer can be used in the logic areas of the same substrate. If it desirous for the poly layer thickness to be thicker in the memory array than the logic area, a cap oxide layer can be formed on the poly layer 38 and patterned to remove the cap oxide layer from the memory area of the device, followed by the deposition of additional polysilicon to thicken the poly layer 38 in the memory area. The additional polysilicon on the cap oxide layer in the logic area will later be removed by a poly CMP described below. The resulting structure is shown in Fig. 13.

[0016] The structure is then planarized by a poly CMP (chemical mechanical polish) to below the tops of the oxide spacers 20. The poly layer 38 can be doped by implantation with material and annealed at this time. The resulting structure is shown in Fig. 14. Photoresist 40 is formed on the structure and patterned leaving only those portions of the poly layer 38 between the oxide spacers 20 and immediately outside of the oxide spacers 20 covered by the photo resist 40. A poly etch is then used to remove the exposed portions of the poly layer 38 not protected by the photo resist 40, leaving blocks 38a of the poly layer 38 adjacent to the outsides of the oxide spacers 20, and a block 38b of the poly layer 38 between the oxide spacers 20. The resulting structure is shown in Fig. 15.

[0017] An implantation is then performed to form drain regions 42 in the substrate adjacent the poly blocks 38a. Spacers 44 of insulation material are then formed on the outsides of poly blocks 38a. Preferably, these spacers are formed by forming one or more insulation layers (e.g., oxide, nitride, oxide) followed by one or more anisotropic etches, as shown in Fig. 16. An additional implant and anneal can then be used to further enhance the drain regions 42. Salicide 46 is then formed on the exposed upper surfaces of the poly blocks 38a and 38b, for improved conductivity. ILD insulation is then formed over the structure, which preferably includes insulation material 48a formed over insulation layers 48b. Contact holes are then formed through the ILD insulation, exposing the drain regions 42. Conductive material is then formed on the structure and patterned, filling the contact holes, to form a bit line 50 extending over the ILD insulation 48, and contacts 52 extending between and providing electrical conduction between the bit line 50 and the drain regions 42. The final structure is shown in Fig. 17.

[0018] As shown in Fig. 17, the process forms pairs of memory cells. Each memory cell pair includes a source region 28 and two drain regions 42, with two channel regions 54 each extending between the source region 28 and one of the drain regions 42. An erase gate 38b is disposed over and insulated from the source region 28 by the thick oxide layer 32. Each memory cell includes a floating gate 14a disposed over and insulated from a first portion of the channel region 54, and a word line gate 38a disposed over and insulated from a second portion of the channel region 54. The floating gate 14a has a sharp tip 14b (caused by the sloping surface) that faces a notch 56 formed in the erase gate 38b, whereby the erase gate 38b wraps around the sharp tip 14b of the floating gate 14a. The sharp tip 14b is insulated from the erase gate 38b by the tunnel oxide layer 30. The word line gates 38a are insulated from the substrate by an oxide layer 36 that is thinner than the oxide 12 between the floating gate 14a and the substrate 10, which is thinner than the oxide 32 between the erase gate 38b and the source region 28. The oxide layer 36 under the word line gate 38a and the tunnel oxide 30 are formed separately, and therefore can be separately adjusted in terms of thickness for optimal performance.

[0019] The cell size can be scaled down by shortening the portion of the channel region 54 under the word line gate 38a (i.e., making the length of word line gate 38a in the direction of the channel region shorter), and thinning the oxide layer 36 under the word line gate 38a (which can be done independently relative to other insulation layers such as the tunnel oxide that can remain thicker) which allows for a higher current drive for the memory cell. The erase gate 38b and word line gates 38a are formed by the same poly deposition, so only two poly

depositions are needed to form the floating gates 14a, the word line gates 38a and the erase gates 38b for all the memory cells. The length of each word line gate 38a (in the direction of the channel region) is determined by photolithography for better dimension control. The height of the word line gates 38a and erase gate 38b are determine by chemical mechanical polish, which avoids defect issues that could exist should the word line gates instead be made by a poly spacer technique. The isolation (oxide) between the floating gate 14a and word line gate 38a can be independently optimized, because that oxide is originally formed as oxide 22 which is then thickened by subsequent processing. Finally, the tunnel oxide 30 is formed as a single layer wrapping around the sharp tip of the floating gate, and thickened by a subsequent wet oxidation process. Using the above method, erase efficiency and word line gate performance can be independently optimized.

[0020] It is to be understood that the present invention is not limited to the embodiment(s) described above and illustrated herein, but encompasses any and all variations falling within the scope of any claims. Materials, processes and numerical examples described above are exemplary only, and should not be deemed to limit the claims. Further, not all method steps need be performed in the exact order illustrated or claimed, but rather in any order that allows the proper formation of the non-volatile memory cells of the present invention. Single layers of material could be formed as multiple layers of such or similar materials, and vice versa. Lastly, the terms "forming" and "formed" as used herein shall include material deposition, material growth, or any other technique in providing the material as disclosed or claimed.

[0021] It should be noted that, as used herein, the terms "over" and "on" both inclusively include "directly on" (no intermediate materials, elements or space disposed there between) and "indirectly on" (intermediate materials, elements or space disposed there between). Likewise, the term "adjacent" includes "directly adjacent" (no intermediate materials, elements or space disposed there between) and "indirectly adjacent" (intermediate materials, elements or space disposed there between), "mounted to" includes "directly mounted to" (no intermediate materials, elements or space disposed there between) and "indirectly mounted to" (intermediate materials, elements or spaced disposed there between), and "electrically coupled" includes "directly electrically coupled to" (no intermediate materials or elements there between that electrically connect the elements together) and "indirectly electrically coupled to" (intermediate materials or elements there between that electrically connect the elements together). For example, forming an element "over a substrate" can include forming the element directly on the substrate with no intermediate materials/elements there between, as well as forming the element indirectly on the substrate with one or more intermediate materials/elements there between.

Claims

1. A method of forming a memory device, comprising:

forming a first insulation layer (12) having a first thickness on a semiconductor substrate (10);
forming a first polysilicon layer (14) on the first insulation layer;
forming first and second spaced apart insulation spacers (20) directly on the first polysilicon layer;
removing portions of the first polysilicon layer such that a first block of the first polysilicon layer (14a) remains under the first insulation spacer and a second block of the first polysilicon layer (14a) remains under the second insulation spacer, wherein each of the first and second blocks of the first polysilicon layer include opposing first and second side surfaces, the first side surfaces face toward each other and the second side surfaces face away from each other, and each of the first and second blocks of the first polysilicon layer has a sloping upper surface that terminates in a sharp edge (14b);
forming oxide spacers (22) on the second side surfaces of the first and second blocks of the first polysilicon layer;
thickening the oxide spacers;
forming a source region (28) in the substrate that is disposed under a gap between the first and second blocks of the first polysilicon layer;
forming a tunnel oxide layer (30) on the sharp edges and the first side surfaces of the first and second block of the first polysilicon layer;
forming a second insulation layer (32) having a second thickness on the semiconductor substrate over the source region, wherein the forming of the second insulation layer includes thickening the tunnel oxide layer;
forming a third insulation layer (36) having a third thickness directly on portions of the semiconductor substrate adjacent the second side surfaces of the first and second blocks of the first polysilicon layer;
forming a second polysilicon layer (38) over the substrate and the first and second insulation spacers;
removing portions of the second polysilicon layer using a chemical mechanical polish that also removes top portions of the insulation spacers such that a first block of the second polysilicon layer (38b) remains that is disposed on the second insulation layer and between the first and second insulation spacers, and second and third blocks of the second polysilicon layer (38a) remain that are disposed on the third insulation layer such that the second and third blocks of the second polysilicon layer are insulated from the substrate only by the third insulation layer,

wherein the first insulation spacer is disposed between the first and second blocks of the second polysilicon layer and wherein the second insulation spacer is disposed between the first and third blocks of the second polysilicon layer;
forming a first drain region (42) in the substrate adjacent the second block of the second polysilicon layer; and
forming a second drain region (42) in the substrate adjacent the third block of the second polysilicon layer;
wherein the first block of the second polysilicon layer includes a first notch (56) that wraps around and is insulated from the sharp edge of the first block of the first polysilicon layer and a second notch (56) that wraps around and is insulated from the sharp edge of the second block of the first polysilicon layer;
wherein the second thickness is greater than the first thickness, and wherein the first thickness is greater than the third thickness.

2. The method of claim 1, further comprising:
forming salicide (46) on upper surfaces of the first, second and third blocks of the second polysilicon layer.

3. The method of claim 1, wherein the forming of the first and second insulation spacers includes:

forming a block of nitride (16) on the first polysilicon layer;
forming oxide on the block of nitride and on the first polysilicon layer;
performing an oxide etch to remove portions of the oxide except for the first and second insulation spacers of the oxide abutting side surfaces of the block of nitride; and
removing the block of nitride.

4. The method of claim 1, wherein the sloping upper surfaces of the first and second blocks of the first polysilicon layer are formed by:

forming a block of nitride (16) on the first polysilicon layer;
performing a poly etch on the upper surface of the first polysilicon layer so that the upper surface of the first polysilicon layer slopes upwardly as it approaches sidewalls of the block of nitride.

5. The method of claim 1, wherein the removing of the portions of the second polysilicon layer includes a photolithographic etch of the second polysilicon layer.

6. The method of claim 1, wherein:

the first insulation layer is oxide;
the second insulation layer is oxide; and
the third insulation layer is oxide.

7. The method of claim 1, wherein:

the first and second notches of the first block of the second polysilicon layer are insulated from the first and second blocks of the first polysilicon layer, respectively, by the tunnel oxide layer having a fourth thickness; and
the third thickness is less than the fourth thickness.

Patentansprüche

1. Verfahren zum Ausbilden einer Speichervorrichtung, umfassend:

Ausbilden einer ersten Isolationsschicht (12), die eine erste Dicke aufweist, auf einem Halbleitersubstrat (10);
Ausbilden der ersten Polysiliziumschicht (14) auf der ersten Isolationsschicht;
Ausbilden eines ersten und eines zweiten voneinander beabstandeten Isolationsabstandshalters (20) direkt auf der ersten Polysiliziumschicht;
Entfernen von Abschnitten der ersten Polysiliziumschicht, derart, dass ein erster Block der ersten Polysiliziumschicht (14a) unter dem ersten Isolationsabstandshalter verbleibt und ein zweiter Block der ersten Polysiliziumschicht (14a) unter dem zweiten Isolationsabstandshalter verbleibt, wobei jeder des ersten und des zweiten Blocks der ersten Polysiliziumschicht sich gegenüberliegende erste und zweite Seitenoberflächen einschließt, wobei die ersten Seitenoberflächen einander zugewandt sind und die zweiten Seitenoberflächen voneinander abgewandt sind, und jeder des ersten und des zweiten Blocks der ersten Polysiliziumschicht eine geneigte obere Oberfläche aufweist, die in einer scharfen Kante (14b) endet;
Ausbilden von Oxidabstandshaltern (22) auf den zweiten Seitenoberflächen des ersten und des zweiten Blocks der ersten Polysiliziumschicht;
Verdickung der Oxidabstandshalter;
Ausbilden einer Quellregion (28) in dem Substrat, die unter einer Lücke zwischen dem ersten und dem zweiten Block der ersten Polysiliziumschicht angeordnet ist;
Ausbilden einer Tunneloxidschicht (30) auf den scharfen Kanten und den ersten Seitenoberflächen des ersten und zweiten Blocks der ersten Polysiliziumschicht;

Ausbilden einer zweiten Isolationsschicht (32), die eine zweite Dicke aufweist, auf dem Halbleitersubstrat über der Quellregion, wobei das Ausbilden der zweiten Isolationsschicht eine Verdicken der Tunneloxidschicht einschließt;
Ausbilden einer dritten Isolationsschicht (36), die eine dritte Dicke aufweist, direkt auf Abschnitten des Halbleitersubstrats angrenzend an die zweiten Seitenoberflächen des ersten und des zweiten Blocks der ersten Polysiliziumschicht;
Ausbilden einer zweiten Polysiliziumschicht (38) über dem Substrat und dem ersten und dem zweiten Isolationsabstandshalter;
Entfernen von Abschnitten der zweiten Polysiliziumschicht unter Verwendung einer chemischen mechanischen Politur, die ebenso obere Abschnitte der Isolierabstandshalter derart entfernt, dass ein erster Block der zweiten Polysiliziumschicht (38b) verbleibt, der auf der zweiten Isolationsschicht und zwischen dem ersten und dem zweiten Isolationsabstandshalter angeordnet ist, und ein zweiter und ein dritter Block der zweiten Polysiliziumschicht (38a) verbleiben, die auf der dritten Isolationsschicht derart angeordnet sind, dass der zweite und der dritte Block der zweiten Polysiliziumschicht nur durch die dritte Isolationsschicht von dem Substrat isoliert sind, wobei der erste Isolationsabstandshalter zwischen dem ersten und dem zweiten Block der zweiten Polysiliziumschicht angeordnet ist, und wobei der zweite Isolationsabstandshalter zwischen dem ersten und dem dritten Block der zweiten Polysiliziumschicht angeordnet ist;
Ausbilden einer ersten Drain-Region (42) in dem Substrat und angrenzend an den zweiten Block der zweiten Polysiliziumschicht; und
Ausbilden einer zweiten Drain-Region (42) in dem Substrat und angrenzend an den dritten Block der zweiten Polysiliziumschicht;
wobei der erste Block der zweiten Polysiliziumschicht eine erste Kerbe (56) einschließt, die sich darum schlingt und von der scharfen Kante des ersten Blocks der ersten Polysiliziumschicht isoliert ist, und eine zweite Kerbe (56), die sich darum schlingt und von der scharfen Kante des zweiten Blocks der ersten Polysiliziumschicht isoliert ist;
wobei die zweite Dicke größer als die erste Dicke ist, und wobei die erste Dicke größer als die dritte Dicke ist.

2. Verfahren nach Anspruch 1, ferner umfassend:
Ausbilden von Salicide (46) auf den oberen Oberflächen des ersten, des zweiten und des dritten Blocks der zweiten Polysiliziumschicht.

3. Verfahren nach Anspruch 1, wobei das Ausbilden des ersten und des zweiten Isolationsabstandshalter einschließt:

Ausbilden eines Nitridblocks (16) auf der ersten Polysiliziumschicht;
Ausbilden von Oxid auf dem Nitridblock und auf der ersten Polysiliziumschicht;
Durchführen einer Oxidätzung, um Abschnitte des Oxids zu entfernen, außer für den ersten und den zweiten Isolationsabstandshalter der Oxidanstoßseitenoberflächen des Nitridblocks; und
Entfernen des Nitridblocks.

4. Verfahren nach Anspruch 1, wobei die geneigten oberen Oberflächen des ersten und des zweiten Blocks der ersten Polysiliziumschicht ausgebildet werden durch:

Ausbilden eines Nitridblocks (16) auf der ersten Polysiliziumschicht;
Durchführen eines Polyätzung auf der oberen Oberfläche der ersten Polysiliziumschicht, derart, dass die obere Oberfläche der ersten Polysiliziumschicht nach oben geneigt ist, wenn sie sich an den Seitenwänden des Nitridblocks annähert.

5. Verfahren nach Anspruch 1, wobei das Entfernen der Abschnitte der zweiten Polysiliziumschicht eine fotolithografische Ätzung der zweiten Polysiliziumschicht einschließt.

6. Verfahren nach Anspruch 1, wobei:

die erste Isolationsschicht Oxid ist;
die zweite Isolationsschicht Oxid ist; und
die dritte Isolationsschicht Oxid ist.

7. Verfahren nach Anspruch 1, wobei:

die erster und zweite Kerbe des ersten Blocks der zweiten Polysiliziumschicht durch die Tunneloxidschicht, die eine vierte Dicke aufweist, von dem ersten und dem zweiten Block der ersten Polysiliziumschicht isoliert sind; und
die dritte Dicke geringer als die vierte Dicke ist.

Revendications

1. Procédé de formation d'un dispositif de mémoire, comprenant :

la formation d'une première couche isolante (12) ayant une première épaisseur sur un substrat semi-conducteur (10) ;
la formation d'une première couche de silicium

polycristallin (14) sur la première couche isolante ;
la formation de premier et second éléments d'espacement d'isolation espacés (20) directement sur la première couche de silicium polycristallin ;
l'élimination de parties de la première couche de silicium polycristallin de sorte qu'un premier bloc de la première couche de silicium polycristallin (14a) demeure sous le premier élément d'espacement isolant et un second bloc de la première couche de silicium polycristallin (14a) demeure sous le second élément d'espacement isolant, dans lequel chacun des premier et second blocs de la première couche de silicium polycristallin comporte des premières et secondes surfaces latérales opposées, les premières surfaces latérales sont orientées l'une vers l'autre et les secondes surfaces latérales sont orientées à l'écart l'une de l'autre, et chacun des premier et second blocs de la première couche de silicium polycristallin a une surface supérieure inclinée qui se termine en un bord effilé (14b) ;
la formation d'éléments d'espacement en oxyde (22) sur les secondes surfaces latérales des premier et second blocs de la première couche de silicium polycristallin ;
l'épaississement des éléments d'espacement en oxyde ;
la formation d'une région de source (28) dans le substrat laquelle est disposée sous un espace entre les premier et second blocs de la première couche de silicium polycristallin ;
la formation d'une couche d'oxyde tunnel (30) sur les bords effilés et les premières surfaces latérales des premier et second blocs de la première couche de silicium polycristallin ;
la formation d'une deuxième couche isolante (32) ayant une deuxième épaisseur sur le substrat semi-conducteur par-dessus la région de source, la formation de la deuxième couche isolante comportant un épaississement de la couche d'oxyde tunnel ;
la formation d'une troisième couche isolante (36) ayant une troisième épaisseur directement sur des parties du substrat semi-conducteur adjacentes aux secondes surfaces latérales des premier et second blocs de la première couche de silicium polycristallin ;
la formation d'une seconde couche de silicium polycristallin (38) par-dessus le substrat et les premier et second éléments d'espacement isolants ;
l'élimination de parties de la seconde couche de silicium polycristallin à l'aide d'un polissage chimico-mécanique qui élimine également des parties supérieures des éléments d'espacement isolants de sorte que demeure un premier bloc de la seconde couche de silicium polycristallin (38b) qui est disposé sur la deuxième couche isolante et entre les premier et second éléments d'espacement isolant, et demeurent des deuxième et troisième blocs de la seconde couche de silicium polycristallin (38a) qui sont disposés sur la troisième couche isolante de sorte que les deuxième et troisième blocs de la seconde couche de silicium polycristallin sont isolés du substrat uniquement par la troisième couche isolante, dans lequel le premier élément d'espacement isolant est disposé entre les premier et deuxième blocs de la seconde couche de silicium polycristallin et dans lequel le second élément d'espacement isolant est disposé entre les premier et troisième blocs de la seconde couche de silicium polycristallin ;
la formation d'une première région de drain (42) dans le substrat, adjacente au deuxième bloc de la seconde couche de silicium polycristallin ; et
la formation d'une seconde région de drain (42) dans le substrat, adjacente au troisième bloc de la seconde couche de silicium polycristallin ;
dans lequel le premier bloc de la seconde couche de silicium polycristallin comporte une première encoche (56) qui enveloppe le, et est isolée du, bord effilé du premier bloc de la première couche de silicium polycristallin et une seconde encoche (56) qui enveloppe le, et est isolée du, bord effilé du second bloc de la première couche de silicium polycristallin ;
dans lequel la deuxième épaisseur est supérieure à la première épaisseur, et dans lequel la première épaisseur est supérieure à la troisième épaisseur.

2. Procédé selon la revendication 1, comprenant en outre :
la formation de saliciure (46) sur des surfaces supérieures des premier, deuxième et troisième blocs de la seconde couche de silicium polycristallin.

3. Procédé selon la revendication 1, dans lequel la formation des premier et second éléments d'espacement isolants comporte :

la formation d'un bloc de nitrure (16) sur la première couche de silicium polycristallin ;
la formation d'oxyde sur le bloc de nitrure et sur la première couche de silicium polycristallin ;
la mise en oeuvre d'une gravure d'oxyde pour éliminer des parties de l'oxyde à l'exception des premier et second éléments d'espacement isolants des surfaces latérales en contact avec l'oxyde, du bloc de nitrure ; et
l'élimination du bloc de nitrure.

4. Procédé selon la revendication 1, dans lequel les surfaces supérieures inclinées des premier et second blocs de la première couche de silicium polycristallin sont formées par :

la formation d'un bloc de nitrure (16) sur la première couche de silicium polycristallin ;
la mise en oeuvre d'une poly-gravure sur la surface supérieure de la première couche de silicium polycristallin de sorte que la surface supérieure de la première couche de silicium polycristallin s'incline vers le haut à mesure qu'elle se rapproche des parois latérales du bloc de nitrure.

5. Procédé selon la revendication 1, dans lequel l'élimination des parties de la seconde couche de silicium polycristallin comporte une gravure photolithographique de la seconde couche de silicium polycristallin.

6. Procédé selon la revendication 1, dans lequel :

la première couche isolante est un oxyde ;
la deuxième couche isolante est un oxyde ; et
la troisième couche isolante est un oxyde.

7. Procédé selon la revendication 1, dans lequel :

les première et seconde encoches du premier bloc de la seconde couche de silicium polycristallin sont isolées des premier et second blocs de la première couche de silicium polycristallin, respectivement, par la couche d'oxyde tunnel ayant une quatrième épaisseur ; et
la troisième épaisseur est inférieure à la quatrième épaisseur.

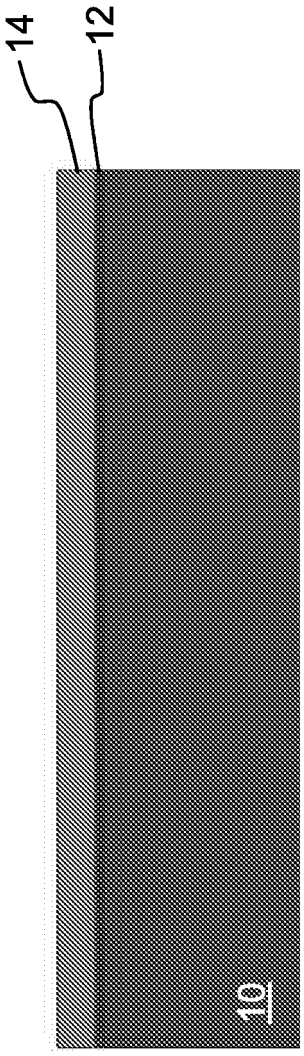


Figure 1

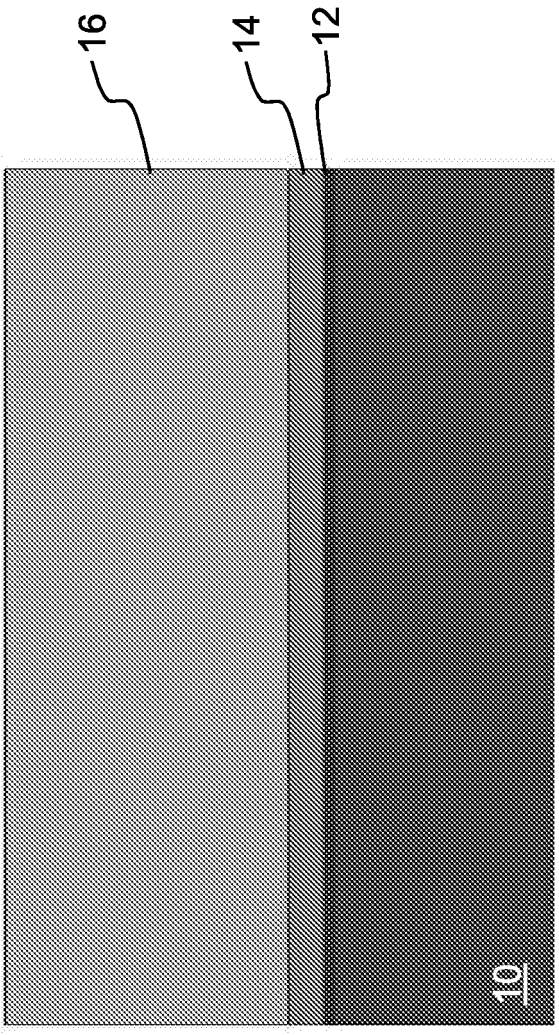
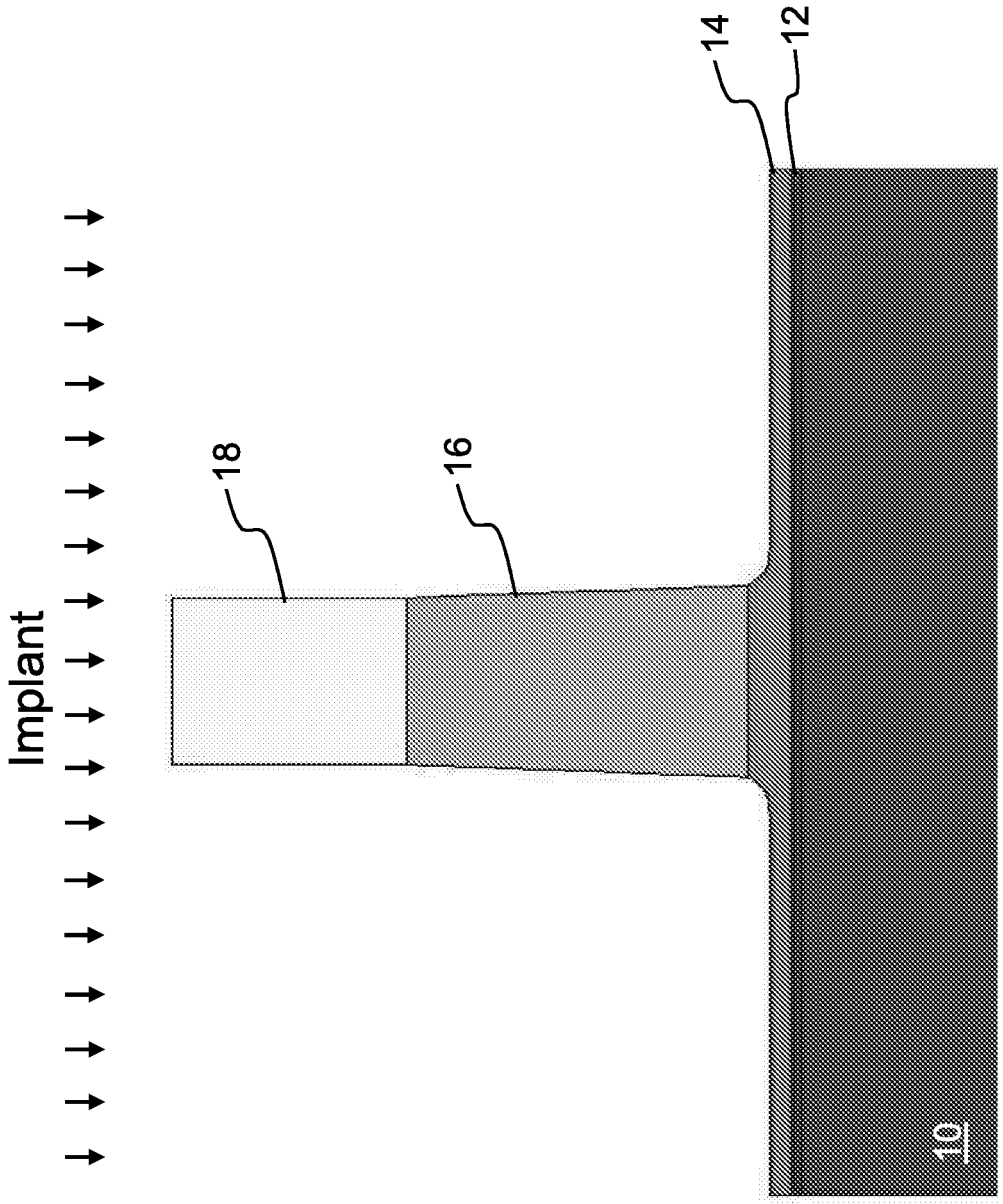


Figure 2



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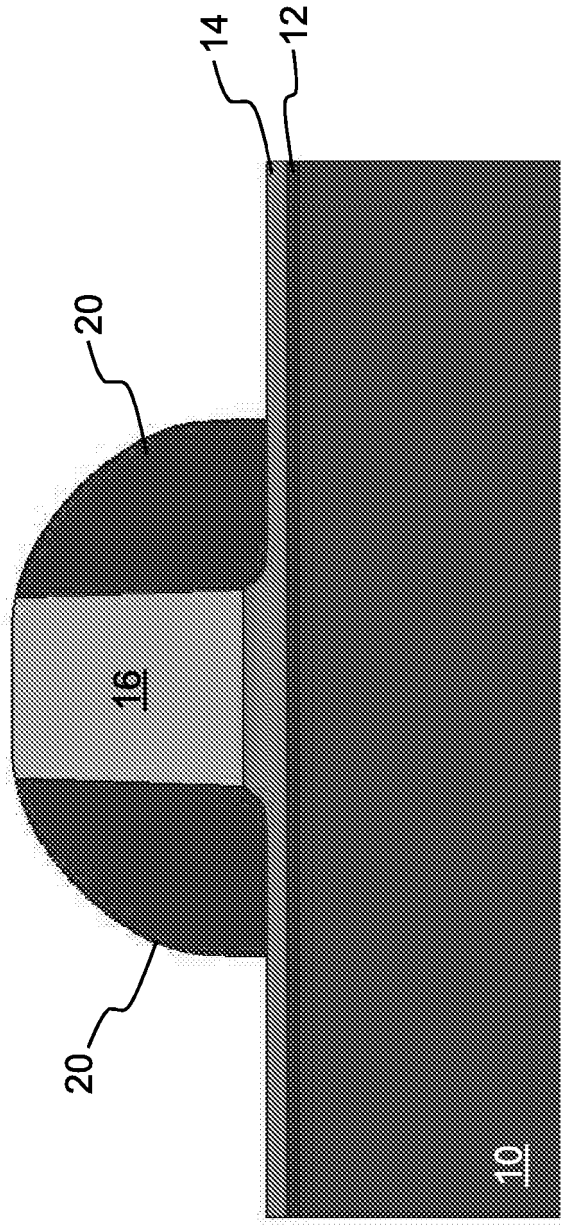

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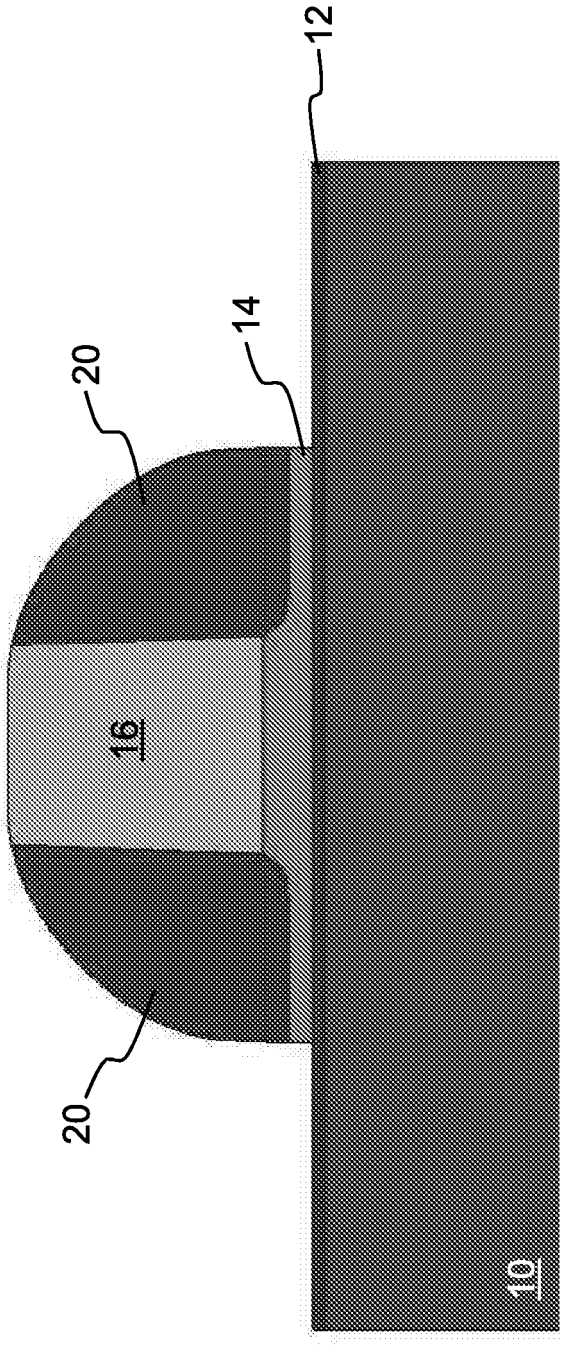

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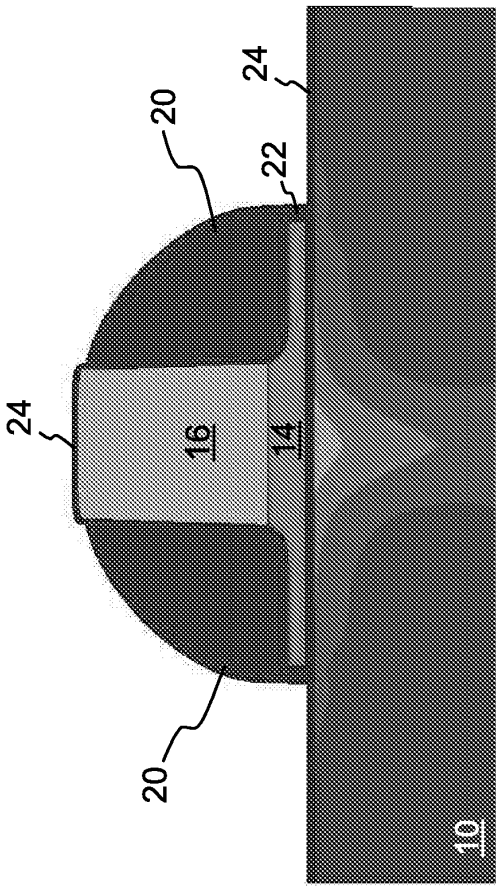

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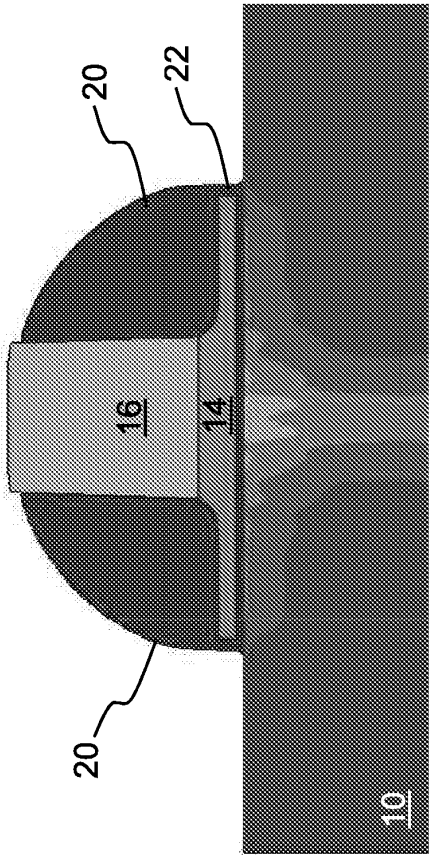

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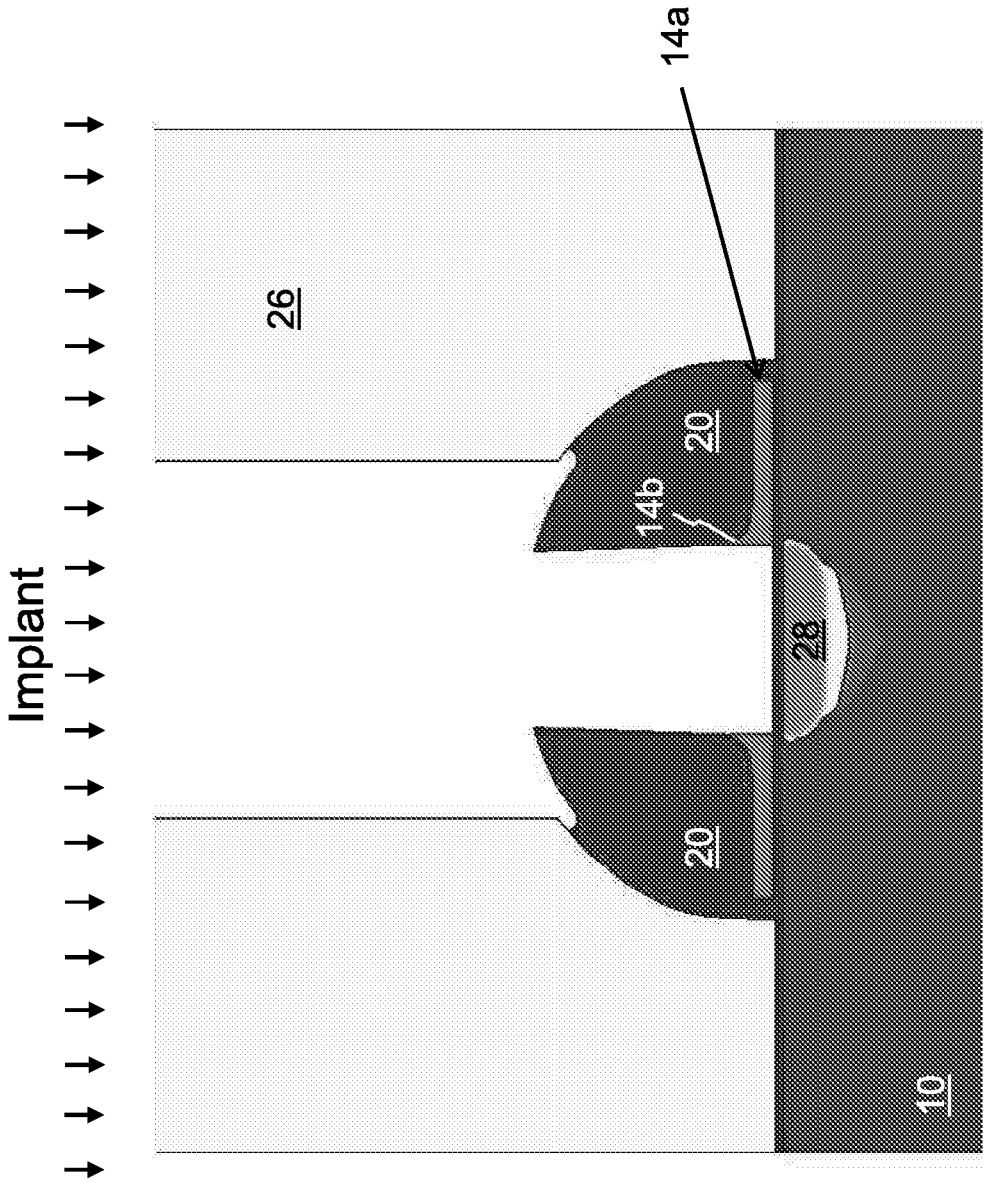

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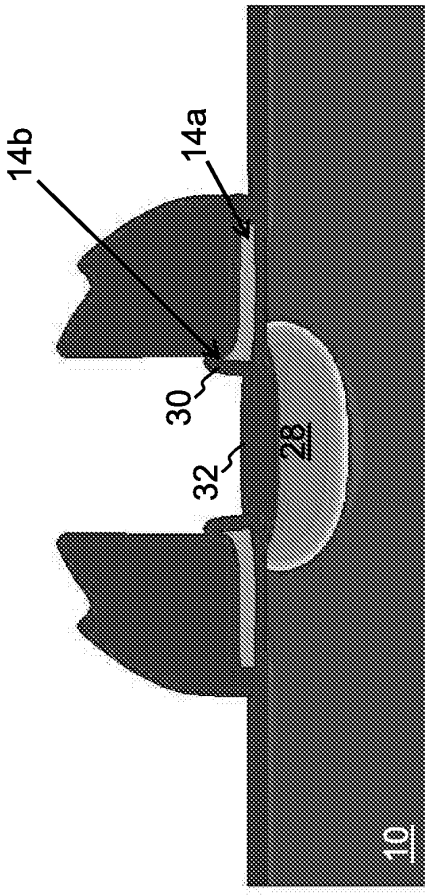

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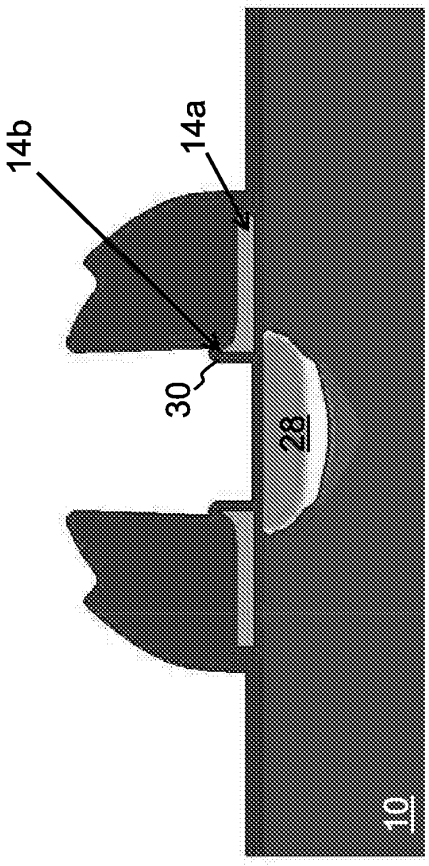

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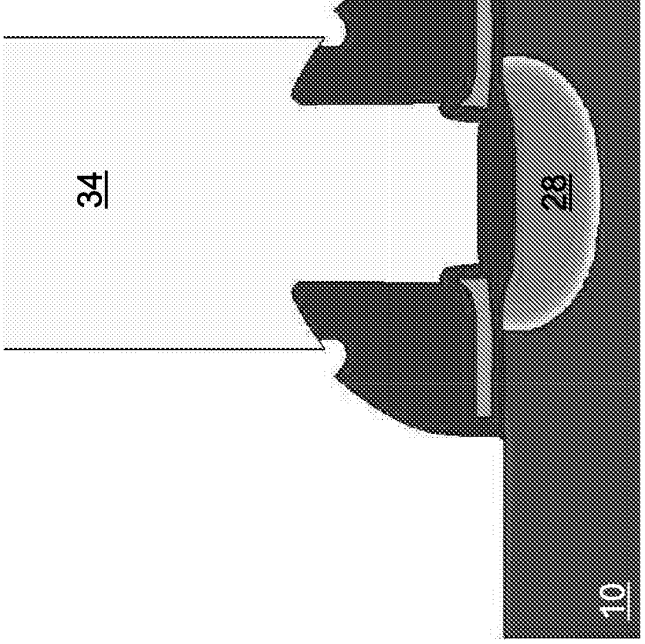

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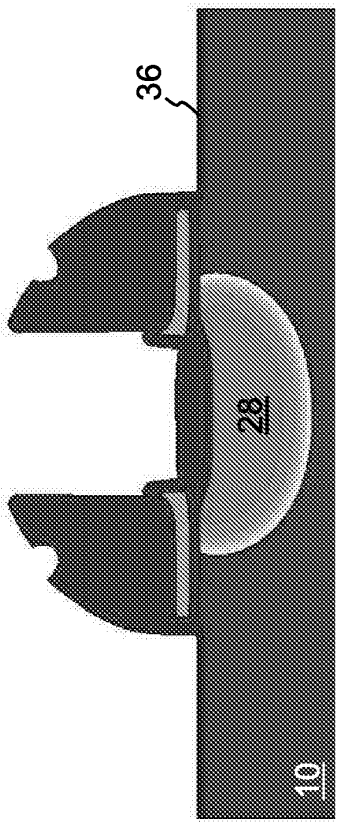
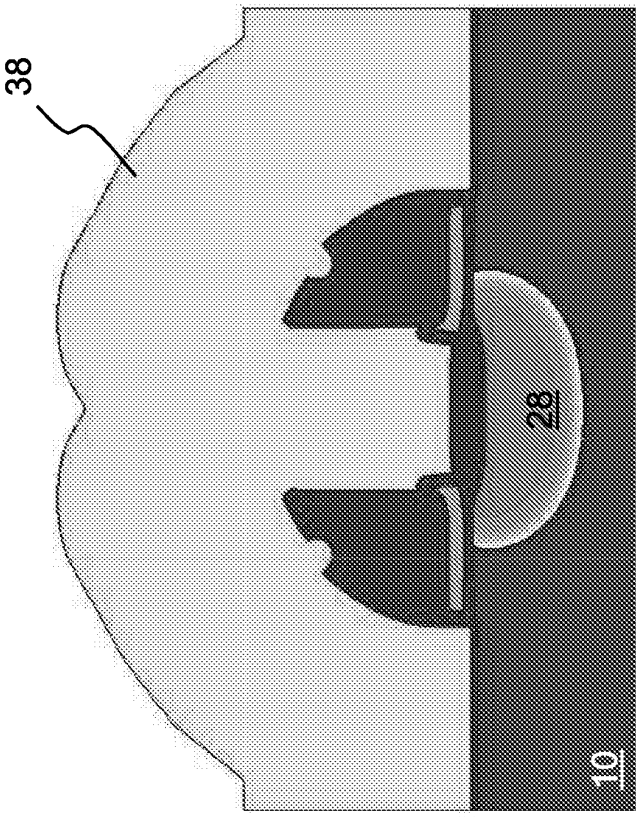


Figure 12



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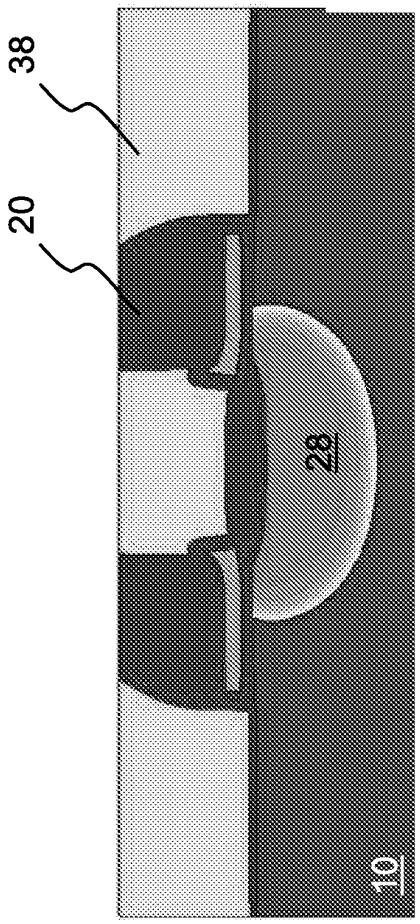

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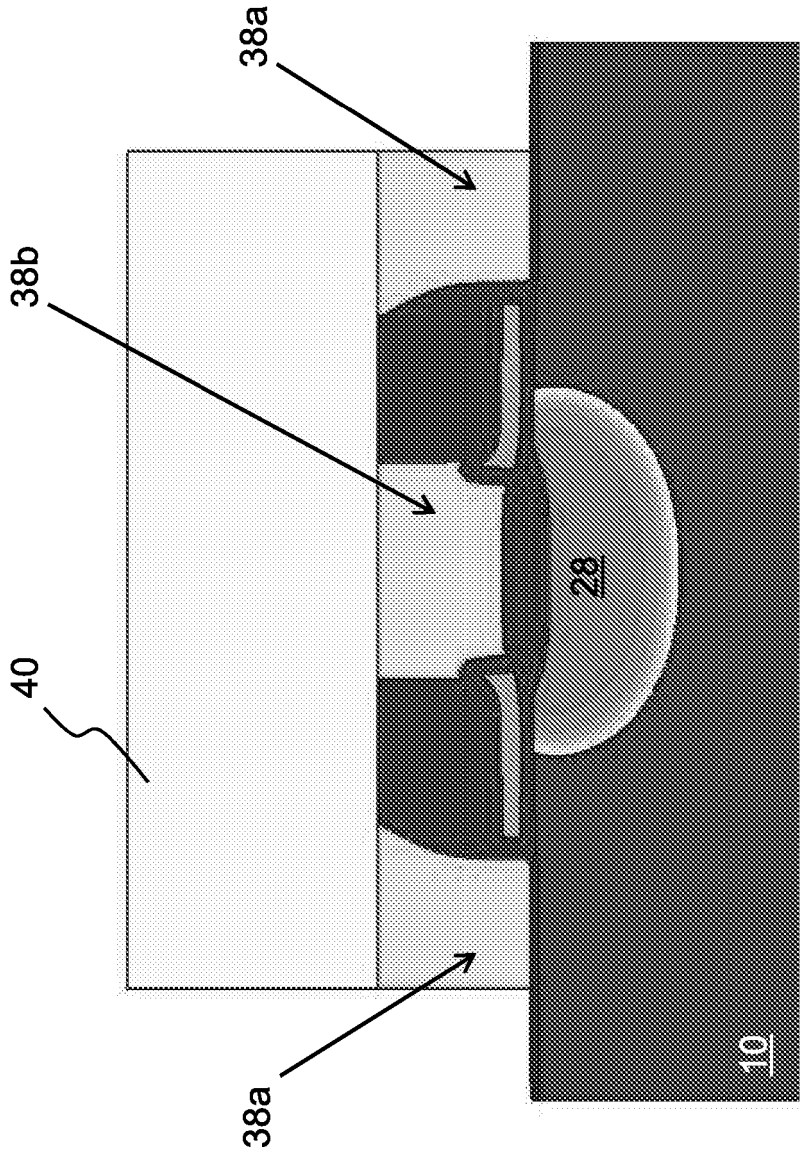

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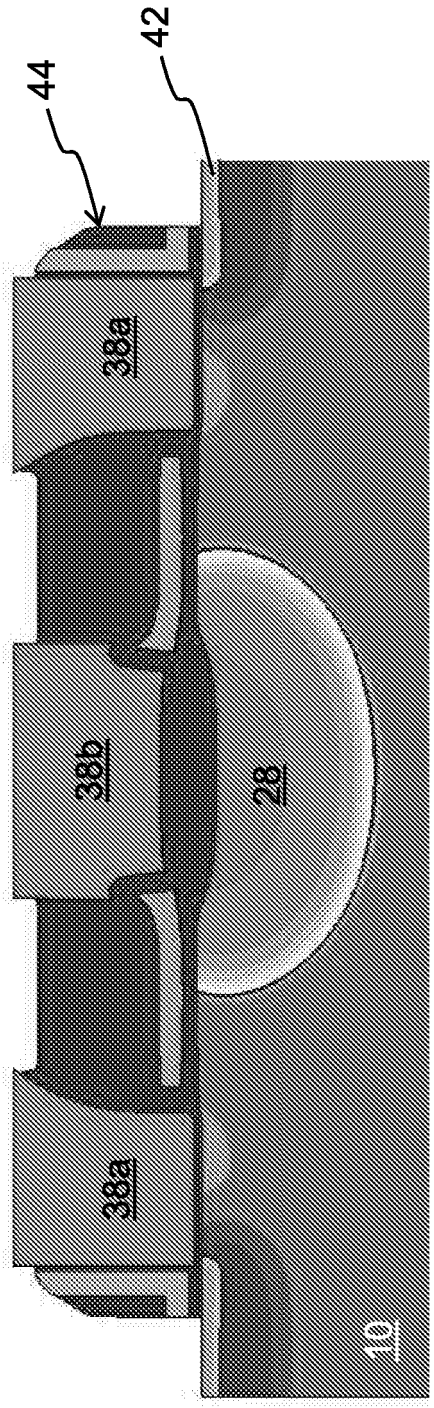

Figure 16

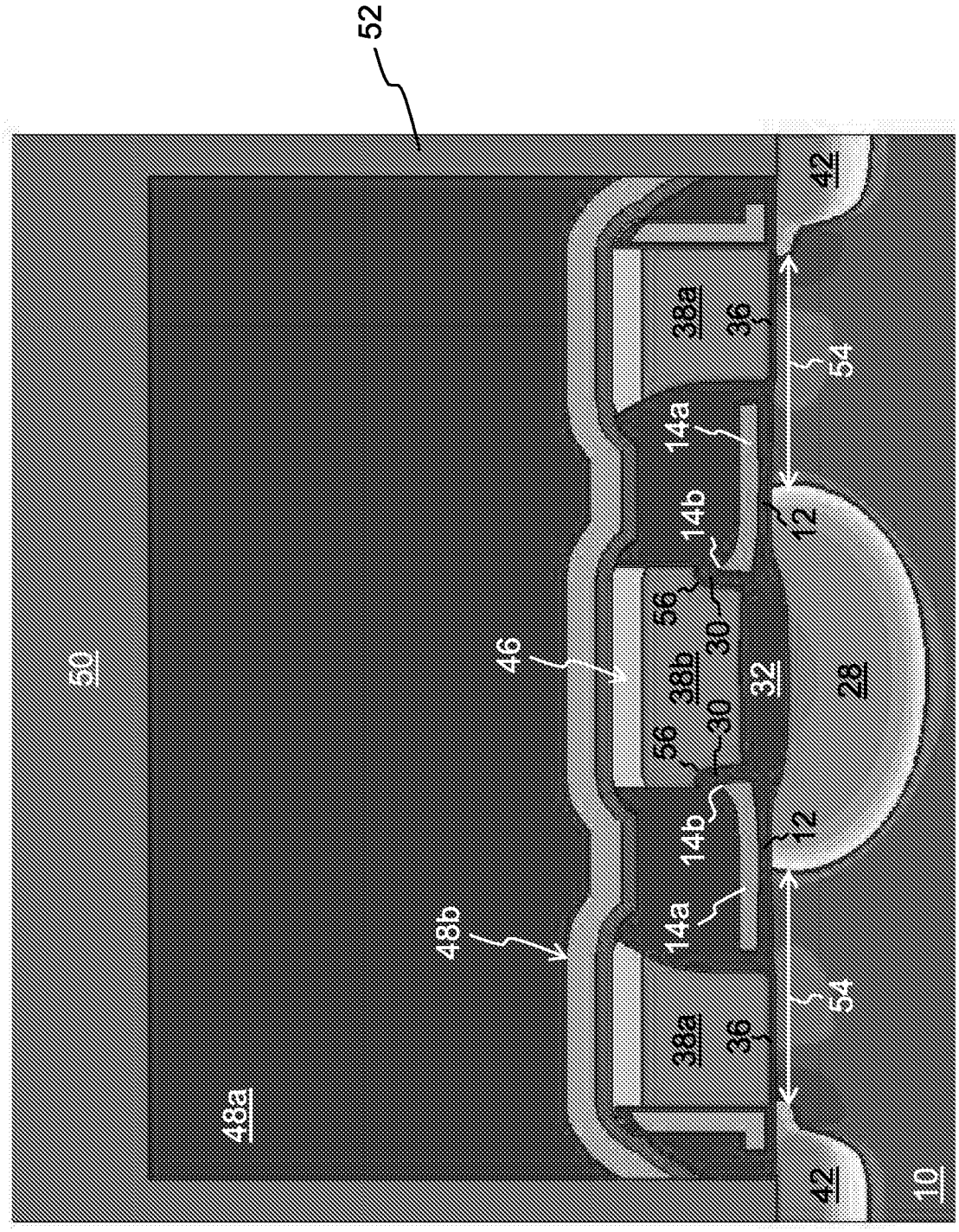

Figure 17

REFERENCES CITED IN THE DESCRIPTION

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