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(54) **STATIC RANDOM ACCESS MEMORY SUPPORTING A SINGLE CLOCK CYCLE READ-MODIFY-WRITE OPERATION**

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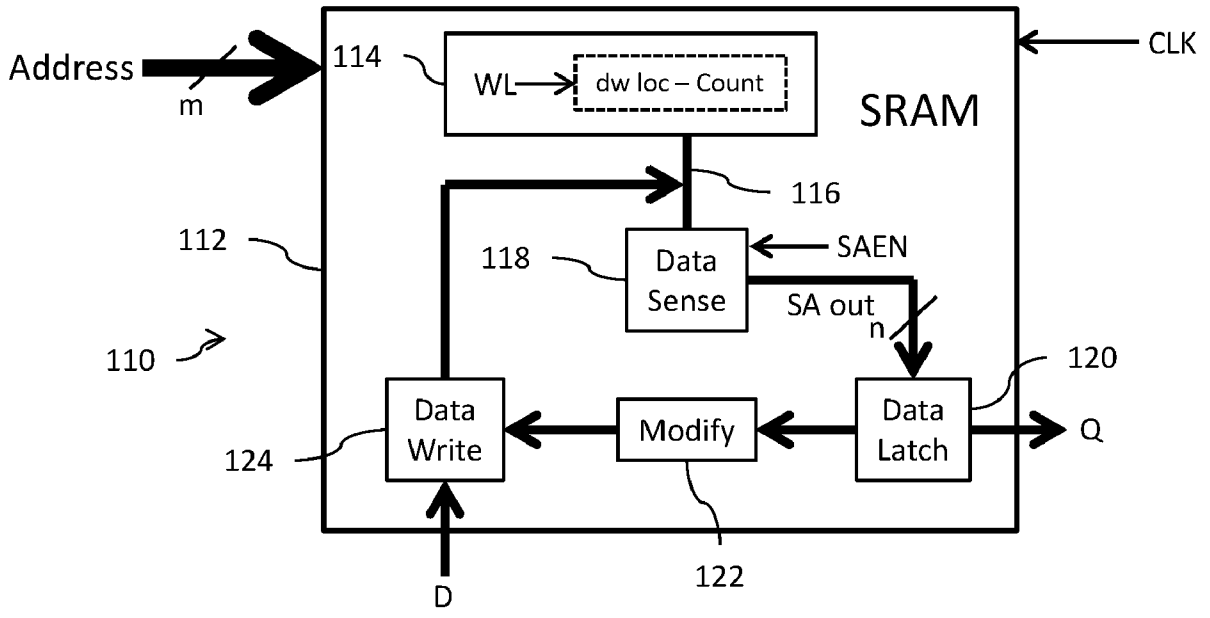
(57) **ABSTRACT**

A memory array includes memory cells forming a data word location accessed in response to a word line signal. A data sensing circuit configured to sense data on bit lines associated with the memory cells. The sensed data corresponds to a current data word stored at the data word location. A data latching circuit latches the sensed data for the current data word from the data sensing circuit. A data modification circuit then performs a mathematical modify operation on the current data word to generate a modified data word. The modified data word is then applied by a data writing circuit to the bit lines for writing back to the memory cells of the memory array at the data word location. The operations are advantageously performed within a single clock cycle.



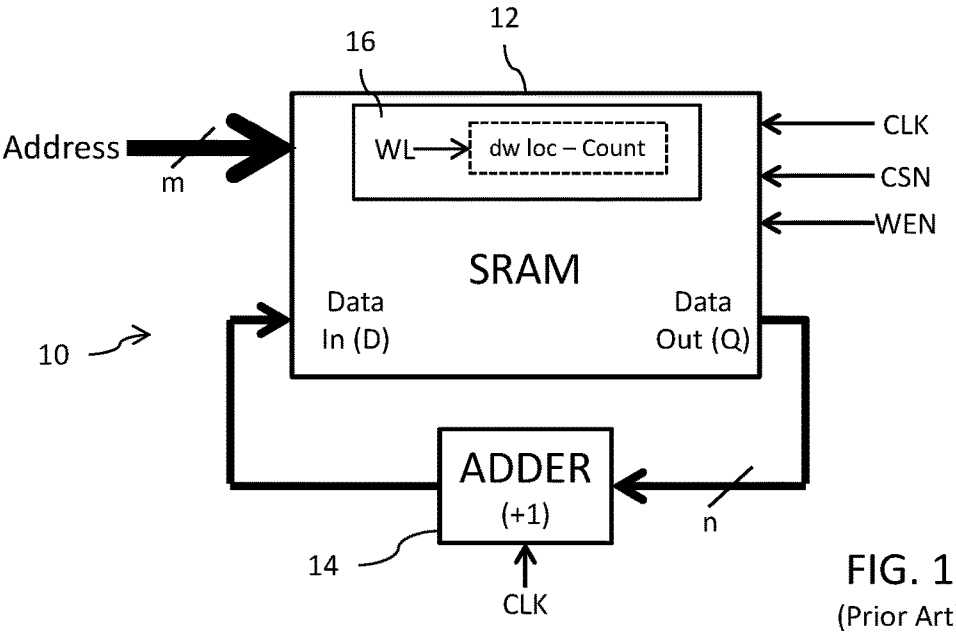


FIG. 1
(Prior Art)

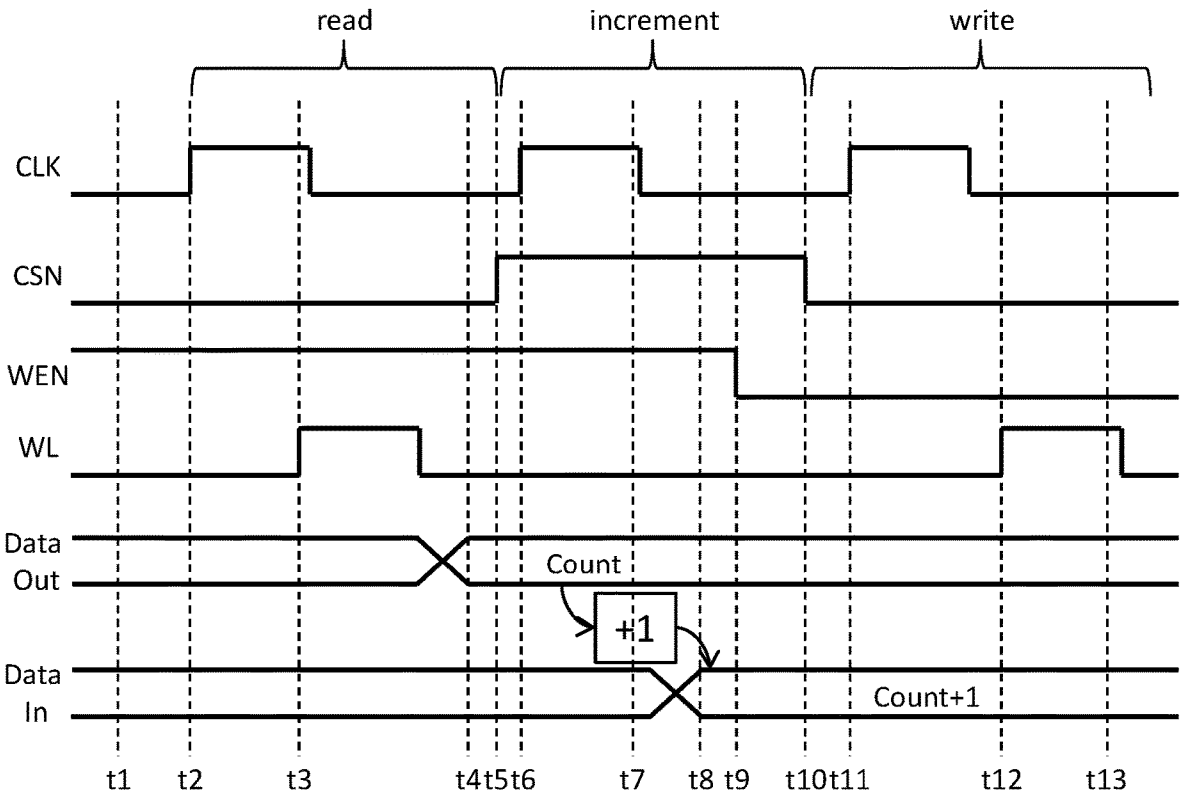


FIG. 2
(Prior Art)

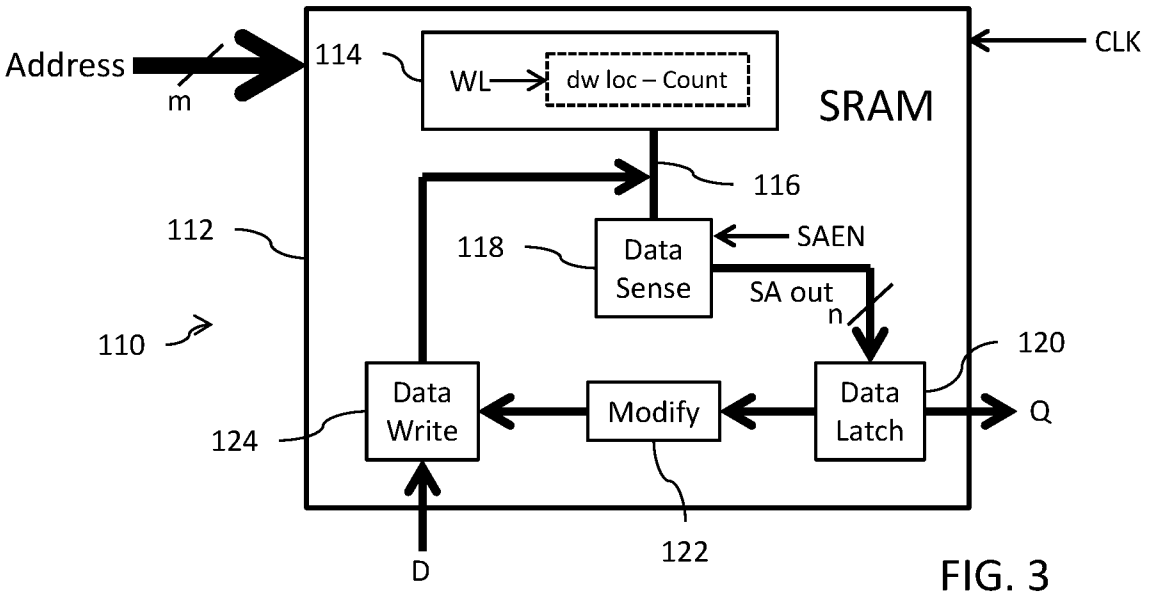

Address
m
114
WL
dw loc – Count
SRAM
CLK
116
112
118
Data Sense
SAEN
SA out
n
110
120
Data Write
Modify
Data Latch
Q
124
122
D

FIG. 3

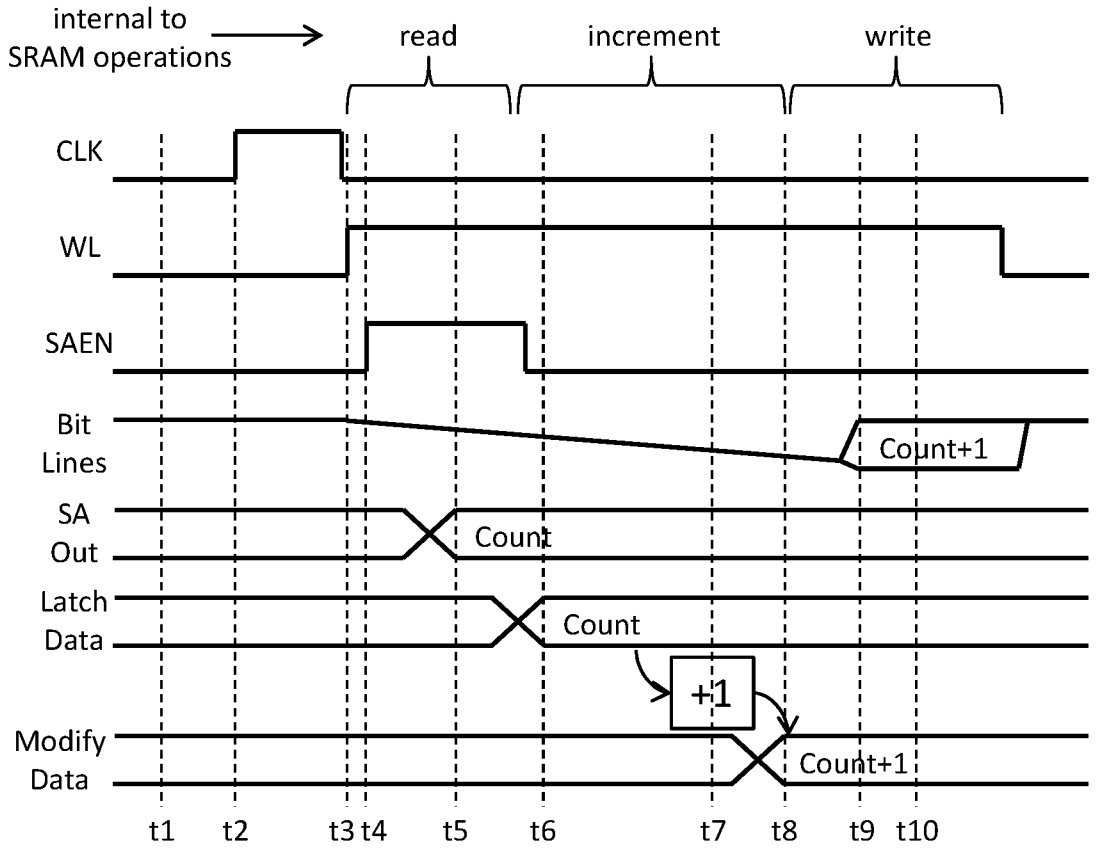
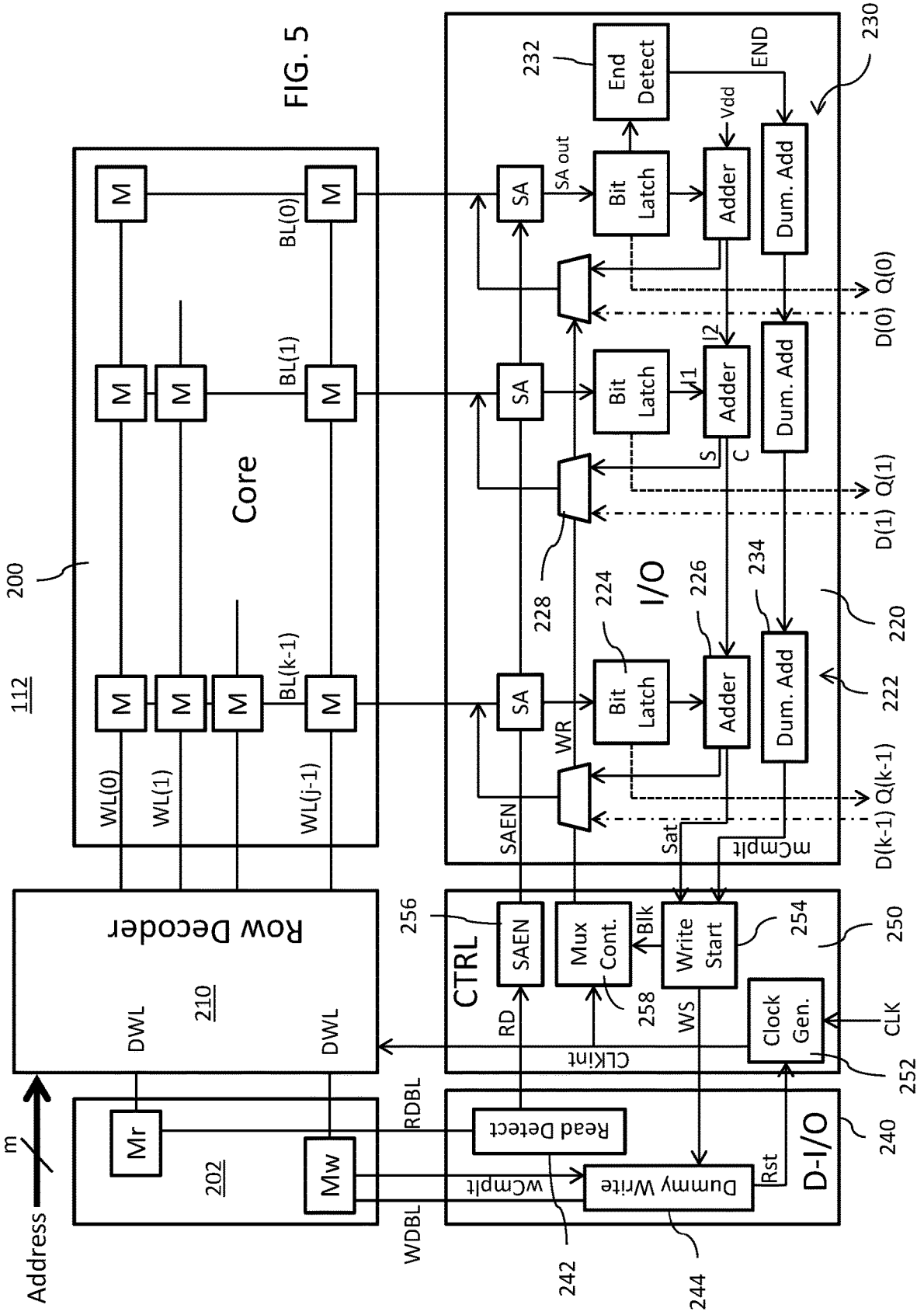

internal to SRAM operations
read
increment
write
CLK
WL
SAEN
Bit Lines
Count+1
SA Out
Count
Latch Data
Count
+1
Modify Data
Count+1
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10

FIG. 4

FIG. 5


Address
m
Row Decoder
210
DWL
DWL
Mr
Mw
202
RDBL
WDBL
Read Detect
Dummy Write
wCmplt
242
244
D-I/O
240
Rst
CTRL
SAEN
Mux Cont.
Write Start
Clock Gen.
CLK
CLKint
RD
WS
Blk
256
258
254
250
252
Core
112
200
WL(0)
WL(1)
WL(j-1)
BL(0)
BL(1)
BL(k-1)
M
SA
SA out
WR
SAEN
Sat
mCmplt
I/O
224
226
228
234
220
222
Bit Latch
Adder
Dum. Add
End Detect
232
230
END
Vdd
I2
I1
S
C
D(0)
Q(0)
D(1)
Q(1)
D(k-1)
Q(k-1)

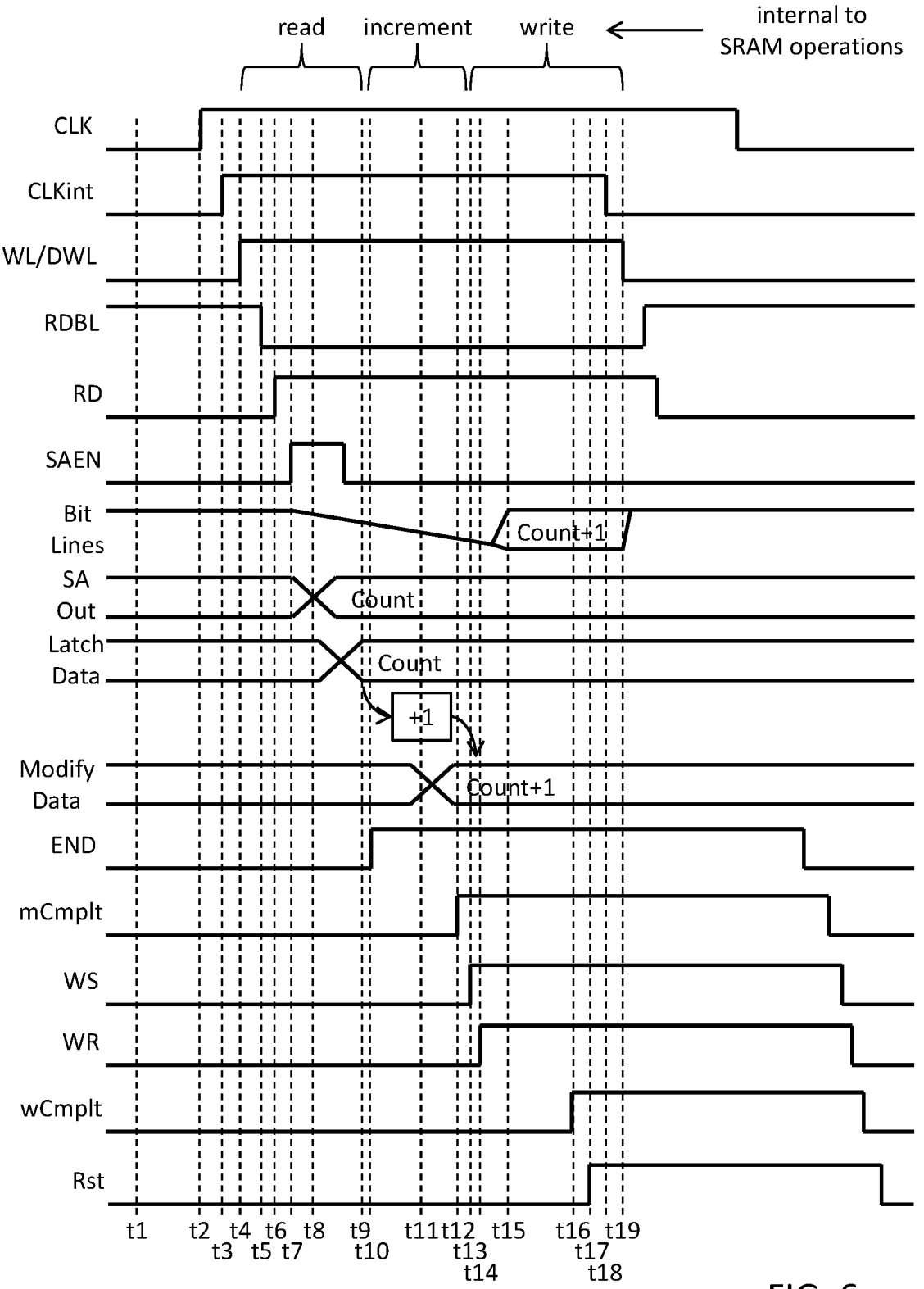

read
increment
write
internal to SRAM operations
CLK
CLKint
WL/DWL
RDBL
RD
SAEN
Bit Lines
Count+1
SA Out
Count
Latch Data
Count
+1
Modify Data
Count+1
END
mCmplt
WS
WR
wCmplt
Rst
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14
t15
t16
t17
t18
t19

FIG. 6

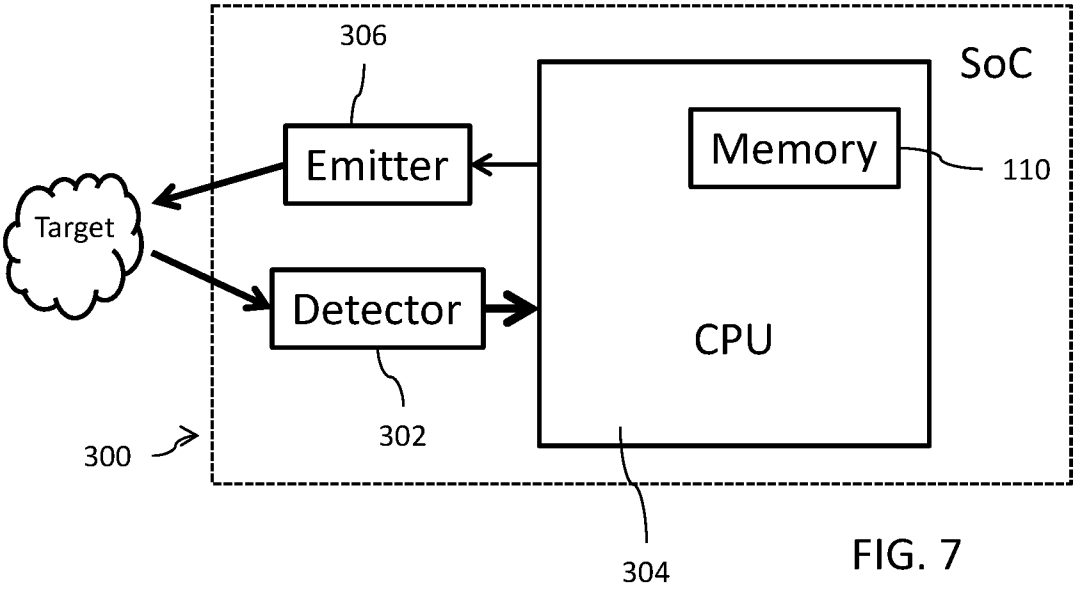


FIG. 7

STATIC RANDOM ACCESS MEMORY SUPPORTING A SINGLE CLOCK CYCLE READ-MODIFY-WRITE OPERATION

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. Provisional Application Patent No. 63/231,851, filed Aug. 11, 2021, the disclosure of which is incorporated by reference.

TECHNICAL FIELD

[0002] The present invention generally relates to a static random access memory (SRAM) circuit and, in particular, to an SRAM circuit configured to perform a read-modify-write operation in a single clock cycle.

BACKGROUND

[0003] Reference is made to FIG. **1** which shows a block diagram of a circuit **10** including a static random access memory (SRAM) **12** that is configured to store data. In a particular application, the stored data is histogram data where each data word location (dw loc) in the memory array **16** of the SRAM **12** stores a count value (Count). As part of the operation of the circuit **10** for building a histogram, the count value is modified in some way (for example, incremented by one) each time the data word location is accessed. This operation typically involves three steps: step **1**) reading the n-bit current count value from a particular data word location accessed in response to an m-bit memory address (Address); step **2**) mathematically modifying the current count value (for example, incrementing by one); and step **3**) writing the modified count value back to the SRAM **12** at the accessed data word location. The step **2**) operation for mathematically modifying the count value is performed here by a data modification circuit **14** that is external to (and separate from) the SRAM **12**. The data modification circuit **14** is coupled to the data output (Q) port and data input (D) port of the SRAM **12** through one or more n-bit data bus circuits. As an example, the data modification circuit **14** may comprise an n-bit adder circuit that operates on the current count value read from the memory at the data output (Q) to increment by one and output the modified count value to be written back to the memory at the data input (D).

[0004] Reference is now made to FIG. **2** which shows a timing diagram for the operation of the circuit **10**. At time t**1**, the chip select signal (CSN) is asserted logic low to select the SRAM **12** and the write enable signal (WEN) is deasserted logic high to place the SRAM **12** in data read mode. At time t**2**, the memory address (Address) is applied and the clock signal CLK pulses a first time to initiate a read operation. The Address is decoded by the SRAM **12** and the word line (WL) coupled to the data word location (dw loc) corresponding to the decoded Address is asserted logic high at time t**3**. The count value (Count) is then read (step **1**) from the addressed data word location in the array **16** and output at time t**4** through the data output (Q) port of the SRAM **12**. The chip select signal (CSN) is then deasserted logic high at time t**5** to deselect the SRAM **12** so that the SRAM **12** does not perform an operation in response to the next pulse of the clock signal CLK. At time t**6**, the clock signal CLK pulses a second time to cause the data modification circuit **14** to perform the mathematical modify operation (step **2**) at time t**7**, which in this example case is an increment by one (+1) operation. The modified count value (Count+1) is then applied by the data modification circuit **14** to the data input (D) port of the SRAM **12** at time t**8**. At time t**9**, the write enable signal (WEN) is asserted logic low to place the SRAM **12** in write mode. The chip select signal (CSN) is then asserted logic low at time t**10** to select the SRAM **12**. At time t**11**, the memory address (Address) is applied (e.g., remains applied from the read) and the clock signal CLK pulses a third time to initiate a data write operation. The Address is decoded by the SRAM **12** and the word line (WL) coupled to the data word location (dw loc) is asserted logic high at time t**12**. The modified count value (Count+1) is then written (step **3**) from the data input port of the SRAM **12** at time t**13** to the addressed data word location.

[0005] There are a number of concerns with the circuit **10** of FIG. **1** and its operation as detailed in FIG. **2**. The circuit operation is multi-cycle in that it requires three clock cycles and two separate word line assertions to complete. Because of this multi-cycle operation, there is significantly high power consumption in the circuit **10** due to data signal toggling. The power consumption concern is further magnified by the fact that the mathematical modify part of the operation (step **2**) occurs external to the SRAM **12** and thus there is toggling of data for the data signals at both the data output (Q) port and data input (D) port.

[0006] There is accordingly a need in the art to address the power consumption concerns and provide a more efficient implementation of the read-modify-write operation.

SUMMARY

[0007] In an embodiment, a circuit comprises: a memory array including memory cells forming a data word location accessed in response to a word line signal; a plurality of bit lines associated with said memory cells; a data sensing circuit configured to sense data on said plurality of bit lines, said sensed data corresponding to a current data word stored at the data word location; a data latching circuit configured to latch the sensed data for said current data word from the data sensing circuit; a data modification circuit configured to perform a mathematical modify operation on the current data word to generate a modified data word; and a data writing circuit configured to apply data for the modified data word to the plurality of bit lines for writing back to the memory cells of the memory array at said data word location.

[0008] The circuit is clocked by a clock signal. In a preferred implementation, the sensing of the data on said plurality of bit lines, the latching of the sensed data, the performing of the mathematical modify operation and the writing back of the modified data word all occur within a single cycle of the clock signal.

[0009] In an embodiment, a circuit comprises: a memory array including memory cells forming a data word location accessed in response to a word line signal; a plurality of bit lines associated with said memory cells; and an input/output circuit for each bit line. Each input/output circuit comprises: a sensing circuit configured to sense and latch data on the bit line; an adder circuit configured to perform an addition operation, said adder circuit having a first input coupled to receive latched data from the sensing circuit, a second input coupled to receive data from the adder circuit of the input/output circuit for a lower significance bit line, a sum output, and a carry output coupled to supply data to the second input of the adder circuit of the input/output circuit for a higher

significance bit line; and a pass circuit configured to selectively pass the sum output of the adder circuit to the bit line for writing back to the data word location.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] For a better understanding of the embodiments, reference will now be made by way of example only to the accompanying figures in which:

[0011] FIG. **1** shows is a block diagram of a circuit configured to perform a read-modify-write operation with respect to a count value stored in a static random access memory (SRAM) using an external modify circuit;

[0012] FIG. **2** shows a timing diagram for operation of the circuit of FIG. **1**;

[0013] FIG. **3** shows is a block diagram of a circuit configured to perform a read-modify-write operation with respect to a count value stored in a static random access memory (SRAM) using an internal modify circuit;

[0014] FIG. **4** shows a timing diagram for operation of the circuit of FIG. **3**;

[0015] FIG. **5** shows a detailed block diagram of an SRAM for the circuit of FIG. **3**;

[0016] FIG. **6** shows a timing diagram for operation of the circuit of FIG. **5**; and

[0017] FIG. **7** is a schematic representation of a device, for example in form of an image sensor, which utilizes the circuit of FIG. **3** or **5**.

DETAILED DESCRIPTION

[0018] Reference is made to FIG. **3** which shows a block diagram of a circuit **110** including a static random access memory (SRAM) **112** that is configured to store data. In a particular application, the stored data is histogram data where each data word location (dw loc) in the SRAM **112** stores a count value (Count). As part of the operation of the circuit **110** for building a histogram, the count value is modified in some way (for example, incremented by one) each time the data word location is accessed. This operation typically involves three steps: step **1**) reading the n-bit current count value from a particular data word location accessed in response to an m-bit memory address (Address); step **2**) mathematically modifying the current count value (for example, incrementing by one); and step **3**) writing the modified count value back to the particular data word location in the SRAM **112**. The step **2**) operation for mathematically modifying the count value is advantageously performed internally within the SRAM **112**. Because of this, there is no need to toggle data signals at the data output (Q) port and data input (D) port of the SRAM **112**, and there is no external data calculation operation performed, and thus there is a reduction in power consumption in comparison to the solution shown in FIG. **1**. Still further, by performing the mathematical modify operation internally for step **2**) of the read-modify-write operation, there is no implication of external circuitry and the overall operation can be performed by the SRAM itself in a single clock cycle.

[0019] The SRAM **112** is clocked by a clock signal CLK and includes a memory array **114** comprising a plurality of n-bit accessible data word locations (dw loc). In response to an applied m-bit memory address (Address) and a pulsing of the clock signal CLK, a word line WL is asserted to select and access one of the data word locations in the memory array **114**. The bit lines **116** of the memory array **114** are coupled to a data sensing circuit **118**. The data sensing circuit **114** is formed by a plurality of sense amplifiers (one sense amplifier per data bit of the n-bit data word at the accessed data word location). The data sensing circuit **118** is enabled to perform the data sensing operation on the bit lines **116** in response to assertion of a sense amplifier enable (SAEN) signal in order to read the data word (i.e., the count value (Count)) from the accessed data word location in the memory array **114**. As discussed in greater detail below, the timing of assertion of the SAEN signal can be controlled following the leading edge of the clock signal CLK based on a dummy read operation performed by the SRAM **112**. This ensures that the sense amplifiers are not enabled to drive voltages on the sense amplifier output (SA out) lines until it is clear that the data bits are available in response to assertion of the word line signal. A data latch circuit **120** then latches the read data word (here, the count value) from the SA out lines. A data modification circuit **122** that is internal to the SRAM **112** performs a data modification on the latched data word. As an example, the data modification circuit **122** may comprise an n-bit adder circuit that operates on the latched data word (which is the current count value stored in the memory) to increment by one and output the modified data word (i.e., Count+1). As discussed in greater detail below, the timing of completion of the data modification operation can be detected by the SRAM **112** for the purpose of controlling when to begin the write phase. This ensures that the data to be written back to the memory is an accurate modification. A data write circuit **124** then writes the data bits of the modified data word back to the bit lines **116** to be stored at the accessed data word location in the memory array **114**. It will be noted that because of read multiplexing circuitry, not explicitly shown, the data sensing circuit **118** at this point in time has been disconnected from the bit lines and the SAEN signal is no longer asserted. Following completion of the data write, the word line signal is deasserted. As discussed in greater detail below, the timing of completion of the write operation can be controlled based on a dummy write operation performed by the SRAM **112**. This ensures that the data bits of the modified data word remain on the bit lines **116** for a sufficient amount of time to ensure successful write back into the memory cells M.

[0020] Reference is now made to FIG. **4** which shows a timing diagram for operation of the circuit **110**. At time t**1**, the SRAM **112** is enabled for operation and the bit lines **116** are precharged to a precharge voltage level (shown here, by example only, at Vdd). At time t**2**, the memory address (Address) is applied and the clock signal CLK pulses. The Address is decoded by the SRAM **112** and the word line (WL) coupled to the data word location (dw loc) corresponding to the decoded Address is asserted logic high at time t**3**. In response to the asserted word line signal and the logic state of the stored data, the voltage on the bits begins to discharge from Vdd. At time t**4**, the sense amplifier enable (SAEN) signal is asserted logic high to enable operation of the sense amplifiers within the data sensing circuit **118**. The sense amplifiers respond at time t**5** to sense the voltage on the bit lines **116** and drive corresponding output signals (SA out) from the data sensing circuit **118** to logic high or logic low levels dependent on the logic state of the bits of the data word stored in the accessed data word location. Thus, the data word has been read (step **1**) from the memory array **114** and the output of the data sensing circuit **118** now reflects the

count value (Count). The data latch circuit **120** latches the read data word from the output of the data sensing circuit **118** at time t**6**, and thus the latched data also reflects the count value (Count). The data modification circuit **122** then performs the mathematical modify operation (step **2**) at time t**7**, which in this example case is an increment by one (+1) operation, and the output modified data from the data modification circuit **122** at time t**8** reflects the incremented count value (Count+1). The data write circuit **124** then applies the data bits of the modified data word back to the bit lines **116** (noting here that the voltage of the bit line(s) has continued to slowly discharge in response to the assertion of the wordline signal). Because the signal on the word line (WL) remains asserted logic high, the modified data word is then written (step **3**) at time t**9** for storage at the accessed data word location in the memory array **114**. Following completion of the data write operation at time t**10**, a reset is performed and the word line (WL) is deasserted logic low.

[0021] Reference is now made to FIG. **5** which shows a detailed block diagram of the SRAM **112** for the circuit **110** of FIG. **3**. The memory array **114** includes a memory core **200** and a dummy memory area **202**. The memory core **200** and dummy memory area **202** each include a plurality of SRAM cells (M) (for example, of the 6T or 8T type as is well known in the art).

[0022] In the memory core **200**, the cells M are arranged in an array including j rows and k columns. The cells M in each row of the memory core **200** are coupled to a corresponding word line (WL), and the cells in each column are coupled to at least one corresponding bit line (BL). In an implementation using the 6T type SRAM circuit, a pair of complementary bit lines are present and are used in connection with both writing data to and reading data from the memory cell of a column. In an implementation using the 8T type SRAM circuit, a pair of complementary write bit lines and a single read bit line are present, with the write bit lines used in connection with writing data to the memory cell and the read bit line used in connection with reading data from the memory cell. The j memory cells M of each row at a given memory address location form a bin which stores a data word corresponding to a count value (Count) of the histogram. In the illustrated implementation, the bit stored in the memory cell of column 0 is the least significant bit (LSB) of the count value and the bit stored in the memory cell of column k−1 is the most significant bit (MSB) of the count value.

[0023] The dummy memory area **202** includes a dummy read cell Mr and a dummy write cell Mw. The dummy cells Mr and Mw are, like the cells M of the memory core **200**, implemented using either a 6T or 8T type SRAM circuit. The dummy read cell Mr is programmed with a fixed logic state (for example, logic low). The dummy cells Mr and Mw are both actuated in response to assertion of a signal on a dummy word line (DWL) for the dummy memory area **202**. The dummy read cell Mr is coupled to a read dummy bit line (RDBL), and the dummy write cell Mw is coupled to a write dummy bit line (WDBL). In an implementation using the 6T type SRAM circuit, the bit line comprises a pair of complementary dummy bit lines. In an implementation using the 8T type SRAM circuit, the bit line comprises a pair of complementary dummy write bit lines and a single dummy read bit line. The dummy write cell Mw further includes circuitry configured to sense the write operation and generate a write complete signal (wCmplt) in response to successful completion of a data write into the dummy write cell Mw.

[0024] The SRAM **112** further includes a row decoder circuit **210** that is configured to receive the memory address (Address) and an internal clock signal CLKint. The row decoder circuit **210** responds thereto by decoding the receive memory address and selectively actuating one word line (WL) which corresponds to the decoded memory address in the memory core **200** and further actuating the dummy word line (DWL) for the dummy memory area **202**. Details of the circuitry for the row decoder circuit **210** are not provided as such circuitry is well known to those skilled in the art.

[0025] The data input/output (I/O) circuitry **220** for the SRAM **112** includes an I/O circuit **222** for each column of the memory core **200**. Each I/O circuit **222** includes a sense amplifier SA circuit connected to the bitline BL of the corresponding column. The sense amplifier SA circuit functions, in response to assertion of a sense amplifier enable SAEN signal, to drive an output signal (SA out) to a supply rail (Vdd or ground, for example) as a function of the logic state of the data bit stored in the memory cell M of the row which is selected by the actuation of the word line WL. The plurality of sense amplifier SA circuits in the data input/output (I/O) circuitry **220** form the data sensing circuit **118** (see, FIG. **3**). The logic state of the data bit output by the sense amplifier SA circuit in the SA out signal is then latched by a bit latch circuit **224**. The plurality of bit latch circuits **224** in the data input/output (I/O) circuitry **220** form the data latch circuit **120** (see, FIG. **3**). In connection with a conventional data read mode of operation for the SRAM **112**, the output of each bit latch circuit **224** is coupled (see, dotted arrows) to a data output line Q(0), . . . , Q(k−1) for a corresponding bit of the data output port.

[0026] To support the read-modify-write operation with an internal modify, each I/O circuit **222** further comprises an adder circuit **226** and a write multiplexer circuit **228**. Each adder circuit **226** includes a first input (I**1**) that is coupled to receive the latched data bit from its corresponding bit latch circuit **224** and a second input (I**2**) that is coupled to a carry output of a preceding adder circuit (except for the first adder circuit associated with the least significant bit column which is coupled to a logic high voltage supply node (Vdd) for the second input). Each adder circuit **226** further includes a sum output (S) that is coupled to a first input of the write multiplexer circuit **228** and a carry output (C) that is coupled to the second input of a succeeding adder circuit (except for the last adder circuit associated with the most significant bit column which provides a saturation signal Sat for the carry output). The plurality of adder circuits **226** in the data input/output (I/O) circuitry **220** form the data modification circuit **122** (see, FIG. **3**) and function to perform an increment by one operation on the data word provided by the bits latched by the bit latch circuits **224** of the data latch circuit **120**. In a preferred implementation, each adder circuit **226** is a half-adder circuit whose configuration is well known to those skilled in the art. In connection with a conventional data write mode of operation for the SRAM **112**, the second input of each multiplexer circuit **228** is coupled (see, dotted-dashed arrows) to a data input line D(0), . . . , D(k−1) for a corresponding bit of the data input port. The select control input for the multiplexer circuits **228** is coupled to receive a write control signal WR. When the write control signal WR is in a first logic state, the multiplexer circuits **228** pass the data from the data input lines D(0), . . . , D(k−1) for

application to the corresponding bit lines BL in order to write external data into the memory core **200**. Conversely, when the write control signal WR is in a second logic state, the multiplexer circuits **228** pass the data from the adder circuits **226** relating to the modified data in order to write internal data to the memory core **200**.

[0027] The data input/output (I/O) circuitry **220** for the SRAM **112** further includes a data modification timing circuit **230**. The data modification timing circuit **230** comprises a latching end detect circuit **232** that is coupled to the bit latch circuit **224** for the least significant bit column. The latching end detect circuit **232** operates to detect when that least significant bit latch circuit **224** has successfully completed latching of the data logic state of the least significant bit of data sensed by the sense amplifier SA circuit. In response to this detection, the latching end detect circuit **232** asserts an end signal END. The data modification timing circuit **230** further comprises a dummy adder circuit **234** corresponding to each adder circuit **226** (i.e., the circuits are copies or replicas of each other). Each dummy adder circuit **234** includes a first input coupled to receive a logic high voltage (Vdd; not explicitly shown) and a second input that is coupled to an output of a preceding dummy adder circuit (except for the first dummy adder circuit associated with the least significant bit column which is coupled to receive the end signal END). Each dummy adder circuit **234** further includes an output (specifically the carry output) that is coupled to the second input of a succeeding dummy adder circuit (except for the last dummy adder circuit associated with the most significant bit column which provides a data modification complete signal mCmplt output by the data modification timing circuit **230**). Each dummy adder circuit **234** has a propagation delay from input to output which corresponds to a propagation delay from input to output of the adder circuit **226**. Thus, the data modification complete signal mCmplt is asserted in response to propagation of the end signal END through the series of dummy adder circuit **234** and this corresponds to an amount of time (for example, a worst case) taken by the plurality of adder circuits **226** of the data modification circuit **122** to complete the increment by one operation.

[0028] Although the latching end detect circuit **232** is shown in FIG. **5** to be coupled to the bit latch circuit **224** for the least significant bit column, it will be understood that this is by example only. In an alternate configuration of the circuit where the most significant bit column is furthest from the row decoder circuit **210**, it would be preferable for the end detection to be made with respect to latching of that bit data for the signal SA out output from the sense amplifier.

[0029] A dummy data input/output (D-I/O) circuitry **240** for the SRAM **112** includes a read detect circuit **242** that is coupled to the read dummy bit line RDBL for the dummy read cell Mr that is actuated by assertion of the dummy word line DWL. The read detect circuit **242** may include a digital logic circuit (not explicitly shown) to sense a specific lower voltage level on the read dummy bitline RDBL as a function of the logic state of the fixed data bit stored in the dummy read cell Mr, and thus this circuit operates to determine timing of completion of a read of the fixed data bit stored in the dummy read cell Mr. For example, a threshold comparison circuit of the read detect circuit **242** determines when the voltage on the read dummy bit line passes a certain threshold level. In response to that determination, dummy read is complete and the read detect circuit **242** asserts an output read detect RD signal.

[0030] The dummy data input/output (D-I/O) circuitry **240** for the SRAM **112** further includes a write driver and write detect (dummy write) circuit **244** that is coupled to the write dummy bit line WDBL for the dummy write cell Mw that is actuated by assertion of the dummy word line DWL. The write driver functionality of the dummy write circuit **244** is actuated in response to a write start WS signal and operates to write a certain logic state into the dummy write cell Mw. The write detect functionality of the dummy write circuit **244** receives the write complete signal (wCmplt) which is asserted by the dummy write cell Mw in response to successful completion of the data write. In response to receipt of the write complete signal (wCmplt), the dummy write circuit **244** asserts a reset signal (Rst).

[0031] A control circuit (CTRL) **250** for the SRAM **112** includes a clock generator circuit **252**. The clock generator circuit **252** receives the external clock signal CLK and the reset signal (Rst), and generates the internal clock signal CLKint. The clock signals CLK and CLKint have a same frequency, but are phase offset from each other and have different duty cycles (pulse widths). The duty cycle of the internal clock signal CLKint is controlled by an edge of the clock signal CLK and the assertion of the reset signal Rst.

[0032] A write start circuit **254** of the control circuit **250** receives the data modification complete signal mCmplt from the last dummy adder circuit **234** of the data modification timing circuit **230** and the saturation signal Sat from the last adder circuit **226** of the data modification circuit **122**. The write start circuit **254** asserts the write start WS signal in response to the data modification complete signal mCmplt. Thus, the dummy write operation performed by the write driver and write detect circuit **144** occurs only after the data modification timing circuit **230** indicates through assertion of the data modification complete signal mCmplt that the data modify operation being performed by the data modification circuit **122** has been completed. The write start circuit **254** further asserts a block signal Blk in response to the saturation signal Sat. The block signal Blk is asserted in the situation where the data modify operation being performed by the data modification circuit **122** results in an overflow. For example, consider the situation where the read count value from the memory is at a maximum value such as <1,1,1, . . . , 1,1,1>. In this case, the increment by one operation being performed by the data modification circuit **122** will produce an output value of <0,0,0, . . . , 0,0,0> with the carry of one from the addition operation being indicated by the assertion of the saturation signal Sat. In this scenario, it would be undesirable for the write operation to be performed as this would cause a loss of the histogram data for that bin of the memory by essentially resetting the count value to zero. The assertion of the block signal Blk is used to control a blocking of the performance of the write operation from occurring. Conversely, the block signal Blk is deasserted, in the absence of the saturation signal Sat, in response to the data modification complete signal mCmplt.

[0033] The control circuit **250** further includes a multiplexer controller **258** that receives the internal clock signal CLKint and the block signal Blk. The multiplexer controller **258** generates the write control signal WR which is applied to the select control input for the multiplexer circuits **228**. The write control signal WR is asserted in the second logic

state only if the internal clock signal CLKint is asserted and the block signal Blk is deasserted. In that case, the multiplexer circuits **228** respond to the second logic state of the write control signal WR by passing the data from the adder circuits **226** in order to write internal data to the memory core **200**. If the block signal Blk is asserted, indicating that the result of the increment by one operation being performed by the data modification circuit **122** is a saturation (i.e., overflow), the write control signal WR is deasserted in the first logic state and the writing of the data from the adder circuits **226** to the memory is blocked.

[0034] A sense amplifier enable circuit **256** of the control circuit **250** receives the read detect RD signal output by the read detect circuit **242**. In response thereto, the sense amplifier enable circuit **256** asserts the sense amplifier enable SAEN signal. Thus, the sense amplifier SA circuits are enabled for operation only after the read detect circuit **242** has determined that a read of the data bit stored in the dummy read cell Mr has been completed.

[0035] Reference is now made to FIG. **6** which shows a timing diagram for operation of the circuit SRAM **112** of FIG. **5**. At time t**1**, the SRAM **112** is enabled for operation and the bit lines **116** are precharged to a precharge voltage level (shown here, by example only, at Vdd). At time t**2**, the memory address (Address) is applied and the clock signal CLK pulses. In response to the leading edge of the clock signal CLK pulse, the clock generator circuit **252** generates the leading each of the internal clock signal CLKint at time t**3**. The Address is decoded by the row decoder **210** and the word line (WL) coupled to the data word location (dw loc) corresponding to the decoded Address is asserted logic high at time t**4**. At the same time, the row decoder **210** also asserts the dummy word line (DWL) logic high. The dummy read cell Mr is accessed by the asserted dummy word line (DWL) and the logic state of the read dummy bit line RDBL falls at time t**5** to a logic low level matching the fixed logic state programmed in the dummy read cell Mr. The read detect circuit **242** of the dummy input/output (D-I/O) circuit **240** detects completion of the dummy read operation and asserts the read detect RD signal at time t**6**. The sense amplifier enable circuit **256** of the control circuit **250** responds to the asserted read detect RD signal by asserting the sense amplifier enable SAEN signal to enable the sense amplifier SA circuits at time t**7**. The sense amplifier circuits respond at time t**8** to drive the sense amplifier output signals SA out to logic high or logic low levels dependent on the logic state of the bits of the data word stored in the accessed data word location. Thus, the data word has been read (step **1**) from the memory array **114** and the logic states of the sense amplifier output signals SA out now reflect the count value (Count). The read data bits of the data word from the amplifier output signals SA out are then latched at time t**9** by the bit latches **224**, and thus the latched data also reflects the count value (Count). The end detect circuit **232** detects that the bit latch **224** of the least significant bit column has successfully latched the bit data from the bit lines and asserts the end detect END signal at time t**10**. The data modification circuit **122** then performs the mathematical modify operation (step **2**) at time t**11**, which in this example case is an increment by one (+1) operation, and the output modified data from the adder circuits **226** reflects the incremented count value (Count+1) at time t**12**. The dummy adder circuits **234** of the data modification timing circuit **230** perform a parallel mathematical modify operation and the data modification complete signal mCmplt is asserted at time t**12** in response to completion of the parallel operation. The write start circuit **254** then asserts the write start WS signal at time t**13** in response to the data modification complete signal mCmplt. The block signal Blk is also not asserted at this time by the write start circuit **254** (assuming here that there is no saturation due to the increment operation), and so the multiplexer control circuit **258** will then assert the write control signal WR in the second logic state at time t**14**. The data bits of the modified data word are then applied to the bit lines **116** through the multiplexer circuits **228** at time t**15** and the modified data word is then written (step **3**) for storage at the accessed data word location in the memory array **114**. In the meantime, the write driver and write detect (dummy write) circuit **244** responds to assertion of the write start WS signal by performing a data write to the dummy write cell Mw. The dummy write cell Mw responds to completion of the data write by asserting the write complete signal wCmplt at time t**16**. The dummy write circuit **244** then responds to receipt of the write complete signal wCmplt by asserting the reset signal Rst at time t**17**. The clock generator circuit **252** then generates the trailing edge of the internal clock signal CLKint at time t**18**, and deassertion of the word lines (WL and DWL) is made by the clock generator circuit **252** at time t**19**.

[0036] It will be noted that in the situation where there is a saturation due to the increment operation, the block signal Blk will be asserted at time t**13** by the write start circuit **254** and the multiplexer control circuit **258** will accordingly deassert the write control signal WR in the first logic state at time t**14**. This blocks the multiplexer circuits **228** from applying the data bits of the modified data word to the bit lines **116**, so as to preserve the previous count value for the histogram.

[0037] Reference is now made to FIG. **7** which shows a schematic representation of a device **300** which utilizes the circuit **110** of FIG. **3** or **5**. The device **300** may, for example, comprise an image sensor in the form of a System on Chip (SoC) that includes a photosensitive circuit **302** having output that is processed by a central processing unit **304**. The circuit **110** may, for example, comprise a memory which is coupled to or embedded in the central processing unit **304**. In a particularly pertinent example, the image sensor may comprise a time of flight (ToF) sensor as is well known in the art. Such a sensor includes an emitter circuit **306** configured to emit light pulses which are reflected by a target back towards the photosensitive circuit **302**. In response to detections of the reflected light pulses, the circuit **110** is accessed by the CPU **304** at memory addresses associated with timing measurements. Each access causes a mathematical modification (for example, increment by one) of a stored count value which over time provides histogram data useful in identifying targets and the distances to those targets.

[0038] While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are considered illustrative or exemplary and not restrictive; the invention is not limited to the disclosed embodiments. Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims.

What is claimed is:

1. A circuit that is clocked by a clock signal, comprising:

a memory array including memory cells forming a data word location accessed in response to a word line signal;

a plurality of bit lines associated with said memory cells;

a data sensing circuit configured to sense data on said plurality of bit lines, said sensed data corresponding to a current data word stored at the data word location;

a data latching circuit configured to latch the sensed data for said current data word from the data sensing circuit;

a data modification circuit configured to perform a mathematical modify operation on the current data word to generate a modified data word; and

a data writing circuit configured to apply data for the modified data word to the plurality of bit lines for writing back to the memory cells of the memory array at said data word location;

wherein the sensing of the data on said plurality of bit lines, the latching of the sensed data, the performing of the mathematical modify operation and the writing back of the modified data word all occur within a single cycle of the clock signal.

2. The circuit of claim **1**, further comprising a decoder circuit configured to decode a memory address identifying said data word location and continuously assert said word line signal starting with accessing the data word location and ending after completion of the writing back of the modified data word.

3. The circuit of claim **2**, further comprising a write timing circuit configured to perform a dummy write operation to a dummy memory cell in response to completion of the mathematical modify operation, wherein said ending of the continuous assertion of said word line signal occurs in response to completion of said dummy write operation.

4. The circuit of claim **1**, wherein the mathematical modify operation is an increment by one operation.

5. The circuit of claim **1**, wherein said data word location forms a bin for storing a histogram data word.

6. The circuit of claim **1**, further comprising a read timing circuit configured to control timing for actuation of the data sensing circuit in response to completion of a dummy read operation from a dummy memory cell.

7. The circuit of claim **1**, further comprising a data modification timing circuit configured to control actuation of said data writing circuit in response to completion of a dummy mathematical modify operation.

8. The circuit of claim **7**, wherein said dummy mathematical modify operation is actuated in response to completion of latching the sensed data for said current data word by said data latching circuit.

9. The circuit of claim **1**, further comprising a write timing circuit configured to control timing for resetting of the circuit in response to completion of a dummy write operation to a dummy memory cell.

10. The circuit of claim **1**, further comprising an input/output circuit for each bit line, said input/output circuit comprising:

a sense amplifier circuit coupled to the bit line;

a bit latch circuit coupled to said sense amplifier circuit; and

an adder circuit for performing the mathematical modify operation, said adder circuit having a first input coupled to receive a data bit from the bit latch circuit, a second input coupled to receive data from the adder circuit of the input/output circuit for a lower significance bit line, a sum output, and a carry output coupled to supply data to the second input of the adder circuit of the input/output circuit for a higher significance bit line.

11. The circuit of claim **10**, wherein said input/output circuit further comprises:

a multiplexer circuit having a first input coupled to a bit of a data input port of the circuit, a second input coupled to the sum output of the adder circuit, and an output coupled to the bit line.

12. The circuit of claim **11**, wherein the multiplexer circuit is controlled in a first mode to pass the data at the sum output to the bit and is controlled in a second mode to pass the data at the data input port of the circuit.

13. The circuit of claim **10**, wherein said input/output circuit further comprises a pass circuit configured to selectively pass the sum output of the adder circuit to the bit line.

14. The circuit of claim **13**, wherein the sum output of the adder circuit is blocked from passing to the bit line when the mathematical modify operation produces a saturation result.

15. The circuit of claim **13**, wherein the sum output of the adder circuit is permitted to pass to the bit line when the mathematical modify operation performed by the data modification circuit has been completed.

16. The circuit of claim **15**, further comprising a data modification timing circuit configured to detect completion of a dummy mathematical modify operation and in response thereto permit the pass circuit to pass the sum output of the adder circuit to the bit line.

17. The circuit of claim **1**, further comprising a blocking circuit configured to block the data writing circuit from applying data for the modified data word to the plurality of bit lines in response to detection that the modified data word is saturated.

18. The circuit of claim **1**, wherein the circuit comprises a data memory and wherein the memory array, the plurality of bit lines, the data sensing circuit, the data latching circuit, the data modification circuit and the data writing circuit are all component parts of the data memory which is clocked by said clock signal.

19. The circuit of claim **1**, wherein said circuit is a component of an image sensing circuit.

20. A circuit, comprising:

a memory array including memory cells forming a data word location accessed in response to a word line signal;

a plurality of bit lines associated with said memory cells; and

an input/output circuit for each bit line, comprising:

a sensing circuit configured to sense and latch data on the bit line;

an adder circuit configured to perform an addition operation, said adder circuit having a first input coupled to receive latched data from the sensing circuit, a second input coupled to receive data from the adder circuit of the input/output circuit for a lower significance bit line, a sum output, and a carry output coupled to supply data to the second input of the adder circuit of the input/output circuit for a higher significance bit line; and

a pass circuit configured to selectively pass the sum output of the adder circuit to the bit line for writing back to the data word location.

21. The circuit of claim **20**, wherein the sensing circuit comprises:

a sense amplifier circuit coupled to the bit line; and

a bit latch circuit coupled to said sense amplifier circuit.

22. The circuit of claim **20**, further comprising:

an end detect circuit configured to detect latching of the data on the bit line by the sensing circuit for the least significant bit line and generate an end signal; and

a dummy addition circuit configured to process the end signal and generate an addition complete signal;

wherein selective passage of the sum output of the adder circuit to the bit line by said pass circuit occurs in response to the addition complete signal.

23. The circuit of claim **22**, wherein the dummy addition circuit comprises a plurality of dummy adder circuits, one for each adder circuit of the input/output circuit, that are connected in series with each other, where the end signal is received as input and the addition complete signal is generated as output.

24. The circuit of claim **20**, wherein the pass circuit comprises:

a multiplexer circuit having a first input coupled to a bit of a data input port of the circuit, a second input coupled to the sum output of the adder circuit, and an output coupled to the bit line.

25. The circuit of claim **24**, wherein the multiplexer circuit is controlled in a first mode to pass the data at the sum output to the bit and is controlled in a second mode to pass the data at the data input port of the circuit.

26. The circuit of claim **20**, wherein the sum output of the adder circuit is blocked by the pass circuit from passing to the bit line when the carry output of the adder circuit for the input/output circuit of a most significant bit line indicates a saturation result.

27. The circuit of claim **20**, wherein the circuit comprises a data memory and wherein the memory array, the plurality of bit lines and the input/output circuits are all component parts of the data memory.

28. The circuit of claim **27**, wherein the data memory is clocked by a clock signal, and wherein the sensing and latching of the data by the sensing circuit, the addition operation performed by the adder circuit, and the selectively passing performed by the pass circuit all occur within a single cycle of the clock signal.

29. The circuit of claim **20**, wherein said data word location forms a bin for storing a histogram data word.

30. The circuit of claim **20**, further comprising a read timing circuit configured to control timing for actuation of the sensing circuit in response to completion of a dummy read operation from a dummy memory cell.

31. The circuit of claim **20**, further comprising an addition timing circuit configured to control actuation of said pass circuit in response to completion of a dummy addition operation.

32. The circuit of claim **20** further comprising a write timing circuit configured to control timing for resetting of the circuit in response to completion of a dummy write operation to a dummy memory cell.

33. The circuit of claim **20**, further comprising a decoder circuit configured to decode a memory address identifying said data word location and continuously assert said word line signal starting with accessing the data word location and ending after completion of the writing back to the data word location.

34. The circuit of claim **33**, further comprising a write timing circuit configured to perform a dummy write operation to a dummy memory cell, wherein said ending of the continuous assertion of said word line signal occurs in response to completion of said dummy write operation.

35. The circuit of claim **20**, wherein said circuit is a component of an image sensing circuit.

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