US 20080277694A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2008/0277694 A1

(43) Pub. Date: Nov. 13, 2008

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(54) **SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE**

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(21) Appl. No.: **11/746,437**

(22) Filed: **May 9, 2007**

Publication Classification

(51) **Int. Cl.**

H01L 27/095	(2006.01)
H01L 21/44	(2006.01)
H01L 29/76	(2006.01)

(52) **U.S. Cl.** .. **257/213**; 257/471; 438/571; 257/E29.226; 257/E21.476; 257/E27.068

(57) **ABSTRACT**

A semiconductor component that includes a Schottky device, an edge termination structure, a non-Schottky semiconductor device, combinations thereof and a method of manufacturing the semiconductor component. A semiconductor material includes a first epitaxial layer disposed on a semiconductor substrate and a second epitaxial layer disposed on the first epitaxial layer. The second epitaxial layer has a higher resistivity than the semiconductor substrate. A Schottky device and a non-Schottky semiconductor device are manufactured from the second epitaxial layer. In accordance with another embodiment, a semiconductor material includes an epitaxial layer disposed over a semiconductor substrate. The epitaxial layer has a higher resistivity than the semiconductor substrate. A doped region is formed in the epitaxial layer. A Schottky device and a non-Schottky semiconductor device are manufactured from the epitaxial layer.

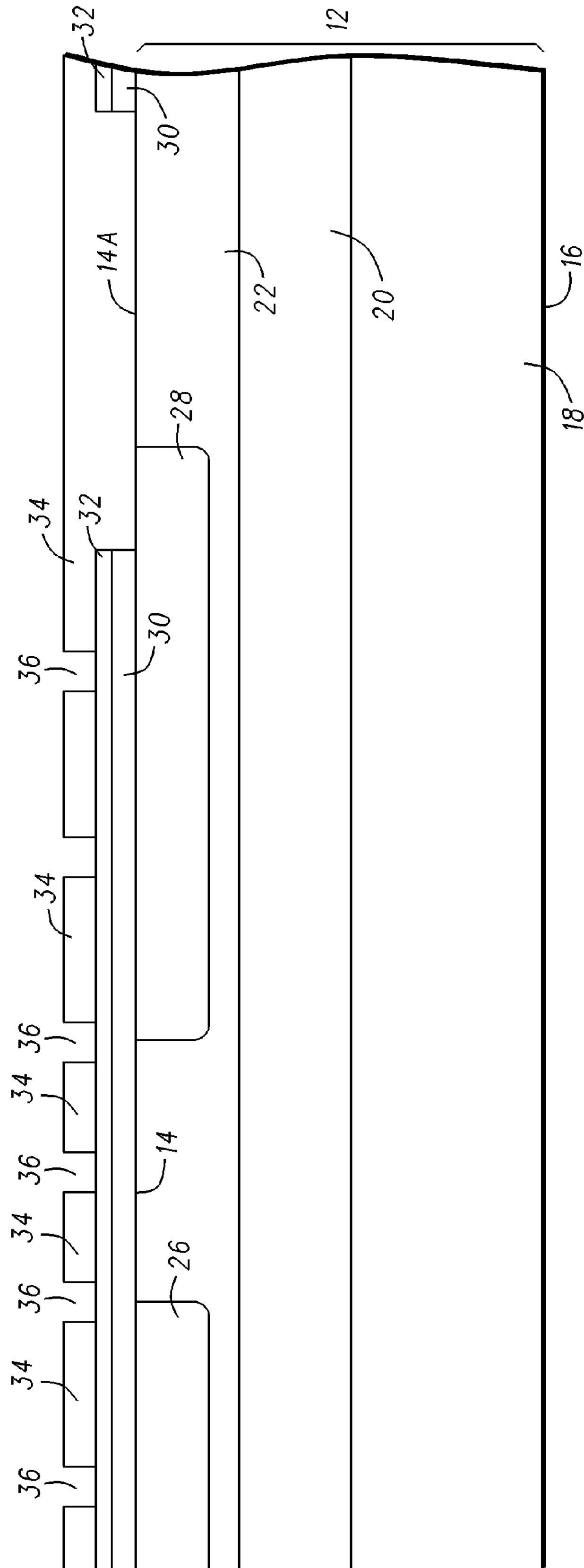

FIG. 1

10

FIG. 2

12
30
48A
22
20
16
18
28
30
55
55A
65
28
45
30
54
64
54A
28
44
30
28
53
63
53A
52
43
62
52A
51
42
61
51A
41
26
30
14
50
60
50A
30
26
40

10

FIG. 3

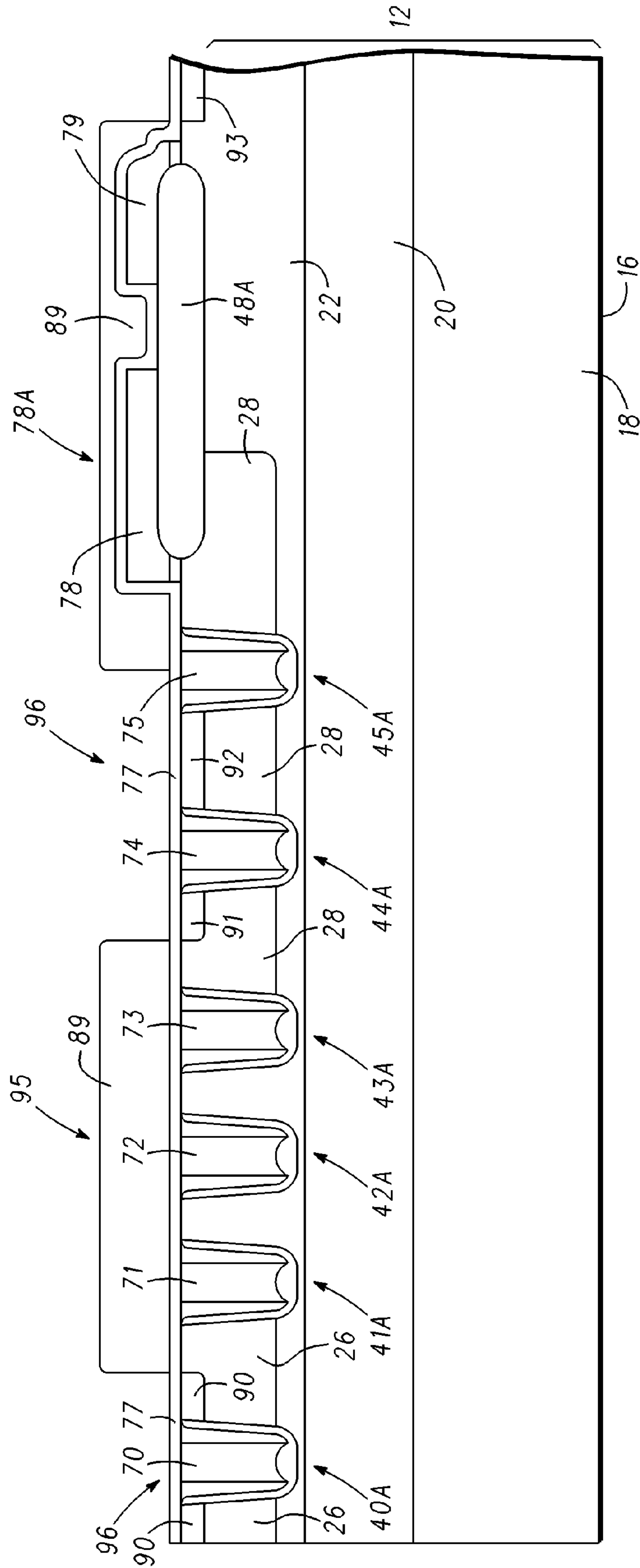

FIG. 4

10

FIG. 5

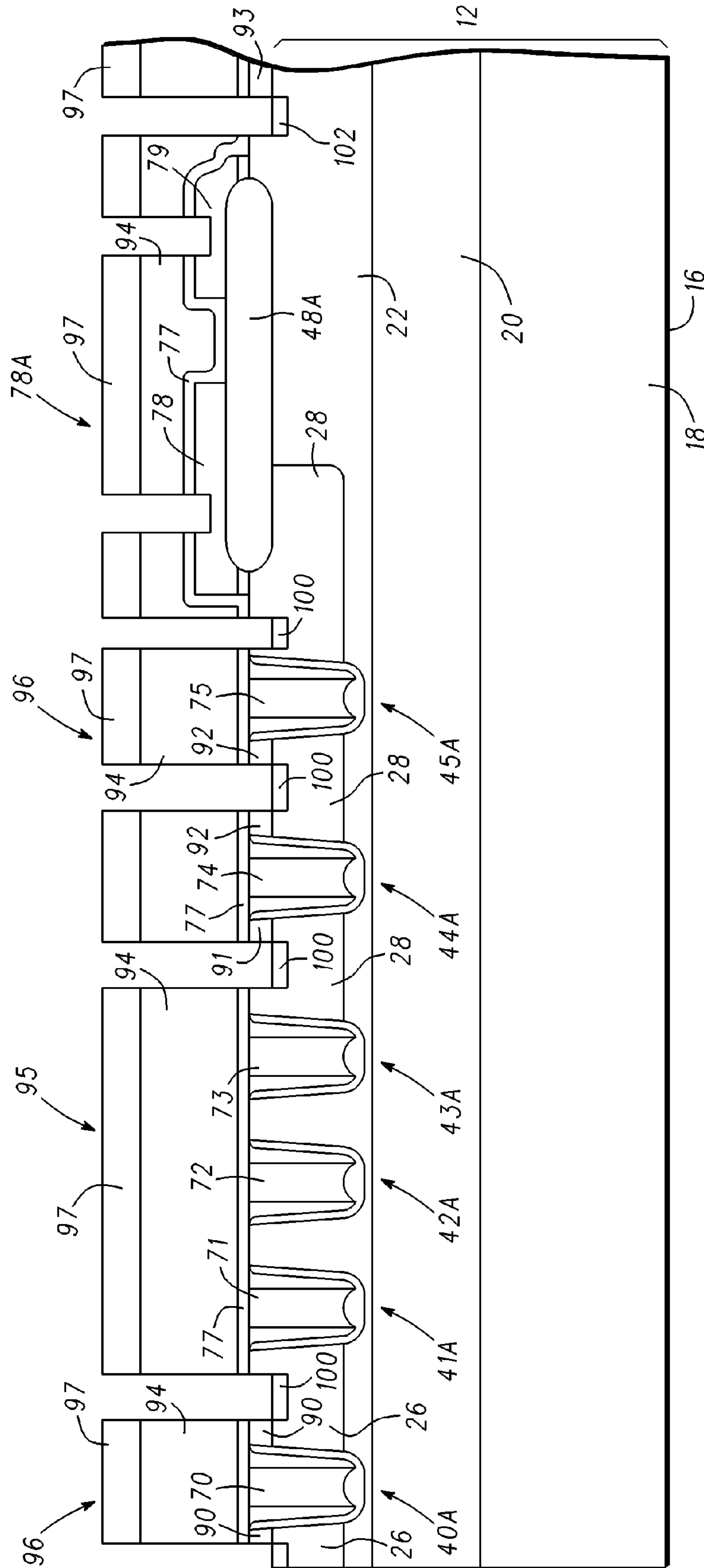

FIG. 6

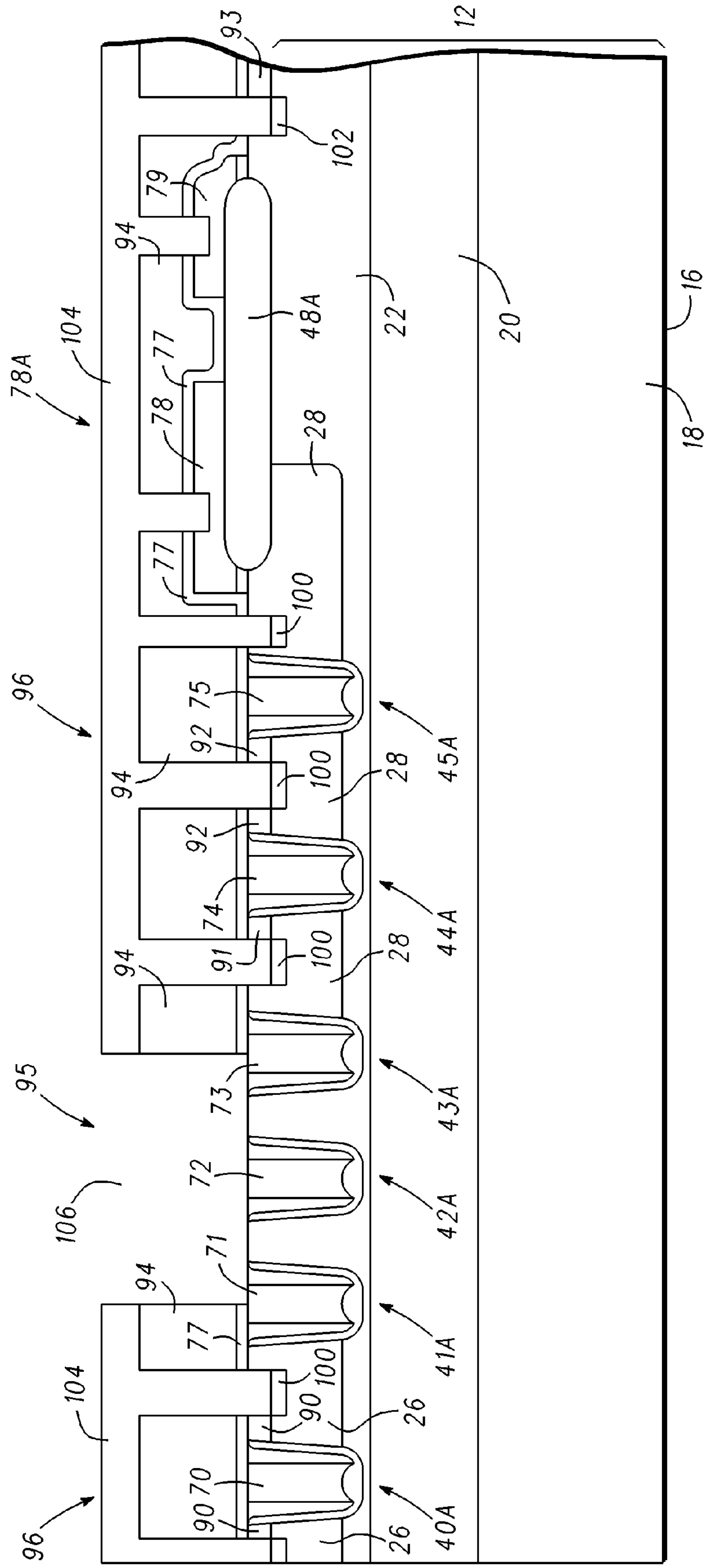

FIG. 7

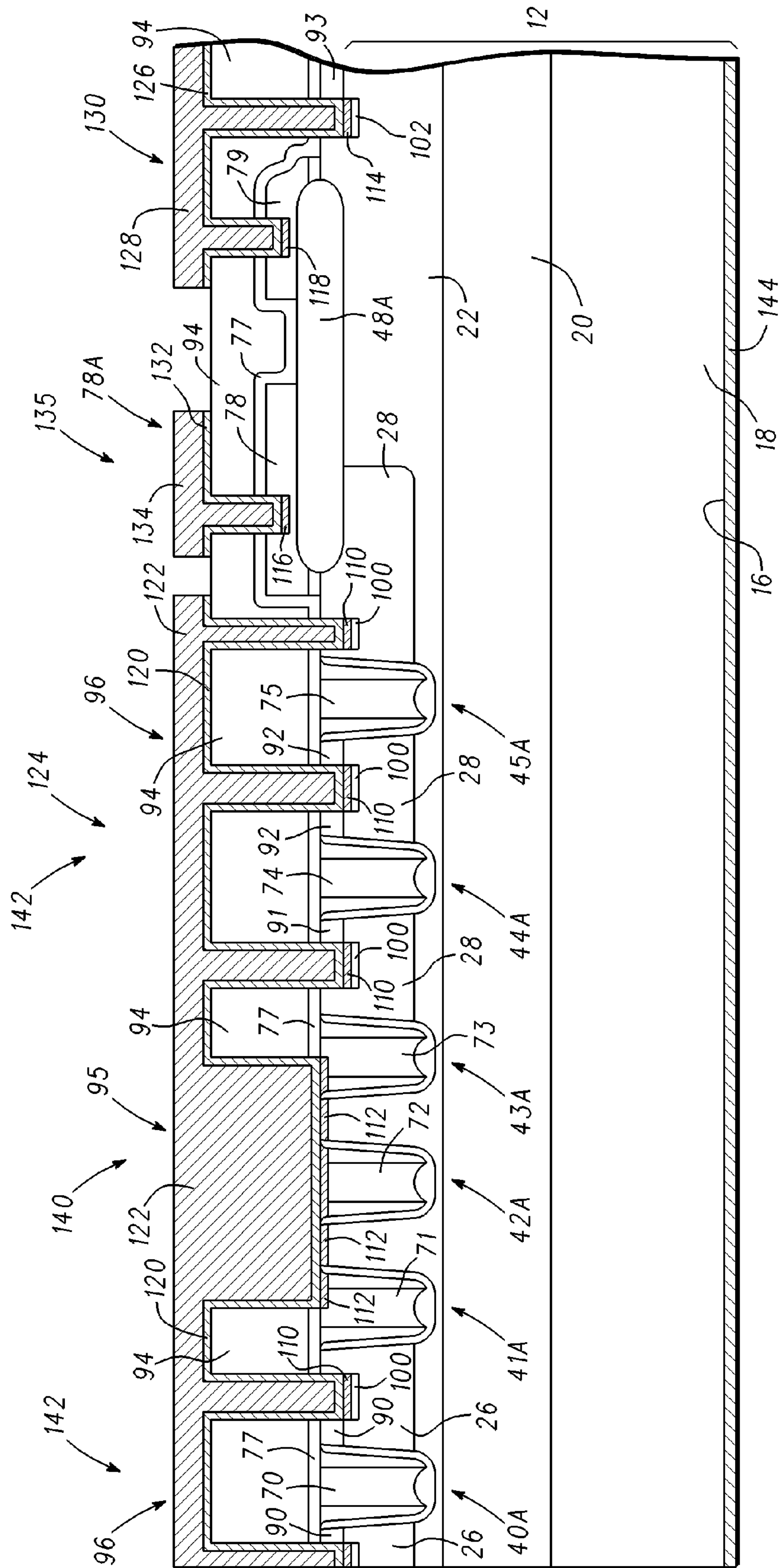

FIG. 8

150

FIG. 9

SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE

TECHNICAL FIELD

[0001] The present invention relates, in general, to semiconductor components and, more particularly, to power switching semiconductor components.

BACKGROUND

[0002] Metal-Oxide Semiconductor Field Effect Transistors ("MOSFETs") are a common type of power switching device. A MOSFET device includes a source region, a drain region, a channel region extending between the source and drain regions, and a gate structure provided adjacent to the channel region. The gate structure includes a conductive gate electrode layer disposed adjacent to and separated from the channel region by a thin dielectric layer. When a voltage of sufficient strength is applied to the gate structure to place the MOSFET device in an on state, a conduction channel region forms between the source and drain regions thereby allowing current to flow through the device. When the voltage that is applied to the gate is not sufficient to cause channel formation, current does not flow and the MOSFET device is in an off state.

[0003] Today's high voltage power switch market is driven by two major parameters: breakdown voltage ("BVdss") and on-state resistance ("Rdson"). For a specific application, a minimum breakdown voltage is required, and in practice, designers typically can meet a BVdss specification. However, this is often at the expense of Rdson. This trade-off in performance is a major design challenge for manufacturers and users of high voltage power switching devices. Another challenge arises because Power MOSFET devices have an inherent P-N diode between a P-type conductivity body region and an N-type conductivity epitaxial region. This inherent P-N diode turns on under certain operating conditions and stores charge across the P-N junction. When a sudden reverse bias is applied to the P-N diode, the stored charge produces a negative current flow until the charge is completely depleted. The time for the charge to become depleted is referred to as the reverse recovery time ("Trr") and delays the switching speed of the power MOSFET devices. In addition, the stored charge ("Qrr") also causes a loss in the switching voltage levels due to the peak reverse recovery current ("Irr") and the reverse recovery time.

[0004] Accordingly, it would be advantageous to have a semiconductor component that has a lower Rdson with a higher breakdown voltage and lower switching losses, i.e., lower Qrr losses, and a method for manufacturing the semiconductor component. It would be of further advantage for the semiconductor component to be cost efficient to manufacture.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention will be better understood from a reading of the following detailed description, taken in conjunction with the accompanying drawing figures, in which like reference numbers designate like elements and in which:

[0006] FIG. **1** is a cross-sectional view of a semiconductor component at an early stage of manufacture in accordance with an embodiment of the present invention;

[0007] FIG. **2** is a cross-sectional view of the semiconductor component of FIG. **1** at a later stage of manufacture;

[0008] FIG. **3** is a cross-sectional view of the semiconductor component of FIG. **2** at a later stage of manufacture;

[0009] FIG. **4** is a cross-sectional view of the semiconductor component of FIG. **3** at a later stage of manufacture;

[0010] FIG. **5** is a cross-sectional view of the semiconductor component of FIG. **4** at a later stage of manufacture;

[0011] FIG. **6** is a cross-sectional view of the semiconductor component of FIG. **5** at a later stage of manufacture;

[0012] FIG. **7** is a cross-sectional view of the semiconductor component of FIG. **6** at a later stage of manufacture;

[0013] FIG. **8** is a cross-sectional view of the semiconductor component of FIG. **7** at a later stage of manufacture; and

[0014] FIG. **9** is a cross-sectional view of a semiconductor component during manufacture in accordance with another embodiment of the present invention.

[0015] For simplicity of illustration and ease of understanding, elements in the various figures are not necessarily drawn to scale, unless explicitly so stated. In some instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present disclosure. The following detailed description is merely exemplary in nature and is not intended to limit the disclosure of this document and uses of the disclosed embodiments. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding text, including the title, technical field, background, or abstract.

DETAILED DESCRIPTION

[0016] Generally, the present invention provides a semiconductor component that may include a Schottky device, a semiconductor device such as a field effect transistor or a trench field effect transistor, a vertical power field effect transistor, a power field effect transistor, an edge termination structure, or combinations thereof. It should be noted that a power field effect transistor is also referred to as a vertical power device and a vertical field effect transistor is also referred to as a power device. In accordance with one embodiment, a semiconductor component is formed in a semiconductor material comprising two layers of epitaxial material disposed over a semiconductor substrate. The epitaxial layers and the semiconductor substrate have the same conductivity type, but the resistivity of the top epitaxial layer is greater than that of the semiconductor substrate. The Schottky device and a power field effect transistor are formed from the top epitaxial layer. The Schottky device is formed from a plurality of trench structures.

[0017] In accordance with another embodiment, the devices are formed in a semiconductor material comprising a single layer of epitaxial material disposed over a semiconductor substrate. The epitaxial layer and the semiconductor substrate have the same conductivity type, but the resistivity of the epitaxial layer is greater than that of the semiconductor substrate. A doped region of the same conductivity type as the epitaxial layer is formed in the epitaxial layer. The Schottky device is formed from a plurality of trench structures. Preferably, the distance between the trench structures in the single epitaxial layer embodiment is less than the distance between the trench structures in the double epitaxial layer embodiment. For example the distance between Schottky trench structures in the single epitaxial layer embodiment may be about 0.6 micrometers whereas the distance between Schot-

tky trench structures in the double epitaxial layer embodiment may be about 1.2 micrometers.

[0018] In accordance with another embodiment, an edge termination structure is formed from the top epitaxial layer of a semiconductor material comprising two epitaxial layers.

[0019] In accordance with another embodiment, an edge termination structure is formed from an epitaxial layer in which a doped region of the same conductivity type as the epitaxial layer has been formed.

[0020] FIG. **1** is a cross-sectional view of a portion of a semiconductor component **10** during manufacture in accordance with an embodiment of the present invention. What is shown in FIG. **1** is a semiconductor material **12** having opposing surfaces **14** and **16**. Surface **14** is also referred to as a front or top surface and surface **16** is also referred to as a bottom or back surface. In accordance with one embodiment, semiconductor material **12** comprises an epitaxial layer **20** disposed on a semiconductor substrate **18** and an epitaxial layer **22** disposed on epitaxial layer **20**. Preferably, substrate **18** is silicon that is heavily doped with an N-type dopant or impurity material and epitaxial layers **20** and **22** are silicon lightly doped with an N-type dopant. In an example of a semiconductor device having a 30 volt breakdown voltage, the resistivity of substrate layer **18** may be less than about 0.01 Ohm-centimeters ("Ω-cm"), the resistivity of epitaxial layer **20** may be greater than about 0.1 Ω-cm, and the resistivity of epitaxial layer **22** may be greater than about 0.2 Ω-cm and preferably greater than about 0.4 Ω-cm. Substrate layer **18** provides a low resistance conduction path for the current that flows through a power transistor and a low resistance electrical connection to a bottom drain conductor that is formed on bottom surface **16** of substrate **12**, a top drain conductor, or both. A region or layer doped with an N-type dopant is referred to as having an N-type conductivity or an N conductivity type and a region or layer doped with a P-type dopant is referred to as having a P-type conductivity or a P conductivity type.

[0021] P-type conductivity doped regions **26** and **28** are formed in epitaxial layer **22**. Doped regions **26** and **28** are laterally spaced apart from each other and preferably are doped with boron. Doped regions **26** and **28** may be formed using an implantation technique with a dose ranging from about 1×10^{13} ions per centimeter squared (ions/cm^2) to about 1×10^{14} ions/cm^2. The technique for forming doped regions **26** and **28** is not limited to an implantation technique.

[0022] A layer of dielectric material **30** is formed on or from epitaxial layer **22** and a protective layer **32** is formed on dielectric layer **30**. In accordance with one embodiment, the material of dielectric layer **30** is silicon dioxide and the material of protective layer **32** is silicon nitride. Preferably, the materials of layers **30** and **32** are selected so that protective layer **32** restricts oxygen diffusion and therefore protects underlying layers from oxidation. Although protective layer **32** is shown as a single layer of material, it can also be a multi-layered structure of different material types. A layer of photoresist (not shown) is formed on protective layer **32** and patterned to expose portions of protective layer **32**. The exposed portions of protective layer **32** and the portions of dielectric layer **30** under the exposed portions of protective layer **32** are anisotropically etched to expose a portion **14**A of surface **14**. Exposed portion **14**A will be oxidized during field oxide formation. The layer of photoresist is removed and another layer of photoresist is formed on protective layer **32** and on portion **14**A of surface **14**. The layer of photoresist is patterned to form a masking structure **34** having openings **36** that expose portions of protective layer **32**. It should be noted that a masking structure is also referred to as a mask.

[0023] Referring now to FIG. **2**, the exposed portions of protective layer **32** and the portions of dielectric layer **30** and semiconductor layer **22** below the exposed portions of protective layer **32** are anisotropically etched using, for example, a reactive ion etch to form trenches **40**, **41**, **42**, **43**, **44**, and **45**. Trenches **41-43** are typically referred to as Schottky trenches. In accordance with one embodiment, layers **32** and **30** are etched using an anisotropic fluorine based reactive ion etch and trenches **40-45** are formed in semiconductor layer **22** using a reactive ion etch with a chlorine or bromine chemistry or fluorine based techniques such as the Bosch process. Preferably, the distance that trenches **40-45** extend from surface **14** into epitaxial layer **22** is greater than the distance that doped regions **26** and **28** extend from surface **14** into epitaxial layer **22**. Although trenches **40-45** are shown as being within epitaxial layer **22**, this is not a limitation of the present invention. For example, trenches **40-45** may extend through epitaxial layer **22** and into epitaxial layer **20**.

[0024] Trenches **40-45** generally have sidewalls that are aligned with the edges of the openings through layers **32** and **30**. The sidewalls are oxidized to form an oxide layer that extends into the sidewalls and the bottoms of each trench **40-45** causing the sidewalls to be pulled-back or recessed under protective layer **32**. The oxide is removed from the sidewalls and the bottoms of trenches **40-45**. The amount of the pull-back or recess usually is determined by the thickness of the oxide layers and the amount of oxide that is removed. Preferably, each oxide layer is formed to have a thickness of about 100 nanometers ("nm"). During the removal of each oxide layer from the sidewalls, a portion of dielectric layer **30** is also removed from under the portions of protective layer **32** that are adjacent to the openings in protective layer **32**. Typically, the process for removing the oxide layers is preferential to oxide and follows the portions of dielectric layer **30** that are abutting the oxide layers.

[0025] Removing the portions of dielectric layer **30** also removes portions of the trench sidewalls near surface **14** giving a curvature in the portions of the trench sidewalls near surface **14**. The removal of the portion of dielectric layer **30** underlying protective layer **32** leaves portions of protective layer **32** overhanging the openings of trenches **40-45**. The overhanging portions serve as ledges. The undercutting of protective layer **32** also causes the widths of the mouths of trenches **40-45** proximal to surface **14** to be wider than the widths of trenches **40-45** along the portions of their sidewalls that are distal from surface **14**.

[0026] Silicon dioxide layers **50**, **51**, **52**, **53**, **54**, and **55** are formed along the sidewalls and bottoms of trenches **40-45**, respectively, and a silicon dioxide layer **48** is formed on exposed portion **14**A of surface **14**. In a preferred embodiment, the portions of silicon dioxide layers **50**, **54**, and **55** formed along the sidewalls of trenches **40**, **44**, and **45**, respectively, serve as gate oxide layers for power transistors. Typically, the thickness of each silicon dioxide layer **50-55** ranges from about 20 nm to about 100 nm. A conformal layer of polysilicon having a thickness ranging from about 20 nm to about 50 nm is formed on silicon dioxide layers **50-55**, protective layer **32**, and oxide layer **48**. The polysilicon layer is anisotropically etched to expose the portions of silicon dioxide layers **50-55** at the bottoms of the respective trenches **40-45**. After the anisotropic etch, portions **60**, **61**, **62**, **63**, **64**,

and **65** of the polysilicon layer remain disposed on the portions of silicon dioxide layers **50-55** adjacent the sidewalls of trenches **40-45**, respectively.

[0027] A protective layer (not shown) is formed on layer **32**, oxide layer **48**, polysilicon portions **60-65**, and the exposed portions of silicon dioxide layers **50-55** at the bottom of trenches **40-45**, respectively. The protective layer is generally formed from the same material as layer **32**. The protective layer is anisotropically etched to form portions **80**, **81**, **82**, **83**, **84**, **85**, and **88** on polysilicon portions **60-65** and oxide layer **48**, respectively.

[0028] Referring now to FIG. **3**, the thicknesses of oxide layers **50-55** along the bottoms of trenches **40-45** are increased to form thick oxide portions **50**A, **51**A, **52**A, **53**A, **54**A, and **55**A, respectively. The increased thicknesses are formed without substantially increasing or changing the thicknesses of oxide layers **50-55** along the sidewalls of the respective trenches **40-45**. Thick oxide layers **50**A-**55**A are formed by further oxidizing the material at the bottoms of trenches **40-45**. This oxidation also oxidizes the portions of semiconductor material **22** under oxide layer **48** to form field oxide **48**A. In accordance with an embodiment of the present invention, a wet oxidation in a hydrogen and oxygen ambient at a temperature of about 1,000 degrees Celsius (° C.) is performed to form portions **50**A-**55**A, which increases the thicknesses of oxide layers **50-55** near the bottoms of trenches **40-45**, respectively, by an amount ranging from about 200 nm to about 400 nm. Silicon nitride layer **32** and portions **80**, **81**, **82**, **83**, **84**, **85**, and **88** are removed using, for example, hot phosphoric acid. The method for removing silicon nitride layer **32** and portions **80-85** and **88** is not a limitation of the present invention.

[0029] Referring now to FIG. **4**, a layer of polysilicon (not shown) is formed in trenches **40-45**, on the remaining portions of dielectric layer **30**, and on field oxide **48**A. Typically, the layer of polysilicon is in-situ doped with a dopant of N-type conductivity, or blanket implanted with a dopant of N-type conductivity followed by driving-in the dopant. The conductivity type of the dopant is not a limitation of the present invention. The polysilicon layer is etched leaving polysilicon plugs **70**, **71**, **72**, **73**, **74**, and **75** in trenches **40-45**. It should be noted that polysilicon plugs **70-75** include polysilicon portions **60-65**, respectively. Trenches **40-45** in combination with polysilicon plugs **70-75** form polysilicon filled trenches **40**A, **41**A, **42**A, **43**A, **44**A, and **45**A, respectively. It should be noted that trenches **40-45** may be fully or partially filled with polysilicon and that both types of filling are referred to as polysilicon filled trenches. In addition, portions **78** and **79** of the polysilicon layer remain after the etch. Polysilicon portion **78** remains over a portion of field oxide **48**A and over a portion of oxide layer **30** that is between field oxide **48**A and polysilicon filled trench **45**A. Polysilicon portion **78** in combination with the portion of doped region **28** between polysilicon filled trench **45**A and field oxide **48**A form a field plate **78**A. Field plate **78**A is also referred to as an edge termination structure. It should be understood that the architecture of the edge termination structure is not a limitation of the present invention. Polysilicon portion **79** remains over a portion of field oxide **48**A and a portion of oxide layer **30** that is adjacent to field oxide **48**A. Polysilicon portion **79** serves as drain polysilicon. The etch chemistry is adjusted to remove the portions of dielectric layer **30** unprotected by polysilicon portions **78** and **79** and the portions of dielectric layers **50-55** and polysilicon portions **60-65** adjacent to the portions of dielectric layer **30** that are unprotected by polysilicon portions **78** and **79**. A screen oxide **77** is formed on polysilicon plugs **70-75**, polysilicon portions **78** and **79**, doped regions **26** and **28**, field oxide **48**A, and the portions of epitaxial layer **22** adjacent field oxide **48**A.

[0030] A layer of photoresist (not shown) is formed over screen oxide **77** and polysilicon portions **78** and **79**. The layer of photoresist is patterned to form a masking structure **89** that protects polysilicon plugs **71**, **72**, and **73**, polysilicon portion **78**, polysilicon portion **79**, and a portion of screen oxide **77** between polysilicon portions **78** and **79**. Thus, masking structure **89** protects Schottky region **95** and polysilicon portions **78** and **79**. The portions of the semiconductor material that are unprotected by masking structure **89** may serve as non-Schottky device regions **96**. When the non-Schottky device is a Field Effect Transistor ("FET") or a MOSFET, non-Schottky device regions **96** may be referred to as FET regions or MOSFET regions. Semiconductor device or field effect transistors that are not Schottky devices are referred to as non-Schottky devices or non-Schottky field effect transistors.

[0031] Still referring to FIG. **4**, an impurity material of N-type conductivity is implanted into the portions of polysilicon filled trenches **40**A-**45**A and epitaxial layer **22** that are unprotected by masking structure **89** to form doped regions **90** adjacent to polysilicon filled trench **40**A, doped region **91** adjacent to polysilicon filled trench **44**A, doped region **92** between polysilicon filled trenches **44**A and **45**A, and doped region **93** adjacent to and laterally spaced apart from field oxide **48**A. Doped regions **90**, **91**, and **92** serve as source regions for power FETs. It should be noted that the doping step that forms doped regions **90-93** also dopes polysilicon plugs **70** and **74-75**. For the sake of clarity the dopant or impurity material is not shown in polysilicon plugs **70**, **74**, and **75**.

[0032] Referring now to FIG. **5**, masking structure **89** is removed and a layer of dielectric material **94** is formed over screen oxide **77**. Dielectric layer **94** typically is referred to as an interlayer dielectric ("ILD") layer. A layer of photoresist is formed on ILD layer **94** and patterned to a form masking structure **97** having openings **98** that expose portions of ILD layer **94** that are over a portion of doped region **26** adjacent to polysilicon filled trench **40**A. Openings **98** also expose portions of ILD layer **94** over the portion of doped region **28** between polysilicon filled trenches **43**A and **44**A and the portion of doped region **28** between polysilicon filled trenches **44**A and **45**A. Openings **98** also expose portions of ILD layer **94** over polysilicon portions **78** and **79**, over doped region **93**, and between polysilicon filled trench **45**A and field oxide region **48**A.

[0033] Referring now to FIG. **6**, the exposed portions of ILD layer **94** and the portions of screen oxide **77** under the exposed portions of ILD layer **94** are anisotropically etched to expose portions of doped regions **26**, **28**, and **93** and polysilicon portions **78** and **79**. Openings are formed in the exposed portions of doped regions **26**, **28**, and **93** and polysilicon portions **78** and **79** using, for example, an anisotropic etch. The opening in doped region **93** exposes a portion of epitaxial layer **22**. Techniques for anisotropically etching dielectric material and semiconductor material are known to those skilled in the art. It should be understood that the techniques for etching ILD layer **94**, screen oxide **77** and doped regions **26**, **28**, and **93** and polysilicon portions **78** and **79** are not limited to anisotropic etching techniques. For example, they can be performed using isotropic etching techniques. An

impurity material of P-type conductivity is implanted into the exposed portions of doped regions **26** and **28** to form doped regions **100**. The P-type conductivity impurity material is also implanted into the exposed portion of epitaxial layer **22** to form a doped region **102**. Doped regions **100** help to form good body contact between doped regions **26** and **28** and a source conductor metal described with reference to FIG. **8**. The exposed portions of polysilicon portions **78** and **79** are also doped with the impurity material forming doped regions **100**. For the sake of clarity the dopant or impurity material is not shown in polysilicon portions **78** and **79**.

[0034] Referring now to FIG. **7**, masking structure **97** is removed and another layer of photoresist (not shown) is formed over ILD layer **94** and in the openings formed in doped regions **26** and **28**, epitaxial layer **22**, and polysilicon portions **78** and **79**. The layer of photoresist is patterned to form a masking structure **104** having an opening **106** that exposes the portion of ILD layer **94** between polysilicon filled trenches **41**A and **43**A and the portion of ILD layer **94** above portions of polysilicon filled trenches **41**A and **43**A. The exposed portion of ILD layer **94** and the portion of screen oxide **77** below the exposed portion of ILD layer **94** are anisotropically etched using, for example, a reactive ion etch to expose polysilicon plugs **71**, **72**, and **73**. It should be noted that the etch is not limited to being an anisotropic etch but can also be an isotropic etch. Masking structure **104** is removed using a technique known to those skilled in the art.

[0035] Referring now to FIG. **8**, a layer of refractory metal (not shown) is conformally deposited over the exposed portions of doped regions **100** and **102**, polysilicon plugs **71-73**, polysilicon portions **78** and **79**, and on ILD layer **94**. By way of example, the refractory metal is titanium having a thickness ranging from about 100 Å to about 1,000 Å. The refractory metal is heated to a temperature ranging from about 350° C. to about 700° C. The heat treatment causes the titanium to react with the silicon to form titanium silicide in all regions in which the titanium is in contact with silicon or polysilicon. Thus, titanium silicide layers **110** are formed from doped regions **100**, a titanium silicide layer **112** is formed from polysilicon plugs **71-73** and portions of epitaxial layer **22** that are between polysilicon plugs **71-73**, a titanium silicide layer **114** is formed from a portion of doped region **102**, a titanium silicide layer **116** is formed from polysilicon portion **78**, and a titanium silicide layer **118** is formed from polysilicon portion **79**. The portions of the titanium over ILD layer **94** remain unreacted. Although the portions of the titanium layer over the exposed portions of oxide layers **51-53** do not form silicide, they are shown as being continuous with silicide layer **112** for the sake of clarity. As those skilled in the art are aware, silicide layers that are self aligned are referred to as salicide layers. Thus, layers **110**, **112**, **114**, **116**, and **118** may be referred to as salicide layers. It should be understood that the type of silicide is not a limitation of the present invention. For example, other suitable silicides include nickel silicide, platinum silicide, cobalt silicide, or the like. As those skilled in the art are aware, silicon is consumed during the formation of silicide and the amount of silicon consumed is a function of the type of silicide being formed.

[0036] A barrier layer is formed in contact with titanium silicide layers **110**, **112**, **114**, **116**, and **118** and over ILD layer **94**. Suitable materials for the barrier layer include titanium nitride, titanium tungsten, or the like. A metal layer such as, for example, aluminum, is formed in contact with the barrier layer. A layer of photoresist (not shown) is formed on the metal layer and patterned to expose portions of the metal layer. The exposed portions of the metal layer and the portions of the barrier layer below the exposed portions of the metal layer are etched to form electrical conductors. More particularly, silicide layers **110**, a portion **120** of the barrier layer, and a portion **122** of the metal layer cooperate to form a source contact and portions of silicide layers **112**, another portion **120** of the barrier layer, and another portion **122** of the metal layer cooperate to form a Schottky contact. The source contact and the Schottky contact share a common metallization system and are therefore referred to as a source electrode **124**. In addition, silicide layers **114** and **118**, portion **126** of the barrier layer, and portion **128** of the metal layer form a top side drain contact **130** and silicide layer **116**, portion **132** of the barrier layer, and portion **134** of the metal layer form a gate contact **135**. Source contact **124** also serves as an anode for a Schottky diode **140** and as source and body contacts for power FETs **142**. A conductor **144** is formed in contact with surface **16** and serves as the cathode of Schottky diode **140** and as a bottom side drain contact for power FETs **142**. Suitable metallization systems for conductor **144** include a gold alloy, titanium-nickel-gold, titanium-nickel-silver, or the like. It should be understood that the type of Schottky device manufactured in Schottky region **95** is not limited to being a Schottky diode. Other types of Schottky devices may also be manufactured in Schottky region **95**. It should be further understood that the type of semiconductor device manufactured from semiconductor material **12** is not limited to being a power FET or a trench FET.

[0037] FIG. **9** is a cross-sectional view of a semiconductor component **150** in accordance with another embodiment of the present invention. What is shown in FIG. **9** is a semiconductor material **152** having opposing surfaces **154** and **16**. Surface **154** is also referred to as a front or top surface and surface **16** is also referred to as a bottom or back surface. In accordance with one embodiment, semiconductor material **152** comprises an epitaxial layer **158** disposed on a semiconductor substrate **18**. Substrate **18** was described with reference to FIG. **1**. Preferably, substrate **18** is silicon that is heavily doped with an N-type dopant or impurity material and epitaxial layer **158** is silicon lightly doped with an N-type dopant. By way of example, the resistivity of substrate layer **18** typically is less than about 0.01 Ω-cm and the resistivity of epitaxial layer **158** typically is greater than about 0.2 Ω-cm and preferably greater than about 0.4 Ω-cm. Substrate layer **18** provides a low resistance conduction path for the current that flows through a power transistor and a low resistance electrical connection to a drain conductor that is formed on bottom surface **16** of substrate **12**. Thus, semiconductor material **152** is similar to semiconductor material **12** except that a single epitaxial layer is formed over semiconductor substrate **18**. In addition, a doped region **160** is formed in the portions of epitaxial layer **158** that are below the source and body regions of power FETs **162** and the anode region of a Schottky diode **164**. By way of example, doped region **160** is formed by implanting an impurity material of N-type conductivity into epitaxial layer **158** at a dose ranging from about 3×10^{12} atoms/cm^2 to about 1×10^{14} atoms/cm^2 and at an implant energy ranging from about 1 Mega electron-volt ("MeV") to about 5 MeV.

[0038] By now it should be appreciated that a semiconductor component comprising a Schottky device, a non-Schottky semiconductor device, an edge termination structure, or combinations thereof have been provided. An advantage of form-

ing two epitaxial layers over the semiconductor substrate such that the upper epitaxial layer has a higher resistivity than the lower epitaxial layer and both epitaxial layers have a higher resistivity than the substrate is that a Schottky contact can be formed to the higher resistivity upper epitaxial layer and portions of field effect transistors can be formed from the lower resistivity lower epitaxial layer. Thus, a Schottky device and a field effect transistor can be formed from the same semiconductor material. Forming the Schottky contact to the higher resistivity upper epitaxial layer lowers the leakage current that occurs at or during pinch-off and forming the body of the field effect transistors from the higher resistivity upper epitaxial layer does not impact the on resistance but rather helps enhance the breakdown voltage. These advantages also occur in embodiments having a single epitaxial layer that has a doped region such as doped region **160**. In addition, the dual layer epitaxial semiconductor material or the single layer epitaxial semiconductor material with doped region **160** increases the edge breakdown voltage of the field effect transistors.

[0039] Although certain preferred embodiments and methods have been disclosed herein, it will be apparent from the foregoing disclosure to those skilled in the art that variations and modifications of such embodiments and methods may be made without departing from the spirit and scope of the invention. For example, the masks or masking structures may be comprised of a single mask or masking structure with a plurality of openings formed therein or there may be a plurality of masks or masking structures spaced apart by one or more openings. In addition, the semiconductor devices may be vertical devices as such as power FET's **142** and **162** or lateral devices. It is intended that the invention shall be limited only to the extent required by the appended claims and the rules and principles of applicable law.

What is claimed is:

1. A method for manufacturing a semiconductor component, comprising:

providing a semiconductor material which includes a first epitaxial layer disposed over a substrate and a second epitaxial layer disposed over a portion of the first epitaxial layer; and

forming a Schottky device from a first portion of the second epitaxial layer.

2. The method of claim **1**, wherein providing the semiconductor material includes providing the substrate, the first epitaxial layer, and the second epitaxial layer of a first conductivity type.

3. The method of claim **2**, wherein the resistivity of the second epitaxial layer is greater than the resistivity of the first epitaxial layer.

4. The method of claim **3**, further including forming a power device from a second portion of the second epitaxial layer.

5. The method of claim **4**, wherein forming the power device comprises forming a power field effect transistor.

6. The method of claim **4**, wherein forming the power device comprises forming a vertical power device.

7. The method of claim **1**, further including forming an edge termination structure over a second portion of the second epitaxial layer.

8. A method for manufacturing a semiconductor component, comprising:

providing a semiconductor substrate of a first conductivity type;

forming a first epitaxial layer of the first conductivity type and a first resistivity over the semiconductor substrate;

forming a second epitaxial layer of the first conductivity type and a second resistivity over the first epitaxial layer, the second resistivity greater than the first resistivity; and

forming a Schottky device from a first portion of the second epitaxial layer.

9. The method of claim **8**, further including forming a first semiconductor device from a second portion of the second epitaxial layer.

10. The method of claim **9**, wherein the first semiconductor device is a field effect transistor.

11. The method of claim **10**, wherein the field effect transistor is a power field effect transistor.

12. The method of claim **8**, wherein the Schottky device is a Schottky diode.

13. The method of claim **8**, further including forming an edge termination structure over a second portion of the second epitaxial layer.

14. A method for manufacturing a semiconductor component, comprising:

providing a semiconductor material which comprises an epitaxial layer of a first conductivity type and a first resistivity disposed over a substrate;

forming a doped region of the first conductivity type and a second resistivity in the epitaxial layer; and

forming an edge termination structure over a first portion of the epitaxial layer.

15. The method of claim **14**, further including forming a semiconductor device from a second portion of the epitaxial layer, the second portion over the doped region.

16. The method of claim **15**, further including forming a field effect transistor as the semiconductor device.

17. The method of claim **14**, further including forming a Schottky device from a second portion of the epitaxial layer, the second portion over the doped region.

18. A semiconductor component, comprising:

a semiconductor substrate of a first conductivity type;

a first epitaxial layer of the first conductivity type and a first resistivity over the semiconductor substrate;

a second epitaxial layer of the first conductivity type and a second resistivity over the first epitaxial layer, the second resistivity greater than the first resistivity; and

an edge termination structure disposed on a first portion of the second epitaxial layer.

19. The semiconductor component of claim **18**, further including a semiconductor device disposed in a second portion of the second epitaxial layer.

20. The semiconductor component of claim **18**, further including a Schottky device disposed in a third portion of the second epitaxial layer.

21. A semiconductor component, comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial layer of the first conductivity type and a first resistivity over the semiconductor substrate;

a doped region of the first conductivity type disposed in a first portion of the epitaxial layer; and

a Schottky device disposed in a second portion of the epitaxial layer, the second portion over the first portion.

22. The semiconductor component of claim **21**, further including a field effect transistor disposed in a third portion of the epitaxial layer.

23. A semiconductor component, comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial layer of the first conductivity type and a first resistivity over the semiconductor substrate;

a doped region of the first conductivity type disposed in a first portion of the epitaxial layer; and

an edge termination structure disposed on a second portion of the epitaxial layer.

24. The semiconductor component of claim **23**, further including a field effect transistor disposed in a third portion of the epitaxial layer.

25. The semiconductor component of claim **24**, further including a Schottky device disposed in a fourth portion of the epitaxial layer.

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