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(54) **SILICON CARBIDE SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME**

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(52) **U.S. Cl.**

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(57) **ABSTRACT**

A silicon carbide semiconductor device includes a silicon carbide substrate, a gate insulating film, a gate electrode, an interlayer insulating film, and a gate interconnection. The silicon carbide substrate includes: a first impurity region; a second impurity region provided on the first impurity region; and a third impurity region provided on the second impurity region so as to be separated from the first impurity region. A trench has a side portion and a bottom portion, the side portion extending to the first impurity region through the third impurity region and the second impurity region, the bottom portion being located in the first impurity region. When viewed in across section, the interlayer insulating film extends from above the third impurity region to above the gate electrode so as to cover the corner portion.

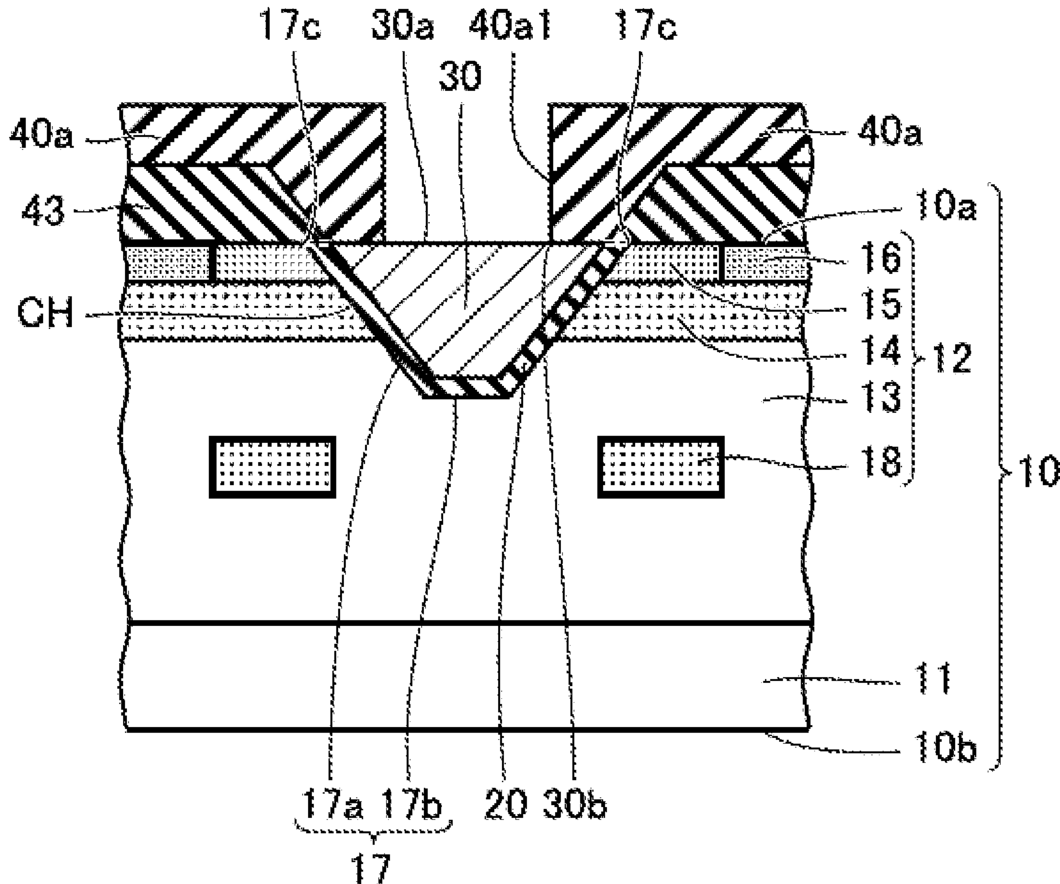


FIG.1

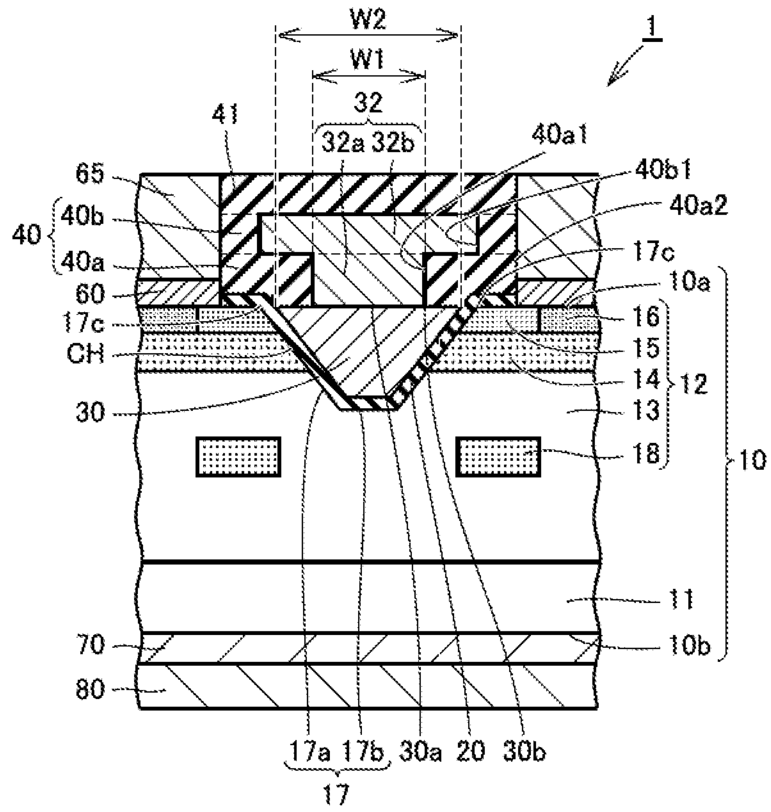


FIG.2

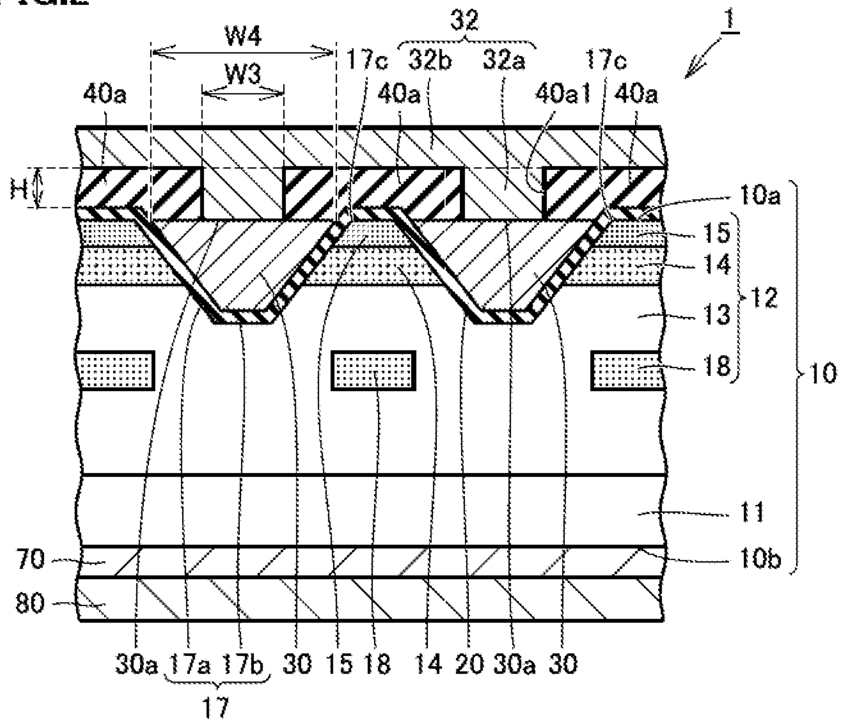


FIG.3

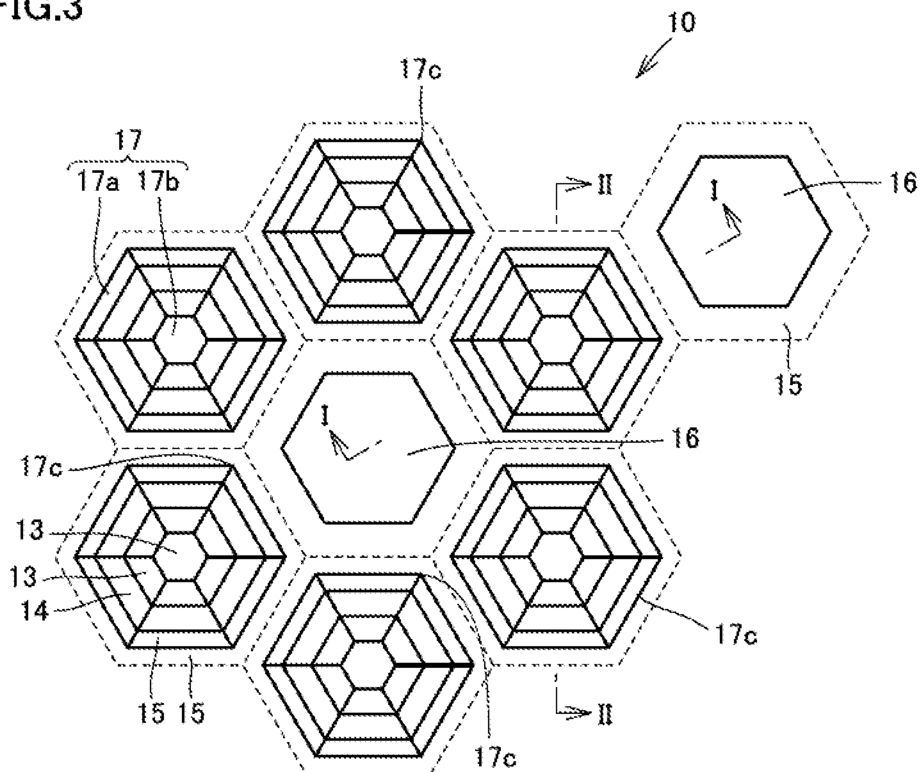


FIG.4

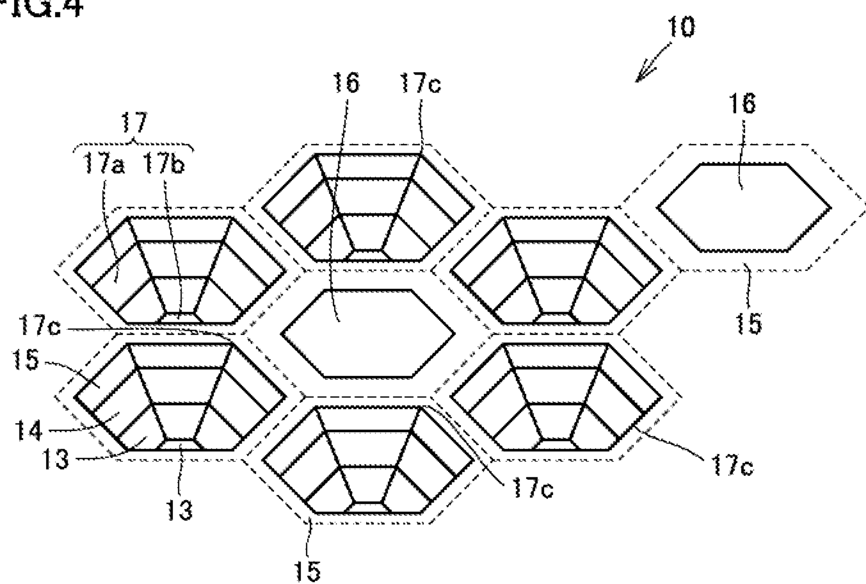


FIG.5

1
32
40a 40a 17c 32c 32d 40a1 17c 40a
10a
15
14
12
13
18
10
11
70
10b
80
30a 17a 17b 30 15 18 14 20 30a 30
17

FIG.6

1
32
40a 40a 17c 32b 32a 40a1 17c
33
41
40a
10a
15
14
12
13
18
10
11
70
10b
80
30a 17a 17b 30 15 18 14 20 30a 30
17

FIG.7

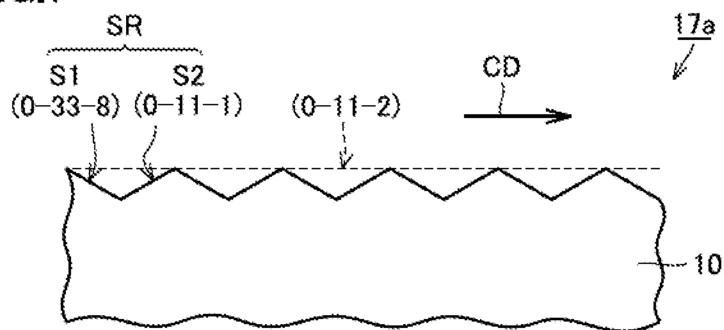


FIG.8

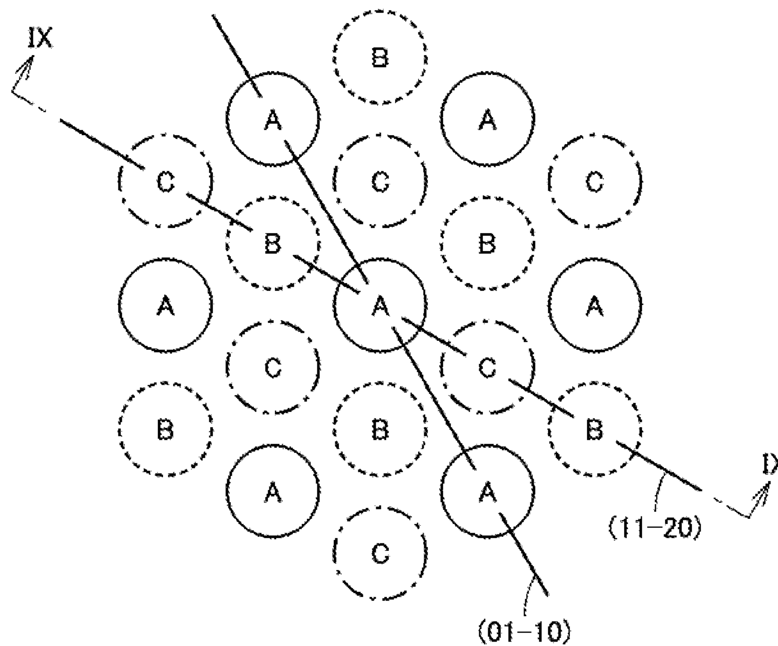


FIG.9

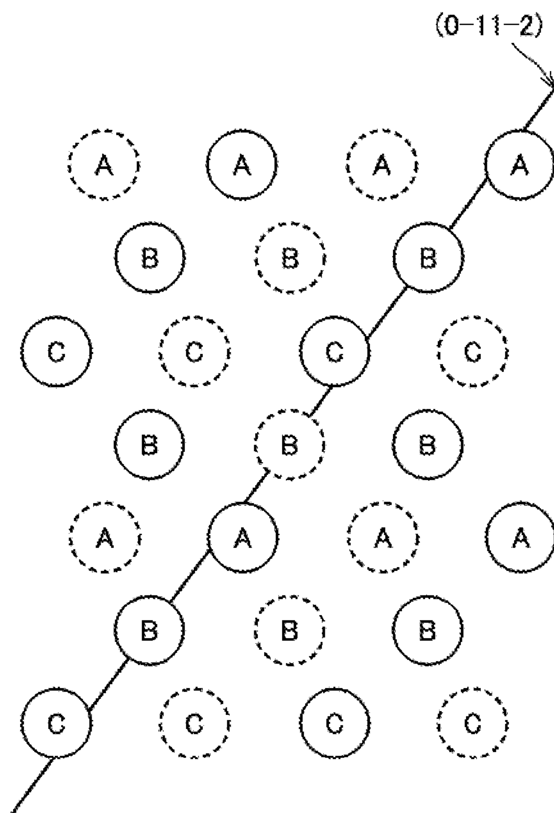


FIG.10

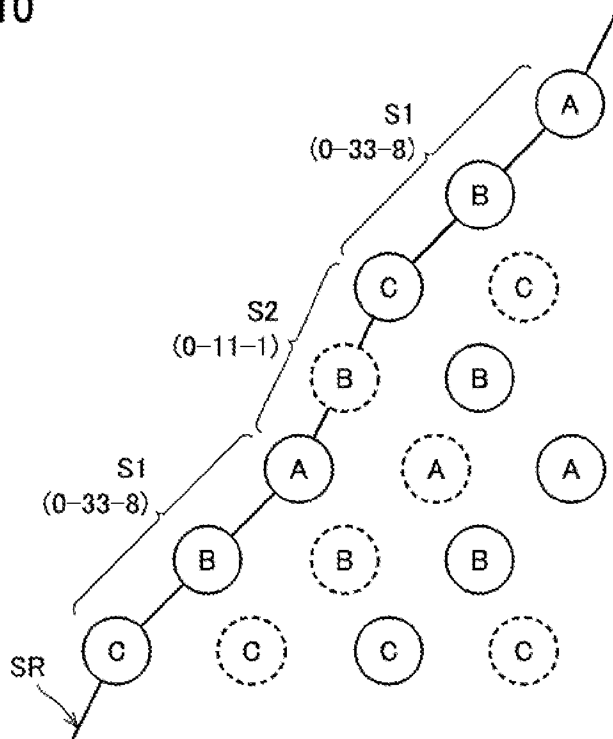


FIG.11

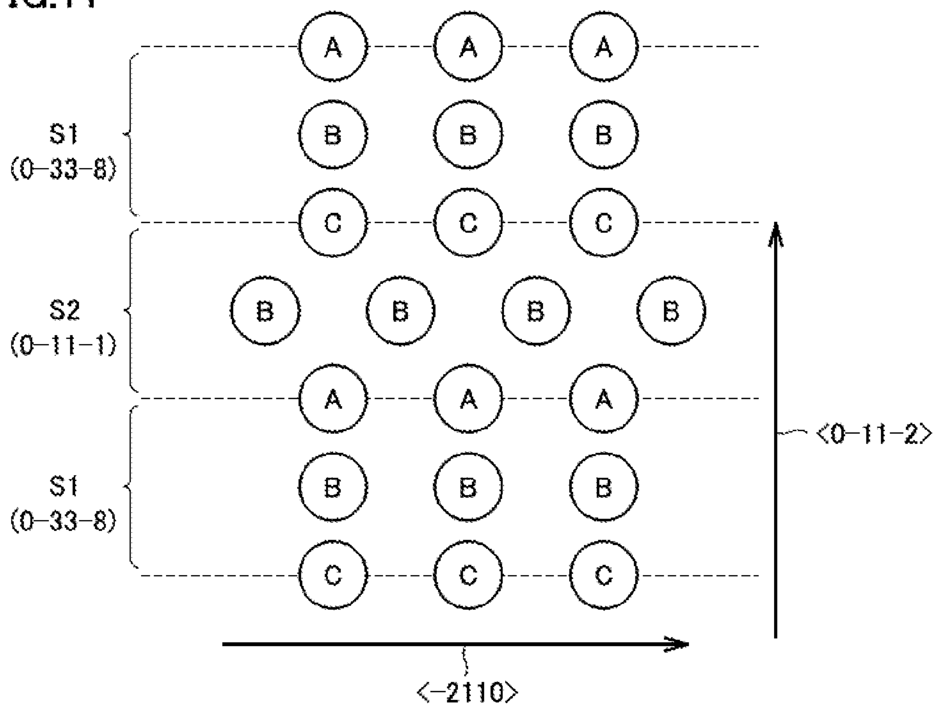


FIG.12

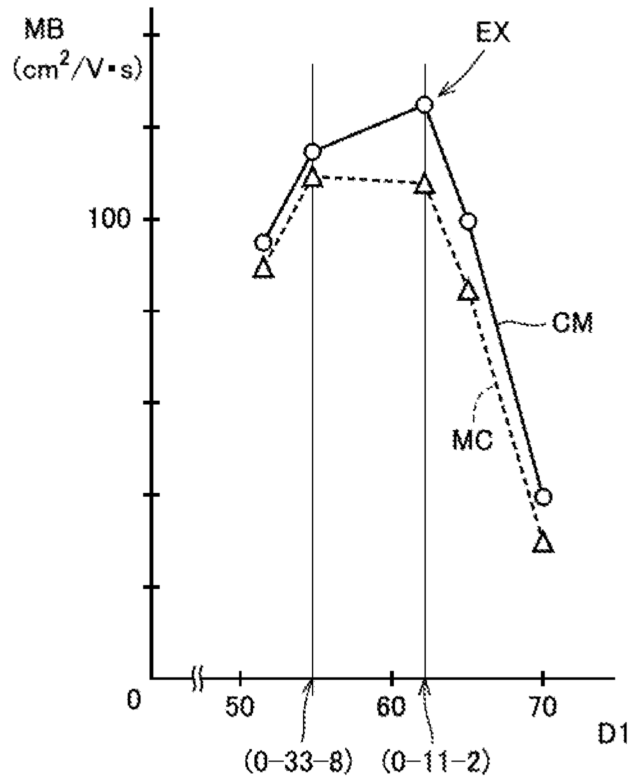


FIG.13

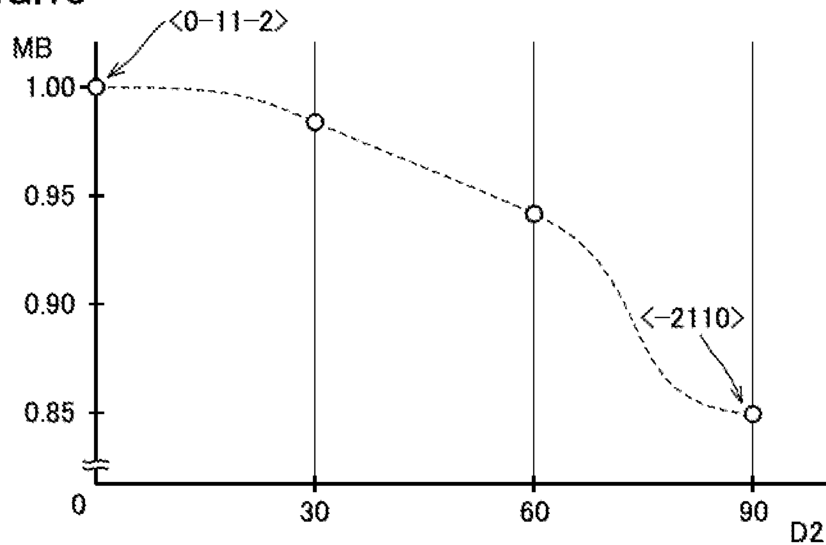


FIG.14

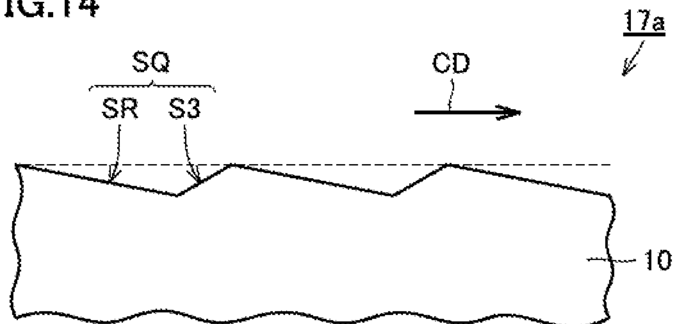


FIG.15

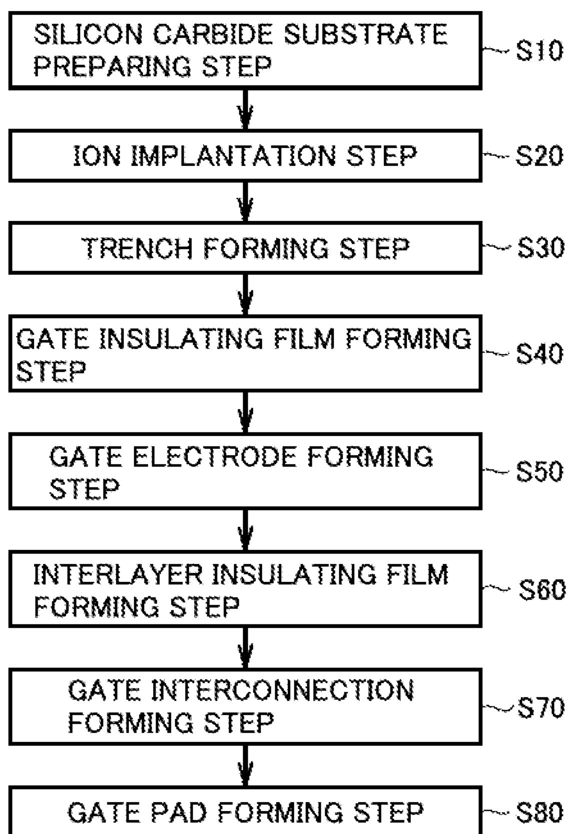


FIG.16

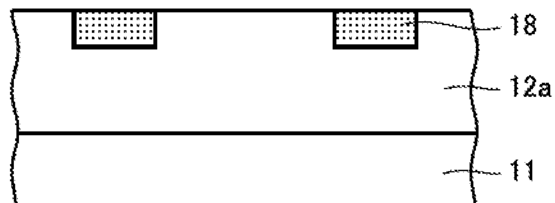


FIG.17

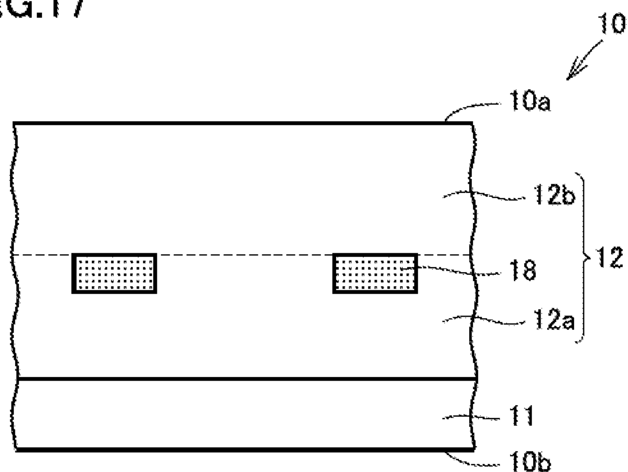


FIG.18

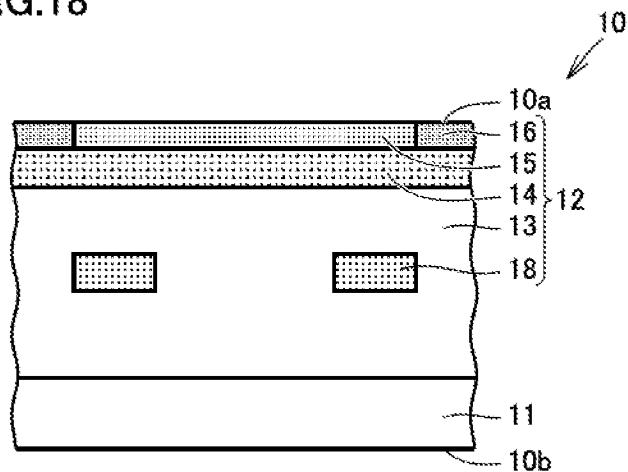


FIG.19

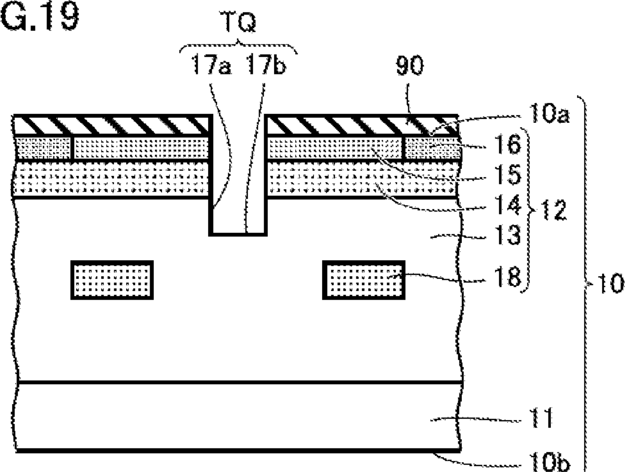


FIG.20

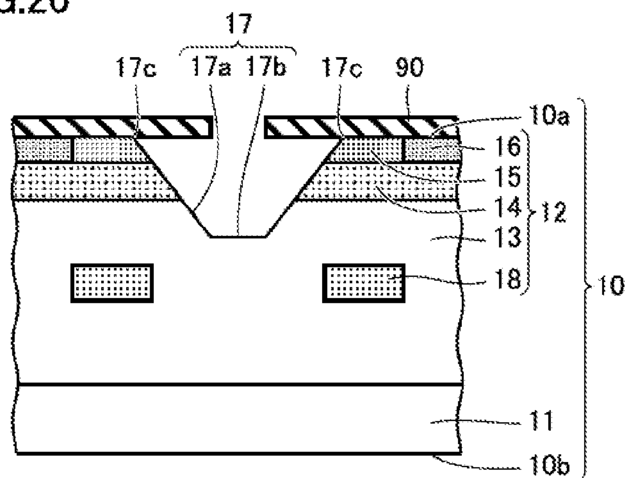


FIG.21

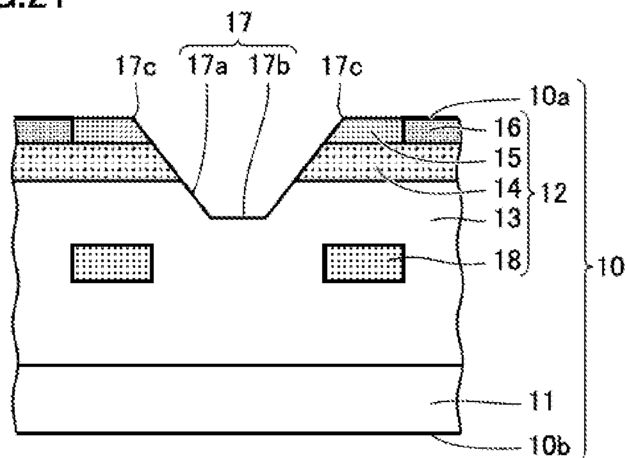


FIG.22

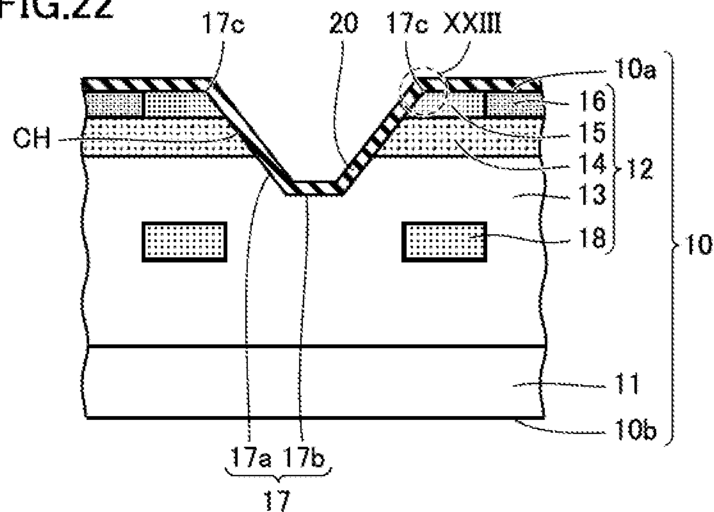


FIG.23

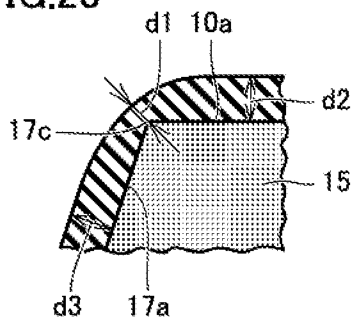


FIG.24

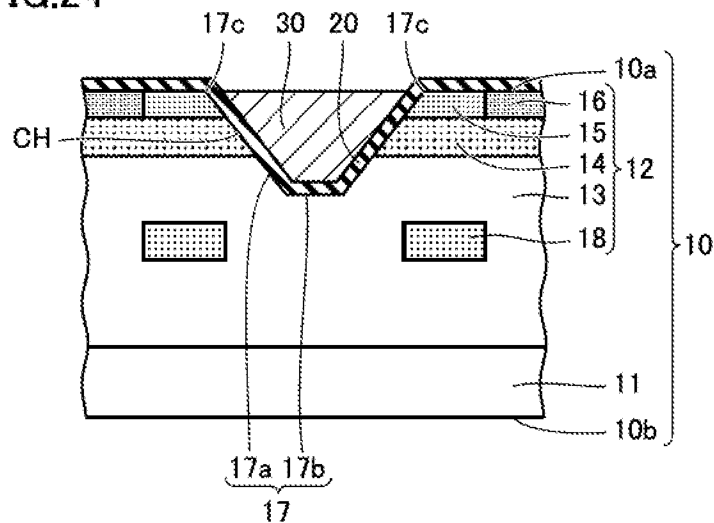


FIG.25

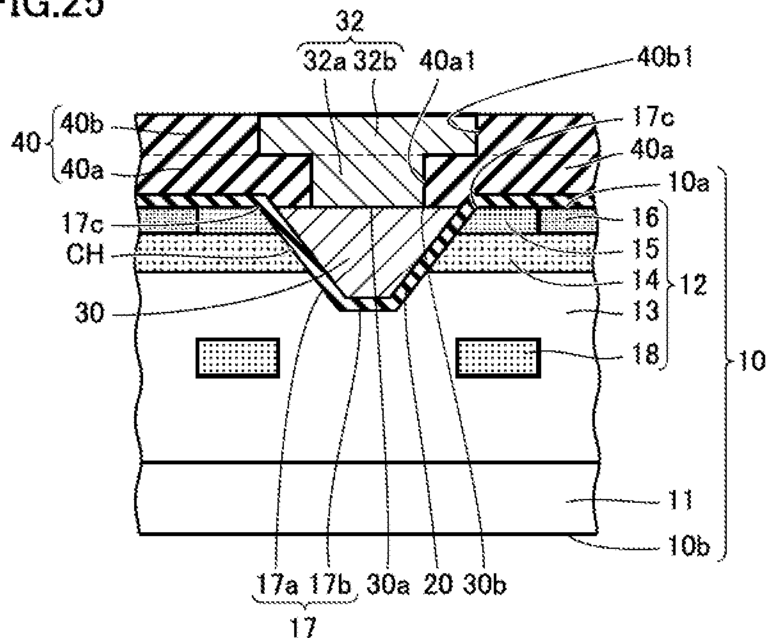


FIG.26

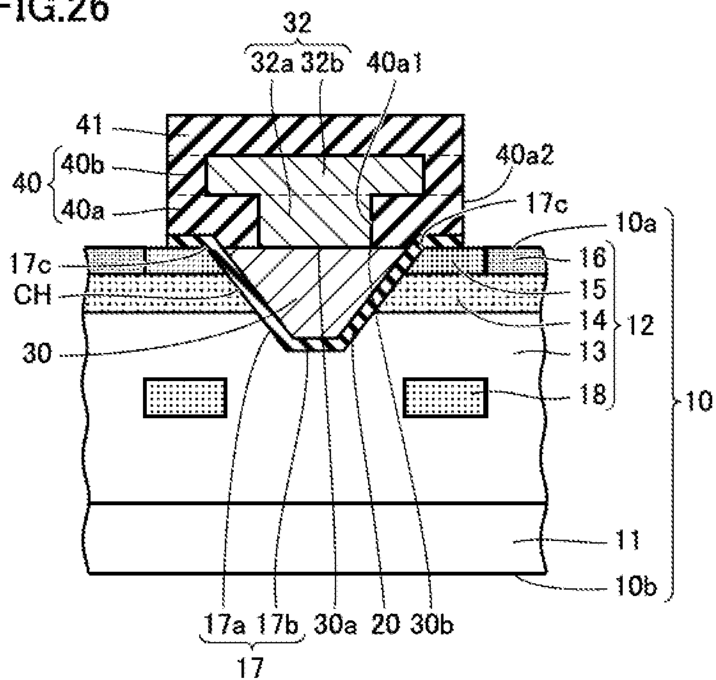
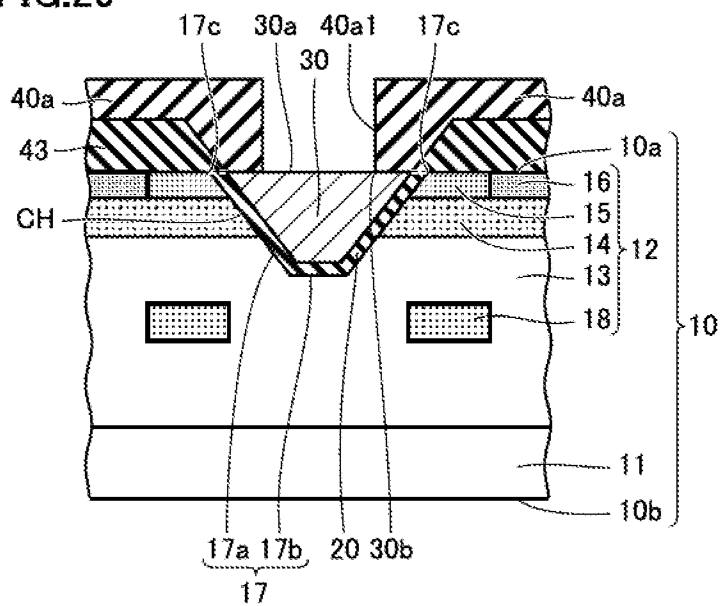


FIG.27

FIG.28

FIG.29



SILICON CARBIDE SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a silicon carbide semiconductor device and a method for manufacturing the silicon carbide semiconductor device, in particular, a silicon carbide semiconductor device provided with a trench and a method for manufacturing such a silicon carbide semiconductor device.

[0003] 2. Description of the Background Art

[0004] In recent years, in order to achieve high breakdown voltage, low loss, and utilization of semiconductor devices, such as a MOSFET (Metal Oxide Semiconductor Field Effect Transistor, under a high temperature environment, silicon carbide has begun to be adopted as a material for a semiconductor device. Silicon carbide is a wide band gap semiconductor having a band gap larger than that of silicon, which has been conventionally widely used as a material for semiconductor devices. Hence, by adopting silicon carbide as a material for a semiconductor device, the semiconductor device can have a high breakdown voltage, reduced on-resistance, and the like. Further, the semiconductor device thus adopting silicon carbide as its material has characteristics less deteriorated even under a high temperature environment than those of a semiconductor device adopting silicon as its material, advantageously.

[0005] in a MOSFET including a substrate having a main surface in which a trench is formed, an electric field is concentrated at a corner portion formed by a side portion, which forms the trench, and the main surface of the substrate with the result that a gate insulating film formed in the vicinity of the corner portion may be broken. For example, Japanese Patent Laying-Open No. 2012-74720 describes a silicon MOSFET in which: a gate electrode is provided in a trench formed in a main surface of a substrate and a field insulating film is formed on the main surface of the substrate and a corner portion formed by a side portion of the trench and the main surface of the substrate.

SUMMARY OF THE INVENTION

[0006] However, a thermal oxidation film. of silicon carbide includes more carbon than a thermal oxidation film of silicon. Therefore, the thermal oxidation film of silicon carbide has a dielectric breakdown strength weaker than the thermal oxidation film of silicon. Accordingly, when MOSFETs respectively including a silicon carbide substrate and a silicon substrate both provided with trench structures having the same shape are formed and the same voltage (for example, 20 V) is applied to their gate electrodes, leakage of gate current is more likely to take place in the MOSFET made of silicon carbide as compared with the MOSFET made of silicon.

[0007] Moreover, in order to form a thick thermal oxidation film by thermally oxidizing the silicon carbide substrate, higher temperature and longer time are required than those in thermally oxidizing the silicon substrate. Thus, it is more difficult to form a thick thermal oxidation film by thermally oxidizing the silicon carbide substrate, as compared with a case of forming a thick thermal oxidation film on the silicon substrate.

[0008] Furthermore, ion implantation is employed to form an impurity region in the silicon carbide substrate. Therefore, after the ion implantation, the silicon carbide substrate needs to be subjected to an activation annealing process at a high temperature of about 1800° C. If a thermal oxidation film is formed on the silicon carbide substrate, the thermal oxidation film will be sublimated in the activation annealing process. Therefore, in the case of forming a field oxide film on the silicon carbide substrate, the field oxide film needs to be formed by a deposition method after forming the impurity region. That is, since the structure and manufacturing method for the field oxide film used for the silicon substrate are actually inapplicable to the silicon carbide substrate, it is difficult to improve dielectric breakdown resistance in the silicon carbide semiconductor device.

[0009] The present invention has been made to solve the foregoing problem, and has an object to provide a silicon carbide semiconductor device capable of improving dielectric breakdown resistance as well as a method for manufacturing such a silicon carbide semiconductor device.

[0010] A silicon carbide semiconductor device according to the present invention includes a silicon carbide substrate, a gate insulating film, a gate electrode, an interlayer insulating film, and a gate interconnection. The silicon carbide substrate has a main surface. The silicon carbide substrate includes: a first impurity region that has a first conductivity type; a second impurity region that is provided on the first impurity region and that has a second conductivity type different from the first conductivity type; and a third impurity region that is provided on the second impurity region so as to be separated from the first impurity region, that forms the main surface, and that has the first conductivity type. The main surface of the silicon carbide substrate is provided with a trench. The trench has a side portion and a bottom portion, the side portion extending to the first impurity region through the third impurity region. and the second impurity region, the bottom portion being located in the first impurity region. The gate insulating film is in contact with a corner portion formed by the side portion and the main surface, the bottom portion, and the side portion. The gate electrode is in contact with the gate insulating film within the trench. In the interlayer insulating film, an opening is formed to expose a portion of the gate electrode. The gate interconnection is disposed in the opening and in contact with the gate electrode. When viewed in a cross section, the interlayer insulating film extends from above the third impurity region to above the gate electrode so as to cover the corner portion.

[0011] A method for manufacturing the silicon carbide semiconductor device according to the present invention includes the following steps. There is prepared a silicon carbide substrate having a main surface. The silicon carbide substrate includes: a first impurity region that has a first conductivity type; a second impurity region that is provided on the first impurity region and that has a second conductivity type different from the first conductivity type; and a third impurity region that is provided on the second impurity region so as to be separated from the first impurity region, that forms the main surface, and that has the first conductivity type. The main surface of the silicon carbide substrate is provided with a trench. The trench has a side portion and a bottom portion, the side portion extending to the first impurity region through the third impurity region and the second impurity region, the bottom portion being located in the first impurity region. A gate insulating film is formed in contact with a

corner portion formed by the side portion and the main surface, the bottom portion, and the side portion. A gate electrode is formed in contact with the gate insulating film within the trench. An interlayer insulating film is formed in which an opening is formed to expose a portion of the gate electrode. A gate interconnection is formed to be disposed in the opening and in contact with the gate electrode. When viewed in a cross section, the interlayer insulating film extends from above the third impurity region to above the gate electrode so as to cover the corner portion.

[0012] The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. **1** is a schematic cross sectional view schematically showing a configuration of a silicon carbide semiconductor device according to one embodiment of the present invention, and is a partial schematic cross sectional view in a region I-I of FIG. **3**.

[0014] FIG. **2** is a partial schematic cross sectional view in a region II-II of FIG. **3**.

[0015] FIG. **3** is a partial schematic plan view schematically showing a configuration of a silicon carbide substrate according to the embodiment of the present invention.

[0016] FIG. **4** is a partial schematic perspective view schematically showing the configuration of the silicon carbide substrate according to the embodiment of the present invention.

[0017] FIG. **5** is a schematic cross sectional view schematically showing a configuration of a first modification of the silicon carbide semiconductor device according to the embodiment of the present invention.

[0018] FIG. **6** is a schematic cross sectional view schematically showing a configuration of a second modification of the silicon carbide semiconductor device according to the embodiment of the present invention.

[0019] FIG. **7** is a partial schematic cross sectional view schematically showing a fine structure of the side portion of the trench provided in the silicon carbide semiconductor device.

[0020] FIG. **8** shows a crystal structure of a (000-1) plane in a hexagonal crystal of polytype 4H.

[0021] FIG. **9** shows a crystal structure of a (11-20) plane along a line XXV-XXV in FIG. **8**.

[0022] FIG. **10** shows a crystal structure in the vicinity of a surface of a combined plane of FIG. **7** within a (11-20) plane.

[0023] FIG. **11** shows the combined plane of FIG. **7** when viewed from a (01-10) plane.

[0024] FIG. **12** is a graph showing an exemplary relation between channel mobility and an angle between a channel surface and the (000-1) plane when macroscopically viewed, in each of a case where thermal etching is performed and a case where no thermal etching is performed.

[0025] FIG. **13** is a graph showing an exemplary relation between the channel mobility and an angle between a channel direction and a <0-11-2> direction.

[0026] FIG. **14** shows a modification of FIG. **7**.

[0027] FIG. **15** is a flowchart schematically showing a method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0028] FIG. **16** is a partial schematic cross sectional view schematically showing a first step of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0029] FIG. **17** is a partial schematic cross sectional view schematically showing a second step of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0030] FIG. **18** is a partial schematic cross sectional view schematically showing a third step of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0031] FIG. **19** is a partial schematic cross sectional view schematically showing a fourth step of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0032] FIG. **20** is a partial schematic cross sectional view schematically showing a fifth step of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0033] FIG. **21** is a partial schematic cross sectional view schematically showing a sixth step of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0034] FIG. **22** is a partial schematic cross sectional view schematically showing a seventh step of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0035] FIG. **23** is an enlarged view of a region XXIII of FIG. **22**.

[0036] FIG. **24** is a partial schematic cross sectional view schematically showing an eighth step of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0037] FIG. **25** is a partial schematic cross sectional view schematically showing a ninth step of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0038] FIG. **26** is a partial schematic cross sectional view schematically showing a tenth step of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0039] FIG. **27** is a partial schematic cross sectional view schematically showing a first step of a modification of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0040] FIG. **28** is a partial schematic cross sectional view schematically showing a second step of the modification of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

[0041] FIG. **29** is a partial schematic cross sectional view schematically showing a third step of the modification of the method for manufacturing the silicon carbide semiconductor device according to the embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0042] [Description of Embodiments of the Invention of the Present Application]

[0043] The following describes embodiments of the present invention with reference to figures. It should be noted that in the below-mentioned figures, the same or corresponding portions are given the same reference characters and are

not described repeatedly. Regarding crystallographic indications in the present specification, an individual orientation is represented by [], a group orientation is represented by <>, and an individual plane is represented by ( ), and a group plane is represented {}. In addition, a negative crystallographic index is normally expressed by putting "–" (bar) above a numeral, but is expressed by putting the negative sign before the numeral in the present specification.

[0044] (1) A silicon carbide semiconductor device **1** according to an embodiment includes a silicon carbide substrate **10**, a gate insulating film **20**, a gate electrode **30**, an interlayer insulating film **40***a,* and a gate interconnection **32**. Silicon carbide substrate **10** has a main surface **10***a*. Silicon carbide substrate **10** includes: a first impurity region **13** that has a first conductivity type; a second impurity region **14** that is provided on first impurity region **13** and that has a second conductivity type different from the first conductivity type; and a third impurity region **15** that is provided on second impurity region **14** so as to be separated from first impurity region **13**, that forms main surface **10***a,* and that has the first conductivity type. Main surface **10***a* of silicon carbide substrate **10** is provided with a trench **17**. Trench **17** has a side portion **17***a* and a bottom portion **17***b,* side portion **17***a* extending to first impurity region **13** through third impurity region **15** and second impurity region **14**, bottom portion **17***b* being located in first impurity region **13**. Gate insulating film **20** is in contact with a corner portion **17***c* formed by side portion **17***a* and main surface **10***a,* bottom portion **17***b* and side portion **17***a*. Gate electrode **30** is in contact with gate insulating film **20** within trench **17**. In interlayer insulating film **40***a,* an opening **40***a***1** is formed to expose a portion of gate electrode **30**. Gate interconnection **32** is disposed in the opening and in contact with gate electrode **30**. When viewed in a cross section, interlayer insulating film **40***a* extends from above third impurity region **15** to above gate electrode **30** so as to cover corner portion **17***c*.

[0045] In accordance with silicon carbide semiconductor device **1** according to (1), when viewed in a cross section, interlayer insulating film **40***a* extends from above third impurity region **15** to above gate electrode **30** so as to cover corner portion **17***c*. Accordingly, the insulating film on corner portion **17***c* can be effectively suppressed from being broken. As a result, the dielectric breakdown resistance of silicon carbide semiconductor device **1** can be improved.

[0046] (2) Preferably in silicon carbide semiconductor device **1** according to (1), gate interconnection **32** is made of a material having a melting point of not less than 1000° C. Accordingly, for example, even when gate interconnection **32** is heated to not less than 1000° C. in the alloying anneal step, gate interconnection **32** can be suppressed from being melted.

[0047] (3) Preferably in silicon carbide semiconductor device **1** according to (2), the material includes at least one material selected from a group consisting of W, Ni, WSi, and polysilicon. Accordingly, gate interconnection **32** can be effectively suppressed from being melted.

[0048] (4) Preferably in silicon carbide semiconductor device **1** according to any one of (1) to (3), interlayer insulating film **40** has a carbon concentration smaller than a carbon concentration of the gate insulating film. Accordingly, the insulating property of the insulating film is improved and leakage current can be reduced.

[0049] (5) Preferably in silicon carbide semiconductor device **1** according to any one of (1) to (4), gate interconnection **32** includes a barrier layer **32***c* in contact with each of gate electrode **30** and interlayer insulating film **40***a*. Accordingly, the insulation performance of silicon carbide semiconductor device **1** can be suppressed from being deteriorated by aluminum being diffused in interlayer insulating film **40***a*.

[0050] (6) Preferably in silicon carbide semiconductor device **1** according to (5), barrier layer **32***c* includes at least one of Ti and TiN. Accordingly, adhesion can be improved between interlayer insulating film **40***a* and gate interconnection **32**.

[0051] (7) Silicon carbide semiconductor device **1** according to any one of (1) to (6) preferably further includes a gate pad **33** in contact with gate interconnection **32**. Accordingly, voltage can be effectively applied to gate interconnection **32**.

[0052] (8) Preferably in silicon carbide semiconductor device **1** according to any one of (1) to (7), side portion **17***a* of the trench includes a first plane **S1** having a plane orientation of {0-33-8}. Accordingly, channel resistance in side portion **17***a* can be reduced, thereby reducing on-resistance.

[0053] (9) Preferably in silicon carbide semiconductor device **1** according to (8), side portion **17***a* of the trench microscopically includes first plane S**1**, and side portion **17***a* microscopically further includes a second plane S**2** having a plane orientation of {0-11-1}. Accordingly, channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0054] (10) Preferably in silicon carbide semiconductor device **1** according to (9), first plane S**1** and second plane S**2** of side portion **17***a* of the trench include a combined plane SR having a plane orientation of {0-11-2}. Accordingly, channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0055] (11) Preferably in silicon carbide semiconductor device **1** according to (10), side portion **17***a* of the trench macroscopically has an off angle of 62±10° relative to a {000-1} plane. Accordingly, channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0056] (12) A method Or manufacturing a silicon carbide semiconductor device according to an embodiment includes the following steps. There is prepared a silicon carbide substrate **10** having a main surface **10***a*. Silicon carbide substrate **10** includes: a first impurity region **13** that has a first conductivity type; a second impurity region **14** that is provided on first impurity region **13** and that has a second conductivity type different from the first conductivity type; and a third impurity region **15** that is provided on second impurity region **14** so as to be separated from first impurity region **13**, that forms main surface **10***a,* and that has the first conductivity type. Main surface **10***a* of silicon carbide substrate **10** is provided with a trench **17**. Trench **17** has a side portion **17***a* and a bottom portion **17***b,* side portion **17***a* extending to first impurity region **13** through third impurity region **15** and second impurity region **14**, bottom portion **17***b* being located in first impurity region **13**. A gate insulating film **20** is formed in contact with a corner portion **17***c* formed by side portion **17***a* and main surface **10***a,* bottom portion **17***b,* and side portion **17***a*. A gate electrode **30** is formed in contact with gate insulating film **20** within trench **17**. An interlayer insulating film **40***a* is formed in which an opening **40***a***1** is formed to expose a portion of gate electrode **30**. A gate interconnection **32** is formed to be disposed in opening **40***a* **1** and in contact with gate electrode **30**. When viewed in a cross section, inter-

layer insulating film **40** extends from above third impurity region **15** to above gate electrode **30** so as to cover corner portion **17***c*.

[0057] In accordance with the method for manufacturing silicon carbide semiconductor device **1** according to (12), when viewed in a cross section, interlayer insulating film **40***a* extends from above third impurity region **15** to above gate electrode **30** so as to cover corner portion **17***c*. Accordingly, the insulating film on corner portion **17***c* can be effectively suppressed from being broken. As a result, the dielectric breakdown resistance of silicon carbide semiconductor device **1** can be improved.

[0058] (13) Preferably in the method for manufacturing silicon carbide semiconductor device **1** according to (12), gate insulating film **20** is formed by thermally oxidizing silicon carbide substrate **10** in which trench **17** is formed. In this way, gate insulating film **20** having excellent insulation performance can be formed.

[0059] (14) Preferably in the method for manufacturing silicon carbide semiconductor device **1** according to (12) or (13), interlayer insulating film **40** is formed by a chemical vapor deposition method. Accordingly, as compared with a case where the insulating film is formed by thermal oxidation, thick interlayer insulating film **40** can be grown for a shorter period of time.

[0060] (15) The method for manufacturing silicon carbide semiconductor device **1** according to any one of (12) to (14) preferably further includes the step of forming an insulating layer **43** in contact with main surface **10***a* of silicon carbide substrate **10** in which trench **17** is formed. In the step of forming gate insulating film **20**, side portion **17***a* and bottom portion **17***b* of trench **17** is thermally oxidized with insulating layer **43** being formed on main surface **10***a*. Accordingly, the thickness of the insulating film on corner portion **17***c* is increased, thereby improving the dielectric breakdown resistance of silicon carbide semiconductor device **1**.

[0061] (16) Preferably in the method for manufacturing silicon carbide semiconductor device **1** according to any one of (12) to (15), the step of forming gate interconnection **32** includes the step of forming a barrier layer **32***c* in contact with each of gate electrode: **30** and interlayer insulating film **40**. Accordingly, the insulation performance of silicon carbide semiconductor device **1** can be suppressed from being deteriorated by aluminum being diffused in interlayer insulating film **40***a*.

[0062] (17) Preferably in the method for manufacturing silicon carbide semiconductor device **1** according to (16), barrier layer **32***c* includes at least one of Ti and TiN. Accordingly, adhesion can be improved between interlayer insulating film **40***a* and gate interconnection **32**.

[0063] (18) The method for manufacturing silicon carbide semiconductor device **1** according to any one of (12) to (17) preferably further includes the step of forming a gate pad **33** in contact with gate interconnection **32**. Accordingly, voltage can be effectively applied to gate interconnection **32**.

[0064] (19) Preferably in the method for manufacturing silicon carbide semiconductor device **1** according to any one of (12) to (18), side portion **17***a* of trench **17** includes a first plane **S1** having a plane orientation of {0-33-8}. Accordingly, channel resistance in side portion **17***a* can be reduced, thereby reducing on-resistance.

[0065] (20) Preferably in the method for manufacturing silicon carbide semiconductor device **1** according to (19), side portion **17***a* of trench **17** microscopically includes first plane **S1**, and side portion **17***a* microscopically further includes a second plane **S2** having a plane orientation of {0-11-1}. Accordingly, channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0066] (21) Preferably in the method for manufacturing silicon carbide semiconductor device **1** according to (20), first plane **S1** and second plane **S2** of side portion **17***a* of trench **17** include a combined plane SR having a plane orientation of {0-11-2}. Accordingly channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0067] (22) Preferably in the method for manufacturing silicon carbide semiconductor device **1** according to (21), side portion **17***a* of trench **17** macroscopically has an off angle of 62±10° relative to a {000-1} plane. Accordingly, channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0068] [Details of Embodiments of the Invention of the Present Application]

[0069] First, the following describes a configuration of a silicon carbide semiconductor device **1** according to one embodiment of the present invention.

[0070] With reference to FIG. **1** to FIG. **4**, a MOSFET 1 serving as the silicon carbide semiconductor device of the present embodiment mainly includes a silicon carbide substrate **10**, a gate insulating film **20**, a gate electrode **30**, an interlayer insulating film **40**, a gate interconnection **32**, a source electrode **60**, a source interconnection layer **65**, a drain electrode **70**, and a lower pad electrode **80**.

[0071] Silicon carbide substrate **10** has a first main surface **10***a*, and a second main surface **10***b* opposite to first main surface **10***a*. Silicon carbide substrate **10** includes a silicon carbide single crystal substrate **11** and a silicon carbide epitaxial layer **12** provided on silicon carbide single crystal substrate **11**. Silicon carbide single crystal substrate **11** has a hexagonal crystal structure of polytype 4H, for example. Silicon carbide single crystal substrate **11** includes an impurity such as nitrogen, and is of n type (first conductivity type).

[0072] Silicon carbide epitaxial layer **12** of silicon carbide substrate **10** mainly includes a drift region **13**, a body region **14**, a source region **15**, a contact region **16**, and an electric field relaxing region **18**.

[0073] Drift region **13** (first impurity region) includes a donor impurity such as nitrogen, and is of n type. Drill region **13** has an impurity concentration lower than that of silicon carbide single crystal substrate **11**. Drift region **13** has an impurity concentration of, for example, not less than $1\times10^{\cdot\cdot}$ cm^{-3} and not more than 5×10^{16} cm^{-3}. Drift region **13** has a thickness of about 15 μm for example.

[0074] Body regions **14** (second impurity region) includes an acceptor impurity such as aluminum, and is of p type (second conductivity type) different from n type. Body region **14** is provided on and in contact with drift region **13**. Body region **14** has an impurity concentration of, for example, not less than 1×10^{17} cm^{-3} and not more than 5×10^{18} cm^{-3}.

[0075] Source regions **15** (third impurity region) includes a donor impurity such as phosphorus, and is of n type. Source region **15** is provided on body region **14** such that source region **15** is separated from drift region **13** by body region **14**. Contact region **16** includes an acceptor impurity such as aluminum, and is of p type. Contact region **16** is in contact with source region **15**, and connects source electrode **60** and body region **14** to each other. Source region **15** and contact region **16** form first main surface **10***a* of silicon carbide substrate **10**.

[0076] With reference to FIG. **3** and FIG. **4**, a trench **17** is provided in first main surface **10***a* of silicon carbide substrate **10**. Trench **17** has a side portion **17***a* and a bottom portion **17***b*, side portion **17***a* extending to drift region **13** through source region **15** and body region **14**, bottom portion **17***b* being located in drift region **13**. In other words, each of drift region **13**, body region **14**, and source region **15** is in contact with side portion **17***a* of trench **17**. Drift region **13** is in contact with bottom portion **17***b* of trench **17**. Side portion **17***a* of trench **17** is continuously connected to bottom portion **17***b*.

[0077] When viewed in a plan view (field of view seen in a direction normal to second main surface **10***b* of silicon carbide substrate **10**), bottom portion **17***b* of trench **17** preferably has a polygonal shape such as a hexagonal shape. When viewed in a plan view, a plurality of trenches **17** may be formed to partially surround contact region **16**, for example. A plurality of trenches **17** may be provided to interpose contact region **16** therebetween. Regarding trenches **17** according to the present embodiment, six trenches are provided to face respective sides of contact region **16** having a hexagonal shape. in other words, contact region **16** is disposed to be surrounded by six trenches **17**. When viewed in a plan view, trench **17** may be provided to be interposed between two contact regions **16**. On body region **14**, side portion **17***a* of trench **17** includes a channel surface CH (see FIG. **1**) of MOSFET 1. When viewed in a plan view, a corner portion **17***c*, which is formed by first main surface **10***a* of silicon carbide substrate **10** and side portion **17***a* of trench **17**, has a polygonal shape, preferably, a hexagonal shape. Corner portion **17***c* may be a position on a side of a hexagon or may be a position on a vertex of a hexagon.

[0078] Side portion **17***a* of trench **17** is inclined relative to first main surface **10***a* of silicon carbide substrate **10**, whereby trench **17** is expanded toward the opening in a tapered manner. First main surface **10***a* of silicon carbide substrate **10** corresponds to, for example, a {000-1} plane, and preferably corresponds to a (000-1) plane. Side portion **17***a* of trench **17** preferably has a plane orientation inclined relative to a {001} plane by not less than 50° and not more than 70°, more preferably, inclined relative to the (000-1) plane by not less than 50° and not more than 70°. Preferably, side portion **17***a* of trench **17** is inclined by about not less than 50° and not more than 70° relative to bottom portion **17***b*. Preferably, side portion **17***a* has a predetermined crystal plane (also referred to as "special plane") particularly at its portion in contact with body region **14**. Details of the special plane will be described later. Bottom portion **17***b* of trench **17** is substantially parallel to each of first main surface **10***a* and second main surface **10***b* of silicon carbide substrate **10**.

[0079] With reference to FIG. **1** and FIG. **2** again, electric field relaxing region **18** includes an acceptor impurity such as aluminum, and is of p type. Electric field relaxing region **18** is provided between body region **14** and second main surface **10***b* of silicon carbide substrate **10** such that electric field relaxing region **18** is surrounded by drift region **13**. In the direction normal to second main surface **10***b* of silicon carbide substrate **10**, electric field relaxing region **18** is provided at the second main surface **10***b* side relative to bottom portion **17***b* of trench **17**. Electric field relaxing region **18** is away from body region **14** by not less than 1 μm and not more than 5 μm, for example. For example, electric field relaxing region **18** has a dose amount of not less than 1×10^{12} cm^{-2} and not more than 1×10^{15} cm^{-2}, preferably, not less than 1×10^{13} cm^{-2} and not more than $5\times cm^{-2}$.

[0080] Gate insulating film **20** is provided in contact with: corner portion **17***c* formed by side portion **17***a* of trench **17** and first main surface **10***a* of silicon carbide substrate **10**; bottom portion **17***b* of trench **17**; side portion **17***a* of trench **17**; and first main surface **10***a* of silicon carbide substrate **10**. Gate insulating film **20** is in contact with source region **15** at each of first main surface **10***a* of silicon carbide substrate **10** and side portion **17***a* of trench **17**, is in contact with body region **14** at side portion **17***a* of trench **17**, and is in contact with drift region **13** at each of side portion **17***a* and bottom portion **17***b* of the trench. Gate insulating film **20** is made of, for example, silicon dioxide.

[0081] Gate electrode **30** is in contact with gate insulating film **20** within trench **17**. Specifically, gate electrode **30** is provided to face each of source region **15**, body region **14**, and drill region **13** with gate insulating film **20** interposed therebetween. Gate electrode **30** is formed of a material including polysilicon having an impurity doped therein, for example.

[0082] With reference to FIG. **1** and FIG. **2**, interlayer insulating film **40** includes a first interlayer insulating film **40***a* and a second interlayer insulating film **40***b* provided on first interlayer insulating film **40***a*. When viewed in a cross section, first interlayer insulating film **40***a* is provided to extend from above source region **15** to above gate electrode **30** so as to cover corner portion **17***c* formed by side portion **17***a* of trench **17** and first main surface **10***a* of silicon carbide substrate **10**. First interlayer insulating film **40***a* is in contact with a portion of an upper surface **30***a* of gate electrode **30**, and is in contact with gate insulating film **20** on corner portion **17***c*. With reference to FIG. **2**, first interlayer insulating film **40***a* is provided to extend over source region **15** from the upper surface of one gate electrode **30** provided in one of two adjacent trenches **17**, **17** to the upper surface of the other gate electrode **30** provided in the other trench **17**.

[0083] First interlayer insulating film **40***a* has an opening **40***a***1** through which the central portion of the upper surface of gate electrode **30** is exposed. When viewed in a cross section (field of view seen in a direction parallel to second main surface **10***b* of silicon carbide substrate **10**), opening **40***a***1** has a width W1, W3 smaller than a width W2, W4 of upper surface **30***a* of gate electrode **30**. Opening **40***a***1** has width W1, W3 of, for example, not less than 0.5 μm and not more than 3.0 μm. Upper surface **30***a* of gate electrode **30** has width W2, W4 of, for example, not less than 1.0 μm and not more than 5.0 μm. Each of first interlayer insulating film **40***a* and second interlayer insulating film **40***b* is made of a material including silicon dioxide, for example. At least one of first interlayer insulating film **40***a* and second interlayer insulating film **40***b* may be made of a material including SiON or SiN. Preferably, first interlayer insulating film **40***a* has a carbon concentration less than the carbon concentration of the gate insulating film. First interlayer insulating film **40***a* has a thickness H of, for example, about not less than 0.1 μm and not more than 2 μm, preferably, about not less than 0.3 μm and not more than 10 μm.

[0084] Gate interconnection **32** is disposed in opening **40***a***1** formed in interlayer insulating film **40**, and is in contact with gate electrode **30**. Width W1 of gate interconnection **32** in a direction along an interface **30***a* between gate electrode **30** and gate interconnection **32** is smaller than width W2 of gate electrode **30**. Gate interconnection **32** includes a first gate interconnection portion **32***a* and a second gate interconnection portion **32***b*. First gate interconnection portion **32***a* is in contact with gate electrode **30**, and is disposed in opening

40*a*1 formed in interlayer insulating film **40**. Second gate interconnection portion **32*b*** is provided on and in contact with first gate interconnection portion **32*a***, and has a width larger than width **W1** of first gate interconnection portion **32*a***. Preferably, gate interconnection **32** is made of a material having a melting point of not less than 1000° C. Specifically, the material of gate interconnection **32** includes at least one material selected from a group consisting of W (tungsten), Ni (nickel), WSi (tungsten silicide) and polysilicon.

[0085] In interlayer insulating film **40** and gate insulating film **20**, an opening **40*a*2** is formed via which contact region **16** and a portion of source region **15** are exposed at first main surface **10*a*** of silicon carbide substrate **10**. Source electrode **60** is in contact with each of source region **15** and contact region **16** at first main surface **10*a*** of silicon carbide substrate **10**. Source interconnection layer **65** is provided on and in contact with source electrode **60**, and is electrically connected to source electrode **60**. Source interconnection layer **65** is, for example, a layer including aluminum. Interlayer insulating film **40** insulates between gate electrode **30** and source electrode **60**.

[0086] With reference to FIG. **5**, gate interconnection **32** may include a barrier layer **32*c*** in contact with each of gate electrode **30** and interlayer insulating film **40**. For example, barrier layer **32*c*** is in contact with the upper surface of first interlayer insulating film **40*a*** and its wall surface that forms opening **40*a*1** in first interlayer insulating film **40*a***, and is in contact with upper surface **30*a*** of gate electrode **30**. Preferably, barrier layer **32*c*** includes at least one of Ti and TiN.

[0087] With reference to FIG. **6**, MOSFET 1 may further include a gate pad **33**. Gate pad **33** is provided on and in contact with gate interconnection **32**, and is configured to be capable of applying voltage to gate electrode **30**. interlayer insulating film **41** provided on gate interconnection **32** is provided with an opening, via which gate pad **33** is electrically connected to gate interconnection **32**. Gate pad **33** is made of a material including AlSiCu, for example. Second gate interconnection portion **32*b*** of gate interconnection **32** is disposed between first interlayer insulating film **40*a*** and interlayer insulating film **41**.

[0088] (Special Plane)

[0089] Side portion **17*a*** of trench **17** described above has a special plane particularly at its portion on body region **14**. As shown in FIG. **7**, side portion **17*a*** having the special plane includes a plane **S1** (first plane) having a plane orientation of {0-33-8}. in other words, on side portion **17*a*** of trench **17**, body region **14** is provided with a surface including plane **S1**. Plane **S1** preferably has a plane orientation of (0-33-8).

[0090] More preferably, side portion **17*a*** microscopically includes plane **S1**, and side portion **17*a*** microscopically further includes a plane **S2** (second plane) having a plane orientation of {0-11-1}. Here, the term "microscopically" refers to "minutely to such an extent that at least the size about twice as large as an interatomic spacing is considered". As a method for observing such a microscopic structure, for example, a TEM (Transmission Electron Microscope) can be used. Plane **S2** preferably has a plane orientation of (0-11-1).

[0091] Preferably, plane **S1** and plane **S2** of side portion **17*a*** form a combined plane SR haying a plane orientation of {0-11-2}. That is, combined plane SR is formed of periodically repeated planes **S1** and **S2**. Such a periodic structure can be observed by, for example, a TEM or an AFM (Atomic Force Microscopy). In this case, combined plane SR has an off angle of 62° relative to the {000-1} plane, macroscopically. Here, the term "macroscopically" refers to "disregarding a tine structure having a size of approximately interatomic spacing". For the measurement of such a macroscopic off angle, a method employing general X-ray diffraction can be used, for example. Preferably, combined plane SR has a plane orientation of (0-11-2). In this case, combined plane SR has an off angle of 62° relative to the (000-1) plane, macroscopically.

[0092] Preferably, a channel direction CD, which is a direction in which a carrier flows on the channel surface (i.e., the thickness direction of the MOSFET (longitudinal direction in FIG. **1** or the like)), is along the direction in which the above-described periodic repetition is made.

[0093] The following describes a detailed structure of combined plane SR.

[0094] Generally, regarding **S1** atoms (or C atoms), when viewing a silicon carbide single crystal of polytype 4H from the (000-1) plane, atoms in a layer A (solid line in the figure), atoms in a layer B (broken line in the figure) disposed therebelow, and atoms in a layer C (chain line in the figure) disposed therebelow, and atoms in a layer B (not shown in the figure) disposed therebelow are repeatedly provided as shown in FIG. **8**. In other words, with four layers ABCB being regarded as one period, a periodic stacking structure such as ABCBABCBABCB . . . is provided.

[0095] As shown in FIG. **9**, in the (11-20) plane (cross section taken along a line IX-IX of FIG. **8**), atoms in each of four layers ABCB constituting the above-described one period are not aligned completely along the (0-11-2) plane. In FIG. **9**, the (0-11-2) plane is illustrated to pass through the locations of the atoms in layers B. In this case, it is understood that each of atoms in layers A and C is deviated from the (0-11-2) plane. Hence, even when the macroscopic plane orientation of the surface of the silicon carbide single crystal, i.e., the plane orientation thereof with its atomic level structure being ignored is limited to (0-11-2), this surface can have various structures microscopically.

[0096] As shown in FIG. **10**, combined plane SR is constructed by alternately providing planes **S1** having a plane orientation of (0-33-8) and planes **S2** connected to planes **S1** and having a plane orientation different from that of each of planes **S1**. Each of planes **S1** and **S2** has a length twice as large as the interatomic spacing of the Si atoms (or C atoms). It should be noted that a plane with plane **S1** and plane **S2** being averaged corresponds to the (0-11-2) plane (FIG. **9**).

[0097] As shown in FIG. **11**, when viewing combined plane SR from the (01-10) plane, the single crystal structure has a portion periodically including a structure (plane **S1** portion) equivalent to a cubic structure. Specifically, combined plane SR is constructed by alternately providing planes **S1** having a plane orientation of (001) in the above-described structure equivalent to the cubic structure and planes **S2** connected to planes **S1** and having a plane orientation different from that of each of planes **S1**. Also in a polytype other than 4H, the surface can be thus constituted of the planes (planes **S1** in FIG. **7**) having a plane orientation of (001) in the structure equivalent to the cubic structure and the planes (planes **S2** in FIG. **7**) connected to the foregoing planes and having a plane orientation different from that of each of the foregoing planes. The polytype may be 6H or 15R, for example.

[0098] Next, with reference to FIG. **12**, the following describes a relation between the crystal plane of side portion **17*a*** and mobility MB of the channel surface. In a graph of FIG. **12**, the horizontal axis represents an angle **D1** between a

macroscopic plane orientation of side portion **17***a* having the channel surface and the (000-1) plane, whereas the vertical axis represents mobility MB. A group of plots CM correspond to a case where side portion **17***a* is finished to correspond to the special plane by thermal etching, whereas a group of plots MC correspond to a case where side wall **17***a* is not thermally etched.

[0099] In group of plots MC, mobility MB is at maximum when the channel surface has a macroscopic plane orientation of (0-33-8). This is presumably due to the following reason. That is in the case where the thermal etching is not performed, i.e., in the case where the microscopic structure of the channel surface is not particularly controlled, the macroscopic plane orientation thereof corresponds to (0-33-8), with the result that a ratio of the microscopic plane orientation of (0-33-8), i.e., the plane orientation of (0-33-8) in consideration of that in atomic level becomes statistically high.

[0100] On the other hand, mobility MB in group of plots CM is at maximum when the macroscopic plane orientation of the channel surface is (0-11-2) (arrow EX). This is presumably due to the following reason. That is, as shown in FIG. **10** and FIG. **11**, the multiplicity of planes S**1** each having a plane orientation of (0-33-8) are densely and regularly arranged with planes S**2** interposed tberebetween, whereby a ratio of the microscopic plane orientation of (0-33-8) becomes high in the channel surface.

[0101] It should be noted that mobility MB has orientation dependency on combined plane SR. In a graph shown in FIG. **13** the horizontal axis represents an angle D**2** between the channel direction and the <0-11-2> direction, whereas the vertical axis represents mobility MB (in any unit) in the channel surface. A broken line is supplementarily provided therein for viewability of the graph. From this graph, it has been found that in order to increase channel mobility MB, channel direction CD (FIG. **7**) preferably has an angle D**2** of not less than 0° and not more than 60°, more preferably, substantially 0°.

[0102] As shown in FIG. **14**, side portion **17***a* may further include a plane S**3** (third plane) m addition to combined plane SR. More specifically, side portion **17***a* may include a combined plane SQ constituted of periodically repeated plane S**3** and combined plane SR. In this case, the off angle of side portion **17***a* relative to the {000-1} plane is deviated from the ideal off angle of combined plane SR, i.e., 62°. Preferably, this deviation is small, preferably, in a range of ±10°. Examples of a surface included in such an angle range include a surface having a macroscopic plane orientation of the {0-33-8} plane. More preferably, the of angle of side portion **17***a* relative to the (000-1) plane is deviated from the ideal off angle of combined plane SR, i.e., 62°. Preferably, this deviation is small, preferably, in a range of ±10. Examples of a surface included in such an angle range include a surface having a macroscopic plane orientation of the (0-33-8) plane.

[0103] Such a periodic structure can be observed using a TEM or an AFM, for example.

[0104] Next, the following describes a method for manufacturing MOSFET **1** (FIG. **1**) serving as the silicon carbide semiconductor device according to the present embodiment with reference to FIG. **15**.

[0105] First, a silicon carbide substrate preparing step (S**10**: FIG. **15**) is performed. With reference to FIG. **16**, a lower drift layer **12***a* to serve as a portion of drift region **13** (FIG. **1**) is formed on silicon carbide single crystal substrate **11**. Specifically, lower drill layer **12***a* of n type is formed through epitaxial growth on silicon carbide single crystal substrate **11**. The epitaxial growth can be achieved by employing a CVD (Chemical Vapor Deposition) method that utilizes a mixed gas of silane (SiH_4) and propane (C_3H_8) as a material gas and utilizes hydrogen gas (H_2) as a carrier gas, for example. During the epitaxial growth, it is preferable to introduce nitrogen (N) or phosphorus (P) as an impurity, for example.

[0106] As shown in FIG. **16**, electric field relaxing region **18** of p type is formed in a portion of lower drift layer **12***a*. Specifically, after forming an implantation mask (not shown) on lower drift layer **12***a*, acceptor ions (impurity ions tot providing p type are implanted in lower drift layer **12***a* using the implantation mask.

[0107] As shown in FIG. **17**, after electric field relaxing region **18** is formed, an upper drift layer **12***b* of n type is formed on lower drift layer **12***a*. Accordingly, electric field relaxing region **18** is buried in drift region **13** including lower drift layer **12***a* and upper drift layer **12***b*. Upper drift layer **12***b* can be formed by the same formation method as that for lower drift layer **12***a*.

[0108] Next, an ion implantation step (S**20**: FIG. **15**) is performed. As shown in FIG. **18**, body region. **14** is formed on drift region **13**, and source region **15** and contact region **16** are formed on body region **14**. Each of body region **14**, source region **15**, and contact region **16** is formed by implanting ions into drift region **13**, for example. In the ion implantation for forming body region **14** and contact region **16**, ions of an impurity for providing p type such as aluminum (Al) are implanted. Meanwhile, in the ion implantation for forming source region **15**, ions of an impurity for providing n type such as phosphorus (P) are implanted, for example. It should be noted that instead of the ion implantation, body region **14**, source region **15**, and contact region **16** may be formed through epitaxial growth involving addition of an impurity.

[0109] Next, a heat treatment (activation annealing) is performed in order to activate the impurities provided in silicon carbide substrate **10** by the ion implantations. The activation annealing is preferably performed at a temperature of not less than 1500° C. and not more than 1900° C., for example, a temperature of approximately 1700° C. The activation annealing is performed for approximately 30 minutes, for example. The atmosphere of the activation annealing is preferably an inert gas atmosphere, such as Ar atmosphere.

[0110] Next, a trench forming step (S**30**: FIG. **15**) is performed. With reference to FIG. **19**, a mask layer **90** having an opening is formed on first main surface **10***a* including source region **15** and contact region **16**. As mask layer **90**, a silicon oxide film or the like can be used, for example. The opening is formed to correspond to the position of trench **17** (FIG. **1**).

[0111] As shown in FIG. **19**, in the opening of mask layer **90**, source region **15**, body region **14**, and a portion of drift region **13** are removed by etching, An exemplary, usable etching method is reactive ion etching (RIE), in particular, inductively coupled plasma (ICP) RIE. Specifically, for example, ICP-RIE can be employed which utilizes SF_6 or mixed gas of SF_6 and O_2 as reactive gas. By means of such etching, in a region in which trench **17** (FIG. **1**) is to be formed, a recess TQ is formed which includes: side portion **17***a* substantially perpendicular first main surface **10***a;* and bottom portion **17***b* continuously connected to side portion **17***a* and substantially parallel to first main surface **10***a*.

[0112] Next, thermal etching is performed in recess TQ. This thermal etching can be performed by, for example, heat-

ing in an atmosphere containing reactive gas having at least one or more types of halogen atom. The at least one or more types of halogen atom include at least one of chlorine (Cl) atom and fluorine (F) atom. This atmosphere is, for example, Cl_2, BCL_3, SF_6, or CF_4. For example, the thermal etching is performed using a mixed gas of chlorine gas and oxygen gas as a reactive gas, at a heat treatment temperature of, for example, not less than 700° C. and not more than 1000° C.

[0113] It should be noted that the reactive gas may contain a carrier gas in addition to the chlorine gas and the oxygen gas. An exemplary, usable carrier gas is nitrogen (N_2) gas, argon gas, helium gas, or the like. When the heat treatment temperature is set at not less than 700° C. and not more than 1000° C. as described above, a rate of etching SiC is approximately, for example, 70 μm/hour. In addition, in the thermal etching, mask layer **90**, which is formed of silicon oxide and therefore has a very large selection ratio relative to Sic, is not substantially etched during the etching of SiC.

[0114] As shown in FIG. **20**, by the thermal etching, trench **17** is formed in first main surface **10***a* of silicon carbide substrate **10**. Trench **17** includes: side portion **17***a* extending to drill region **13** through source region **15** and body region **14**; and bottom portion **17***b* located in drift region **13**. Each of side portion **17***a* and bottom portion **17***b* is away from electric field relaxing region **18**. When each of source region **15**, body region **14**, and drift region **13** is thermally etched to form side portion **17***a* of trench **17**, mask layer **90** is not substantially etched, so that mask layer **90** remains to project front above first main surface **10***a* to above side portion **17***a* of trench **17**. Next, mask layer **90** is removed by means of an appropriate method such as etching (see FIG. **21**).

[0115] Preferably, side portion **17***a* of trench **17** is inclined relative to bottom portion **17***b* at an angle of, for example, not less than 50° and not more than 70°. Preferably, during the formation of trench **17**, the special plane described above is spontaneously formed on side portion **17***a*, in particular, on body region **14**. Specifically, side portion **17***a* of trench **17** includes first plane **S1** having a plane Orientation of {0-33-8}. Preferably, side portion **17***a* of trench **17** microscopically includes first plane **S1**, and side portion **17***a* microscopically further includes second plane **S2** having a plane orientation of {0-11-1}. More preferably, first plane **S1** and second plane **S2** of side portion **17***a* of trench **17** include combined plane SR having a plane orientation of {0-11-2}. Side portion **17***a* of trench **17** macroscopically has an off angle of 62°±10° relative to the {000-1} plane.

[0116] In this way, silicon carbide substrate **10** is prepared which has first main surface **10***a* and second main surface **10***b* opposite to first main surface **10***a* and in which trench **17** is formed in first main surface **10***a*. Silicon carbide substrate **10** includes: drift region **13** (first impurity region) that has n type; body region **14** that is provided on drift region **13** and that has p type; and source region **15** that is provided on body region **14** so as to be separated from drift region **13**, that forms first main surface **10***a*, and that has n type.

[0117] Next, a gate insulating film forming step (S**40**: FIG. **15**) is performed. Preferably, gate insulating film **20** is formed by thermally oxidizing silicon carbide substrate **10** in which trench **17** is formed. Specifically, silicon carbide substrate **10** having trench **17** formed therein is heated at, for example, about 1300° C. in an atmosphere including oxygen., thereby forming Rate insulating film **20**. As shown in FIG. **22**, gate insulating film **20** is formed to cover side portion **17***a* and bottom portion **17***b* of trench **17** and first main surface **10***a*. Gate insulating film **20** is formed to cover corner portion **17***c* formed by side portion **17***a* of trench **17** and first main surface **10***a* of silicon carbide substrate **10**.

[0118] As shown in FIG. **23**, thickness d**1** of gate insulating film **20** in the vicinity of corner portion **17***c* is formed to be smaller than thickness d**2** of gate insulating film **20** on first main surface **10***a* and thickness d**3** of gate insulating film **20** on side portion **17***a* of trench **17**. Accordingly, gate insulating film **20** in the vicinity of corner portion **17***c* becomes more likely to result in dielectric breakdown.

[0119] After thermally oxidizing silicon carbide substrate **10**, a heat treatment (NO annealing) may be performed onto silicon carbide substrate **10** in a nitrogen monoxide (NO) gas atmosphere. In the NO annealing, silicon carbide substrate **10** is held for about 1 hour under a temperature of not less than 1100° C. and not more than 1300° C. Accordingly, nitrogen atoms are introduced in an interface region between gate insulating film **20** and body region **14**. As a result, formation of interface states in the interface region is suppressed, thereby achieving improved channel mobility. It should be noted that a gas other than the NO gas may be employed as the atmospheric gas as long as the nitrogen atoms can be thus introduced. After the NO annealing, Ar annealing may be further performed using argon (Ar) as an atmospheric gas. The Ar annealing is preferably performed at a heating temperature equal to or higher than the heating temperature in the above-described NO annealing and lower than the melting point of gate insulating film **20**. This heating temperature is held for approximately 1 hour, for example. Accordingly, formation of interface states in the interface region between gate insulating film **20** and body region **14** is further suppressed. It should be noted that instead of the Ar gas, an inert gas such as nitrogen gas may be employed as the atmospheric gas.

[0120] Next, a gate electrode forming step (S**50**: FIG. **15**) is performed. As shown in FIG. **24**, gate electrode **30** is formed in contact with gate insulating film **20** within trench **17**. Gate electrode **30** is formed in trench **17** to face each of side portion **17***a* and bottom portion **17***b* of trench **17** with gate insulating film **20** interposed therebetween. Gate electrode **30** is formed by, for example, a LPCVD (Low Pressure Chemical Vapor Deposition) method. Gate electrode **30** is formed within trench **17** so as not to cover corner portion **17***c*.

[0121] Next, an interlayer insulating film forming step (S**60**: FIG. **15**) is performed. With reference to FIG. **25**, interlayer insulating film **40** is formed which is provided with opening **40***a***1** and opening **40***b***1** to expose a portion of gate electrode **30**. Specifically, interlayer insulating film **40** includes: first interlayer insulating film **40***a* in which opening **40***a***1** having a first width is formed; and a second interlayer insulating film **40***b* which is provided on first interlayer insulating film **40***a* and in which opening **40***b***1** having a second width larger than the first width is formed. Interlayer insulating film **40***a* is in contact with an outer circumferential region of upper surface **30***a* of gate electrode **30**, and is not in contact with a central region of upper surface **30***a*. In other words, when viewed in a cross section, interlayer insulating film **40***a* is formed to extend from above source region **15** to above gate electrode **30** so as to cover corner portion **17***c*. Interlayer insulating film **40** is preferably formed by a deposition method, and is more preferably formed by a chemical vapor deposition method. Interlayer insulating film **40** is a material including silicon dioxide, for example.

[0122] Next, a gate interconnection forming step (S**70**: FIG. **15**) is performed. Gate interconnection **32** is formed to fill opening **40***a***1** formed in first interlayer insulating film **40***a,* and is formed to fill opening **40***a***2** formed in second interlayer insulating film **40***b.* Gate interconnection **32** is formed in contact with gate electrode **30** at upper surface **30***a* of gate electrode **30**. Preferably, gate interconnection **32** is made of a material having a melting point of not less than 1000° C. Specifically, the material of gate interconnection **32** includes at least one material selected from a group consisting of W (tungsten), Ni (nickel), WSi (tungsten silicide), and polysilicon. Interlayer insulating film **41** is formed on gate interconnection **32**.

[0123] The gate interconnection forming step may include the step of forming barrier layer **32***c* in contact with each of gate electrode **30** and interlayer insulating film **40**. For example, barrier layer **32***c* is formed in contact with the upper surface of interlayer insulating film **40** and the wall surface forming opening **40***a***1** formed in interlayer insulating film **40** as well as upper surface **30***a* of gate electrode **30** (see FIG. **5**). Preferably, barrier layer **32***c* includes at least one of Ti and TiN.

[0124] Next, a gate pad forming step (S**80**, FIG. **15**) is performed. Gate pad **33** is formed in contact with gate interconnection **32** through the opening formed in interlayer insulating film **41** (see FIG. **6**). Gate pad **33** is made of a material including AlSiCu, for example.

[0125] Next, a source electrode forming step is performed. With reference to FIG. **26**, etching is performed to form opening **40***a***2** in interlayer insulating film **40** and gate insulating film **20**. Through the opening, each of source region **15** and contact region **16** is exposed at first main surface **10***a* of silicon carbide substrate **10**. Next, on first main surface **10***a,* source electrode **60** is formed in contact with each of source region **15** and contact region **16**. Source electrode **60** is made of a material including Ti, Al, and Si, for example. Next, an alloying annealing is performed. Specifically, source electrode **60** in contact with each of source region **15** and contact region **16** is held for about 5 minutes at a temperature of not less than 900° C. and not more than 1100° C., for example. Accordingly, at least a portion of source electrode **60** reacts with silicon included in silicon carbide substrate **10**, whereby it is silicided and alloyed. In this way, source electrode **60** in ohmic contact with source region **15** is formed. Next, drain electrode **70** is formed in contact with second main surface **10***b* of silicon carbide substrate **10**. Next, lower pad electrode **80** is formed in contact with drain electrode **70**. In this way, MOSFET 1 is obtained (FIG. **1**).

[0126] Next, a modification of the gate insulating film forming step (S**40**: FIG. **15**) will be described.

[0127] After forming silicon carbide substrate **10** having first main surface **10***a* in which trench **17** is formed as shown in FIG. **21**, insulating film. **43** is formed in contact with first main surface **10***a* of silicon carbide substrate **10** (see FIG. **27**). Insulating film **43** is formed to extend from above corner portion **17***c* to above contact region **16** via above source region **15**, for example. Insulating film **43** is a material including silicon dioxide, for example. Insulating film **43** may be a material including SiON, SiN, or the like. Preferable, insulating film **43** is formed by the chemical vapor deposition method.

[0128] With reference to FIG. **28**, silicon carbide substrate **10** having first main surface **10***a* in which trench **17** is formed is thermally oxidized. Specifically, side portion **17***a* and bottom portion **17***b* of trench **17** are thermally oxidized with insulating film **43** being formed on first main surface **10***a.* In other words, insulating film **43** and side portion **17***a* and bottom portion **17***b* of trench **17** are oxidized simultaneously. In this way, gate insulating film **20** is formed in contact with insulating film **43** as well as each of side portion **17***a* and bottom portion **17***b* of trench **17**.

[0129] With reference to FIG. **29**, gate electrode **30** is formed in contact with gate insulating film **20** within trench **17**. Next, interlayer insulating film **40***a* is formed in contact with the outer circumferential region of upper surface **30***a* of gate electrode **30** and insulating film **43**. Interlayer insulating film **40***a* is formed to extend from above source region **15** to abode gate electrode **30** so as to cover corner portion **17***c.* In other words, opening **40***a***1** is formed in interlayer insulating film **40***a* to expose the central. region of upper surface **30***a* of gate electrode **30**.

[0130] Although the MOSFET has been illustrated as an example of the silicon carbide semiconductor device in the present embodiment, the silicon carbide semiconductor device may be an IGBT (Insulated Gate Bipolar Transistor). Moreover, in the present embodiment, it has been illustrated that n type corresponds to the first conductivity type and p type corresponds to the second conductivity type, but p type may correspond to the first conductivity type and n type may correspond to the second conductivity type.

[0131] The following describes function and effect of MOSFET 1 serving as the silicon carbide semiconductor device according to the present embodiment.

[0132] In accordance with MOSFET 1 according to the present embodiment, when viewed in a cross section, interlayer insulating film **40***a* extends from above source region **15** to above gate electrode **30** so as to cover corner portion **17***c.* This leads to effective suppression of breakdown of gate insulating film **20** and interlayer insulating film **40***a* on corner portion **17***c.* As a result, the dielectric breakdown resistance of MOSFET 1 can be improved.

[0133] Further, in accordance with MOSFET 1 according to the present embodiment, gate interconnection **32** is made of a material having a melting point of not less than 1000° C. Accordingly, for example, even when gate interconnection **32** is heated to not less than 1000° C. in the alloying annealing step, gate interconnection **32** can be suppressed from being melted.

[0134] Further, in accordance with MOSFET 1 according to the present embodiment, the material includes at least one material selected from a group consisting of W, Ni, WSi, and polysilicon. Accordingly, gate interconnection **32** can be effectively suppressed from being melted.

[0135] Further, in accordance with MOSFET 1 according to the present embodiment, interlayer insulating film **40***a* has a carbon concentration smaller than a. carbon concentration of gate insulating film **20**. Accordingly, the insulating property of the insulating film is improved and leakage current can be reduced.

[0136] Further, MOSFET 1 according to the present embodiment includes barrier layer **32***c* in contact with each of gate. interconnection **32**, gate electrode **30**, and interlayer insulating film **40***a.* Accordingly, the insulation performance of MOSFET 1 can be suppressed from being deteriorated by aluminum being diffused in interlayer insulating film **40***a.*

[0137] Further, in accordance with MOSFET 1 according to the present embodiment, barrier layer **32***c* includes at least

one of Ti and TiN. Accordingly, adhesion can be improved between interlayer insulating film **40***a* and gate interconnection **32**.

[0138] MOSFET 1 according to the present embodiment further includes gate pad **33** in contact with gate interconnection **32**. Accordingly, voltage can be effectively applied to gate interconnection **32**.

[0139] Further, in accordance with MOSFET 1 according to the present embodiment, side portion **17***a* of the trench includes first plane S**1** having a plane orientation of {0-33-8}, Accordingly, channel resistance in side portion **17***a* can be reduced, thereby reducing on-resistance.

[0140] Further, in accordance with MOSFET 1 according to the present embodiment, side portion **17***a* of the trench microscopically includes first plane S**1**, and side portion **17***a* microscopically further includes second plane S**2** having a plane orientation of {0-11-1}. Accordingly, channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0141] Further, in accordance with MOSFET 1 according to the present embodiment, first plane S**1** and second plane S**2** of side portion **17***a* of the trench include a combined plane SR having a plane orientation of {0-11-2}. Accordingly, channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0142] Further, in accordance with MOSFET 1 according to the present embodiment, side portion **17***a* of the trench macroscopically has an off angle of 62°±10° relative to a {000-1} plane. Accordingly, channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0143] In accordance with the method for manufacturing MOSFET 1 according to the present embodiment, when viewed in a cross section, interlayer insulating. film **40***a* extends from above source region **15** to above gate electrode **30** so as to cover corner portion **17***c*. This leads to effective suppression of breakdown of gate insulating film **20** and interlayer insulating film **40***a* on corner portion **17***c*. As a result, the dielectric breakdown resistance of MOSFET 1 can be improved.

[0144] Further, in accordance with the method for manufacturing MOSFET 1 according to the present embodiment, gate insulating film **20** is formed by thermally oxidizing silicon carbide substrate **10** in which trench **17** is formed. In this way, gate insulating film **20** haying excellent insulation performance can be formed.

[0145] Further, in accordance with the method for manufacturing MOSFET 1 according to the present embodiment, interlayer insulating film **40** is formed by a chemical vapor deposition method. Accordingly, as compared with a case where the insulating film is formed by thermal oxidation, thick interlayer insulating film **40** can be grown for a shorter period of time.

[0146] Further, the method for manufacturing MOSFET 1 according to the present embodiment further includes the step of forming insulating film **43** in contact with main surface **10***a* of silicon carbide substrate **10** in which trench **17** is formed. In the step of forming gate insulating film **20**, side portion **17***a* and bottom portion **17***b* of trench **17** is thermally oxidized with insulating film **43** being formed on main surface **10***a*. Accordingly, the thickness of the insulating film on corner portion **17***c* is increased, thereby improving the dielectric breakdown resistance of MOSFET 1.

[0147] Further, in accordance with the method for manufacturing MOSFET 1 according to the present embodiment, the step of forming gate interconnection **32** includes the step of forming barrier layer **32***c* in contact with each of gate electrode **30** and interlayer insulating film **40**. Accordingly, the insulation performance of MOSFET 1 can be suppressed from being deteriorated by aluminum being diffused in interlayer insulating film **40***a*.

[0148] Further, in accordance with the method for manufacturing MOSFET 1 according to the present embodiment, barrier layer **32***c* includes at least one of Ti and TiN. Accordingly, adhesion can be improved between interlayer insulating film **40***a* and gate interconnection **32**.

[0149] The method for manufacturing MOSFET 1 according to the present embodiment further includes the step of forming gate pad **33** in contact with gate interconnection **32**. Accordingly, voltage can be effectively applied to gate interconnection **32**.

[0150] Further, in accordance with the method for manufacturing MOSFET 1 according to the present embodiment, side portion **17***a* of trench **17** includes first plane S**1** having a plane orientation of {0-33-8}. Accordingly, channel resistance in side portion **17***a* can be reduced, thereby reducing on-resistance.

[0151] Further, in accordance with the method for manufacturing MOSFET 1 according to the present embodiment, side portion **17***a* of trench **17** microscopically includes first plane S**1**, and side portion **17***a* microscopically further includes second plane S**2** having a plane orientation of {0-11-1}. Accordingly, channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0152] Further, in accordance with the method for manufacturing MOSFET 1 according to the present embodiment, first plane S**1** and second plane S**2** of side portion **17***a* of trench **17** include combined plane SR having a plane orientation of {0-11-2}. Accordingly, channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0153] Further, in accordance with the method for manufacturing MOSFET 1 according to the present embodiment, side portion **17***a* of trench **17** macroscopically has an off angle of 62°±10° relative to a {000-1} plane. Accordingly, channel resistance in side portion **17***a* can be further reduced, thereby reducing on-resistance.

[0154] Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being interpreted by the terms of the appended claims.

What is claimed:

1. A silicon carbide semiconductor device comprising a silicon carbide substrate having a main surface,

said silicon carbide substrate including

a first impurity region that has a first conductivity type,

a second impurity region that is provided on said first impurity region and that has a second conductivity type different from said first conductivity type, and

a third impurity region that is provided on said second impurity region so as to be separated from said first impurity region, that forms said main surface, and that has said first conductivity type,

said main surface of said silicon carbide substrate being provided with a trench,

said trench having a side portion and a bottom portion, said side portion extending to said first impurity region through said third impurity region and said second impurity region, said bottom portion being located in said first impurity region,

the silicon carbide semiconductor device further comprising:

a gate insulating film in contact with a corner portion formed by said side portion and said main surface, said bottom portion, and said side portion;

a gate electrode in contact with said gate insulating film within said trench;

an interlayer insulating film in which an opening is formed to expose a portion of said gate electrode; and

a gate interconnection disposed in said opening and in contact with said gate electrode,

when viewed in a cross section, said interlayer insulating film extending from above said third impurity region to above said gate electrode so as to cover said corner portion.

2. The silicon carbide semiconductor device according to claim **1**, wherein said gate interconnection is made of a material having a melting point of not less than 1000° C.

3. The silicon carbide semiconductor device according to claim **2**, wherein said material includes at least one material selected from a group consisting of W, Ni, WSi, and polysilicon.

4. The silicon carbide semiconductor device according to claim **1**, wherein said interlayer insulating film has a carbon concentration smaller than a carbon concentration of said gate insulating film.

5. The silicon carbide semiconductor device according to claim **1**, wherein said gate interconnection includes a barrier layer in contact with each of said gate electrode and said interlayer insulating film.

6. The silicon carbide semiconductor device according to claim **5**, wherein said barrier layer includes at least one of Ti and TiN.

7. The silicon carbide semiconductor device according to claim **1**, further comprising a gate pad in contact with said gate interconnection.

8. The silicon carbide semiconductor device according to claim **1**, wherein said side portion of said trench includes a first plane having a plane orientation of {0-33-8}.

9. The silicon carbide semiconductor device according to claim **8**, wherein said side portion of said trench microscopically includes said first plane, and said side portion microscopically further includes a second plane having a plane orientation of {0-11-1}.

10. The silicon carbide semiconductor device according to claim **9**, wherein said first plane and said second plane of said side portion of said trench include a combined plane having a plane orientation of {0-11-2}.

11. The silicon carbide semiconductor device according to claim **10**, wherein said side portion of said trench macroscopically has an off angle of 62°±10° relative to a {000-1} plane.

12. A method for manufacturing a silicon carbide semiconductor device, comprising the step of preparing a silicon carbide substrate having a main surface,

said silicon carbide substrate including

a first impurity region that has a first conductivity type,

a second impurity region that is provided on said first impurity region and that has a second conductivity type different from said first conductivity type, and

a third impurity region that is provided on said second impurity region so as to be separated from said first impurity region, that forms said main surface, and that has said first conductivity type,

said main surface of said silicon carbide substrate being provided with a trench,

said trench having a side portion and a bottom. portion, said side portion extending to said first impurity region through said third impurity region and said second impurity region, said bottom portion being located, in said first impurity region,

the method for manufacturing the silicon carbide semiconductor device further comprising the steps of:

forming a gate insulating film in contact with a corner portion formed by said side portion and said main surface, said bottom portion, and said side portion;

forming a gate electrode in contact with said gate insulating film within said trench;

forming an interlayer insulating film in which an opening is formed to expose a portion of said gate electrode; and

forming a gate interconnection disposed in said opening and in contact with said gate electrode,

when viewed in a cross section, said interlayer insulating film extending from above said third impurity region to above said gate electrode so as to cover said corner portion.

13. The method for manufacturing the silicon carbide semiconductor device according to claim **12** wherein said gate insulating film is formed by thermally oxidizing said silicon carbide substrate in which said trench is formed.

14. The method for manufacturing the silicon carbide semiconductor device according to claim **12**, wherein said interlayer insulating am is formed by a chemical vapor deposition method.

15. The method for manufacturing the silicon carbide semiconductor device according to claim **12**, further comprising the step of forming an insulating layer in contact with said main surface of said silicon carbide substrate in which said trench is formed, wherein

in the step of forming said gate insulating film, said side portion and said bottom portion of said trench is thermally oxidized with said insulating layer being formed on said main surface.

16. The method for manufacturing the silicon carbide semiconductor device according to claim **12**, wherein the step of forming said gate interconnection includes the step of forming a barrier layer in contact with each of said gate electrode and said interlayer insulating film.

17. The method for manufacturing the silicon carbide semiconductor device according to claim **16**, wherein said barrier layer includes at least one of Ti and TiN.

18. The method for manufacturing the silicon carbide semiconductor device according to claim **12**, further comprising the step of forming a gate pad in contact with said gate interconnection.

19. The method for manufacturing the silicon carbide semiconductor device according to claim **12**, wherein said side portion of said trench includes a first plane having a plane orientation of {0-33-8}.

20. The method for manufacturing the silicon carbide semiconductor device according to claim **19**, wherein said side portion of said trench microscopically includes said first plane, and said side portion microscopically further includes a second plane having a plane orientation of {0-11-1}.

21. The method for manufacturing the silicon carbide semiconductor device according to claim **20**, wherein said first plane and said second plane of said side portion of said trench include a combined plane having a plane orientation of {0-11-2}.

22. The method for manufacturing the silicon carbide semiconductor device according to claim **21**, wherein said side portion of said trench macroscopically has an off angle of 62°±10° relative to a {000-1} plane.

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