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- (71) Applicant: **SANDISK TECHNOLOGIES INC.**
[US/US]; Two Legacy Town Center, 6900 North Dallas Parkway, Plano, Texas 75024 (US).
- (72) Inventor: **PICHEN, Abdulla**; #104 IND-WIN Pavillion Apts, Vibuthipura Main Road, Annasandra Palya, Hal Post, Bangalore 560017 (IN).
- (74) Agent: **TOLER, JEFFREY G.**; 8500 Bluffstone Cove, Suite A201, Austin, Texas 78759 (US).

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(54) Title: SYSTEM AND METHOD OF READING DATA FROM MEMORY CONCURRENTLY WITH SENDING WRITE DATA TO THE MEMORY

(57) Abstract: A data storage device includes a memory, a controller, and a communication bus coupled to the memory and to the controller. The controller is configured to send a read-write command and write data to the memory via the communication bus. The read-write command indicates an address of requested data to be read from the memory. The controller is further configured to receive the requested data read from the memory. Communicating the requested data over the communication bus overlaps the write data being stored into the memory.

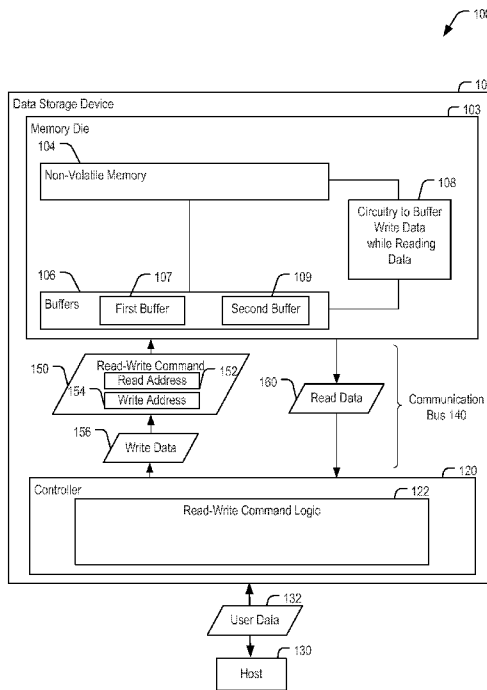


FIG. 1

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**SYSTEM AND METHOD OF READING DATA FROM MEMORY
CONCURRENTLY WITH SENDING WRITE DATA TO THE MEMORY**

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims priority from Indian Application No. 1019/CHE/2013,
5 filed March 12, 2013, the contents of which are incorporated by reference herein in their
entirety.

FIELD OF THE DISCLOSURE

The present disclosure is generally related to retrieving data from and storing in a data
storage device.

10 **BACKGROUND**

Non-volatile data storage devices, such as universal serial bus (USB) flash memory
devices or removable storage cards, have allowed for increased portability of data and
software applications. Flash memory devices may take more time to perform a write
operation than to perform a read operation. When a read operation for reading data
15 stored in the flash memory device is requested while a write operation is being
performed, the flash memory device may complete the write operation before
performing the read operation, which may cause latency in reading the stored data.

SUMMARY

Latency of reading data stored in a memory of a data storage device may be improved
20 by reading data from the memory of the data storage device concurrently with
transferring write data to the memory of the data storage device. A read-write command
and write data may be sent from a controller of the data storage device. The read-write
command indicates requested data to be read from the memory. The requested data is
read from the memory while write data is transferred from the controller. After transfer
25 of the write data from the controller has completed, the requested data may be sent from
to the controller while the write data is written into the memory.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a particular illustrative embodiment of a system including a data storage device including a controller configured to receive requested data read from a memory at least partially concurrently with write data being stored into the memory;

5 FIG. 2 is a timing diagram illustrating a particular embodiment of signals and data associated with the read-write command of the data storage device of FIG. 1; and

FIG. 3 is a flowchart of a particular illustrative embodiment of a method of receiving requested data read from a memory within a data storage device at least partially concurrently with write data being stored into the memory.

10 **DETAILED DESCRIPTION**

Referring to FIG. 1, a particular embodiment of a system 100 includes a data storage device 102 coupled to a host device 130. The data storage device 102 includes a memory die 103 coupled to a controller 120 via a communication bus 140. The data storage device 102 is configured to send requested data from the memory die 103 to the controller 120. Sending the requested data to the controller 120 overlaps with write data 15 156 being written to a memory 104 on the memory die 103.

The host device 130 may be configured to provide data, such as the user data 132, to be stored at the memory 104 or to request data to be read from the memory 104. For example, the host device 130 may include a mobile telephone, a music player, a video 20 player, a gaming console, an electronic book reader, a personal digital assistant (PDA), a computer, such as a laptop computer or notebook computer, any other electronic device, or any combination thereof. The host device 130 communicates via a memory interface that enables reading from the memory 104 and writing to the memory 104. For example, the host device 130 may operate in compliance with a Joint Electron 25 Devices Engineering Council (JEDEC) industry specification, such as a Universal Flash Storage (UFS) Host Controller Interface specification. As other examples, the host device 130 may operate in compliance with one or more other specifications, such as a Secure Digital (SD) Host Controller specification as an illustrative example. The host device 130 may communicate with the memory 104 in accordance with any other 30 suitable communication protocol.

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The data storage device 102 may be a memory card, such as a Secure Digital SD® card, a microSD® card, a miniSD.TM card (trademarks of SD-3C LLC, Wilmington, Delaware), a MultiMediaCard.TM (MMC.TM) card (trademark of JEDEC Solid State Technology Association, Arlington, Virginia), or a CompactFlash® (CF) card
5 (trademark of SanDisk Corporation, Milpitas, California). As another example, the data storage device 102 may be configured to be coupled to the host device 130 as embedded memory, such as eMMC® (trademark of JEDEC Solid State Technology Association, Arlington, Virginia) and eSD, as illustrative examples. To illustrate, the data storage device 102 may correspond to an eMMC (embedded MultiMedia Card) device. The
10 data storage device 102 may operate in compliance with a JEDEC industry specification. For example, the data storage device 102 may operate in compliance with a JEDEC eMMC specification, a JEDEC Universal Flash Storage (UFS) specification, one or more other specifications, or a combination thereof.

The memory die 103 may include the memory 104, a set of buffers 106, and circuitry
15 108 to buffer write data in the set of buffers 106 on the memory die 103 while reading requested data from the memory 104. The memory 104 may be a non-volatile memory, such as a NAND flash memory, and may be configured to store the requested data to be read from the memory die 103 (e.g., a flash die). The memory 104 may include multiple groups of storage elements, such as word lines, pages, or blocks. As an
20 example, the memory 104 may include a multi-level cell (MLC) flash memory.

The set of buffers 106 may include a first buffer 107 and a second buffer 109. The set of buffers 106 may be configured to store requested data, such as read data 160, that is read from the memory 104 while the memory die 103 receives the write data 156 from the controller 120. For example, the first buffer 107 may be configured to store at least
25 a portion of the requested data 160 that is read from the memory 104 while at least a portion of the write data 156 is received via the communication bus 140 and stored to the second buffer 109.

The circuitry 108 may be configured to enable the set of buffers 106 to store the requested data 160 that is read from the memory 104 while the memory die 103 receives
30 the write data 156 from the controller 120. For example, the circuitry 108 may be responsive to receipt of a read-write command 150 to enable the first buffer 107 to store

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at least a portion of the requested data 160 read from the memory 104 while at least a portion of the write data 156 is received via the communication bus 140 and stored to the second buffer 109.

The controller 120 may be configured to receive data and instructions from and to send data to the host device 130 while the data storage device 102 is operatively coupled to the host device 130. The controller 120 may further be configured to send data and commands to the memory 104 and to receive data from the memory 104. For example, the controller 120 may be configured to send data and a write command to instruct the memory 104 to store the data to a specified address. As another example, the controller 120 may be configured to send a read command to read data from a specified address of the memory 104.

The controller 120 includes read-write command logic 122 that is configured to generate the read-write command 150. The read-write command 150 includes a read address 152 and a write address 154. The read address 152 may correspond to a read location in the memory 104 and the write address 154 may correspond to a write location in the memory 104. For example, data read from the memory 104, such as the requested data 160, may be read from the read location in the memory 104 and data sent to the memory 104, such as the write data 156, may be sent to the write location in the memory 104.

The controller 120 may be configured to send the read-write command 150 and the write data 156 to the memory die 103 via the communication bus 140 to instruct the memory 104 to read the requested data 160 from the specified read address 152 of the memory 104 and to store the write data 156 to the specified write address 154 of the memory 104. For example, the controller 120 may be configured to send the write data 156 to the memory die 103 by placing the write data 156 onto the communication bus 140, and the memory die 103 may be configured to receive the write data 156 by retrieving the write data 156 from the communication bus 140 and storing the write data 156 to the second buffer 109. The controller 120 may further be configured to receive the requested data 160 read from the memory 104 while the write data 156 is being stored into the memory 104. For example, the memory die 103 may be configured to place the requested data 160 that is stored in the first buffer 107 onto the communication

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bus 140, and the controller 120 may be configured to receive the requested data 160 by retrieving the requested data 160 from the communication bus 140 while the write data 156 is being sent from the second buffer 109 to the memory 104.

During operation, in response to receiving a read request for the requested data 160
5 from the host device 130 while a write operation is ongoing, the controller 120 may initiate a data read operation at the memory 104. The data read operation may be initiated by the controller 120 during data transfer of the write data 156 to the memory die 103 via the communication bus 140. For example, in response to receiving the read request, the controller 120 may send the read-write command 150 and the write data 156
10 to the memory die 103 via the communication bus 140. The requested data 160 may be read from the read address 152 of the memory 104 while the write data 156 is being transferred to the memory die 103. At least a portion of the requested data 160 read from the memory 104 may be stored to the first buffer 107 while at least a portion of the write data 156 is concurrently stored to the second buffer 109. In one implementation,
15 the requested data 160 read from the memory 104 may remain in the first buffer 107 until transmission of the write data 156 to the memory die 103 via the communication bus 140 is complete. Upon completion of data transfer of the write data 156 on the communication bus 140 to the memory die 103, the controller 120 may receive the read data 160 from the memory die 103 via the communication bus 140.

20 As another example, when the data storage device 102 is performing a sequential write operation, such as when storing multiple sets of data to sequential addresses in the memory 104, and a read request is received from the host device 130, one or more write operations of the sequential write operation may be replaced with a read-write operation. The controller 120 may send the read-write command 150 and the write data
25 156 to the memory die 103 via the communication bus 140 as described above. For example, a read request from the host device 130 may have a higher priority than a write request from the host device 130. When a read operation for reading the read data 160 stored in the memory 104 is requested by the host device 130 while a sequential write operation is being performed, the controller 120 may replace one or more write
30 operations of the sequential write operation with the read-write command 150. As a result, reduced read latency may be experienced by the host device 130.

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By receiving the requested data 160 read from the memory 104 at least partially concurrently with the write data 156 being stored into the memory 104, and by reading the requested data 160 from the memory 104 while the write data 160 is being transferred to the memory die 103, reduced read latency may be experienced by the host device 130 as compared to systems without the read-write command 150.

Referring to FIG. 2, a timing diagram 200 illustrating a particular embodiment of signals and data associated with the read-write command 150 of FIG. 1 is shown. The timing diagram 200 illustrates data transfer with reference to signaling on the communication bus 140 of FIG. 1. However, it should be understood that the read-write command 150 and the communication bus signaling illustrated in FIG. 2 may be implemented in devices or systems other than the data storage device 102 of FIG. 1.

The communication bus 140 may include multiple lines that are logically grouped into an input/output (I/O) portion 210 and control signaling 211. Data that is transferred via the I/O portion 210 is illustrated as an I/O trace 202. The control signaling 211 includes a ready/busy signal 230, a write enable signal 240, and a read enable signal 250.

The ready/busy signal 230 may be asserted by the memory die 103 of FIG. 1 to indicate when the memory die 103 is busy with an erase, program, or read operation. For example, the ready/busy signal 230 may be asserted low (e.g., "busy") when the memory die 103 is busy with an erase, program, or read operation and may be asserted high (e.g., "ready") otherwise.

The write enable signal 240 may be responsible for clocking data, address, or command information into the memory die 103. To illustrate, in a write operation, data to be programmed, such as the write data 156, may be "clocked" (e.g., synchronously transferred as sequential data words) from I/O lines of the communication bus 140 into the buffers 106 on rising edges of the write enable signal 240.

The read enable signal 250 may enable output data buffers, such as one or more of the buffers 106. For example, data that has been read from the memory 104 and that is stored in the buffers 106 may be clocked from the buffers 106 onto I/O lines of the communication bus 140 on rising edges of the read enable signal 250.

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The I/O trace 202 illustrates data transfer to and from the memory die 103. The I/O trace 202 includes a plurality of data transfer units. For example, the plurality of data transfer units may be data packets. Each data packet may include multiple bits that are sent in parallel over multiple lines of the input/output portion 210 of the communication bus 140 during a bus cycle. The data packets may include a command identifier packet 204 and a command termination packet 212. The command identifier packet 204 may include a set of bits to identify the read-write command 150. The command termination packet 212 may indicate that write data transfer is complete.

The read-write command 150 is illustrated with reference to various signals on lines of the communication bus 140 and includes a header (e.g., a command identifier packet 204), the read address 152, and the write address 154. The read-write command 150 and associated data are illustrated as being transferred during multiple bus cycles, illustrated as bus cycle A, bus cycle B, bus cycle C... bus cycle K.

During bus cycle A, the command indicator 204 indicating the read-write command 150 may be transferred via a communication bus between a controller and a memory die. To illustrate, the controller 120 may write the command indicator 204 onto the I/O portion 210 of the communication bus 140 and may drive a rising edge of the write enable signal 240. The memory die 103 may receive the command indicator 204 by reading the command indicator 204 from the communication bus 140, such as by clocking data from the I/O lines 202 into the buffers 106 on a rising edge of the write enable signal 240.

During bus cycle B and bus cycle C, one or more read addresses and write addresses may be transferred via the communication bus between the controller and the memory die. For example, the controller 120 may put the read address 152 and the write address 154 on the communication bus 140 during bus cycle B and bus cycle C, respectively. The memory die 103 may receive the read address 152 and the write address 154 by reading the read address 152 and the write address 154 from the communication bus 140 of FIG. 1, such as by clocking the read address 152 and the write address 154 into the buffers 106 on a rising edge of the write enable signal 240 during bus cycle B and bus cycle C.

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The write data 156 is illustrated as transferred during bus cycles D- G. For example, the controller 120 may write sequential portions of the write data 156 onto the I/O portion 210 during sequential bus cycles and may raise the write enable signal 240 to signal to the memory die 103 to read each portion from the I/O lines 202. The memory die 103
5 may receive the write data 156 by reading the write data 156 from the communication bus 140, such as by clocking sequential portions of the write data 156 into the buffers 106 on a rising edge of the write enable signal 240.

Concurrently with the controller 120 sending the write data 156 and the memory die 103 receiving the write data 156 during bus cycles D-G, the memory die 103 may perform a
10 read operation 232 to read data from a location in the memory 104 corresponding to the read address 152. Data read from the memory 104 may be stored into the buffers 106 for later transfer to the controller 120 via the communication bus 140 after the write data 156 has been transferred. While the read operation 232 is ongoing, the ready/busy signal 230 may be asserted by the memory die 103 indicating that the read operation
15 232 is being performed in the memory die 103. The ready/busy signal 230 may remain asserted until the read operation 232 is complete. However, in other implementations, the ready/busy signal 230 may not be asserted while the read operation 232 is being performed.

During bus cycle H, an indication that write data transfer is complete may be transferred
20 via the communication bus between the controller and the memory die. For example, the controller 120 may put the command termination packet 212 on the communication bus 140 during bus cycle H. The memory die 103 may receive the command termination packet 212 by reading the command termination packet 212 from the communication bus 140. The command termination packet 212 may be clocked into the
25 buffers 106 on a rising edge of the write enable signal 240.

During bus cycles I-K (e.g., after the command termination packet 212 is transferred indicating that write data 156 transfer is complete), a write operation 234 may be performed. For example, the write data 156 may be transferred from the buffers 106 to the memory 104. During the write operation 234, the ready/busy signal 230 may be
30 asserted by the memory die 103 (indicating that the memory die 103 is busy), the write enable signal 240 may not be toggled by the controller 120, and the read enable signal

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250 may be asserted by the controller 120 and toggled to clock the read data 160 from the buffers 106 onto the communication bus 140. Assertion of the read enable signal 250 during the write operation 234 may enable the requested data 160 to be transferred from the memory die 103 via the bus 140 to the controller 120 of FIG. 1 during bus
5 cycles I-K and the write data 156 to be transferred from the buffers 106 to the memory 104 during bus cycles I-K. For example, the memory die 103 may put the requested data 160 that is stored in the buffers 106 on the communication bus 140. The controller 120 may receive the requested data 160 by reading the requested data 160 from the communication bus 140 during bus cycles I-K.

10 The read-write command 150 enables multiple operations to overlap. As used herein, “overlap” may mean complete overlap or partial overlap. An example of complete overlap is transferring the write data 156 over the I/O lines 202 and performing the read operation 232, both operations beginning at bus cycle D and ending at bus cycle G. An example of partial overlap is transfer of the portion of the write data 156 designated
15 “Data 1” during bus cycle E while the read operation 232 is ongoing. Although transfer of the “Data 1” portion begins and ends at different times than the read operation 232 begins and ends, both operations are ongoing during bus cycle E, and therefore the operations partially overlap. More than two operations may overlap. For example, during bus cycle F, the controller 120 writes a portion of the write data 156 onto the I/O
20 lines 202, the read operation 232 is (at least partially) performed at the memory 104, the memory die 103 reads the portion of the write data 156 (“Data 2”) from the I/O lines 202 and into the buffers 106, and the memory die 103 may transfer a portion of the read data 160 from the memory 104 to the buffers 106. As another example, during bus cycle J, the memory die 103 writes a portion of the read data 160 onto the I/O lines 202
25 from the buffers 106, the controller 120 reads a portion of the read data 160 from the I/O lines 202, and the write operation 234 is (at least partially) performed at the memory 104. By performing the read operation 232 while the write data 156 is being transferred to the memory die 103, and by performing the write operation 234 while the read data 160 is being transferred to the controller 120, the host device 130 may experience
30 reduced read latency as compared to systems without the read-write command 150.

Although the read operation 232 is illustrated as having an equal duration as transfer of the write data 156, in other implementations the read operation 232 may be completed

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in a shorter or longer amount of time as compared to an amount of time to transfer the write data 156. If the read operation 232 exceeds the transfer time of the write data 156, one or more bus cycles may elapse where no data is transferred via the I/O lines until the read data 160 is ready to begin transfer to the controller 120. Alternatively, or in
5 addition, transfer of the read data 160 via the I/O lines 202 may begin while the read operation 232 is ongoing. For example, the second buffer 109 of FIG. 1 may function as a first-in-first-out (FIFO) buffer that enables buffered read data to be written onto the communication bus 140 while other read data is being received from the memory 104.

Although the read-write command 150 is illustrated in FIG. 2 as including the command
10 identifier packet 204, the read address 152, and the write address 154, it should be understood that in other embodiment an instruction set definition of the read-write command 150 may define the write command 150 as including or excluding one or more of the components 204, 152, 154, 156, and 212. For example, the command identifier packet 204 may not be transmitted via the I/O lines 202 and instead an
15 indicator of the read-write command 150 may be sent via one or more other lines, such as via a dedicated command line. As another example, the read-write command 150 may be defined as including the command identifier packet 204, or as including the command identifier packet 204 and the command termination packet 212, and may not include one or more of the read address 152, the write address 154, and the write data
20 156 in the instruction set definition.

Although the read address 152 and the write address 154 are each illustrated as occupying a single bus cycle, in other embodiments, the read address 152, the write address 154, or both, may occupy multiple bus cycles or may be combined in a single bus cycle. For example, a 32-bit address may be transmitted in four bus cycles using an
25 8-bit bus, in a single bus cycle using a 32-bit bus, or may be combined with another 32-bit address in a single bus cycle using a 64-bit bus. Although the command termination packet 212 is illustrated as being transferred via the I/O lines 202, in other embodiments, a command termination signal may instead be transferred via one or more other lines or no command termination signal may be provided. For example, in an
30 implementation that uses a defined write data block size, the termination packet 212 may be omitted and transfer of the write data 156 may be determined to have ended when an amount of write data corresponding to the defined write data block size has

been transmitted (or a corresponding count of bus cycles have elapsed) over the communication bus 140.

Referring to FIG. 3, a flowchart of an illustrative embodiment of a method 300 of receiving requested data read from a memory within a data storage device at least partially concurrently with write data being stored into the memory is illustrated. The method 300 may be performed by the data storage device 102 of FIG. 1.

A read-write command and write data may be sent from a controller within a data storage device to a memory within the data storage device via a communication bus within the data storage device, at 302. The read-write command may indicate requested data to be read from the memory. For example, in response to receiving a read request for the requested data 160 from the host device 130 while a write operation is ongoing, the controller 120 may send the read-write command 150 and the write data 156 to the memory die 103 via the communication bus 140.

The requested data read from the memory may be received at the controller, where communicating the requested data over the communication bus overlaps the write data being stored into the memory, at 304. For example, the requested data 160 may be received by the controller 120 from the memory die 103 via the communication bus 140 at least partially concurrently with the write data 156 being sent from the buffers 106 to the non-volatile memory 104. At least a portion of the requested data 160 read from the memory 104 may be stored to the first buffer 107 while at least a portion of the write data 156 is concurrently stored to the second buffer 109. The requested data 160 read from the memory 104 may remain in the first buffer 107 until transmission of the write data 156 to the memory die 103 via the communication bus 140 is complete. Upon completion of data transfer of the write data 156 on the communication bus 140, the controller 120 may receive the requested data 160 from the first buffer 107. Receiving the requested data 160 overlaps the write data 156 being sent from the second buffer 109 to the memory 104.

By receiving the requested data 160 read from the memory 104 at the controller 120 at while the write data 156 is being written into the memory 104, reduced read latency may be experienced by the host device 130 as compared to systems without the read-write command 150.

Although various components depicted herein are illustrated as block components and described in general terms, such components may include one or more microprocessors, state machines, or other circuits configured to enable a data storage device, such as the data storage device 102 of FIG. 1, to perform the particular functions attributed to such components. For example, the read-write command logic 122 of FIG. 1, the circuitry 108, or a combination thereof, may represent physical components, such as controllers, processors, state machines, logic circuits, or other structures to receive requested data read from a memory die within the data storage device 102 of FIG. 1, where receiving the requested data overlaps write data being sent to the memory die 103 of FIG. 1.

10 In a particular embodiment, the data storage device 102 may be implemented in a portable device configured to be selectively coupled to one or more external devices. However, in other embodiments, the data storage device 102 may be embedded within one or more host devices, such as within a housing of a host communication device. For example, the data storage device 102 may be within a packaged apparatus such as a wireless telephone, a personal digital assistant (PDA), a gaming device or console, a portable navigation device, or other device that uses internal non-volatile memory. In a particular embodiment, the data storage device 102 may be coupled to a non-volatile memory, such as a three-dimensional (3D) memory, a flash memory (e.g., NAND, NOR, Multi-Level Cell (MLC), a Divided bit-line NOR (DINOR) memory, an AND memory, a high capacitive coupling ratio (HiCR), asymmetrical contactless transistor (ACT), or other flash memories), an erasable programmable read-only memory (EPROM), an electrically-erasable programmable read-only memory (EEPROM), a read-only memory (ROM), a one-time programmable memory (OTP), or any other type of memory.

25 The illustrations of the embodiments described herein are intended to provide a general understanding of the various embodiments. Other embodiments may be utilized and derived from the disclosure, such that structural and logical substitutions and changes may be made without departing from the scope of the disclosure. This disclosure is intended to cover any and all subsequent adaptations or variations of various
30 embodiments.

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The above-disclosed subject matter is to be considered illustrative, and not restrictive, and the appended claims are intended to cover all such modifications, enhancements, and other embodiments, which fall within the scope of the present disclosure. Thus, to the maximum extent allowed by law, the scope of the present invention is to be
5 determined by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing detailed description.

WHAT IS CLAIMED IS:

1. A method comprising:
in a data storage device that includes a memory, a controller, and a communication bus
coupled to the memory and to the controller, performing:
5 sending a read-write command and write data from the controller to the memory die via
the communication bus, wherein the read-write command indicates requested data to be
read from the memory die; and
receiving, at the controller, the requested data read from the memory, wherein
communicating the requested data over the communication bus overlaps the write data
10 being stored into the memory.
2. The method of claim 1, wherein reading the requested data read from the memory
overlaps the write data being received by the memory via the communication bus.
3. The method of claim 2, wherein a memory die includes the memory and a set of
buffers and wherein at least a portion of the requested data read from the memory is
15 stored to a first buffer of the set of buffers while at least a portion of the write data is
stored to a second buffer of the set of buffers.
4. The method of claim 1, wherein a data read operation is initiated at the memory
during data transfer of the write data via the communication bus.
5. The method of claim 1, wherein the read-write command includes a first address
20 corresponding to a read location in the memory and a second address corresponding to a
write location in the memory.
6. The method of claim 5, wherein the requested data is read from the read location and
the write data is sent to the write location.
7. The method of claim 1, wherein the memory includes a flash memory.
- 25 8. The method of claim 1, wherein the memory includes a three-dimensional (3D)
memory.

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9. A data storage device comprising:
a memory;
a controller coupled to the memory; and
a communication bus coupled to the memory and to the controller, wherein the
5 controller is configured to:
send a read-write command and write data to the memory via the communication bus,
wherein the read-write command indicates an address of requested data to be read from
the memory; and
receive the requested data read from the memory, wherein communicating the requested
10 data over the communication bus overlaps the write data being stored into the memory.
10. The data storage device of claim 9, wherein the controller includes read-write
command logic configured to generate the read-write command.
11. The data storage device of claim 9, further comprising a memory die that includes
the memory and circuitry to buffer the write data on the memory die while reading the
15 requested data.
12. The data storage device of claim 9, wherein the read-write command is sent in
response to receiving a read request from a host device during a write operation.
13. The data storage device of claim 9, wherein the memory includes a non-volatile
memory configured to store the requested data to be read from the memory.
- 20 14. The data storage device of claim 13, wherein reading the requested data from the
non-volatile memory overlaps the write data being received by the memory via the
communication bus.
15. The data storage device of claim 13, further comprising a set of buffers configured
to store the requested data that is read from the non-volatile memory and configured to
25 store the write data that is sent to the memory.

16. The data storage device of claim 15, wherein the set of buffers includes a first buffer and a second buffer, wherein the controller is further configured to store at least a portion of the requested data read from the non-volatile memory to the first buffer while at least a portion of the write data is stored to the second buffer.

5 17. The data storage device of claim 15, wherein the requested data remains in the set of buffers until transmission of the write data via the communication bus is complete.

18. The data storage device of claim 17, wherein, in response to determining that transmission of the write data is complete, the memory is configured to assert a read transfer signal to prevent the controller from sending a next sequential write command
10 until the requested data has been transferred to the controller.

19. The data storage device of claim 13, wherein the read-write command includes a first address corresponding to a read location in the non-volatile memory and a second address corresponding to a write location in the non-volatile memory.

20. The data storage device of claim 19, wherein the requested data is read from the
15 read location and the write data is stored to the write location.

21. The data storage device of claim 13, wherein the controller is further configured to initiate a data read operation at the non-volatile memory during data transfer of the write data via the communication bus.

22. The data storage device of claim 9, wherein the memory includes a three-
20 dimensional (3D) memory.

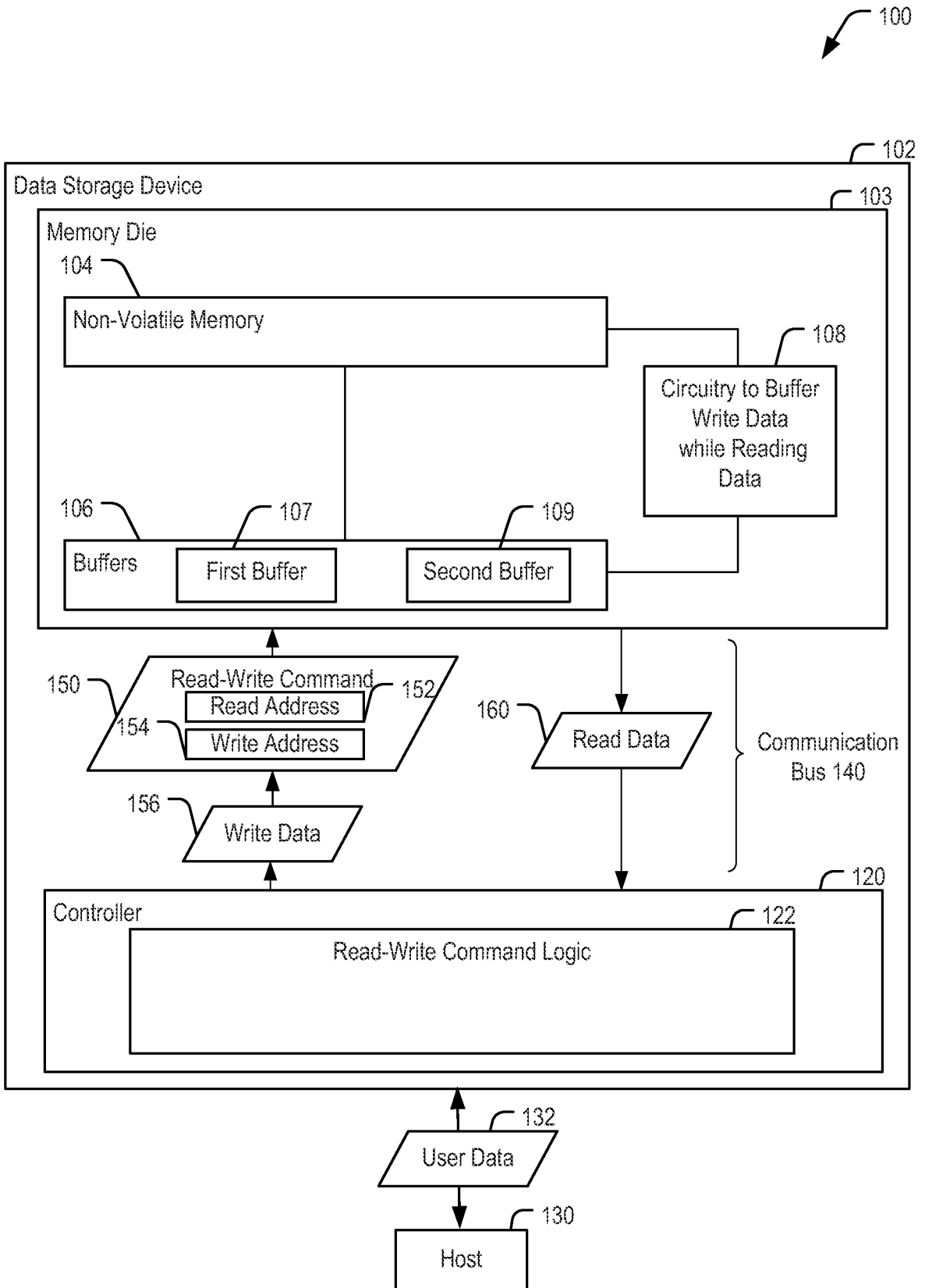


FIG. 1

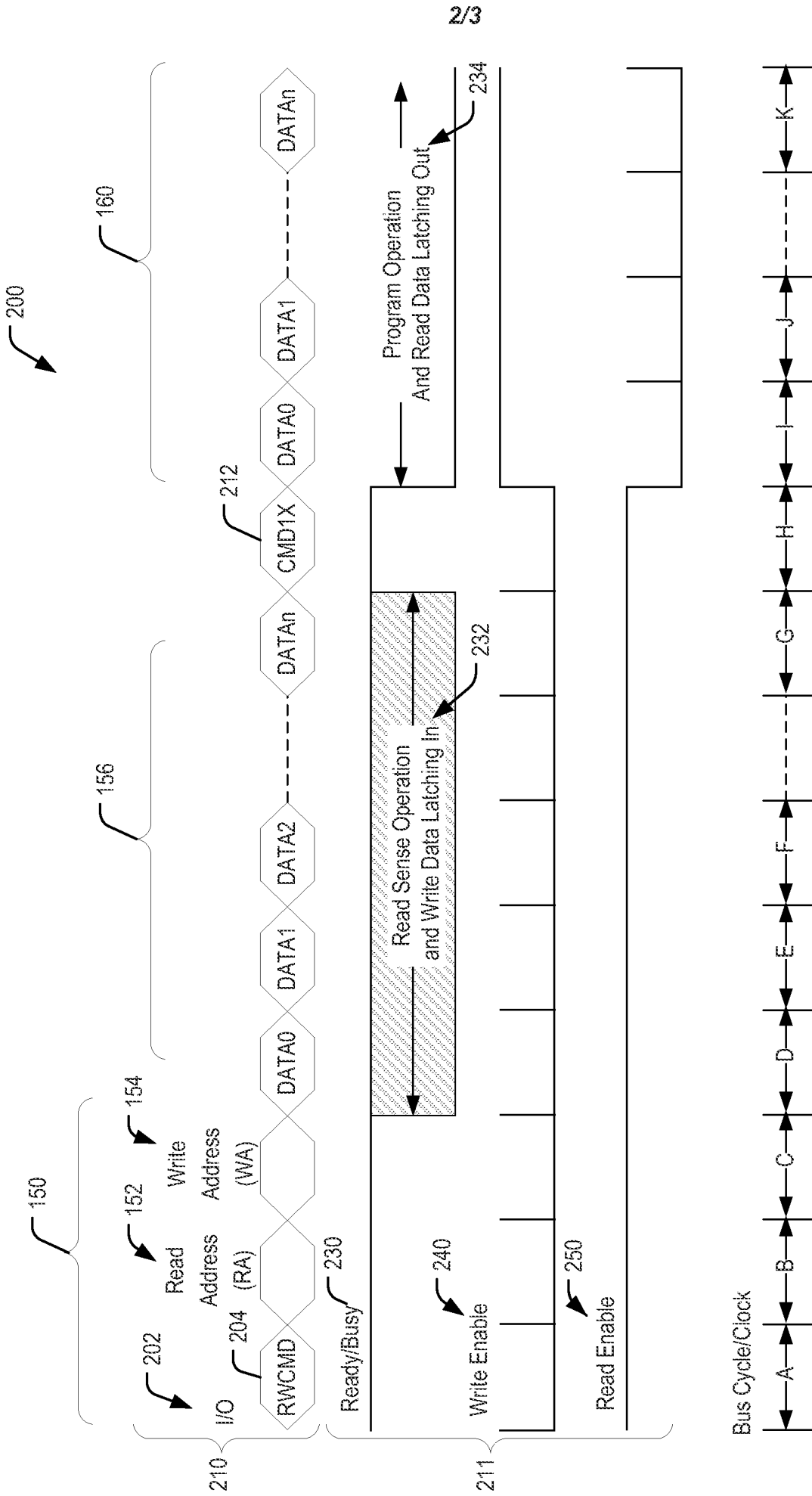
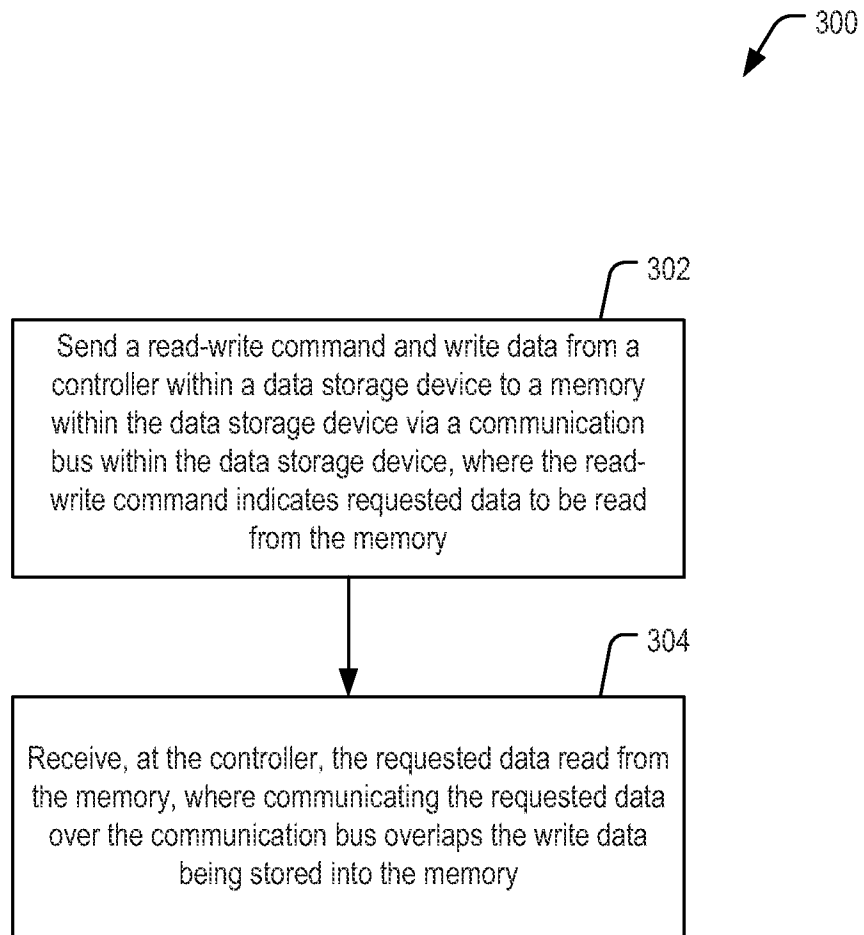


FIG. 2

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**FIG. 3**

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/021362

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C7/10
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/093669 A1 (DAVIS PAUL G [US] ET AL) 21 April 2011 (2011-04-21) figure 10 -----	1-22

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search
11 June 2014

Date of mailing of the international search report
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Name and mailing address of the ISA/
European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer
Ramcke, Ties

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2014/021362

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