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(54) **CIRCUIT AND METHOD FOR CONTACT PAD ISOLATION**

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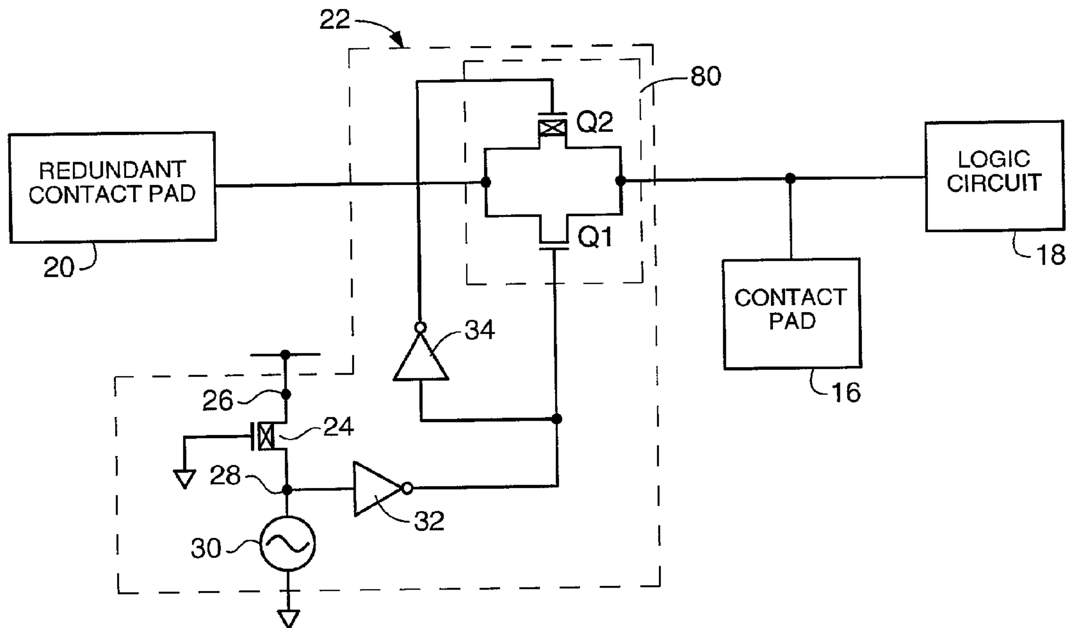
(52) **U.S. Cl.** **326/101**

(57) **ABSTRACT**

A circuit is provided to isolate a contact pad from a logic circuit of a die once the contact pad is no longer needed. This circuit can take many forms including a CMOS multiplexer controlled by a fuse or anti-fuse, an NMOS or PMOS pass gate controlled by a fuse or anti-fuse, or even a fusible link which is severed to effect isolation. Additionally, a circuit is provided that switchably isolates one of two contact pads from a logic circuit.



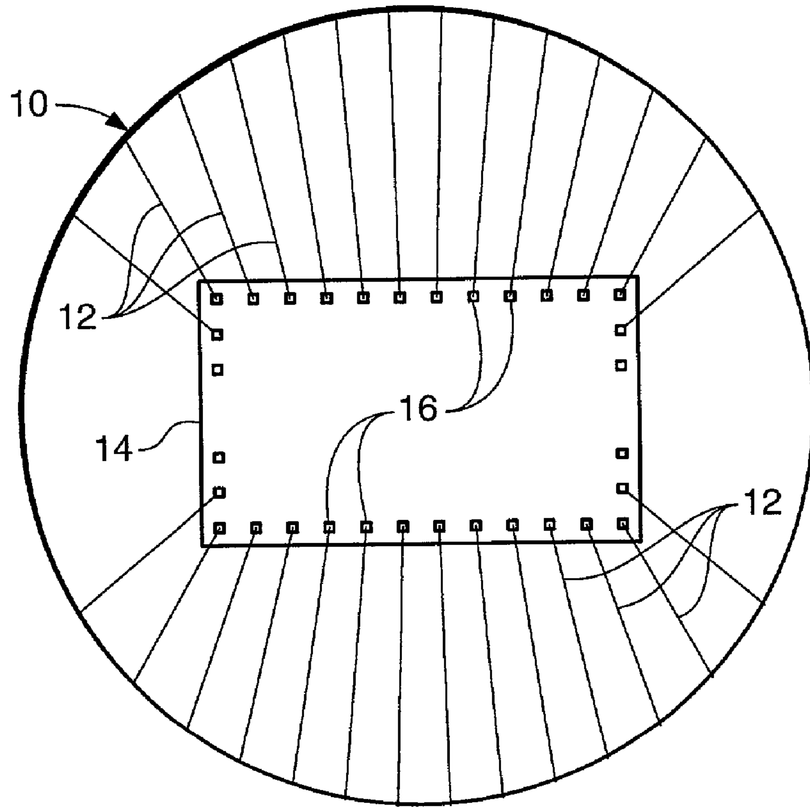


FIG. 1

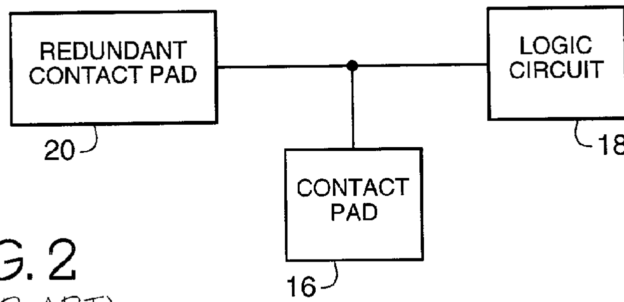


FIG. 2
(PRIOR ART)

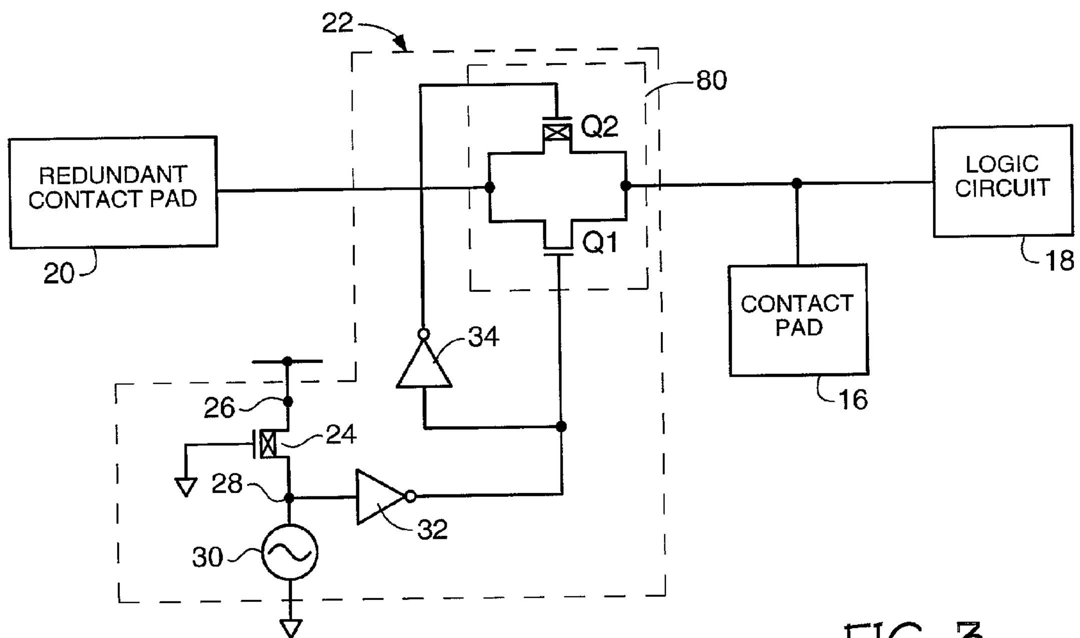


FIG. 3

FIG. 4

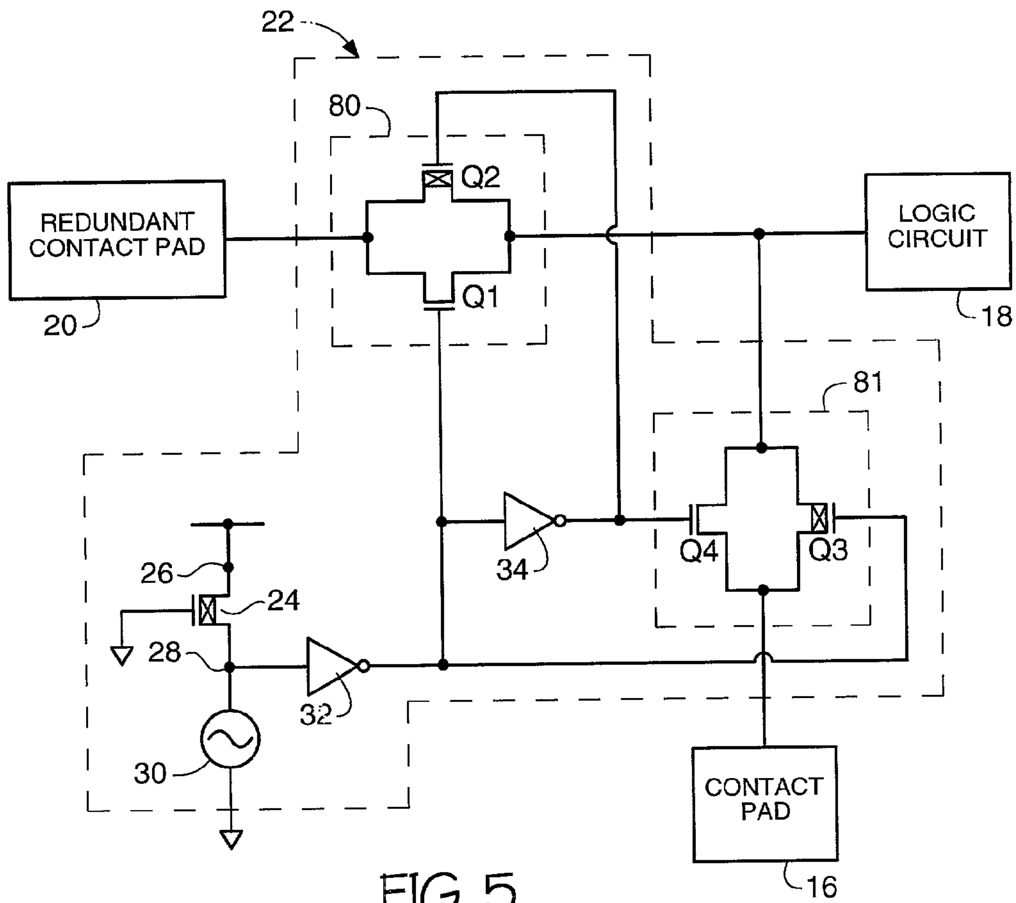


FIG. 5

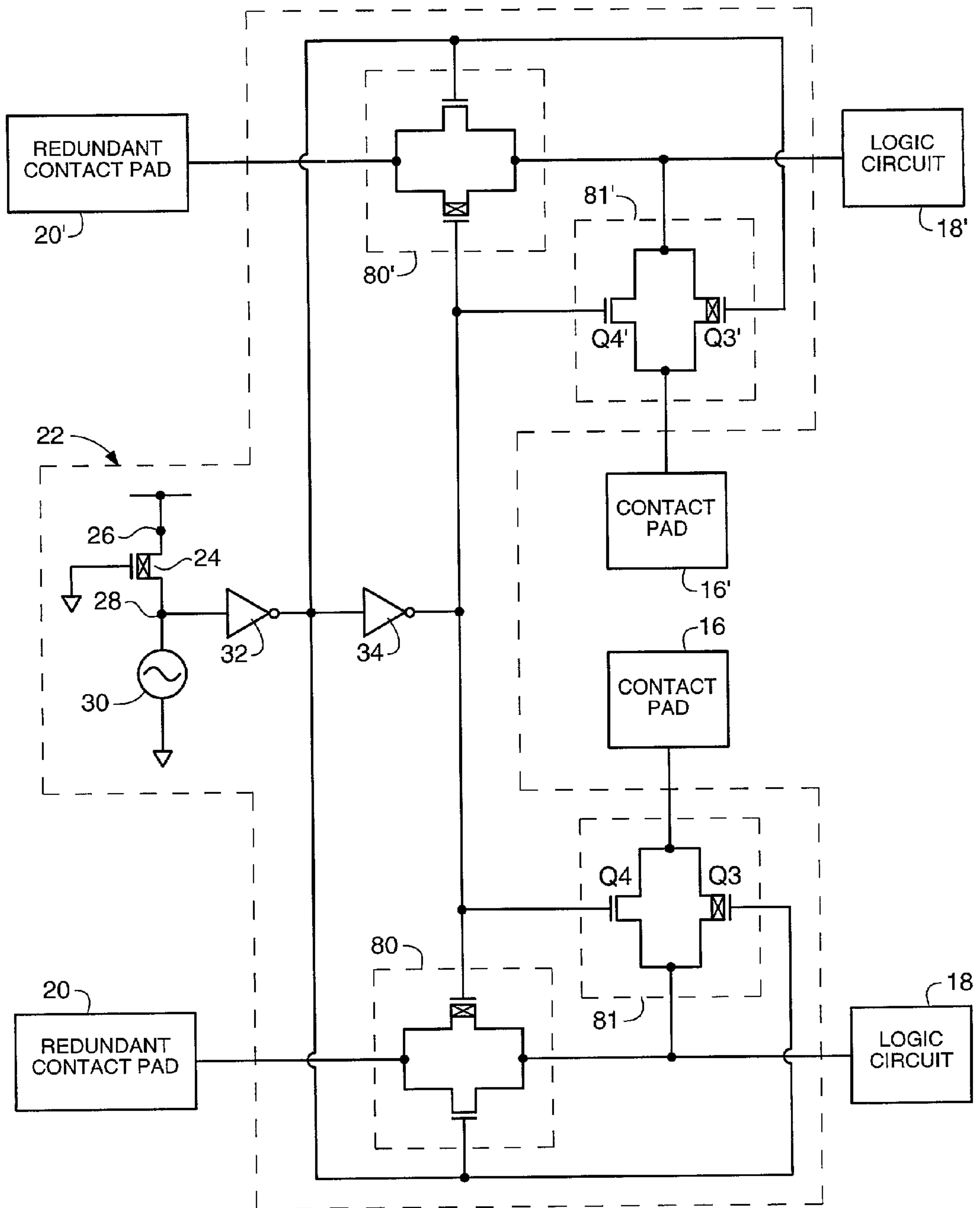


FIG. 6

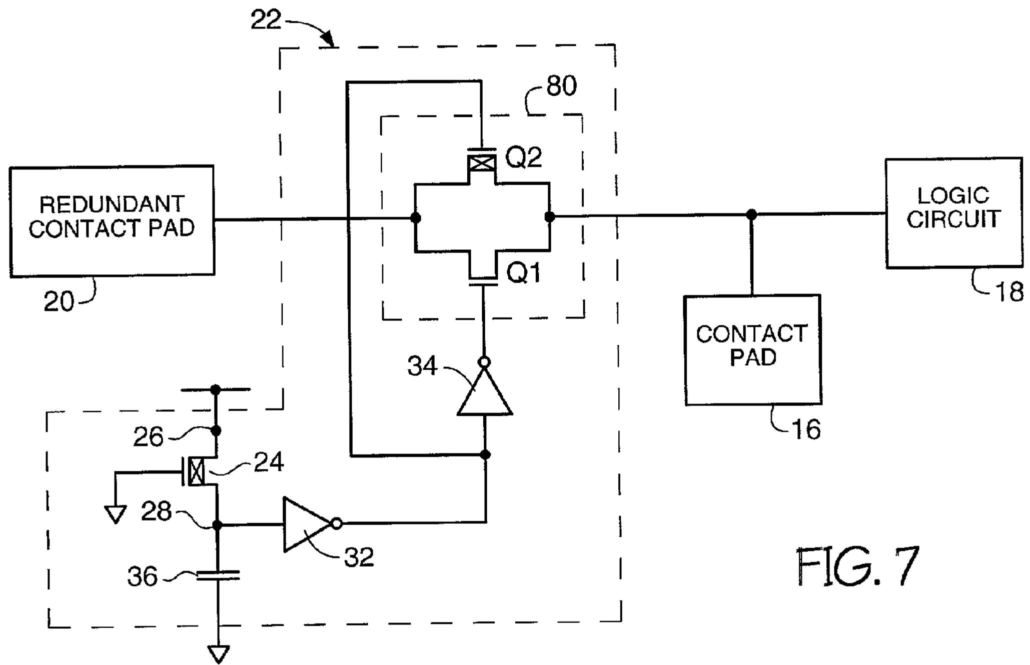


FIG. 7

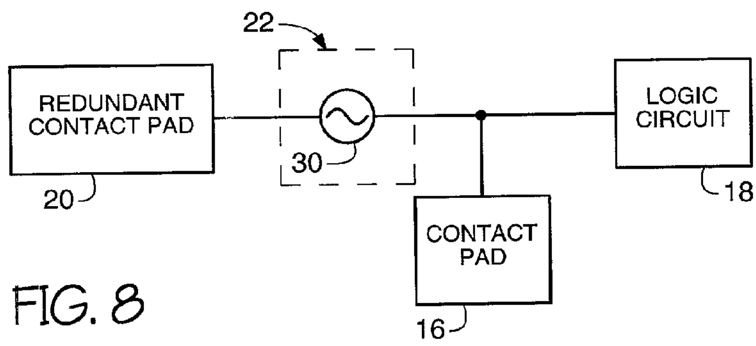


FIG. 8

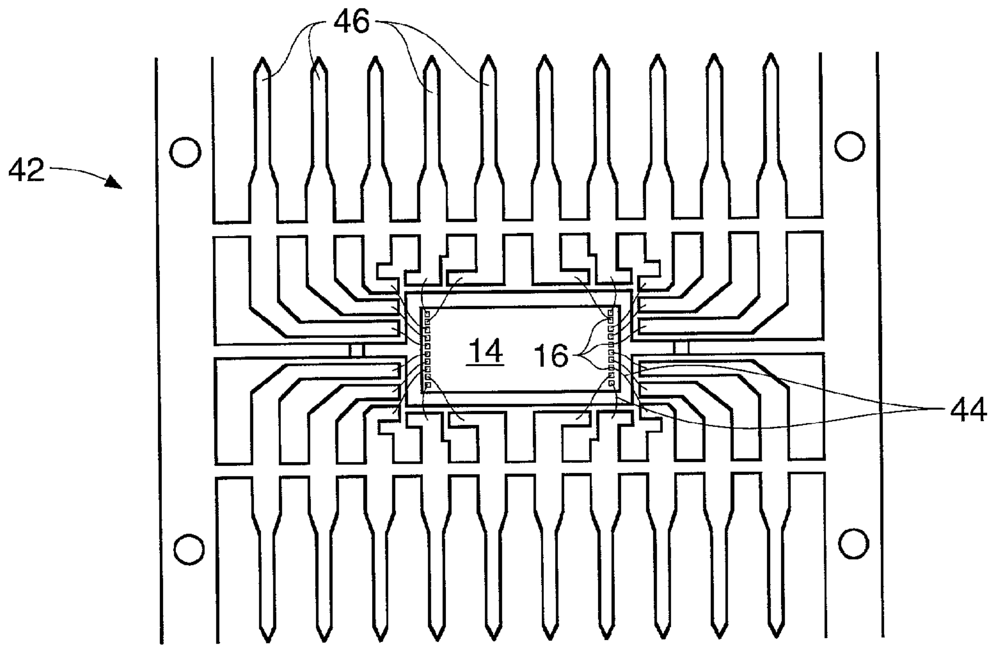


FIG. 9

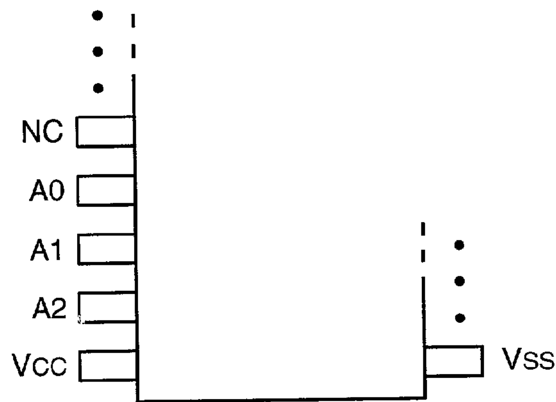


FIG. 10A

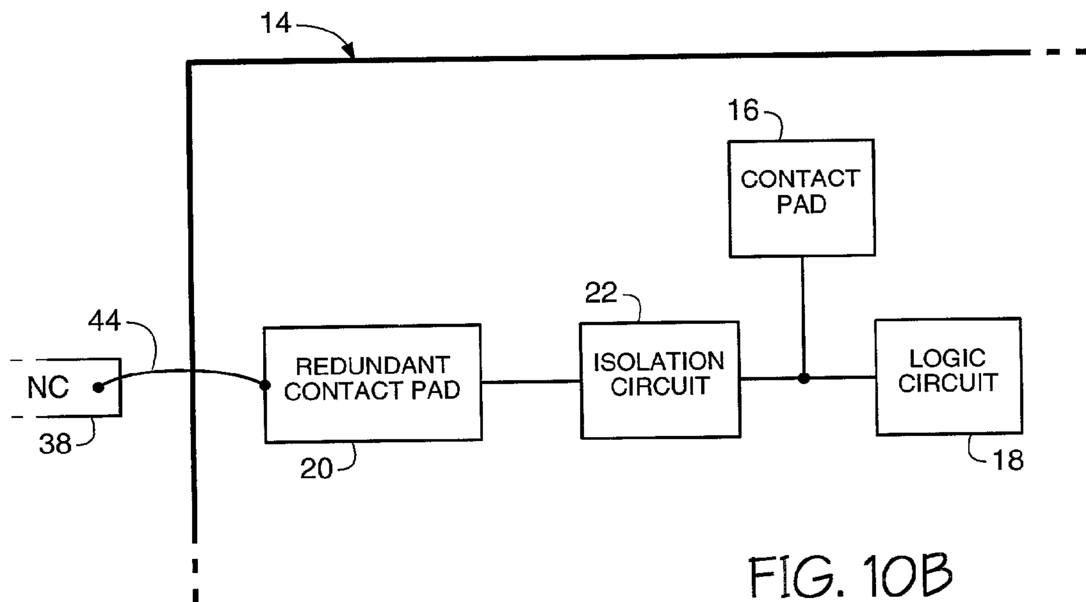


FIG. 10B

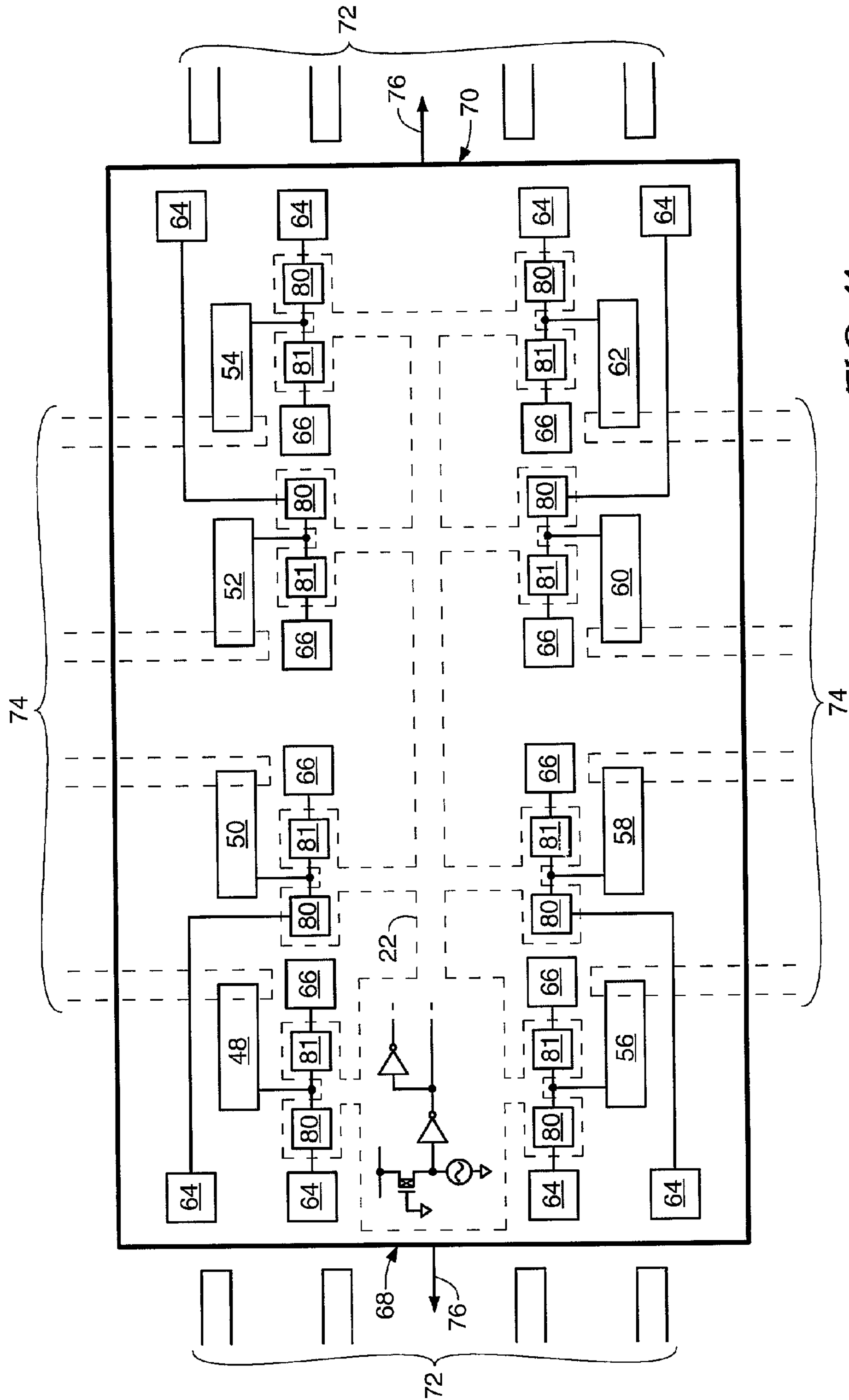


FIG. 11

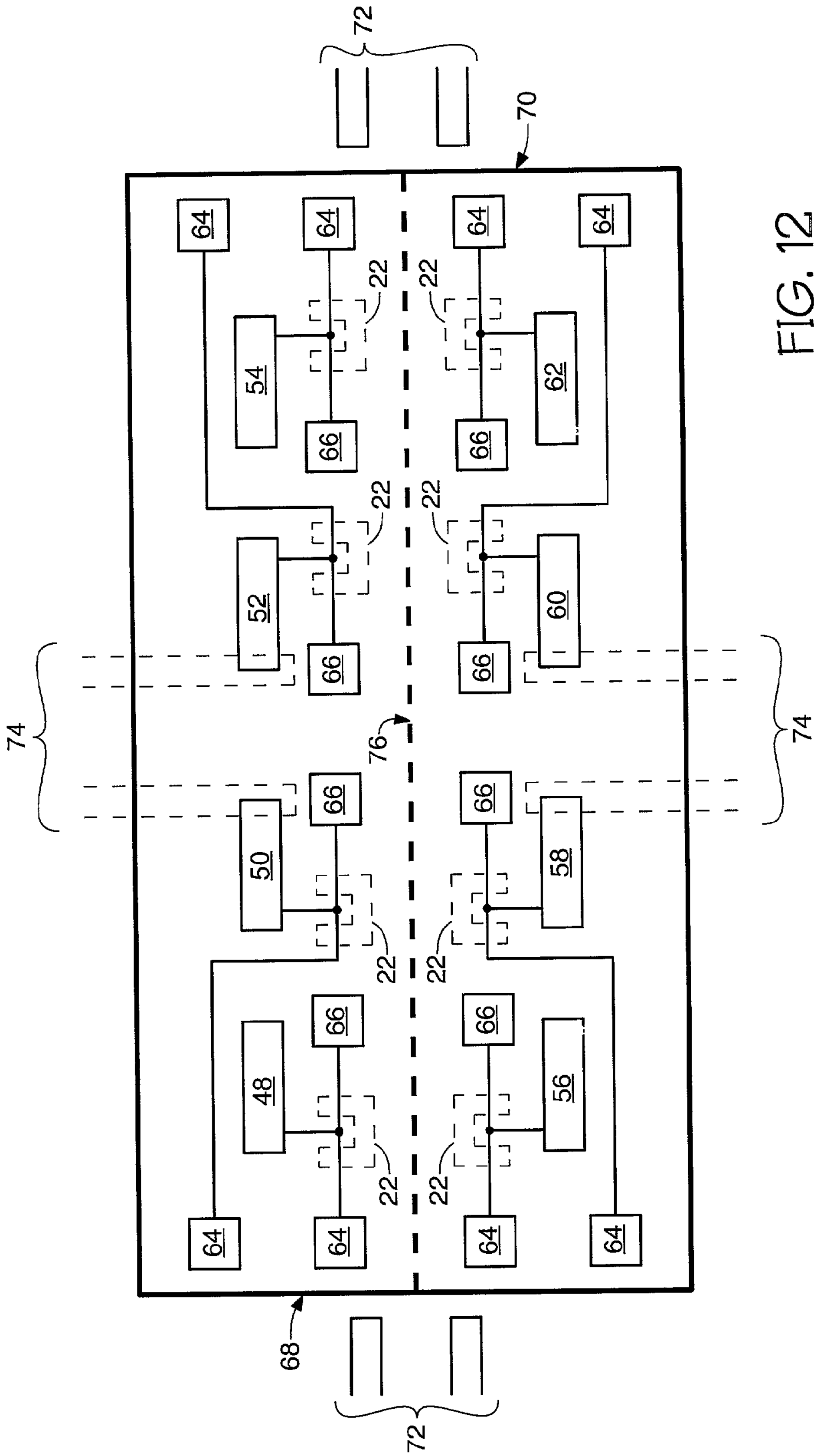


FIG. 12

CIRCUIT AND METHOD FOR CONTACT PAD ISOLATION

TECHNICAL FIELD

[0001] This invention relates generally to electronic devices and, more specifically, to a circuit and method for isolating a contact pad from a logic circuit.

BACKGROUND OF THE INVENTION

[0002] Processed semiconductor wafers typically comprise an array of substantially isolated integrated circuitry locations, which are subsequently separated to form semiconductor dies. In order to test the operability of the integrated circuitry of a die location on a wafer, a wafer probe card is applied to each die location. The wafer probe card includes a series of pins that are placed in physical contact with a die location's contact pads, which in turn connect to the die location's circuitry. The pins apply voltages to the input contact pads and measure the resulting output electrical signals from the output contact pads. However, the wafer probe card's pins may not be able to extend to all of the contact pads. As a result, it is necessary to provide accessible redundant contact pads on the die location and couple them to particular logic circuits.

[0003] An additional hardware limitation relevant to testing the die locations is the spacing between the pins of the wafer probe card. Specifically, the pins may be spaced further apart than the contact pads in a particular area of a die location. As a result, one contact pad in that area may not be serviceable by a pin. As a solution, prior art teaches providing a redundant contact pad in another area of the die location that can be reached by a pin. This redundant pad is connected to the same logic circuit as the unserviceable contact pad.

[0004] There may also be other reasons for including additional contact pads on a die. Regardless of the reasons, prior art allows these redundant contact pads to remain connected to the logic circuit after they are no longer needed. By remaining connected, these redundant contact pads contribute additional capacitance to their associated logic circuits and thereby degrade performance of the die.

SUMMARY OF THE INVENTION

[0005] Accordingly, the present invention provides a circuit for isolating a contact pad from a logic circuit. In a first exemplary embodiment, a complementary metal-oxide semiconductor (CMOS) multiplexer connects a redundant pad to a logic circuit, wherein the CMOS multiplexer is controlled by a fuse. Programming the fuse disables the multiplexer and prevents the redundant contact pad from affecting the logic circuit. Thus, this embodiment has the advantage of removing a parasitic component that might degrade performance of the logic circuit.

[0006] In a second exemplary embodiment, one fuse circuit controls several multiplexers, wherein each multiplexer services a separate logic circuit. This embodiment offers the advantage of reducing capacitance of several logic circuits while simultaneously conserving the die space needed to do so.

[0007] In a third exemplary embodiment, one fuse circuit controls two multiplexers, wherein both multiplexers service the same logic circuit. In addition to interposing a first multiplexer between the redundant contact pad and the logic circuit, a second multiplexer is interposed between a main contact pad and the logic circuit. Further, this second multiplexer is configured to operate conversely to the first multiplexer. Thus, before the fuse is programmed, only the redundant contact pad is in electrical communication with the logic circuit. After the fuse is programmed, only the main contact pad is in electrical communication with the logic circuit. The advantage offered by this embodiment is that, while one contact pad is being used, the other contact pad does not contribute additional capacitance.

[0008] A fourth exemplary embodiment combines the features described in the second and third exemplary embodiments. Thus, not only does one fuse control the electrical communication of several logic circuits, but the fuse also controls which contact pad can be used with each logic circuit. Accordingly, this embodiment combines the advantages found in the second and third embodiments. A fifth embodiment achieves the same advantages discussed above using an anti-fuse in place of the fuse. In addition, all of the embodiments listed above provide capacitance-reducing advantages while avoiding accidental programming of the fuse due to an ESD event.

[0009] Moreover, a sixth exemplary embodiment replaces the fuse controlled multiplexer with the fuse itself for linking the redundant contact pad with the logic circuit. In doing so, this embodiment offers all of the capacitance-reducing advantages of the embodiments discussed above and takes up less die space.

[0010] In a seventh exemplary embodiment, an isolation circuit is used during a test mode to connect a logic circuit to a no-connect pin on an integrated device, thereby providing the advantage of having an additional access point for testing the integrated device. Once the test mode has ended, the fusing element is programmed and the no-connect pin electrically disconnects from the logic circuit.

[0011] In an eighth exemplary embodiment, a die is provided having two groups of contact pads, wherein each group is configured to accommodate a different lead frame. One contact pad from each group is connected to a particular logic circuit. An isolation circuit similar to the fourth exemplary embodiment is provided to regulate electrical communication with the contact pads. Specifically, in an unprogrammed state, the isolation circuit electrically isolates the second group of contact pads from the logic circuits. The first group remains in electrical communication with the logic circuits and may accommodate an appropriate lead frame. If, on the other hand, a lead frame is chosen that is compatible with the second group of contact pads, then the entire first group **64** can be isolated in a single programming step that also serves to enable communication between the entire second group **66** and the logic circuits. This embodiment has the advantage of providing a die that is compatible with two different types of lead frames. In addition, the adaptation requires at most one programming step. As a further advantage, this embodiment restricts additional capacitance from unneeded contact pads once the appropriate lead frame has been determined.

[0012] A ninth exemplary embodiment is configured in a manner similar to the eighth embodiment. Rather than including one all-encompassing isolation circuit, however,

this embodiment includes several isolation circuits—one for each logic circuit. Each isolation circuit resembles the third exemplary embodiment in that the isolation circuit can be used to determine which contact pad communicates with the logic circuit - either the pad from the first group or the pad from the second group. By allowing a programming choice for each logic circuit, this embodiment provides a die that can adapt to other lead frames in addition to the two lead frames addressed in the eighth embodiment. Accordingly this embodiment also restricts additional capacitance from unneeded contact pads once the appropriate lead frame has been determined.

[0013] In addition to these circuit embodiments, the present invention encompasses various methods for achieving these advantages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] **FIG. 1** depicts a wafer probe card superimposed over a die.

[0015] **FIG. 2** demonstrates a circuit used in the prior art for testing a logic circuit on a die.

[0016] **FIG. 3** illustrates a first exemplary embodiment of the present invention.

[0017] **FIG. 4** illustrates a second exemplary embodiment of the present invention.

[0018] **FIG. 5** illustrates a third exemplary embodiment of the present invention.

[0019] **FIG. 6** illustrates a fourth exemplary embodiment of the present invention.

[0020] **FIG. 7** portrays a fifth exemplary embodiment of the present invention.

[0021] **FIG. 8** depicts a sixth exemplary embodiment of the present invention.

[0022] **FIG. 9** depicts a lead frame having a conductive lead configuration and accommodating a plurality of dies.

[0023] **FIG. 10*a*** is a partial pin-out diagram of a typical integrated device that exists in the prior art.

[0024] **FIG. 10*b*** demonstrates a seventh exemplary embodiment of the present invention.

[0025] **FIG. 11** displays an eighth exemplary embodiment of the present invention.

[0026] **FIG. 12** displays a ninth exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0027] **FIG. 1** illustrates the top view of a wafer probe card **10** having a series of pins **12** extending from two sides of the wafer probe card **10**. In order to test a particular die **14** on a wafer, this wafer probe card **10** is placed over the die **14**. The die **14** includes a plurality of contact pads **16**. For purposes of this application, a contact pad is defined to include any conductive surface configured to permit temporary or permanent electrical communication with a circuit or node. During testing, the pins **12** of the wafer probe card are in communication with nearby contact pads **16**. Given the configuration of the wafer probe card **10**, however, the pins **12** may not be able to reach contact pads **16** on certain areas of the die **14**.

[0028] **FIG. 2** demonstrates the solution in the prior art for this problem. If the contact pad **16** for a logic circuit **18** cannot be accessed by the wafer probe card **10**, then a redundant contact pad **20** is provided in a more accessible location and coupled to the logic circuit **18**. After testing, the original contact pad **16** is once again used to access the logic circuit **18**. The redundant contact pad **20**, however, also remains coupled to the logic circuit **18** and, as described above, may adversely affect the performance of the logic circuit in particular and the entire die in general.

[0029] **FIG. 3** illustrates one embodiment of the current invention that solves the problem remaining in the prior art solution. An isolation circuit **22** is electrically interposed between the redundant contact pad **20** and the logic circuit **18** in order to regulate electrical communication therebetween. The isolation circuit **22** in this embodiment comprises a p-channel long L device **24** having a source coupled to a potential node **26**. The potential node **26** is configured to accept a voltage source. The p-channel long L device **24** also has a drain coupled to a signal node **28**. The gate of the long L device **24** is bled to ground, thereby allowing signal node **28** to constantly receive a voltage signal from the potential node **26**.

[0030] The signal node **28** carries the voltage signal through a pathway leading to ground, but that pathway is interrupted by a fuse **30**. Moreover, the signal node **28** is coupled to a first inverter **32**. The output of the first inverter **32** connects to the gate of an n-channel transistor Q1, which is a component of a multiplexer **80** electrically interposed between the redundant contact pad **20** and the logic circuit **18**. In addition, the output of the first inverter **32** serves as the input for a second inverter **34**. This second inverter **34** connects to the gate of a p-channel transistor Q2, which is another component of the multiplexer **80**.

[0031] In operation, the potential node **26**, the p-channel long L device **24**, the signal node **28**, and the fuse **30** cooperate to determine the drive state of the multiplexer **80**. The fuse **30** is initially intact and provides grounding communication for the signal node **28**. Because the signal node **28** is grounded, a low voltage signal, or "logic 0," is generated and carried to the first inverter **32**. Accordingly, the first inverter outputs a high voltage signal, or "logic 1." The high signal drives the n-channel transistor Q1. The high signal also serves as input to the second inverter **34**, and the resulting low signal drives the p-channel transistor Q2. With transistors Q1 and Q2 on, a range of signals may be transmitted between the redundant contact pad **20** and the logic circuit **18**.

[0032] The redundant contact pad **20** can then be isolated by programming or "blowing" the fuse **30**. With fuse **30** blown, the signal node **28** no longer has a direct path to ground. As a result, a high signal is sent in a new direction—to the first inverter **32**. The resulting low signal turns off the n-channel transistor Q1. Further, the low signal is changed by the second inverter **34** to a high signal that turns off the p-channel transistor Q2. With both transistors Q1 and Q2 off, electrical communication between the redundant contact pad **20** and the logic circuit **18** is prevented.

[0033] Moreover, the potential node **26**/signal node **28**/fuse **30** configuration, hereinafter referred to as a "pro-

gram circuit," is not limited to driving only one multiplexer. As seen in **FIG. 4**, first inverter **32** and second inverter **34** can also be coupled to transistors Q1' and Q2' of a second multiplexer **80'**, wherein the second multiplexer **80'** is electrically interposed between another logic circuit **18'** and another redundant contact pad **20'**. As a result, this embodiment provides for the electrical isolation of two redundant contact pads by blowing only one fuse. Contact pads **16** and **16'** maintain electrical communication with their respective logic circuits **18** and **18'**. It follows that additional logic circuits could be similarly accommodated.

[**0034**] In yet another embodiment illustrated in **FIG. 5, a** multiplexer **81** is electrically interposed between contact pad **16** and the logic circuit **18**. As with multiplexer **80**, multiplexer **81** is comprises a p-channel transistor Q3 and an n-channel transistor Q4. However, whereas the first inverter **32** is coupled, to the n-channel transistor Q1 of multiplexer **80**, the first inverter **32** is instead coupled to the p-channel transistor Q3 of multiplexer **81**. Similarly, the second inverter **34** connects to the p-channel transistor Q2 in multiplexer **80** but drives the n-channel transistor Q4 in multiplexer **81**. By switching the driving signals in this fashion, the initial signals that serve to turn on multiplexer **80** also turn off multiplexer **81**. Conversely, blowing the fuse, which turns off multiplexer **80**, serves to turn on multiplexer **81**.

[**0035**] Further, the embodiments depicted in **FIGS. 4 and 5** could be combined so that blowing one fuse **30** switches the communication arrangement for two or more logic circuits. Thus, as demonstrated in **FIG. 6**, multiplexers **80'** and **81'** are driven by the program circuit to allow electrical communication between logic circuit **18'** and redundant contact pad **20'**, while at the same time electrically isolating contact pad **16'**. Meanwhile, the same program circuit allows for electrical communication between logic circuit **18** and redundant contact pad **20** and electrically isolates contact pad **16**. Blowing fuse **30** switches the electrical communication pathways for both logic circuits **18** and **18'**.

[**0036**] **FIG. 7** demonstrates another embodiment of the current invention. The isolation circuit **22** has a similar configuration to the one in **FIG. 3** except that (1) the fuse **30** has been replaced with an anti-fuse **36**; (2) the second inverter **34** now drives the n-channel transistor Q1; and (3) the first inverter **32** directly drives the p-channel transistor Q2. Given this configuration, the direct path from the signal node **28** to ground is initially barred by the anti-fuse **36**. Consequently, a high signal is transmitted to the first inverter **32**. The low signal output drives the p-channel transistor Q2. The second inverter **34** turns this low signal into a high signal in order to drive the n-channel transistor Q1. With both transistors Q1 and Q2 on, the redundant contact pad is fully coupled to the logic circuit. Once the anti-fuse is programmed, however, the signal node **28** becomes grounded and a low signal is transmitted to the first inverter **32**, which sends a high turnoff signal to the p-channel transistor Q2. Moreover, this high signal is altered by the second inverter **34** so that a low signal turns off the n-channel transistor Q1. With both transistors Q1 and Q2 off, the redundant contact pad **20** is no longer in electrical communication with logic circuit **18**.

[**0037**] It can be appreciated that an anti-fuse **36** could replace the fuse many of the embodiments of this invention. Accordingly the "program circuit" could include an anti-fuse.

[**0038**] An embodiment illustrated in **FIG. 8** demonstrates that the isolation circuit **22** can comprise the fuse **30** directly interposed between the redundant contact pad **20** and the logic circuit **18**, wherein programming the fuse isolates the redundant contact pad **20**. Programming can occur at the completion of testing or at a stage in any other application where isolation of a contact pad is beneficial. It should be noted that, while this embodiment conserves die space, embodiments such as those in **FIGS. 3 through 7** are better at preventing accidental programming due to an ESD event.

[**0039**] If wafer testing indicates a likelihood that the wafer has a yield of good quality dies, the dies are separated from the wafer and undergo a packaging process. Many such processes involve attaching a die **14** to a lead frame **42**, such as one shown in **FIG. 9**, and using bond wires **44** to connect the contact pads **16** to the conductive leads **46** of the lead frame **42**. The die/lead frame assembly may then be encased, with the outer ends of the conductive leads **46** remaining exposed to allow communication with external devices. However, some conductive leads may not be connected to the contact pads of a die. Such a conductive lead is designated as a "no-connect" or "NC" pin, as demonstrated in the pin-out diagram of **FIG. 10***a*.

[**0040**] After assembly, a packaged device may then be subjected to further testing. **FIG. 10***b* depicts an embodiment of the current invention that makes use of the no-connect pin **38** of the packaged die **14** for such testing. Prior to assembly, the die **14** is configured to include a redundant contact pad **20** coupled to a logic circuit **18** through an isolation circuit **22**. Further, the no-connect pin **38** is connected to the redundant contact pad **20** by a bond wire **44**. As a result, communication with the logic circuit **18** may be accomplished during testing of the device through the no-connect pin **38**. Once testing is complete, the isolation circuit **22**, which may comprise one of the configurations described above, is programmed, thereby halting communication between the no-connect pin and the logic circuit.

[**0041**] Moreover, other embodiments of the current invention allow for isolating an additional contact pad that is not necessarily a test-mode pad. As shown in **FIG. 11**, isolation circuits can be used to allow a die to adapt to more than one lead frame configuration. **FIG. 11** shows eight logic circuits **48, 50, 52, 54, 56, 58, 60**, and **62** coupled to a first group of contact pads **64** located on opposing sides **68, 70** of a die **14**. These eight logic circuits are also coupled to a second group of contact pads **66** extending along a center axis **76** of the die **14** between the between the opposing sides **68, 70**. An isolation circuit **22** is also provided. In this embodiment, the isolation circuit **22** resembles the one depicted in **FIG. 6**, where the isolation circuit **22** not only services more than one logic circuit but also enables exclusive electrical communication within a logic circuit to be switched between two contact pads.

[**0042**] **FIG. 11** further demonstrates that the first group of contact pads **64** is configured to accommodate a lead frame having conductive leads **72** that address the opposing sides **68** and **70** of the die **14**. The second group of contact pads **66** will favorably receive a lead frame having conductive

leads **74** addressing internal portions of the die, such as s those near the center axis **76**. Thus, depending on the lead frame ultimately chosen, the current invention allows for particular contact pads to be isolated accordingly. As in **FIG. 6**, the isolation circuit in **FIG. 11** is assumed to be configured to turn on the transistors in multiplexers **80** when the fuse is intact. It should also be noted that multiplexers **80** are interposed between the first group of contact pads **64** and their respective logic circuit. Further, multiplexers **81** are interposed between the second group of contact pads **66** and their respective logic circuit. Thus, if the fuse **30** is not blown, then electrical communication with the logic circuits **48, 50, 52, 54, 56, 58, 60,** and **62** is achieved solely through the first group of contact pads **64**. Should it be determined to package the die **14** with a lead frame having conductive leads **72**, the fuse remains unprogrammed, the conductive leads **72** are wire bonded to that group, and the second group of contact pads **66** remain isolated. If, however, a lead frame including conductive leads **74** is to be packaged with the die **14**, then by programming a single fuse **30**, the second group of contact pads will be in electrical communication with the logic circuits **48, 50, 52, 54, 56, 58, 60,** and **62**. Moreover, the first group of contact pads **64**, having been isolated due to blowing the fuse, will not contribute additional capacitance to the circuit operations.

[**0043**] The embodiment illustrated in **FIG. 12** can accommodate still other lead frames, wherein only some of the contact pads of a group need to be isolated. While the logic circuit/contact pad layout in **FIG. 12** is similar to the configuration in **FIG. 11**, the isolation circuitry is preferably more like the arrangement in **FIG. 5**. Furthermore, It would be beneficial in this embodiment to use a plurality of isolation circuits **22** in order to provide one fuse **30** for every contact pad pair associated with a logic circuit. Given this configuration, each fuse **30** can be programmed as needed to accommodate the lead frame. For example, the lead frame in **FIG. 12** has some conductive leads **74** addressing internal portions of the die near the center axis **76**, and the lead frame has other conductive leads **72** that address opposing sides **68** and **70** of the die **14**. Therefore, only some of the contact pads in the first group **64** should be isolated, as should some of the contact pads in the second group **66**. The embodiment in **FIG. 12** allows this selectivity.

[**0044**] It would be a further benefit to associate a particular group of contact pads with multiplexers having the same initial state. For example, assuming that each contact pad in the first group **64** is respectively coupled to the multiplexer **80** of each isolation circuit **22**, it follows that the entire first group **64** is initially in electrical communication with the logic circuits **48, 50, 52, 54, 56, 58, 60,** and **62**. It also follows that the entire second group **66** is associated with the multiplexers **81** of the isolation circuits **22** and are therefore isolated. In order to accommodate the conductive leads **72, 74** illustrated in **FIG. 12**, it is relatively easy, given contact pad/isolation circuit association, to determine that only the fuses **30** corresponding to logic circuits **50, 52, 58,** and **60** need to be blown.

[**0045**] In addition, one can appreciate that other lead frame adapter embodiments could use isolation circuits similar to those depicted in **FIGS. 3, 7,** and **8**.

[**0046**] Finally, one of ordinary skill can appreciate that, although specific embodiments of this invention has been described for purposes of illustration, various modifications can be made without departing from the spirit and scope of the invention. For example, concerning the embodiments discussed above that use a fuse, such a fuse could comprise one of various types of fuses, including a link fuse or a laser fuse. Alternatively, the fuse could be replaced by an anti-fuse with minor configuration changes. Moreover, embodiments such as those in **FIG. 3** through **7** using both a p-channel and an n-channel transistor as a link could be modified to use only one of the transistors. Accordingly, the invention is not limited except as stated in the claims.

What is claimed is:

1. An isolation circuit for a contact pad coupled to a logic circuit, comprising:

a multiplexer electrically interposed between said contact pad and said logic circuit, wherein said multiplexer is configured to prevent electrical communication between said contact pad and said logic circuit in response to a cut-off signal; and

a drive circuit coupled to said multiplexer and configured to connect to a voltage source and to ground, wherein said drive circuit has a program mode and a non-program mode and is configured to transmit said cut-off signal during said program mode.

2. The isolation circuit in claim 1, wherein said drive circuit further comprises:

a source node;

a signal node coupled to said source node and to said multiplexer;

a fuse coupled to said signal node and having a program function, wherein an initiation of said program function represents a shift into said program mode; and

a ground node coupled to said fuse.

3. The isolation circuit in claim 2 wherein said fuse is selected from a group comprising a laser fuse, a light programmable fuse, and an electrically programmable fuse.

4. A communication device for a logic circuit, comprising:

a logic circuit access terminal;

a connection circuit electrically interposed between said logic circuit and said logic circuit access terminal, wherein said connection circuit is configured to couple said logic circuit to said logic circuit access terminal in response to a coupling signal; and

a signal generation circuit coupled to said connection circuit and configured to receive a voltage source and a grounding pathway, wherein said signal generation circuit has a non-isolation mode and an isolation mode and said signal generation circuit is configured to transmit said coupling signal during said non-isolation mode.

5. The device in claim 4, wherein said signal generation circuit further comprises:

a source node;

a signal node coupled to said source node and to said connection circuit;

an anti-fuse coupled to said signal node; and

a ground node coupled to said anti-fuse, wherein a transmission of said coupling signal through said anti-fuse to said ground node represents a shift into said isolation mode.

6. An isolation circuit for a pathway having a first terminal and a second terminal, comprising:

a first potential node configured to accept a voltage source;

a long L p-channel transistor comprising:

a source coupled to said first potential node, and

a drain;

a signal node coupled to:

said drain of said long L p-channel transistor,

a first conduit, and

a second conduit,

wherein said signal node is configured to receive a signal from said first potential node, and further configured to selectively establish a signal path to said first conduit and to said second conduit;

a signal direction device coupled to said first conduit and having a first mode and a second mode, wherein said signal direction device is configured to maintain said signal path during said first mode, and further configured to change said signal path during said second mode;

a second potential node coupled to said signal direction device and configured to couple to ground;

a connector circuit coupled to said second conduit; and

a multiplexer coupled to said connector circuit and further coupled to said pathway and electrically interposed between said first terminal and said second terminal.

7. The isolation circuit in claim 6, wherein:

said signal node is configured to send said signal through one of said first and second conduits and send a complementary signal through another of said first and second conduits;

said signal direction device is configured to achieve a switch of said signal and said complementary signal with respect to said first and second conduits; and

said multiplexer is configured to electrically separate said first terminal from said second terminal in response to said switch.

8. The isolation circuit in claim 7, wherein said connector circuit comprises:

a first inverter having an input coupled to said signal node and an output coupled to said multiplexer; and

a second inverter having an input coupled to said output of said first inverter, wherein said second inverter also has an output coupled to said multiplexer.

9. The isolation circuit in claim 8, wherein said multiplexer comprises:

a p-channel transistor coupled to said pathway and electrically interposed between said first terminal and said second terminal, wherein said p-channel transistor has a PMOS gate; and

an n-channel transistor coupled to said pathway and to said p-channel transistor, wherein said n-channel transistor is further electrically interposed between said first terminal and said second terminal and has an NMOS gate.

10. The isolation circuit in claim 9, wherein:

said signal direction device is a fuse;

said output of said first inverter is coupled to said NMOS gate; and

said output of said second inverter is coupled to said PMOS gate.

11. The isolation circuit in claim 9, wherein:

said signal direction device is an anti-fuse;

said output of said first inverter is coupled to said PMOS gate; and

said output of said second inverter is coupled to said NMOS gate.

12. A signal regulation device coupled between a first conductive path and a second conductive path, comprising:

a signal reception device configured to carry a first signal having a first voltage and a second signal having a second voltage;

a signal control device coupled to said signal reception device and having an initial mode and an isolation mode, wherein:

said signal control device is configured to accept said first signal and divert said second signal during said initial mode, and

said signal control device is further configured to accept said second signal and divert said first signal during said isolation mode; and

a signal transmission device coupled to said first conductive path, said second conductive path, and to said signal control device, wherein:

said communication device is configured to receive a diverted signal selectively comprising said first signal and said second signal, and

said communication device is configured to allow electrical communication between said first conductive path and said second conductive path in response to receiving said first signal, and said communication device is further configured to prevent said electrical communication in response to receiving said second signal.

13. The signal regulation device in claim 12, wherein said first voltage is higher than said second voltage.

14. The signal regulation device in claim 12, wherein said second voltage is higher than said first voltage.

15. A test mode completion device for a circuit coupled to a redundant contact pad through a test conduit, comprising:

an isolation element, wherein:

said isolation element is incorporated within said test conduit; and

said isolation element is configured to electrically sever said test conduit before said circuit enters a non-test mode.

16. The test made completion device in claim 15, wherein said isolation element is configured to physically sever said test conduit before said logic circuit enters a non-test mode.

17. The test mode completion device in claim 16, wherein said isolation element comprises a fuse.

18. A test device for an integrated device having a no-connect pin and a die, wherein said die has a logic circuit as well as a test contact pad coupled to said no-connect pin, comprising:

an isolation circuit coupled to said test contact pad and to said logic circuit, wherein said isolation circuit is configured to establish electrical communication between said test contact pad and to said logic circuit in a primary mode and prevent electrical communication between said test contact pad and to said logic circuit in a secondary mode.

19. The test device in claim 18, wherein said isolation circuit is configured to transition from said primary mode to said secondary mode in general correspondence with a transition from a test mode of said integrated device to a non-test mode of said integrated device.

20. A die having logic circuitry and selectively connected to a first group of conductive leads and a second group of conductive leads, comprising:

a first group of contact pads located in a first area on said die, wherein said first area is accessible by said first group of conductive leads;

a second group of contact pads located in a second area on said die, wherein said second area is accessible by said second group of conductive leads; and

an isolation device coupled to said first group of contact pads and to said logic circuitry, wherein said isolation device is configured to regulate electrical communication between said first group of contact pads and said logic circuitry.

21. The die in claim 20, wherein said isolation device is further configured to selectively permanently prevent electrical communication between said first group of contact pads and said logic circuitry.

22. The die in claim 21, wherein:

a prevention of electrical communication between said first group of contact pads and said logic circuitry generally corresponds to an alignment of said second group of contact pads and said second group of conductive leads.

23. The die in claim 22, wherein:

said first group conductive leads are part of a first lead frame; and

said second group of conductive leads are part of a second lead frame.

24. The die in claim 22, wherein said first group conductive leads and said second group of conductive leads are part of a common lead frame.

25. The die in claim 24, wherein a number of contact pads of said first group of contact pads is greater than a number of conductive leads of said first group of conductive leads.

26. The die in claim 25, wherein a number of contact pads of said second group of contact pads is greater than a number of conductive leads of said second group of conductive leads.

27. An adapter for a die having a first and a second contact pad coupled to a logic circuit of said die, wherein said first contact pad is configured to align with a first lead frame and said second contact pad is configured to align with a second lead frame, and wherein said adapter comprises:

a first communication isolator, wherein:

said first communication isolator is electrically inserted between said first contact pad and said logic circuit; and

said first communication isolator is configured to activate generally coincidentally with an alignment between said second contact pad and said second lead frame.

28. The adapter in claim 27, further comprising a second communication isolator, wherein said second communication isolator is electrically inserted between said second contact pad and said logic circuit; and said second communication isolator is configured to activate generally coincidentally with an alignment between said first contact pad and said first lead frame.

29. An isolation circuit for a semiconductor device having a first logic circuit and a second logic circuit, wherein said first logic circuit is coupled to a first contact pad and to a second contact pad, and said second logic circuit is coupled to a third contact pad and to a fourth contact pad, and wherein said isolation circuit comprises:

a program circuit;

a first multiplexer coupled to said program circuit and configured to be selectively driven by said program circuit and further configured to regulate electrical communication to and from one of said first and second logic circuits; and

a second multiplexer coupled to said program circuit and configured to be selectively driven by said program circuit and further configured to regulate electrical communication to and from one of said first and second logic circuits.

30. The isolation circuit in claim 29, wherein said first and second multiplexers are configured to operate concurrently.

31. The isolation circuit in claim 30, wherein said first multiplexer is electrically interposed between said first logic circuit and said first contact pad, and wherein said second multiplexer is electrically interposed between said second logic circuit and said primary contact pad.

32. The isolation circuit in claim 29, wherein said first and second multiplexers are configured to operate selectively.

33. The isolation circuit in claim 32, wherein said first multiplexer is electrically interposed between said first logic circuit and said first contact pad, and wherein said second multiplexer is electrically interposed between said first logic circuit and said second contact pad.

34. A circuit for a plurality of logic circuits respectively coupled to a plurality of contact pads, comprising:

a program circuit configured to have an initial operating characteristic and further configured to optionally permanently transition to a final operating characteristic in response to a reception by said program circuit of a program signal; and

a plurality of multiplexers coupled to said program circuit and respectively electrically interposed between said plurality of logic circuits and said plurality of contact pads, and further configured to deactivate in response to a transition to said final operating characteristic of said program circuit.

35. A selective electrical communication circuit for a logic circuit coupled to a first contact pad and a second contact pad, comprising:

a first multiplexer electrically interposed between said first contact pad and said logic circuit;

a second multiplexer electrically interposed between said second contact pad and said logic circuit and conversely operable in relation to said first multiplexer; and

a program circuit coupled to said first multiplexer and said second multiplexer and configured to drive said first multiplexer and said second multiplexer.

36. The selective electrical communication circuit in claim 35, wherein:

said first multiplexer further comprises:

a first p-channel electrically interposed between said first contact pad and said logic circuit, and

a first n-channel transistor coupled to said first p-channel transistor and electrically interposed between said first contact pad and said logic circuit;

said second multiplexer further comprises:

a second p-channel transistor electrically interposed between said second contact pad and said logic circuit, and

a second n-channel transistor coupled to said second p-channel transistor and electrically interposed between said second contact pad and said logic circuit;

said selective electrical communication circuit further comprises:

a first inverter coupled to said program circuit, to said first n-channel transistor, and to said second p-channel transistor, and

a second inverter coupled to said first inverter, to said first p-channel transistor, and to said second n-channel transistor, and

said program circuit is configured to transmit a first driving signal and further configured to transmit a complementary driving signal in response to a one-time programming event.

37. The selective electrical communication circuit in claim 35, wherein:

said first multiplexer has:

a first communication mode, and

a first non-communication mode;

said second multiplexer has:

a second communication mode concurrent with said first non-communication mode, and

a second non-communication mode concurrent with said first communication mode; and

said program circuit has:

a first operations mode generally concurrent with said first communication mode, and

a second operations mode generally concurrent with said first non-communication mode.

38. A communication regulator circuit for a plurality of logic circuits, comprising:

a first group of multiplexers respectively coupled to said plurality of logic circuits and further configured to allow electrical communication to and from said plurality of logic circuits in response to a reception of a driving signal;

a second group of multiplexers respectively coupled to said plurality of logic circuits and further configured to allow electrical communication to and from said plurality of logic circuits in response to a reception of said driving signal; and

at least one driving circuit coupled to said first group and said second group of multiplexers and configured to initially transmit said driving signal exclusively to said first group of multiplexers and further configured to optionally permanently transmit said driving signal exclusively to said second group of multiplexers.

39. The communication regulator circuit of claim 38 comprising only one driving circuit.

40. The communication regulator circuit of claim 38 comprising a plurality of driving circuits, wherein each driving circuit of said plurality of driving circuits is respectively coupled to a multiplexer in said first group and to a multiplexer in said second group.

41. A testing circuit for a first logic circuit and a second logic circuit, wherein said first logic circuit is coupled to a first main contact pad and a first redundant contact pad, and wherein said second logic circuit is coupled to a second main contact pad and a second redundant contact pad, comprising:

a program circuit configured to transmit a test mode signal before a program event and further configured to transmit a non-test mode signal after said program event;

a first test mode multiplexer coupled to said program circuit, said first logic circuit, and to said first redundant contact pad; and further configured to support electrical communication between said first logic circuit and said first redundant contact pad during a transmission of said test mode signal;

a first non-test mode multiplexer coupled to said program circuit, said first logic circuit, and to said first main contact pad; and further configured to support electrical

communication between said first logic circuit and said first main contact pad during a transmission of said non-test mode signal;

a second test mode multiplexer coupled to said program circuit, said second logic circuit, and to said second redundant contact pad; and further configured to support electrical communication between said second logic circuit and said second redundant contact during said transmission of said test mode signal; and

a second non-test mode multiplexer coupled to said program circuit, said second logic circuit, and to said second main contact pad; and further configured to support electrical communication between said second logic circuit and said second main contact pad during said transmission of said non-test mode signal.

42. A method of regulating transmissions between a contact pad and a logic circuit, comprising:

interposing an isolation circuit between said contact pad and said logic circuit;

initially diverting an activation signal from said isolation circuit; and

ultimately directing said activation signal toward said isolation circuit.

43. The method in claim 42, wherein:

initially diverting said activation signal further comprises providing a generally direct path to ground for said activation signal; and

subsequently directing said activation signal further comprises impeding said generally direct path to ground.

44. A method of altering electrical communication between a contact pad and a logic circuit, comprising:

providing an electrical communication circuit between said contact pad and said logic circuit;

initially directing an activation signal to said electrical communication circuit; and

subsequently diverting said activation signal from said electrical communication circuit.

45. The method in claim 44, wherein:

initially directing said activation signal further comprises obstructing a generally direct path to ground for said activation signal; and

subsequently diverting said activation signal further comprises overcoming an obstruction to said generally direct path to ground.

46. A method of testing a logic circuit connected to a first access device, comprising connecting a second access device to said logic circuit;

examining said logic circuit through said second access device; and

electrically isolating said second access device from said logic circuit.

47. A method of evaluating a logic circuit through a test node, comprising:

inserting at least one transistor between said test node and said logic circuit;

generating a transistor turn-off signal;

providing a ground communication for said transistor turn-off signal;

testing said logic circuit; and

interfering with said ground communication.

48. The method of claim 47, further comprising providing a transistor communication for said transistor turn-off signal.

49. The method in claim 48, wherein inserting at least one transistor comprises inserting at least one p-channel transistor.

50. A method of evaluating a logic circuit through a test node, comprising:

inserting at least one transistor between said test node and said logic circuit;

generating a transistor turn-on signal;

providing a transistor drive communication for said transistor turn-on signal;

testing said logic circuit; and

interfering with said transistor drive communication.

51. The method in claim 50, wherein interfering with said transistor drive communication comprises providing a ground communication for said transistor turn-on signal.

52. The method in claim 51, wherein inserting at least one transistor comprises inserting at least one n-channel transistor.

53. A method of driving a transmission circuit electrically interposed between a first terminal and a second terminal, comprising:

providing a signal to a first node within said transmission circuit;

diverting said signal to a second node within said transmission circuit; and

preventing electrical communication between said first terminal and said second terminal in response to diverting said signal.

54. The method in claim 53, wherein said first node is a driving node and said second node is an isolation node.

55. The method in claim 54, wherein:

diverting said signal comprises programming a fuse; and

providing a signal comprises providing a logic 0 signal.

56. The method in claim 55, wherein:

diverting said signal comprises programming an anti-fuse; and

providing a signal comprises providing a logic 1 signal.

57. A method of preparing a circuit for non-test use, wherein said circuit is coupled to a main contact pad and a test contact pad, comprising:

providing a separation device between said circuit and said test contact pad; and

triggering said separation device.

58. A method of configuring a die to accommodate a plurality of lead frames, wherein said die has logic circuitry, comprising:

providing access to said logic circuitry through a first group of contact pads on said die, wherein said first group of contact pads corresponds to conductive leads of a first lead frame of said plurality of lead frames;

providing access to said logic circuitry through a second group of contact pads on said die, wherein said second group of contact pads corresponds to conductive leads of a second lead frame of said plurality of lead frames;

selecting one lead frame of said plurality of lead frames for attachment to said die; and

providing an accommodating isolation status of said second group of contact pads.

59. The method in claim 58, wherein providing an accommodating isolation status further comprises isolating said second group of contact pads from said logic circuitry in response to selecting said first lead frame.

60. The method in claim 58 wherein providing an accommodating isolation status further comprises maintaining access to said logic circuitry through said second group of contact pads in response to selecting said second lead frame.

61. The method in claim 58, wherein:

selecting one lead frame further comprises selecting a third lead frame having at least one a first conductive lead corresponding to one of said first group of contact pads and having at least a second conductive lead corresponding to one of said second group of contact pads; and

providing an accommodating isolation status further comprises isolating contact pads of said second group of contact pads that do not correspond to a conductive lead of said third lead frame.

62. A method of preparing a die, comprising:

providing a circuit on said die;

accommodating a first lead frame with a first contact pad;

allowing for access to said circuit through said first contact pad;

accommodating a second lead frame with a second contact pad;

allowing for access to said circuit through said second contact pad;

connecting said die to said first lead frame; and

denying access to said circuit through said second contact pad.

63. A method of controlling a communication device between a contact pad and a logic device, comprising:

sending a first signal to a transmission circuit of said communication device;

activating said transmission circuit with said first signal;

sending a second signal to a programmable circuit of said communication device; and

switching said first and second signals.

64. The method in claim 63, wherein switching said first and second signals comprises:

sending said first signal to said programmable circuit; and

sending said second signal to said transmission circuit.

65. The method in claim 64, further comprising deactivating said transmission circuit with said second signal.

66. The method in claim 65, wherein said programmable circuit has a resistance and switching further comprises changing said resistance of said programmable circuit.

67. The method in claim 65, wherein said programmable circuit has a capacitance and switching further comprises changing said capacitance of said programmable circuit.

68. A method of providing test-mode access for an integrated device having a plurality of pins and a die, wherein said die has a logic circuit, comprising:

establishing a temporary connection between said logic circuit and one pin of said plurality of pins; and

maintaining said temporary connection during a test mode of said die.

69. The method in claim 68, further comprising disabling said temporary connection before a non-test mode begins.

70. The method in claim 69, wherein disabling further comprises disabling said temporary connection after said test mode ends.

71. A method of using a no-connect pin of an integrated device during a test mode, wherein said integrated device includes a logic circuit, comprising:

attaching said no-connect pin to a disconnection circuit;

attaching said disconnection circuit to said logic circuit;

allowing a transmission between said no-connect pin and said logic circuit; and

activating said disconnection circuit.

72. The method in claim 71, wherein activating said disconnection circuit further comprises preventing further transmissions between said no-connect pin and said logic circuit.

73. The method in claim 72, wherein attaching said no-connect pin to said disconnection circuit comprises attaching said no-connect pin to said disconnection circuit through a contact pad.

74. A method of regulating electrical communication with a logic circuit coupled to a first communication terminal and a second communication terminal, comprising:

initially allowing electrical communication between said logic circuit and said first communication terminal and between said logic circuit and said second communication terminal; and

subsequently preventing electrical communication between said logic circuit and said second communication terminal.

75. A method of modifying electrical communication between a logic circuit and first and second communication terminals, comprising:

subjecting electrical communication between said logic circuit and said first communication terminal to a multiplexing function; and

making said multiplexing function dependent upon an operational state of a programming element.

76. A method of regulating electrical communication with a logic circuit coupled to a first communication terminal and a second communication terminal, comprising:

allowing electrical communication between said logic circuit and a selection of said first communication terminal and said second communication terminal; and

optionally changing said selection.

77. The method in claim 76, wherein allowing electrical communication further comprises:

multiplexing electrical communication between said logic circuit and said first communication terminal; and

conversely multiplexing electrical communication between said logic circuit and said second communication terminal.

78. The method in claim 76, wherein optionally changing said selection comprises providing for oppositely multiplexing electrical communication between said logic circuit and said first communication terminal and between said logic circuit and said second communication terminal.

79. A method of configuring a die to accommodate a first lead frame and a second lead frame, comprising:

providing a first group of contact pads on said die, wherein said first group of contact pads generally corresponds to conductive leads of said first lead frame;

providing a second group of contact pads on said die, wherein said second group of contact pads generally corresponds to conductive leads of said second lead frame;

providing one of said first and second lead frames for use with said die; and

isolating one group of said first and second groups of contact pads, wherein said one group does not correspond to a provided lead frame.

80. The method in claim 79, wherein:

said method further comprises:

configuring said first group of contact pads to couple to logic circuitry on said die, and

configuring said second group of contact pads to couple to said logic circuitry on said die; and

isolating further comprises restricting electrical communication between said logic circuitry and said one group.

81. The method in claim 80, wherein restricting electrical communication between said logic circuitry and said one group further comprises:

providing a programmable element on said die, wherein said programmable element has a pre-programmed state and a post-programmed state;

making restricted electrical communication between said logic circuitry and said one group dependent upon one state from said pre-programmed state and said post-programmed state; and

providing said one state.

82. The method in claim 81, wherein:

making restricted electrical communication between said logic circuitry and said one group dependent upon one state of said programmable element further comprises making restricted electrical communication between said logic circuitry and said one group dependent upon said pre-programmed state of said programmable element; and

providing said one state comprises maintaining said pre-programmed state.

83. The method in claim 81, wherein:

making restricted electrical communication between said logic circuitry and said one group dependent upon one state of said programmable element further comprises making restricted electrical communication between said logic circuitry and said one group dependent upon said post-programmed state of said programmable element; and

providing said one state comprises programming said programmable element.

84. A method accommodating a first lead frame and a second lead frame with a die, comprising:

providing a first group of contact pads on said die, wherein said first group has a first isolation state and is compatible with said first lead frame;

providing a second group of contact pads on said die, wherein said second group has a second isolation state and is compatible with said second lead frame;

providing one programmable element on said die having an initial operations state and a subsequent operations state;

associating said first isolation state of all contact pads in said first group with said initial operations state; and

associating said second isolation state of all contact pads in said second group with said subsequent operations state.

85. The method in claim 84, further comprising:

selecting said first lead frame for use with said die; and

transitioning to said subsequent operations state.

86. The method in claim 85, wherein transitioning further comprises programming said programmable element.

87. The method in claim 84, further comprising:

selecting said second lead frame for use with said die; and

maintaining said initial operations state.

88. The method in claim 87, wherein maintaining further comprises retaining a configuration of said programmable element.

89. A method of accommodating a plurality of lead frames with a die having logic circuitry, comprising:

providing a first group of contact pads on said die;

providing a second group of contact pads on said die;

providing a plurality of programmable elements on said die, wherein each programmable element of said plurality of programmable elements has an initial operations state and a subsequent operations state;

coupling each programmable element of said plurality of programmable elements to two contact pads, wherein one contact pad is a first group contact pad and another contact pad is a second group contact pad;

isolating one of said two contact pads for each programmable element during said initial operations state; and

isolating another of said two contact pads for each programmable element in response to a transition to said subsequent operations state.

90. The method in claim 89, further comprising:

selecting a lead frame from said plurality of lead frames for use with said die;

transitioning to said subsequent operations state for generally every programmable element having an isolated contact pad corresponding to a conductive lead of said lead frame; and

retaining said initial operations state for generally every programmable element having an isolated contact pad failing to correspond to a conductive lead of said lead frame.

91. The method in claim **90**, wherein transitioning further comprises permanently transitioning to said subsequent operations state.

92. The method in claim **91**, wherein:

isolating one contact pad of said two contact pads for each programmable element further comprises isolating a first group contact pad; and

isolating another contact pad of said two contact pads for each programmable element further comprises isolating a second group contact pad in response to a transition to said subsequent operations state.

93. The method in claim **91**, wherein:

transitioning comprises programming generally every programmable element in which said first group contact pad corresponds to a conductive lead of said lead frame; and

retaining comprises refraining from programming generally every programmable element in which said second group contact pad corresponds to a conductive lead of said lead frame.

94. A method of configuring a die to adapt to one of a plurality of lead frames, comprising:

providing a first group of communication terminals on said die;

providing a second group of communication terminals on said die;

selecting a lead frame from said plurality of lead frames; and

isolating communication terminals that do not correspond to a conductive lead of said lead frame.

95. A method of controlling communication with a first logic circuit and a second logic circuit, wherein a first pathway joins a first contact pad and said first logic circuit, a second pathway joins a second contact pad and said first logic circuit, a third pathway joins a third contact pad and said second logic circuit, and a fourth pathway joins a fourth contact pad and said second logic circuit, wherein said method comprises:

multiplexing said first pathway;

multiplexing said third pathway;

commonly initiating a first multiplexed state at said first and third pathways;

allowing electrical communication through any pathway that is in said first multiplexed state;

allowing a one-time common change to a second multiplexed state at said first and third pathways; and

preventing electrical communication through any pathway that is in said second multiplexed state.

96. The method in claim **95**, further comprising:

multiplexing said second pathway;

multiplexing said fourth pathway;

commonly initiating said second multiplexed state at said second and fourth pathways; and

commonly establishing said first multiplexed state at said second and fourth pathways in response to said one-time common change.

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