US 20240272359A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2024/0272359 A1**

(43) **Pub. Date: Aug. 15, 2024**

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(54) **OPTICAL POWER SPLITTERS INCORPORATING ONE OR MORE SPIRAL ELEMENTS**

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(21) Appl. No.: **18/109,294**

(22) Filed: **Feb. 14, 2023**

Publication Classification

(51) **Int. Cl.**

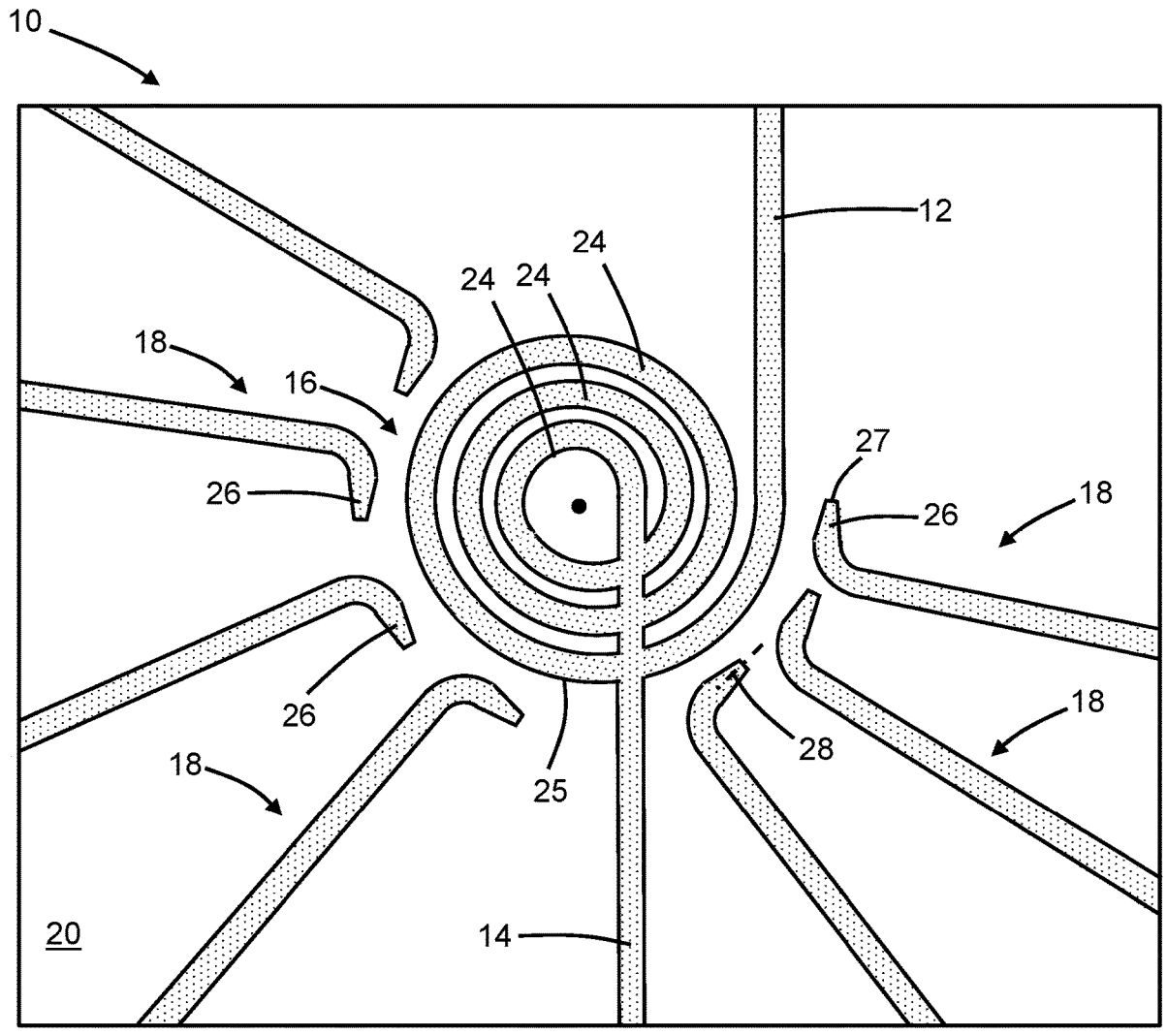
G02B 6/125	(2006.01)
G02B 6/122	(2006.01)
G02B 6/13	(2006.01)

(52) **U.S. Cl.**

CPC ***G02B 6/125*** (2013.01); ***G02B 6/1228*** (2013.01); ***G02B 6/13*** (2013.01); *G02B 2006/12061* (2013.01); *G02B 2006/12147* (2013.01); *G02B 2006/1215* (2013.01)

(57) **ABSTRACT**

Structures for an optical power splitter and methods of forming a structure for an optical power splitter. The structure comprises a spiral waveguide core having an outer perimeter. The structure further comprises a plurality of waveguide cores. Each waveguide core has a section disposed adjacent to the outer perimeter of the spiral waveguide core.



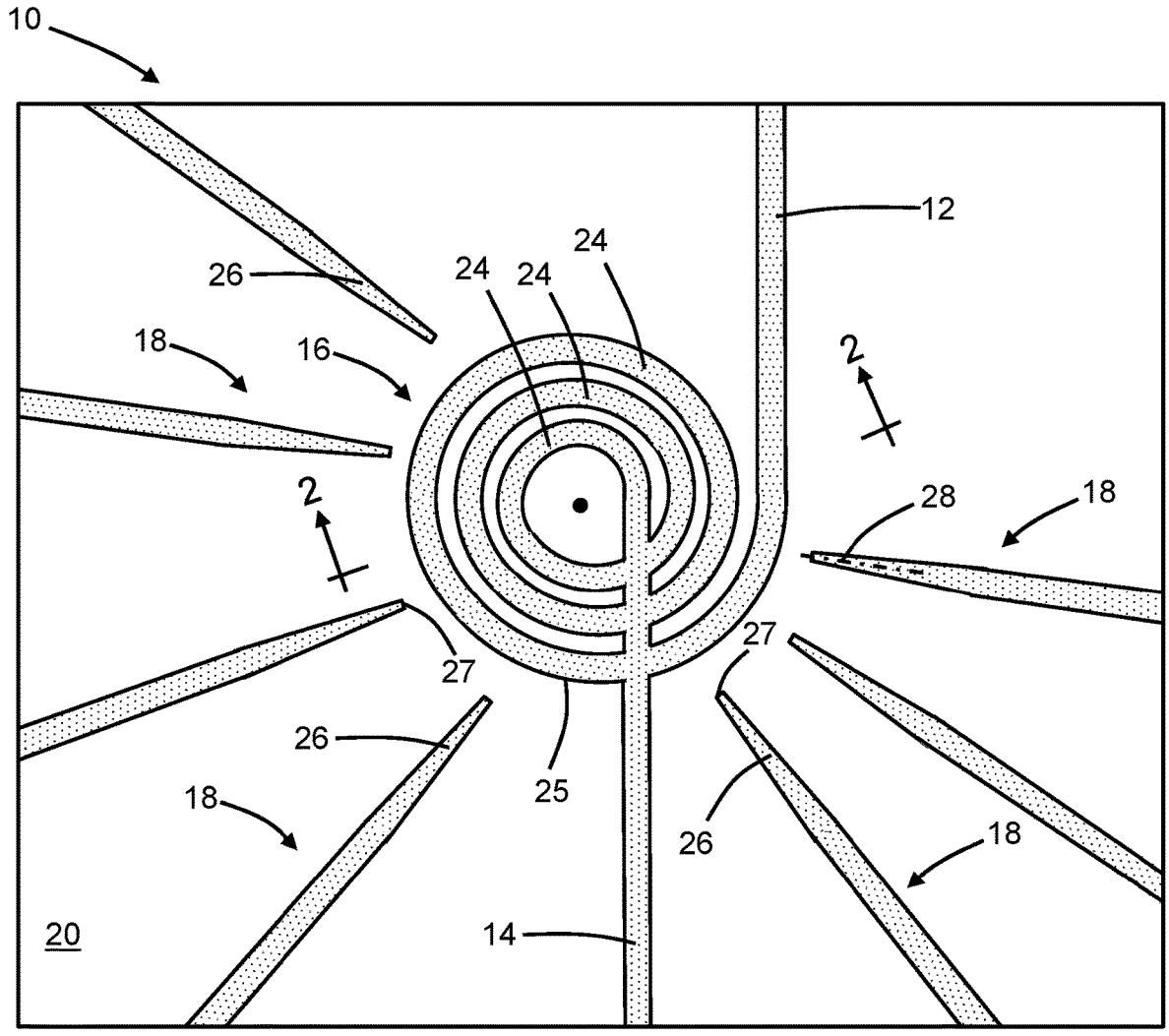


FIG. 1

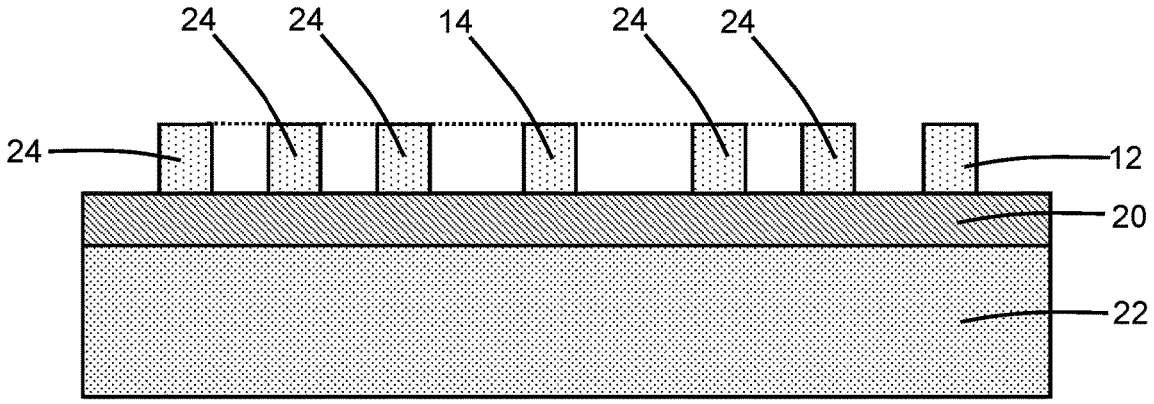


FIG. 2

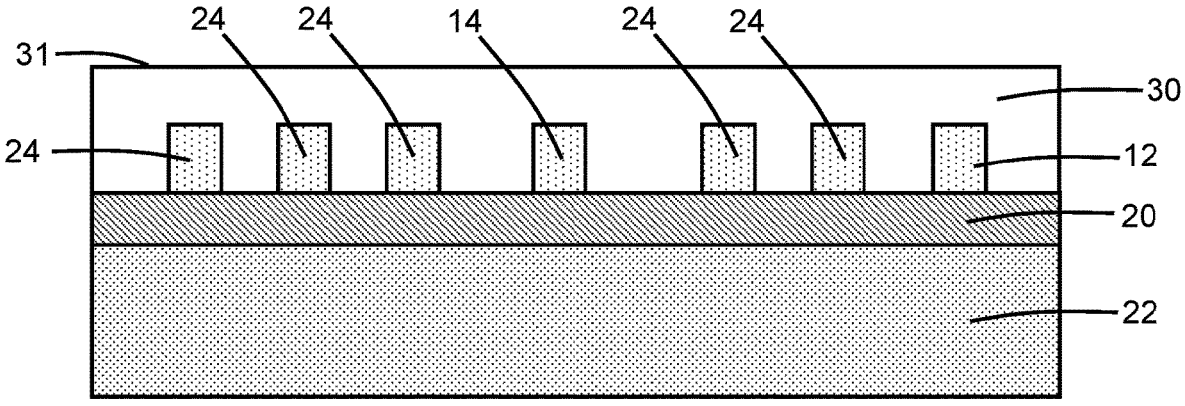


FIG. 3

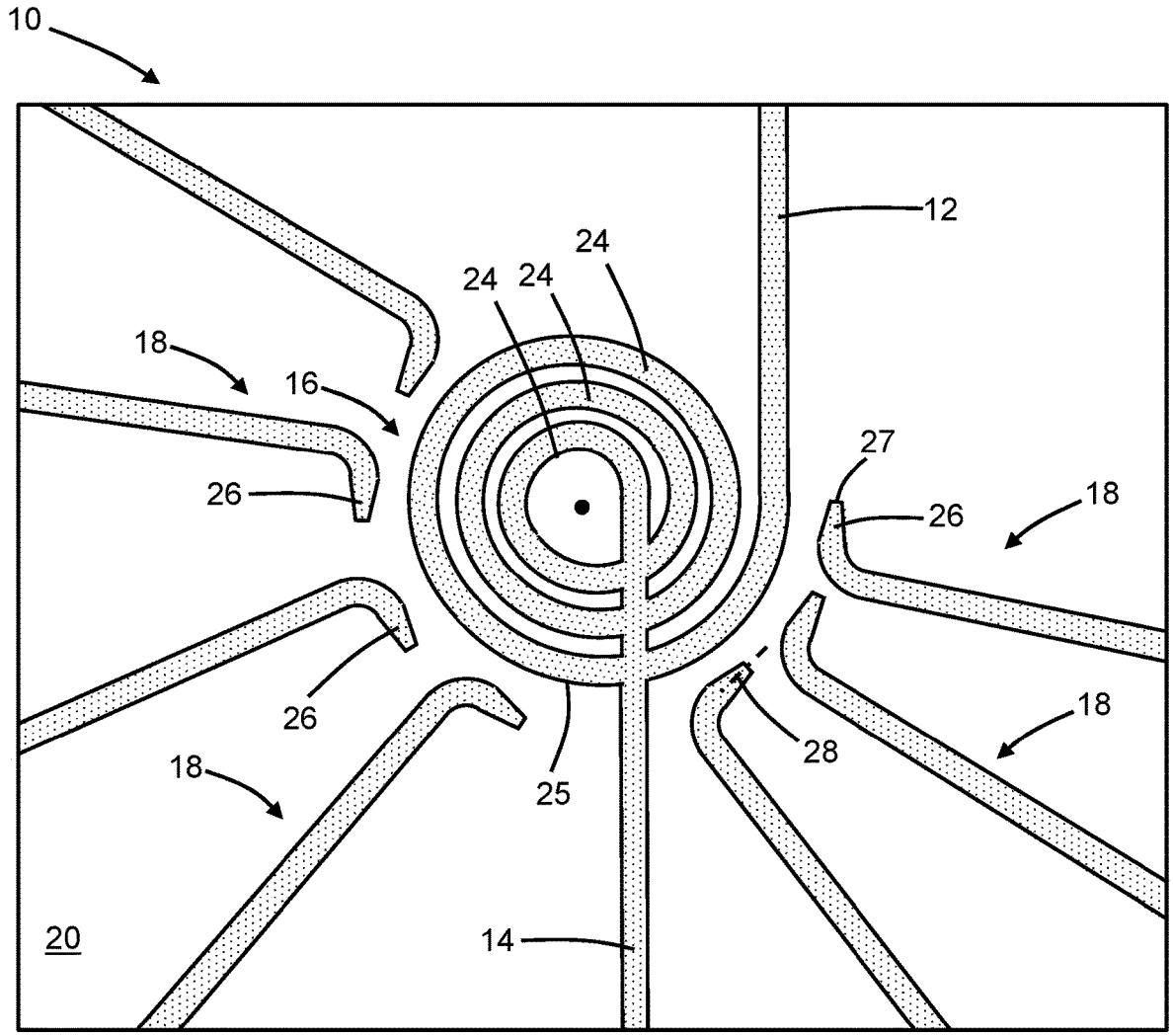


FIG. 4

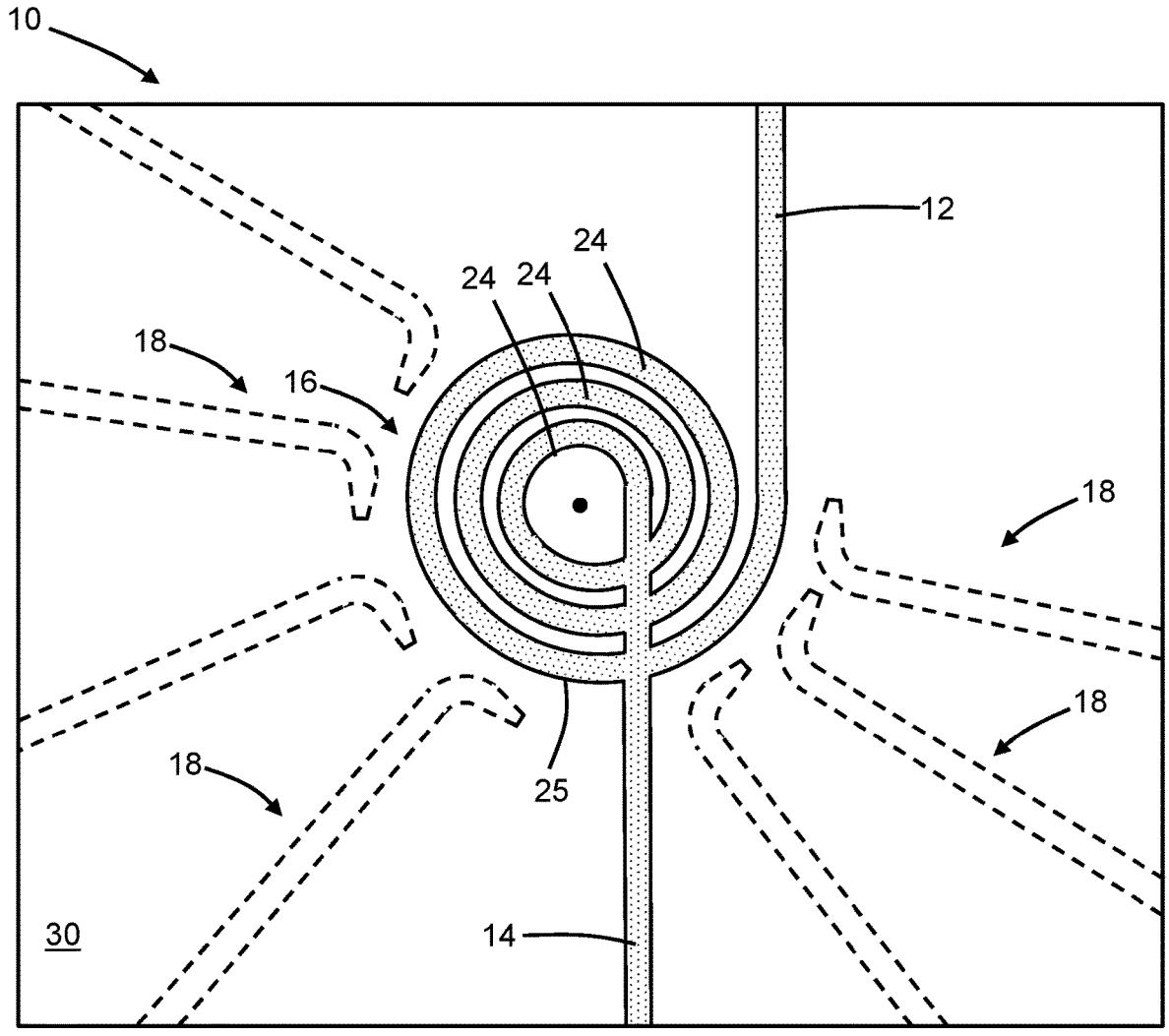


FIG. 5

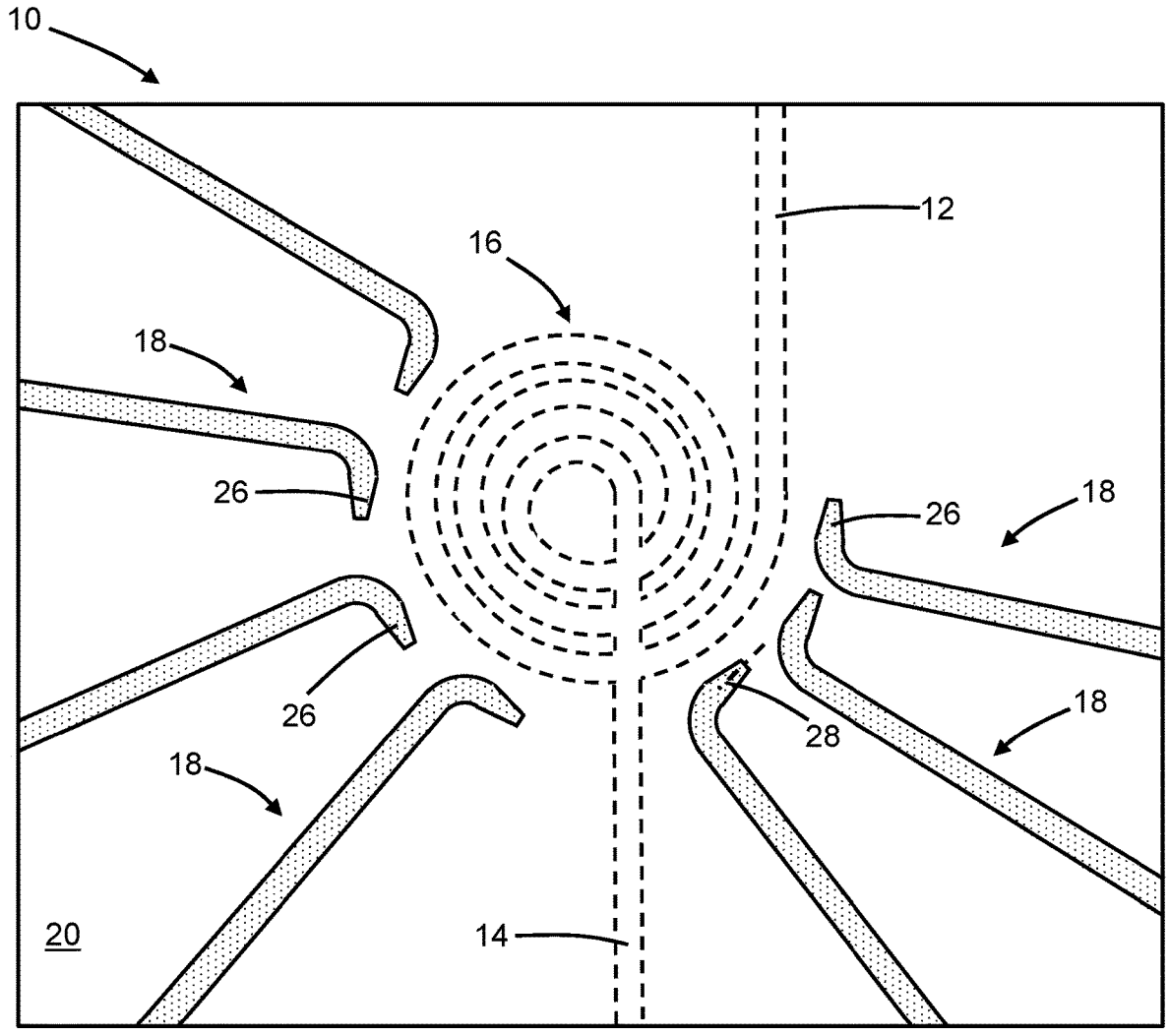


FIG. 6

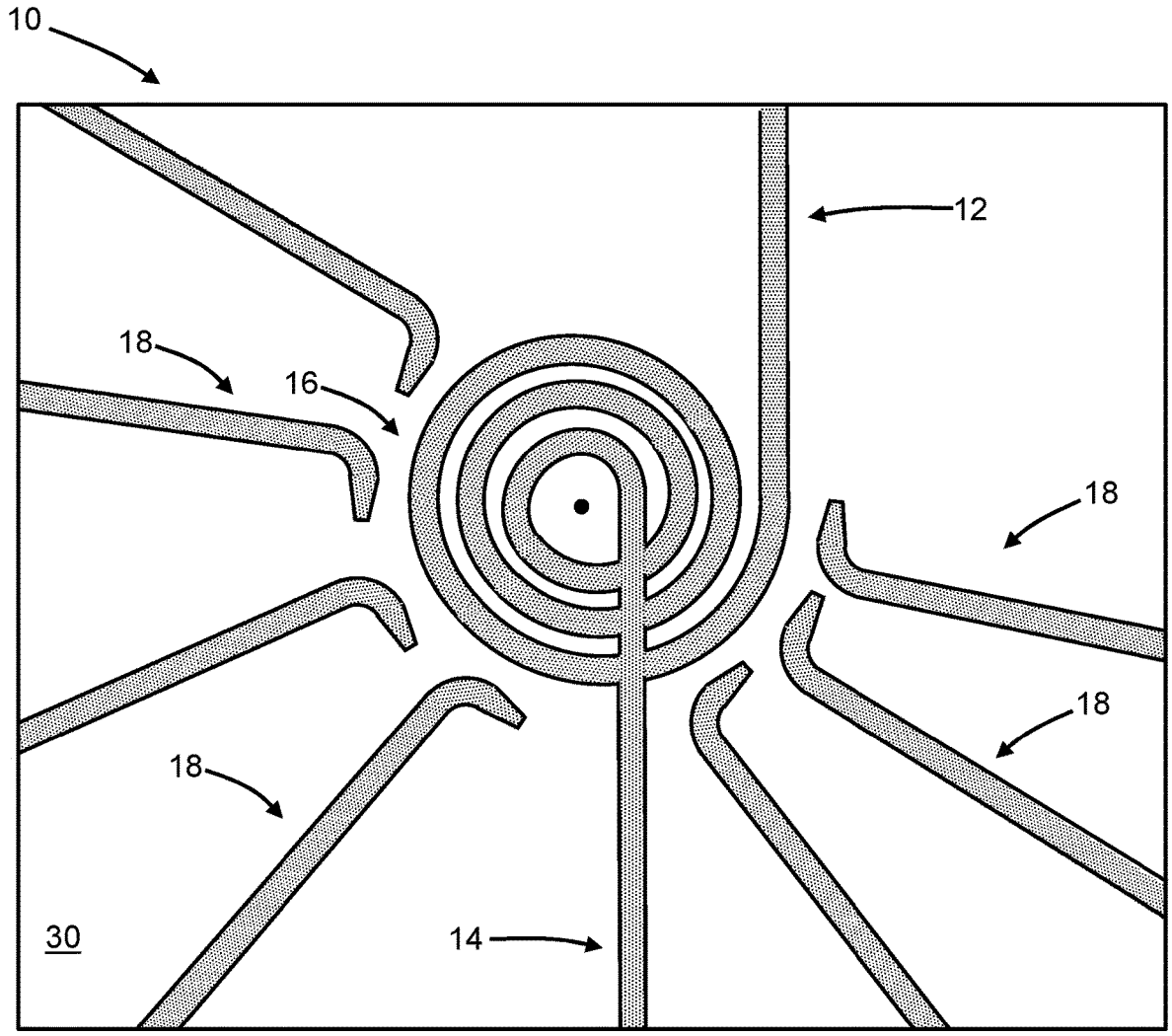


FIG. 7

OPTICAL POWER SPLITTERS INCORPORATING ONE OR MORE SPIRAL ELEMENTS

BACKGROUND

[0001] The disclosure relates to photonics chips and, more specifically, to structures for an optical power splitter and methods of forming a structure for an optical power splitter.

[0002] Photonics chips are used in many applications and systems including, but not limited to, data communication systems and data computation systems. A photonics chip may integrate optical components and electronic components into a unified platform. Among other factors, layout area, cost, and operational overhead may be reduced by the integration of both types of components on the same chip.

[0003] An optical power splitter is an optical component that is used in photonics chips to split optical power between multiple output waveguides based upon principles of multi-mode interference (MMI). Multiple multi-mode interference regions may be cascaded to build an optical power splitter having a single waveguide serving as an input channel and multiple waveguides serving as output channels. However, cascaded multi-mode interference regions increase the complexity of a photonics circuit, enlarge the footprint of an optical power splitter, and increase the variability in the splitting ratio.

[0004] Improved structures for an optical power splitter and methods of forming a structure for an optical power splitter.

SUMMARY

[0005] In an embodiment of the invention, a structure for an optical power coupler is provided. The structure comprises a spiral waveguide core having an outer perimeter. The structure further comprises a plurality of waveguide cores. Each waveguide core has a section disposed adjacent to the outer perimeter of the spiral waveguide core.

[0006] In an embodiment of the invention, a method of forming a structure for an optical power coupler is provided. The method comprises forming a spiral waveguide core that has an outer perimeter, and forming a plurality of waveguide cores. Each waveguide core has a section disposed adjacent to the outer perimeter of the spiral waveguide core.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate various embodiments of the invention and, together with a general description of the invent ion given above and the detailed description of the embodiments given below, serve to explain the embodiments of the invention. In the drawings, like reference numerals refer to like features in the various views.

[0008] FIG. **1** is a top view of a structure at an initial fabrication stage of a processing method in accordance with embodiments of the invention.

[0009] FIG. **2** is a cross-sectional view taken generally along line **2-2** in FIG. **1**.

[0010] FIG. **3** is a cross-sectional view of the structure at a fabrication stage subsequent to FIGS. **1**, **2**.

[0011] FIG. **4** is a top view of a structure in accordance with alternative embodiments of the invention.

[0012] FIG. **5** is a top view of a structure in accordance with alternative embodiments of the invention.

[0013] FIG. **6** is a top view of a structure in accordance with alternative embodiments of the invention.

[0014] FIG. **7** is a top view of a structure in accordance with alternative embodiments of the invention.

DETAILED DESCRIPTION

[0015] With reference to FIGS. **1**, **2** and in accordance with embodiments of the invention, a structure **10** for an optical power splitter includes a waveguide core **12**, a waveguide core **14**, a spiral waveguide core **16** that connects the waveguide core **12** to the waveguide core **14**, and waveguide cores **18** that are spaced from the spiral waveguide core **16**. The waveguide cores **12**, **14**, **16**, **18** are positioned on, and over, a dielectric layer **20** and a semiconductor substrate **22**. In an embodiment, the dielectric layer **20** may be comprised of a dielectric material, such as silicon dioxide, and the semiconductor substrate **22** may be comprised of a semiconductor material, such as single-crystal silicon. In an embodiment, the dielectric layer **20** may be a buried oxide layer of a silicon-on-insulator substrate, and the dielectric layer **20** may be disposed between the waveguide cores **12**, **14**, **16**, **18** and the semiconductor substrate **22**. The dielectric layer **20** may function as a lower cladding layer for the waveguide cores **12**, **14**, **16**, **18**.

[0016] In an embodiment, the waveguide cores **12**, **14**, **16**, **18** may be comprised of a material having a refractive index that is greater than the refractive index of silicon dioxide. In an embodiment, the waveguide cores **12**, **14**, **16**, **18** may be comprised of a semiconductor material. In an embodiment, the waveguide cores **12**, **14**, **16**, **18** may be comprised of single-crystal silicon. In an embodiment, the waveguide cores **12**, **14**, **16**, **18** may be comprised of polysilicon or amorphous silicon. In an embodiment, the waveguide cores **12**, **14**, **16**, **18** may be comprised of a dielectric material, such as silicon nitride, silicon oxynitride, or aluminum nitride. In alternative embodiments, other materials, such as a polymer or a III-V compound semiconductor, may be used to form the waveguide cores **12**, **14**, **16**, **18**.

[0017] In an embodiment, the waveguide cores **12**, **14**, **16**, **18** may be formed by patterning a layer comprised of their constituent material with lithography and etching processes. In an embodiment, an etch mask may be formed by a lithography process over the layer to be patterned, and unmasked sections of the deposited layer may be etched and removed by an etching process. In an embodiment, the waveguide cores **12**, **14**, **16**, **18** may be formed by patterning the semiconductor material (e.g., single-crystal silicon) of a device layer of a silicon-on-insulator substrate. In an embodiment, the waveguide cores **12**, **14**, **16**, **18** may be formed by patterning a deposited layer comprised of their constituent material (e.g., silicon nitride, polysilicon, or amorphous silicon). In an embodiment, the waveguide cores **12**, **14**, **16**, **18** may be disposed within the same plane.

[0018] In an embodiment, the spiral waveguide core **16** may include a set of spiral elements **24** defining concentric nested turns that are continuously wound in a spiral about a center point. The spiral elements **24** of the spiral waveguide core **16** may wind around the center point at a continuously decreasing radius from the center point. In an embodiment, the spiral waveguide core **16** may be mathematically characterized as an Archimedean spiral. In an embodiment, the spiral waveguide core **16** may be an Archimedean spiral that

is characterized by spiral elements **24** that are evenly spaced independent of radius from the center point. The spiral waveguide core **16** may have an outer perimeter **25**. In an embodiment, the outer perimeter **25** of the spiral waveguide core **16** may be defined by the outer radius of the outermost spiral element **24**. In an embodiment, the spiral elements **24** of the spiral waveguide core **16** may have a uniform or substantially uniform width over the length of the spiral.

[0019] In an embodiment, each spiral element **24** may have a circular shape. In alternative embodiments, each spiral element **24** may have a non-circular shape, such as oblong, rectangular, or square. In alternative embodiments, the spiral elements **24** may include a combination of different shapes. In an alternative embodiment, the spiral elements **24** may be divided into segments that are dimensioned and positioned at small enough pitch so as to define a sub-wavelength grating, and the gaps between the segments may be subsequently filled with dielectric material to define a metamaterial structure.

[0020] The waveguide core **12** may provide an input for light into an end of the spiral waveguide core **16** of the optical power splitter. In an embodiment, the waveguide core **12** may be coupled to an end of the outermost spiral element **24** of the spiral waveguide core **16**. In an embodiment, each waveguide core **18** may include a section in the representative form of a taper **26** that is positioned adjacent to the outer perimeter **25** of the spiral waveguide core **16**. Each taper **26** may extend along a longitudinal axis **28** and may terminate at an end **27**. Each taper **26** may have a width dimension that increases with increasing distance from the end **27**. The tapers **26** may receive light that is transferred from the spiral waveguide core **16**, and the waveguide cores **18** may route the transferred light to other optical components on the photonics chip.

[0021] The tapers **26** of the waveguide cores **18** are disposed at different positions adjacent to, and spaced apart about, the outer perimeter **25** of the spiral waveguide core **16**. In an embodiment, the spiral waveguide core **16** may output light at spaced-apart locations that are distributed about the outer perimeter **25**. In an embodiment, the tapers **26** of the waveguide cores **18** may be placed adjacent to the locations about the outer perimeter **25** at which the spiral waveguide core **16** outputs light. The splitting ratio for each waveguide core **18** may be determined by, among other parameters, the separation between the end **27** of the associated taper **26** and the outer perimeter **25** and the position of the taper **26** about the outer perimeter **25**. In an embodiment, the tapers **26** of the waveguide cores **18** may be spaced about the outer perimeter **25** to provide splitting ratios that are equal or substantially equal. In an embodiment, the tapers **26** of the waveguide cores **18** may be spaced about the outer perimeter **25** to provide splitting ratios that are different. In an embodiment, the longitudinal axis **28** of each taper **26** may be aligned perpendicular to a tangent at a point on the outer perimeter **25** of the spiral waveguide core **16**. In an alternative embodiment, the longitudinal axis **28** of each taper **26** may be aligned at an acute angle relative to a point on the outer perimeter **25** of the spiral waveguide core **16**. In an embodiment, the waveguide cores **18** may number four or more.

[0022] The waveguide core **14** may provide an output for light from an end of the spiral waveguide core **16** of the optical power splitter. In an embodiment, the waveguide core **14** may be coupled to the innermost spiral element **24** of the spiral waveguide core **16**. The waveguide core **14** may be used to direct residual light out of the spiral waveguide core **16** that is not transferred from the spiral waveguide core **16** to the waveguide cores **18**. The waveguide core **14** may intersect the spiral elements **24** along its outward path. In an alternative embodiment, the waveguide core **14** may be omitted from the structure **10**.

[0023] In an alternative embodiment, the spiral waveguide core **16** may include a single spiral element **24** that winds around the center point at a continuously decreasing radius from the center point. The waveguide core **12** may be coupled to one end of the single spiral element **24** and the waveguide core **14** may be coupled to the opposite end of the single spiral element **24**.

[0024] With reference to FIG. **3** in which like reference numerals refer to like features in FIGS. **1**, **2** and at a subsequent fabrication stage, a dielectric layer **30** is formed on, and over, the waveguide core **12**, the waveguide core **14**, the spiral waveguide core **16**, and the waveguide cores **18**. The dielectric layer **30** may be comprised of a dielectric material, such as silicon dioxide, having a refractive index that is less than the refractive index of the material constituting the waveguide cores **12**, **14**, **16**, **18**. The dielectric layer **30** may have a top surface **31**, the waveguide cores **12**, **14**, **16**, **18** may be embedded in the dielectric layer **30**, and the dielectric layer **30** may have a thickness greater than a height of the waveguide cores **12**, **14**, **16**, **18**.

[0025] In use, light (e.g., laser light) may be guided on a photonics chip by the waveguide core **12** to the spiral waveguide core **16** of the optical power coupler. Light propagating in the spiral waveguide core **16** is transferred with respective splitting ratios from the spiral waveguide core **16** to the tapers **26** and directed by the waveguide cores **18** away from the optical power splitter. The light coupling between the spiral waveguide core **16** and the tapers **26** of the waveguide cores **18** may be characterized as free space coupling. In an embodiment, light may also exit the optical power splitter via the waveguide core **14**.

[0026] The structure **10** provides an optical power splitter of reduced complexity and footprint in comparison with optical power splitters that include cascaded multi-mode interference regions. In that regard, the spiral elements **24** of the spiral waveguide core **16** may reduce the space needed on the photonics chip to construct an optical power splitter due to the compactness of the spiral shape. In addition, the optical power splitter provided by the structure **10** may decrease the variability in the splitting ratio.

[0027] With reference to FIG. **4** and in accordance with alternative embodiments, the taper **26** of each of the waveguide cores **18** may be oriented such that the longitudinal axis **28** is aligned tangential to a point on the outer perimeter **25** of the spiral waveguide core **16**. The dimensions of the tapers **26** and the gaps between the tapers **26** and the outer perimeter **25** may be selected to provide adiabatic light coupling. Each waveguide core **18** may include a bend that is configured to route the waveguide core **18** away from spiral waveguide core **16**.

[0028] With reference to FIG. **5** and in accordance with alternative embodiments, the waveguide cores **18** may be arranged in a different elevation or level of the structure **10** than the waveguide core **12**, the waveguide core **14**, and the spiral waveguide core **16**. Specifically, the waveguide cores **12**, **14**, **16** may be disposed on the dielectric layer **30** in a level that is above the level containing the waveguide cores

18. The waveguide cores **18** are positioned in a vertical direction between the semiconductor substrate **22** and the waveguide cores **12**, **14**, **16**. The waveguide cores **18** may be comprised of a different material than the waveguide cores **12**, **14**, **16**. In an embodiment, the waveguide cores **12**, **14**, **16** may be comprised of a dielectric material, such as silicon nitride, and the waveguide cores **18** may be comprised of silicon. With reference to FIG. **6** and in accordance with alternative embodiments, the waveguide cores **18** may be arranged in a different elevation or level of the structure **10** than the waveguide core **12**, the waveguide core **14**, and the spiral waveguide core **16**. Specifically, the waveguide cores **18** may be disposed on the dielectric layer **30** in a level that is above the level containing the waveguide cores **12**, **14**, **16**. The waveguide core **12**, **14**, **16** are positioned in a vertical direction between the semiconductor substrate **22** and the waveguide cores **18**. The waveguide cores **18** may be comprised of a different material than the waveguide cores **12**, **14**, **16**. In an embodiment, the waveguide cores **18** may be comprised of a dielectric material, such as silicon nitride, and the waveguide cores **12**, **14**, **16** may be comprised of silicon.

[0029] With reference to FIG. **7** and in accordance with alternative embodiments, the waveguide cores **12**, **14**, **16**, **18** may be multiple-layer stacked waveguide cores that include a lower layer of material (FIG. **1**) and an upper layer of material (FIG. **7**) stacked over the lower layer of material. The lower layer may be patterned and formed on the dielectric layer **20** as shown in FIG. **1**, and the upper layer may be patterned and formed on the dielectric layer **30** as shown in FIG. **7**. The lower layer may be separated from the upper layer by the dielectric material of the dielectric layer **30**. In an embodiment, the lower and upper layers the waveguide cores **12**, **14**, **16**, **18** may be comprised of different materials. In an embodiment, the lower layer of the waveguide cores **12**, **14**, **16**, **18** may be comprised of silicon, and the upper layer of the waveguide cores **12**, **14**, **16**, **18** may be comprised of silicon nitride.

[0030] The methods as described above are used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (e.g., as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. The chip may be integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either an intermediate product or an end product. The end product can be any product that includes integrated circuit chips, such as computer products having a central processor or smartphones.

[0031] References herein to terms modified by language of approximation, such as "about", "approximately", and "substantially", are not to be limited to the precise value specified. The language of approximation may correspond to the precision of an instrument used to measure the value and, unless otherwise dependent on the precision of the instrument, may indicate a range of +/−10% of the stated value(s).

[0032] References herein to terms such as "vertical", "horizontal", etc. are made by way of example, and not by way of limitation, to establish a frame of reference. The term "horizontal" as used herein is defined as a plane parallel to a conventional plane of a semiconductor substrate, regardless of its actual three-dimensional spatial orientation. The terms "vertical" and "normal" refer to a direction in the frame of reference perpendicular to the horizontal, as just defined. The term "lateral" refers to a direction in the frame of reference within the horizontal plane.

[0033] A feature "connected" or "coupled" to or with another feature may be directly connected or coupled to or with the other feature or, instead, one or more intervening features may be present. A feature may be "directly connected" or "directly coupled" to or with another feature if intervening features are absent. A feature may be "indirectly connected" or "indirectly coupled" to or with another feature if at least one intervening feature is present. A feature "on" or "contacting" another feature may be directly on or in direct contact with the other feature or, instead, one or more intervening features may be present. A feature may be "directly on" or in "direct contact" with another feature if intervening features are absent. A feature may be "indirectly on" or in "indirect contact" with another feature if at least one intervening feature is present. Different features may "overlap" if a feature extends over, and covers a part of, another feature with either direct contact or indirect contact.

[0034] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

What is claimed is:

1. A structure for an optical power coupler, the structure comprising:

a spiral waveguide core having an outer perimeter; and

a plurality of first waveguide cores, each of the first waveguide cores having a section disposed adjacent to the outer perimeter of the spiral waveguide core.

2. The structure of claim **1** wherein the spiral waveguide core includes a plurality of spiral elements that are arranged in a spiral.

3. The structure of claim **2** wherein the spiral is an Archimedes spiral.

4. The structure of claim **2** wherein the spiral elements include an outermost spiral element that defines the outer perimeter, and further comprising:

a second waveguide core connected to the outermost spiral element.

5. The structure of claim **2** wherein the spiral elements include an innermost spiral element, and further comprising:

a second waveguide core connected to the innermost spiral element.

6. The structure of claim **1** wherein the spiral waveguide core and the first waveguide cores are disposed in the same plane.

7. The structure of claim **1** wherein the section of each of the first waveguide cores is a taper terminated by an end.

8. The structure of claim **7** wherein the taper of each of the first waveguide cores has a longitudinal axis that is aligned perpendicular to a tangent at a point on the outer perimeter of the spiral waveguide core.

9. The structure of claim **7** wherein the taper of each of the first waveguide cores has a longitudinal axis that is aligned tangential to a point on the outer perimeter of the spiral waveguide core.

10. The structure of claim **7** wherein the taper of each of the first waveguide cores has a longitudinal axis that is aligned at an acute angle relative to a point on the outer perimeter of the spiral waveguide core.

11. The structure of claim **1** wherein the spiral waveguide core comprises a first material, and the first waveguide cores comprise a second material different from the first material.

12. The structure of claim **11** wherein the first material is silicon, and the second material is silicon nitride.

13. The structure of claim **11** wherein the first material is silicon nitride, and the second material is silicon.

14. The structure of claim **1** wherein the spiral waveguide core and the first waveguide cores include a lower layer and an upper layer stacked over the lower layer, the upper layer comprises a first material, the lower layer comprises a second material different from the first material, and the lower layer is separated from the upper layer by dielectric material.

15. The structure of claim **1** further comprising:

a dielectric layer over the spiral waveguide core,

wherein the first waveguide cores are disposed on the dielectric layer.

16. The structure of claim **14** wherein the spiral waveguide core comprises silicon, and the first waveguide cores comprise silicon nitride.

17. The structure of claim **1** further comprising:

a dielectric layer over the first waveguide cores,

wherein the spiral waveguide core is disposed on the dielectric layer.

18. The structure of claim **17** wherein the spiral waveguide core comprises silicon nitride, and the first waveguide cores comprise silicon.

19. The structure of claim **1** wherein the first waveguide cores number four or more.

20. A method of forming a structure for an optical power coupler, the method comprising:

forming a spiral waveguide core that has an outer perimeter; and

forming a plurality of waveguide cores, wherein each waveguide core has a section disposed adjacent to the outer perimeter of the spiral waveguide core.

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