(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 March 2009 (05.03.2009)

PCT

(10) International Publication Number
WO 2009/028800 A1

(51) International Patent Classification:
H01L 23/60 (2006.01)

(21) International Application Number:
PCT/KR2008/004410

(22) International Filing Date: 29 July 2008 (29.07.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10-2007-0087349 30 August 2007 (30.08.2007) KR

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(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(54) **Title:** ELECTROSTATIC DISCHARGE PROTECTION DEVICE OF OUTPUT DRIVER STAGE

[Fig. 2]

(57) **Abstract:** Provided is an electrostatic discharge (ESD) protection device of an output driver stage of a semiconductor chip. The ESD protection device of an output driver stage, which includes a p-channel metal-oxide-semiconductor (PMOS) transistor having a source connected to a first source voltage and an n-channel metal-oxide-semiconductor (NMOS) transistor having a source connected to a second source voltage, the MOS transistors having gates applied with output signals from an internal circuit and drains connected to the output pad, wherein a distance between contacts formed on a drain region and a gate poly of the MOS transistors is relatively greater than a value according to a predetermined design rule.

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Description

ELECTROSTATIC DISCHARGE PROTECTION DEVICE OF OUTPUT DRIVER STAGE

Technical Field

[1] The present invention relates to an electrostatic discharge (ESD) protection device, and more particularly, to an ESD protection device of an output driver stage for preventing ESD from flowing into an internal circuit from the output driver stage.

Background Art

[2] When electrostatic discharge (ESD) caused from the human body or machinery flows into an integrated semiconductor chip, internal microcircuits in the semiconductor chip may be damaged or generate errors. The ESD mainly flows into input/output driver stages of the semiconductor chip.

[3] On the other hand, input driver stages of almost all semiconductor chips may include ESD protection devices. When a concept about the ESD for the output driver stages of semiconductor chips was not established, additional ESD protection devices were not used. However, recently, ESD protection devices for preventing ESD that may flow into the output driver stages of the semiconductor chips from flowing into internal circuits have been widely used.

[4] FIG. 1 illustrates a conventional ESD protection device of an output driver stage.

[5] Referring to FIG. 1, the conventional ESD protection device 100 of the output driver stage includes two diodes DP and DN and a limiting resistor R1. The limiting resistor R1 has a function of preventing the buildup of a discharge path of ESD toward a p-channel metal-oxide-semiconductor (PMOS) transistor P1 and an n-channel metal-oxide-semiconductor (NMOS) transistor N1 included in the output driver stage when ESD flows into an output pad. Instead, the ESD flows out through a discharge path formed at one of the two diodes DP and DN. Therefore, the ESD does not flow into an internal circuit 110.

[6] However, the diodes DP and DN and the limiting resistor R1 for ESD protection of the output driver stage may result in increase in the entire chip size.

Disclosure of Invention

Technical Problem

[7] The present invention provides an electrostatic discharge (ESD) protection device of an output driver stage capable of preventing ESD from flowing into an internal circuit in the output driver stage without diodes and limiting resistors.

Technical Solution

[8] According to an aspect of the present invention, there is provided an electrostatic

discharge (ESD) protection device of an output driver stage, which includes a p-channel metal-oxide-semiconductor (PMOS) transistor having a source connected to a first source voltage and an n-channel metal-oxide-semiconductor (NMOS) transistor having a source connected to a second source voltage, the MOS transistors having gates applied with output signals from an internal circuit and drains connected to the output pad, wherein a distance between contacts formed on a drain region and a gate poly of the MOS transistors is relatively greater than a value according to a predetermined design rule.

[9] According to another aspect of the present invention, there is provided an ESD protection device of an output driver stage, which includes a PMOS transistor P1 having a source connected to a first source voltage and an NMOS transistor having a source connected to a second source voltage, the MOS transistors having gates applied with output signals from an internal circuit and drains connected to the output pad, wherein a resistor is formed between the drain and the output pad of the MOS transistors.

Advantageous Effects

[10] The electrostatic discharge (ESD) protection device of the output driver stage according to the present invention can prevent ESD that flows from the output pad from flowing into the internal circuit by increasing the drain resistors of the MOS transistors included in the output driver stage or using the active resistor. Therefore, the conventional diodes and limiting resistor are not needed and the entire chip size can be reduced.

Brief Description of the Drawings

[11] FIG. 1 illustrates a conventional electrostatic discharge (ESD) protection device of an output driver stage.

[12] FIG. 2 illustrates an ESD protection device of an output driver stage according to an embodiment of the present invention.

[13] FIG. 3 illustrates an example of implementing the ESD protection device illustrated in FIG. 2.

[14] FIG. 4 illustrates another example of implementing the ESD protection device illustrated in FIG. 2.

Best Mode for Carrying Out the Invention

[15] Exemplary embodiments of the present invention will now be described in detail with reference to the accompanying drawings.

[16] FIG. 2 illustrates an electrostatic discharge (ESD) protection device of an output driver stage according to an embodiment of the present invention.

[17] An output driver stage 200 includes a p-channel metal-oxide-semiconductor (PMOS)

transistor P1 and an n-channel metal-oxide-semiconductor (NMOS) transistor N1, and the PMOS transistor P1 and the NMOS transistor N1 are selectively turned on. In FIG. 2, the PMOS transistor P1 has a source connected to a first source voltage VH, a drain connected to a node N1 connected to an output pad, and a gate applied with an output signal from an internal circuit 210. The NMOS transistor N1 has a source connected to a second source voltage VL, a drain connected to a node N1 connected to the output pad, and a gate applied with the output signal from the internal circuit 210 similarly to the PMOS transistor P1. The first and second source voltages VH and VL have different voltage levels, and in FIG. 2, the first source voltage VH has a relatively higher voltage level than the second source voltage VL. However, the opposite case can also be implemented.

[18] The ESD protection device of the output driver stage illustrated in FIG. 2 does not have conventional diodes DP and DN and a limiting resistor R1. Instead, a drain resistor, an active resistor, well resistors RN and RP, and the like may be included therein.

[19] Here, for examples, for the drain resistor, in a MOS transistor manufacturing process, according to a design rule determined in consideration of electromagnetic characteristics, a minimum distance between a contact formed on a drain region and a gate poly is needed. Accordingly, the drain resistor necessarily exists. However, in a case where the MOS transistors are manufactured according to the determined design rule, a value of resistance of the drain resistor is not that high and not that effective for the ESD protection.

[20] In a case where the distance between the contact formed on the drain region and the gate poly is increased, the drain resistor can have an increased value. In this case, referring to FIG. 2, if ESD flows into the output pad, most of the flow of ESD is consumed through the drain resistors RN and RP. Therefore, the ESD exerts no or less influence on the internal circuit 210.

[21] FIG. 3 illustrates an example of implementing the ESD protection device illustrated in FIG. 2.

[22] Referring to FIG. 3, in an active region 300, a number of contacts 302 for drain output from each of MOS transistors P1 and N1 and a number of contacts 303 for source voltage connection to each of the MOS transistors, are formed in a vertical direction. In addition, on an upper portion of the active region 300, a gate poly 301 for forming a gate of each of the MOS transistors is formed.

[23] Here, the gate poly 301 is disposed at predetermined intervals from the contacts 302 formed on a drain region and the contacts 303 formed on a source region. This applies the same concept as the aforementioned design rule. Here, an active region between the contacts 302 formed on the drain region and the gate poly 301 becomes a drain

resistor 310. A value of resistance of the drain resistor 310 is determined by the distance d1 between the contacts 302 formed on the drain region and the gate poly 301. As the distance d1 between the contacts 302 formed on the drain region and the gate poly 301 is closer to a value according to the determined design rule, the value of resistance of the drain resistor 310 decreases. However, as the distance d1 between the contacts 302 formed on the drain region and the gate poly 301 increases, the value of resistance of the drain resistor 310 increases. As the value of resistance of the drain resistor 310 increases, a more amount of ESD flowing into the output pad is consumed.

[24] Therefore, by increasing the distance d1 between the contacts 302 formed on the drain region and the gate poly 301 to be greater than the value according to the determined design rule, the ESD flowing into the output pad can be properly removed by the drain resistor 310 and prevented from flowing into the distance circuit 210, without the conventional diodes DP and DN and limiting resistor R1.

[25] Here, when the distance d1 between the contacts 302 formed on the drain region and the gate poly 301 is increased, an area of the MOS transistor is also increased. However, removing the conventional diodes DP and DN and the limiting resistor R1 is much more effective than increasing the distance d1 between the contacts 302 formed on the drain region and the gate poly 301 to be greater than the value according to the determined design rule, in terms of the chip size. Therefore, a disadvantage of increasing the area of the MOS transistor can be overcome. The distance d1 between the contacts 302 formed on the drain region and the gate poly 301 may be increased by at least 5% from the value according to the determined design rule.

[26] FIG. 4 illustrates another example of implementing the ESD protection device illustrated in FIG. 2. In FIG. 4, a more number of resistors are formed between a drain and an output pad of a MOS transistor.

[27] In an active region 400, a number of contacts 402 formed on a drain region and a number of contacts 403 formed on a source region are formed. The resistors may be formed as an active region having a relatively higher impurity concentration or a well region having a relatively lower impurity concentration. If a relatively lower resistance is required, the active region is formed as the resistor, and if a relatively higher resistance is required, the well region is formed as the resistor.

[28] Referring to FIG. 4, on the active region 410 functioning as the resistor, a number of contacts 411 relatively closer to the contacts 402 formed on the drain region and a number of contacts 412 relatively closer to the output pad are formed. Here, the contacts 411 relatively closer to the contacts 402 formed on the drain region become an equipotential by metal 421, and accordingly, the contacts 411 relatively closer to the contacts 402 formed on the drain region may be omitted.

[29] The contacts 412 relatively closer to the output pad are connected to the output pad

by metal 422. Here, in order to occupy an enough region to consume ESD in preparation for the inflow of the ESD, an overlap distance d2 of the contacts 412 relatively closer to the output pad may be increased by 5% from a value according to the determined design rule. Here, the overlap distance d2 of each of the contacts 412 relatively closer to the output pad means a distance occupied from the corresponding contact to an edge of the active region 410.

[30] In the illustrated example of FIG. 4, a portion that practically serves the resistor is a region 413 between the contacts 411 relatively closer to the drain region and the contacts 413 relatively closer to the output pad. Therefore, when ESD flows into the output pad, most of the inflow of ESD is consumed by the region 413 that practically serves the resistor in the active region. Therefore, an enough ESD protection effect can be obtained through the aforementioned manner. In this case, the distance between the contacts 402 formed on the drain region and the gate poly 401 may be determined as the value according to the determined design rule.

[31] In FIG. 2, in order to increase the ESD protection effect of the PMOS transistor P1 and the NMOS transistor N1, an ESD protection circuit 220 may further be included between the first and second source voltages VH and VL. Here, the ESD protection circuit 220 between the source voltages may be diodes connected in series, a bipolar transistor, or a combination thereof.

[32] While the present invention has been shown and described in connection with the exemplary embodiments, it will be apparent to those skilled in the art that modifications and variations can be made without departing from the spirit and scope of the invention as defined by the appended claims.

Claims

[1] An ESD (electrostatic discharge) protection device of an output driver stage, which includes a PMOS (p-channel metal-oxide-semiconductor) transistor having a source connected to a first source voltage and an NMOS (n-channel metal-oxide-semiconductor) transistor having a source connected to a second source voltage, the MOS transistors having gates applied with output signals from an internal circuit and drains connected to the output pad,
wherein a distance between contacts formed on a drain region and a gate poly of the MOS transistors is relatively greater than a value according to a predetermined design rule.

[2] The ESD protection device of claim 1, wherein the interval between the contacts formed on the drain region and the gate poly of the MOS transistors is greater than the value according to the predetermined design rule by at least 5%.

[3] An ESD protection device of an output driver stage, which includes a PMOS transistor P1 having a source connected to a first source voltage and an NMOS transistor having a source connected to a second source voltage, the MOS transistors having gates applied with output signals from an internal circuit and drains connected to the output pad,
wherein a resistor is formed between the drain and the output pad of the MOS transistors.

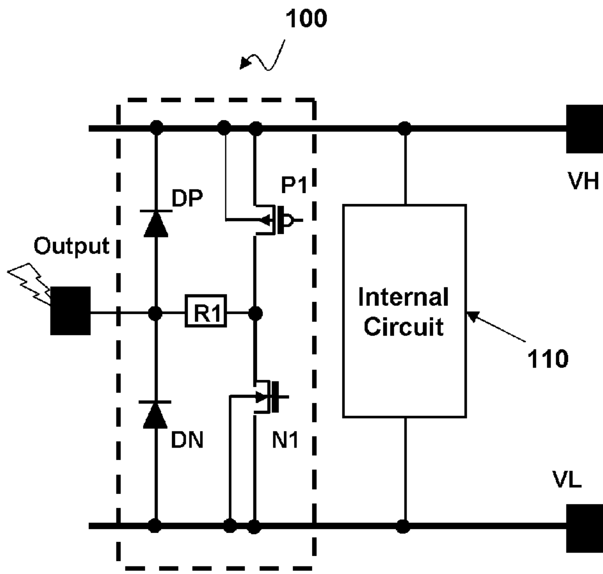
[4] The ESD protection device of claim 3, wherein the resistor is formed as an active region or a well region.

[5] The ESD protection device of claim 4, wherein an overlap distance of contacts relatively closer to the output pad from among contacts formed on the active region or the well region is relatively greater than a value according to a predetermined design rule.

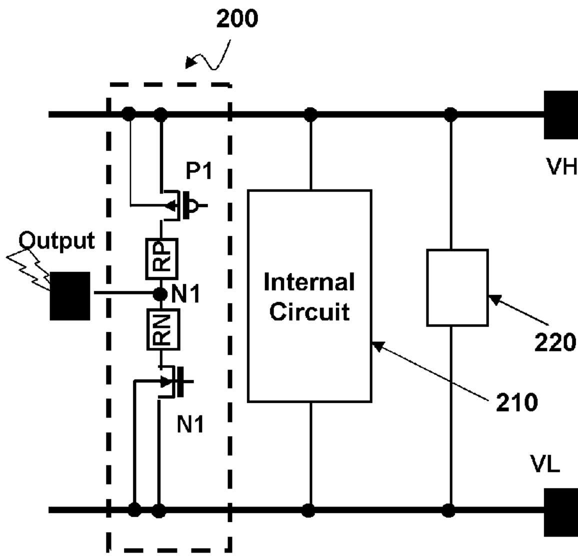
[6] The ESD protection device of claim 5, wherein the overlap distance of the contacts relatively closer to the output pad is greater than the value according to the predetermined design rule by at least 5%.

[7] The ESD protection device of any one of claims 1 to 6, further comprising an ESD protection circuit formed between the first and second source voltages.

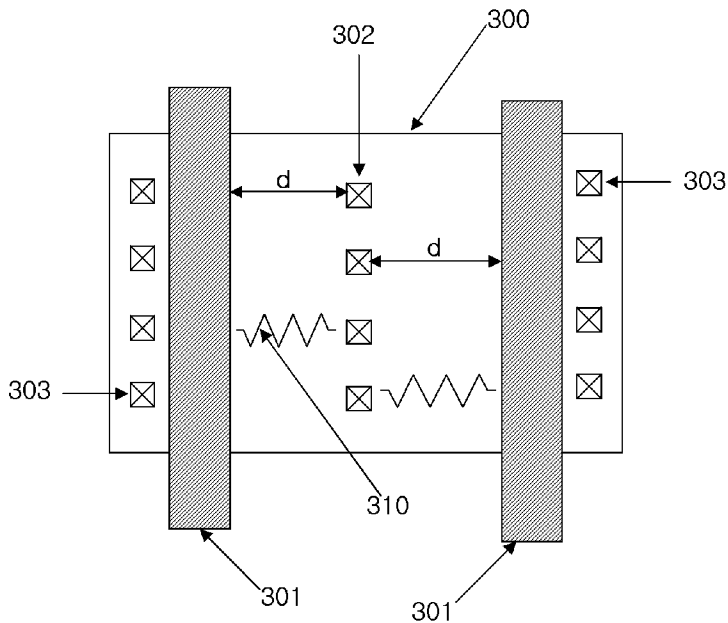
[Fig. 1]



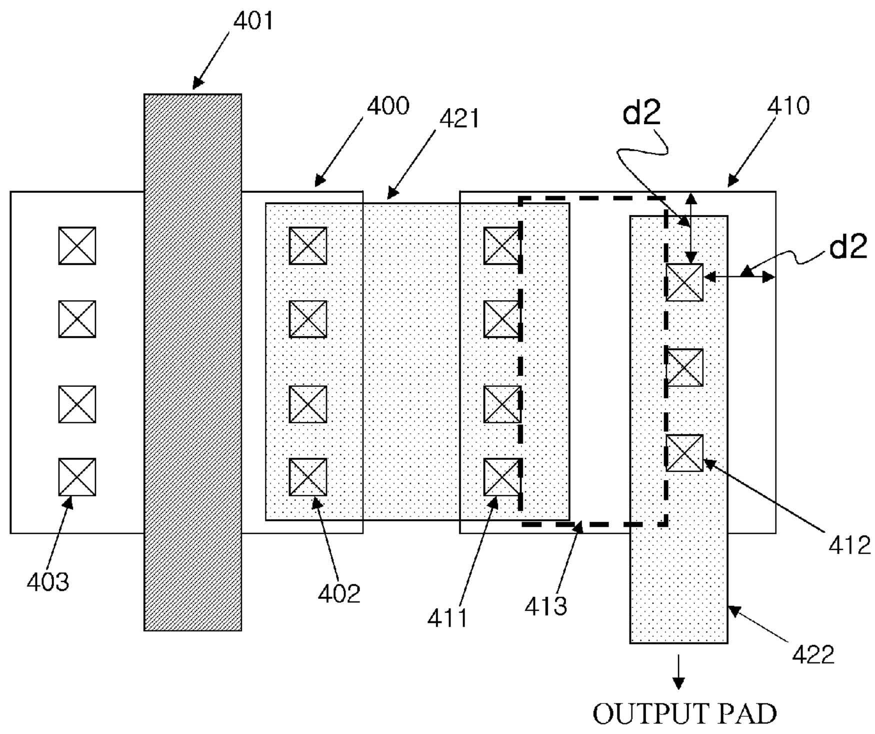
[Fig. 2]



[Fig. 3]



[Fig. 4]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2008/004410

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/60(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 8 : H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models since 1975.
Japanese utility models and applications for utility models since 1975.

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKIPASS (KIPO internal) & keywords : "semiconductor", "ESD", "PMOS", "NMOS" and "MOS"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2006-0042676 A (MAGNACHIP SEMICONDUCTOR, LTD.) 15 May 2006 See abstract and figures 6-9.	1-7
A	KR 10-2000-0003590 A (HYUNDAI ELECTRONICS IND. CO., LTD.) 15 January 2000 See claims 1-9 and figure 8.	1-7
A	JP 2003-031672 A (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.) 31 January 2003 See paragraphs [0040]-[0053] and figure 1.	1-7
A	KR 10-1998-0036986 A (HYUNDAI MICRO ELECTRONICS CO., LTD.) 5 August 1998 See abstract and figures 3a-4b.	1-7

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 OCTOBER 2008 (29.10.2008)	**29 OCTOBER 2008 (29.10.2008)**

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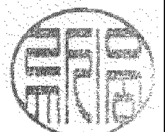

Telephone No. 82-42-481-5980

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/KR2008/004410

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