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(54) HETEROJUNCTION BIPOLAR TRANSISTOR AND METHOD OF MANUFACTURING THE SAME

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(52) **U.S. Cl.** **257/183**

(57) **ABSTRACT**

A heterojunction bipolar transistor comprises a collector layer, a base layer, and an emitter layer stacked sequentially. The base layer comprises a first base layer joined to the collector layer in an inward base area directly below the emitter layer and a second base layer joined to the collector layer in an outward base area adjacent to the inward base area. The second base layer is formed of a semiconductor with a wider energy band gap than the collector layer.

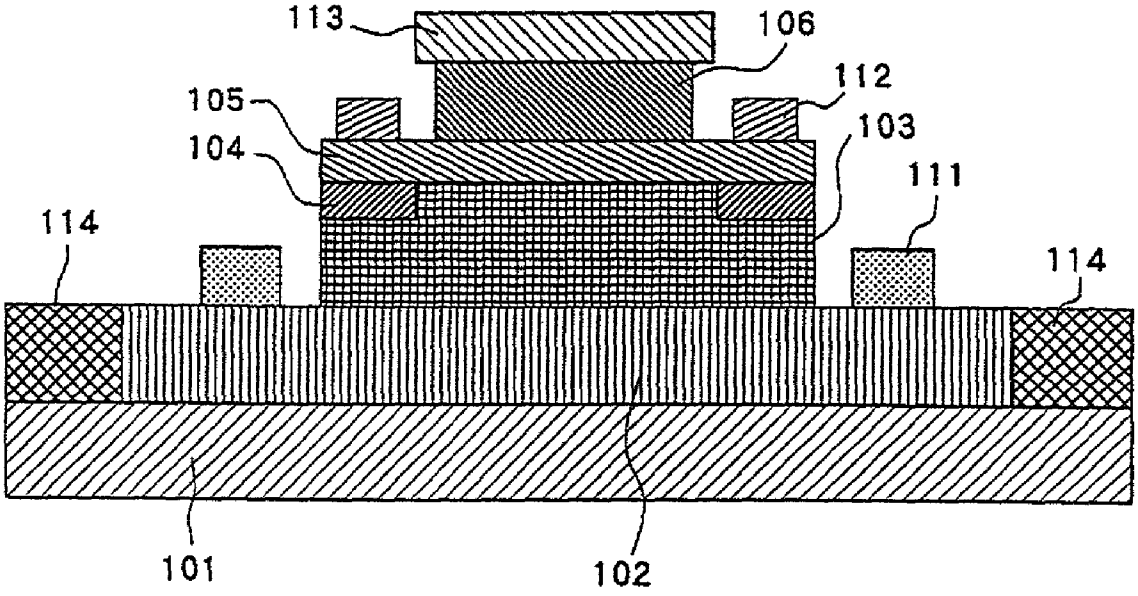


Fig. 1
(PRIOR ART)

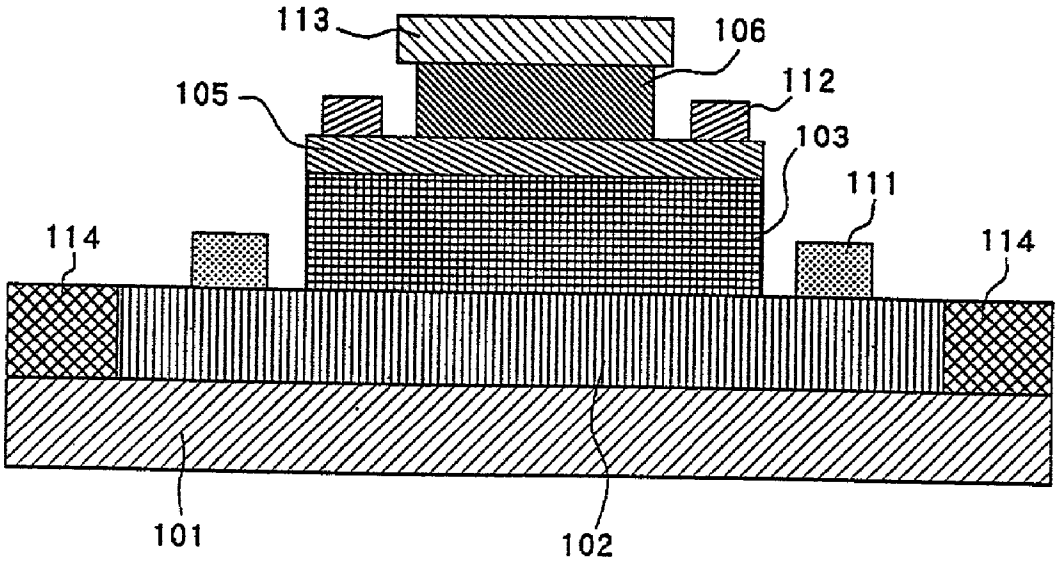


Fig. 2 a
(PRIOR ART)

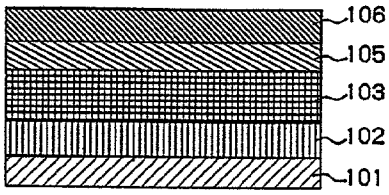


Fig. 2 b
(PRIOR ART)

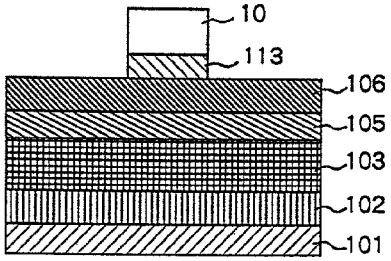


Fig. 2 c
(PRIOR ART)

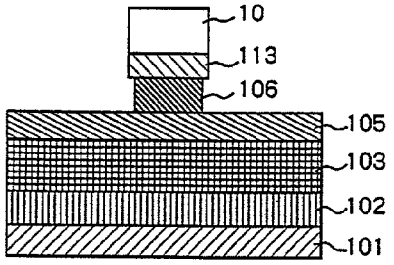


Fig. 2 d
(PRIOR ART)

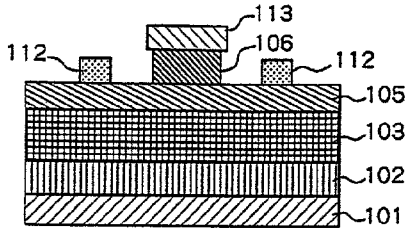
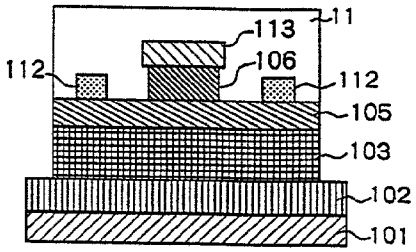


Fig. 2 e
(PRIOR ART)



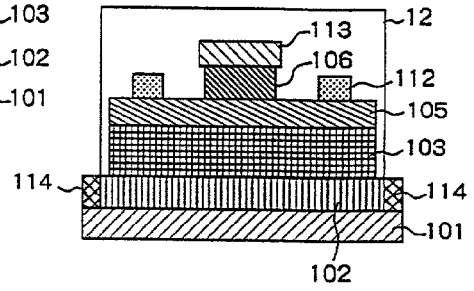


Fig. 2 f
(PRIOR ART)

Fig. 3 (PRIOR ART)

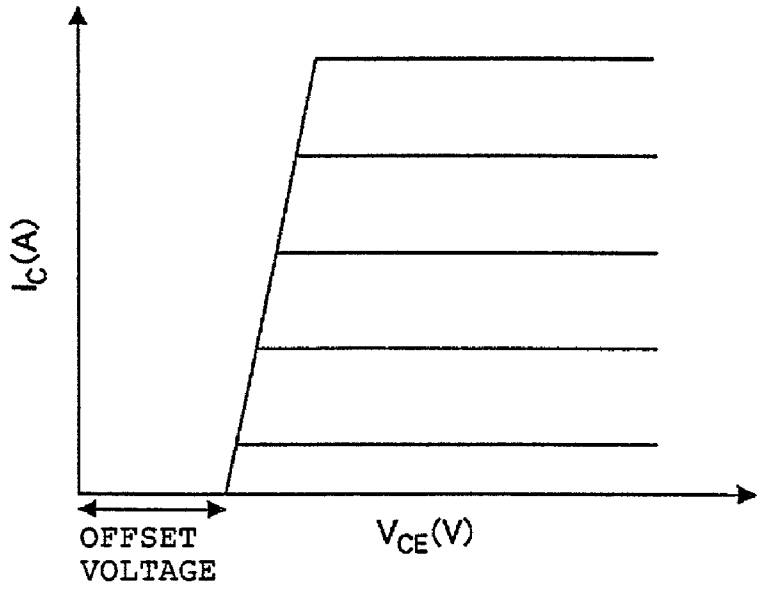


Fig. 4 (PRIOR ART)

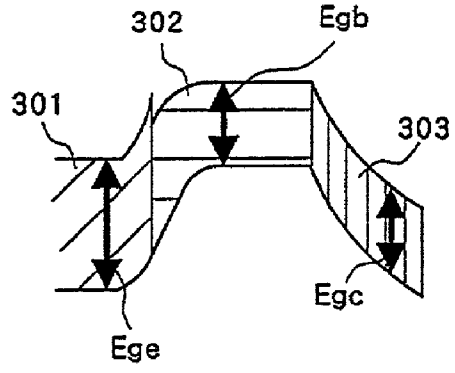


Fig. 5 (PRIOR ART)

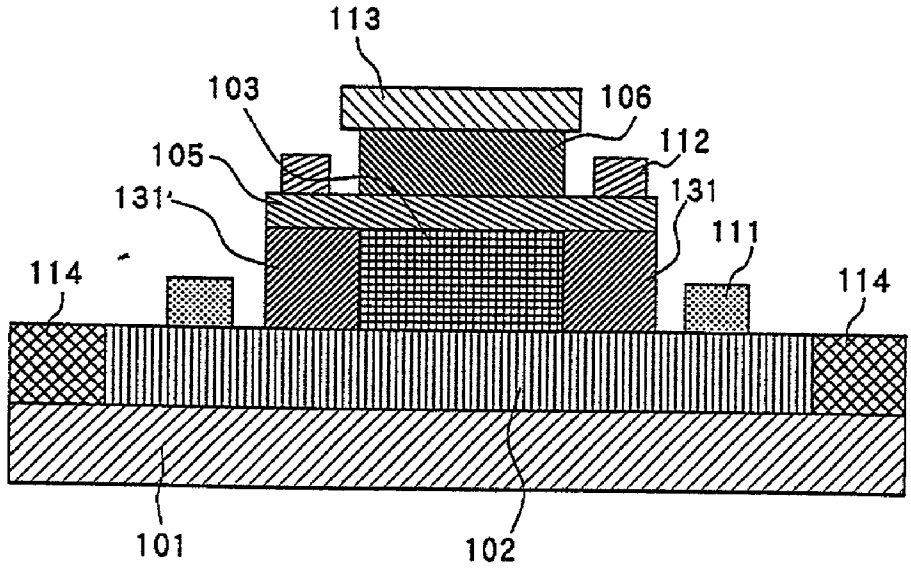


Fig. 6 (PRIOR ART)

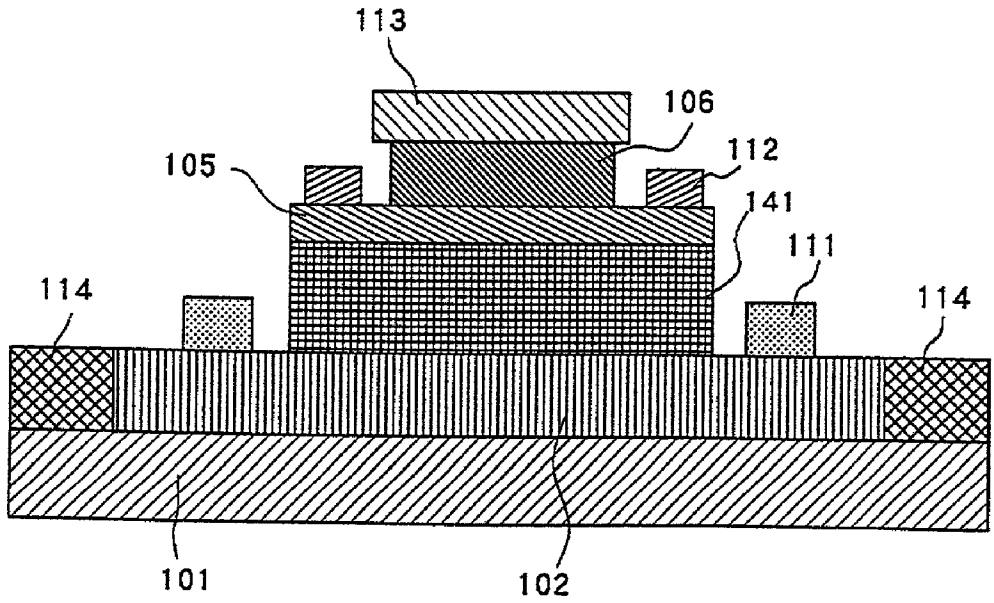
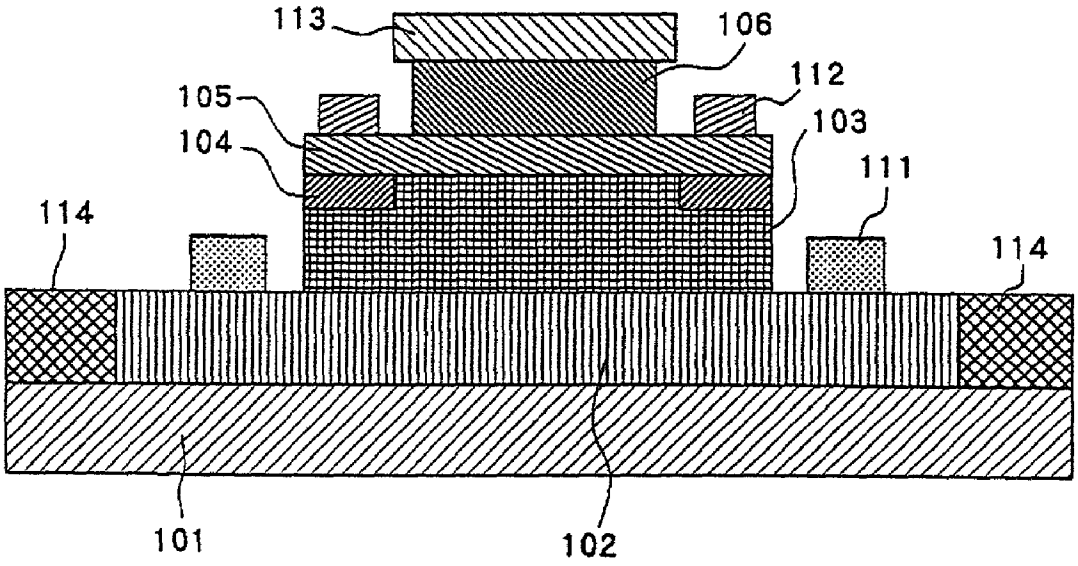


Fig. 7



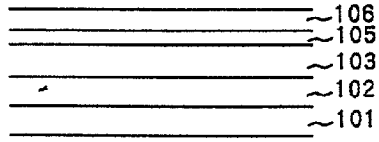


Fig. 8 a

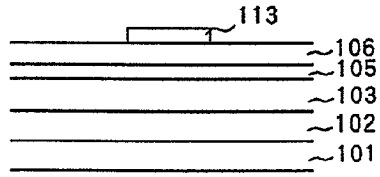


Fig. 8 b

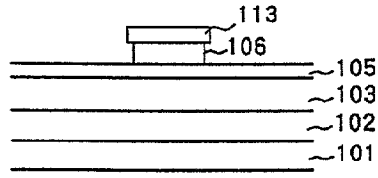


Fig. 8 c

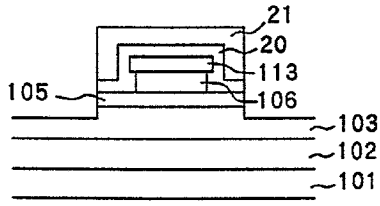


Fig. 8 d

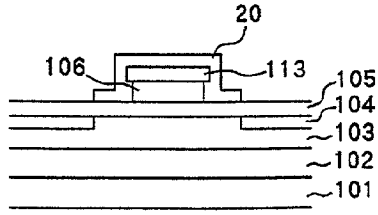


Fig. 8 e

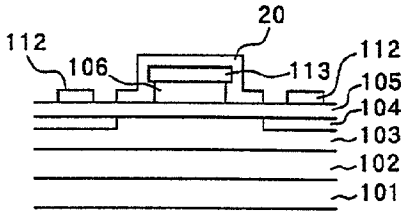


Fig. 8 f

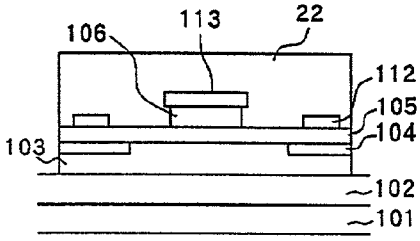


Fig. 8 g

Fig. 9

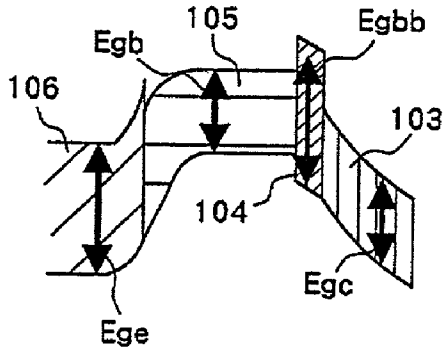
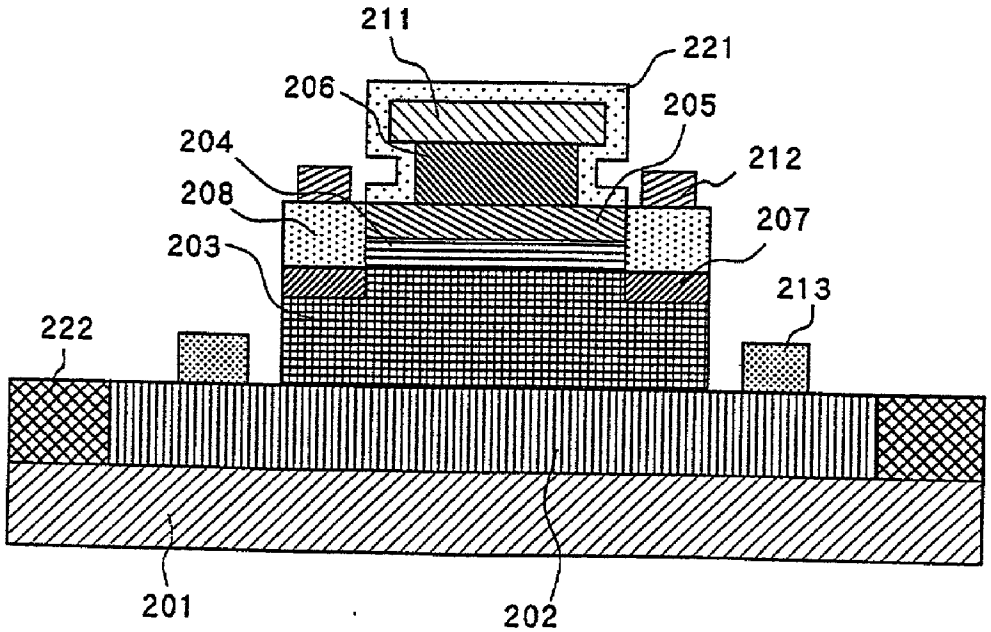

105
Egb
Egbb
106
103
104
Egc
Ege

Fig. 10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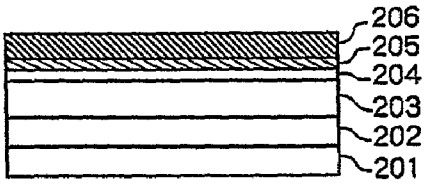


Fig. 11a

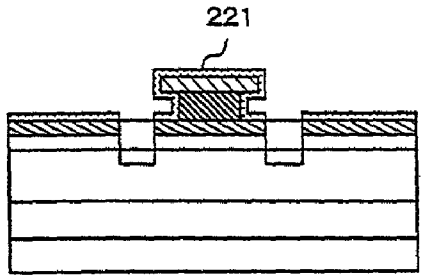


Fig. 11e

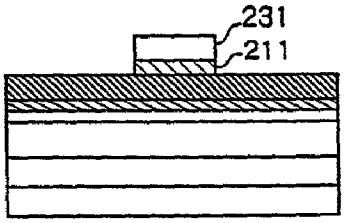


Fig. 11b

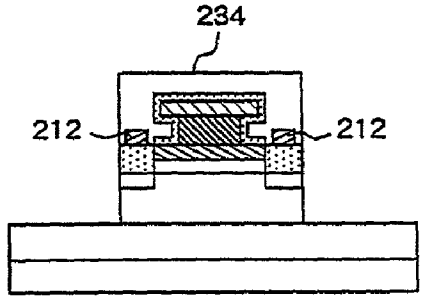


Fig. 11f

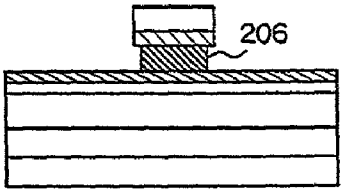


Fig. 11c

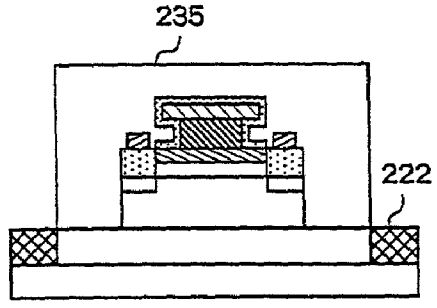


Fig. 11g

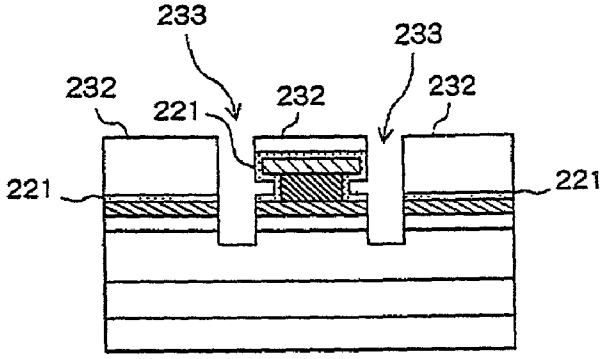


Fig. 11d

Fig. 12a

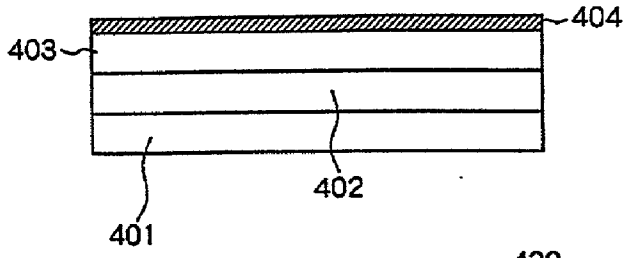


Fig. 12b

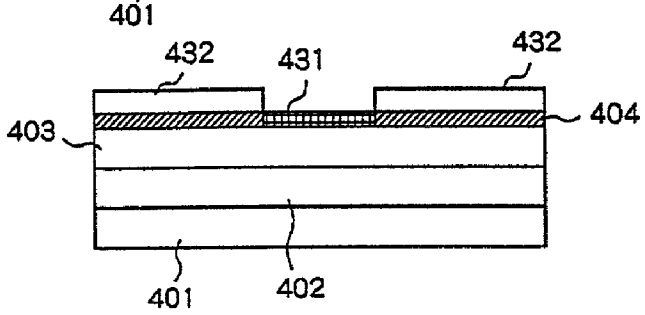


Fig 12c

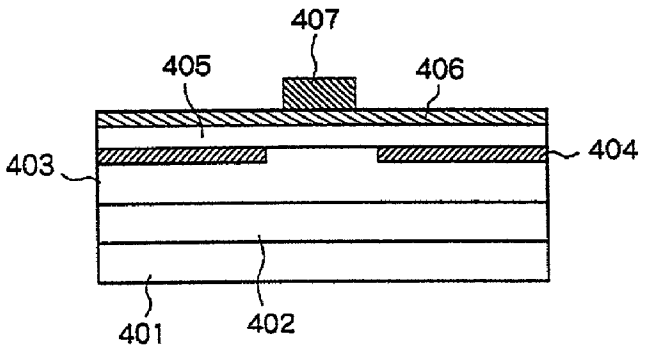


Fig. 12d

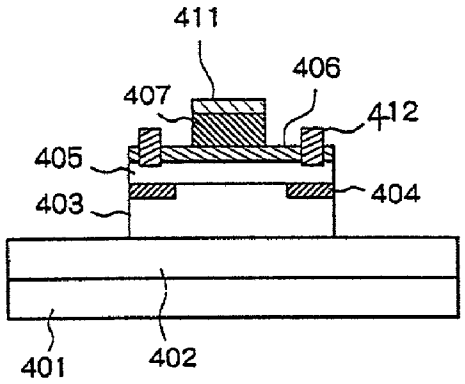
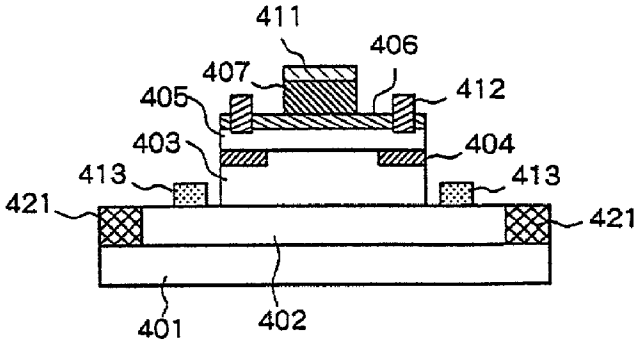


Fig. 12e



HETEROJUNCTION BIPOLAR TRANSISTOR AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

[0001] (1) Field of the Invention

[0002] The present invention relates to a heterojunction bipolar transistor comprising different kinds of joined semiconductors, and a manufacturing method thereof.

[0003] (2) Description of the Prior Art

[0004] A heterojunction bipolar transistor (HBT) is a transistor for use in compound semiconductor integrated circuits. As an exemplary device structure of the HBT, **FIG. 1** shows a structure of an npn-type HBT with its emitter on the top, and **FIGS. 2***a* to **2***f* illustrate manufacturing steps thereof.

[0005] In the first place, as shown in **FIG. 2***a,* subcollector layer **102**, collector layer **103**, base layer **105**, and emitter layer **106** are sequentially formed on insulating substrate **101** by using an epitaxial growth method or the like. Then, a metal film which is to serve as emitter electrode **113**, later described, is deposited over the entire surface thereof.

[0006] Next, as shown in **FIG. 2***b,* photoresist **10** of a predetermined pattern is formed on the metal film and used as a mask to process the metal film, thereby providing emitter electrode **113**. Then, photoresist **10** and emitter electrode **113** are used as a mask to remove emitter layer **106** until the surface of base layer **105** is exposed as shown in **FIG. 2***c.*

[0007] Subsequently, photoresist **10** is removed, and a new photoresist mask of a predetermined pattern is formed on the exposed surface of base layer **105** and used to form base electrode **112** as shown in **FIG. 2***d* through vapor deposition and lift-off procedures. Next, as shown in **FIG. 2***e,* photoresist **11** of a predetermined pattern is formed and used as a mask to remove collector layer **103** until the surface of subcollector layer **102** is exposed.

[0008] Then, photoresist **11** is removed and photoresist **12** of a predetermined pattern is formed and used as a mask to inject a predetermined impurity into subcollector layer **102** with an ion implantation technique, thereby forming insulating injection area **114** as shown in **FIG. 2***f.*

[0009] Finally, photoresist **12** is removed, a photoresist of a predetermined pattern is formed on the exposed surface of subcollector layer **102** and used as a mask to form collector electrode **111** through vapor deposition and lift-off procedures, thereby obtaining the npn-type HBT device in **FIG. 1**.

[0010] In the aforementioned npn-type HBT, since the junction area (SBC) between base layer **105** and collector layer **103** is larger than the junction area (SBE) between emitter layer **106** and base layer **105**, offset voltage occurs in a three-terminal I-V characteristic as shown in **FIG. 3**. In **FIG. 3**, the vertical axis represents collector current I_C(A) while the horizontal axis represents voltage V_{CE}(V) between the collector and the emitter. The offset voltage shown in **FIG. 3** also occurs on conditions as described below.

[0011] **FIG. 4** is a diagram showing energy bands in an HBT. In the example, difference ΔEBC (=Egc-Egb) between the band gap (Egb) of base layer **302** and the band gap (Egc) of collector layer **303** is smaller than difference ΔEBE (=Ege-Egb) between the band gap (Ege) of emitter layer **301** and the band gap (Egb) of base layer **302**. The offset voltage occurs when ΔEBC<ΔEBE as in the example.

[0012] When the aforementioned offset voltage is large, power consumption is greater in a digital IC using an HTB, or power added efficiency is lower in a power amplifier using an HBT, for example.

[0013] To avoid the problems, several device structures have been proposed for reducing the offset voltage. As an example, **FIG. 5** shows a cross-sectional structure of an HBT which achieves a reduction in offset voltage. The HBT includes collector layer insulation area **131** obtained by insulating the portion of collector layer **103** in the aforementioned HBT shown in **FIG. 1** which is joined to an outward base area (an area adjacent to an inward base area directly below the emitter layer) of base layer **105**. The provision of collector layer insulation area **131** in collector layer **103** in this manner can reduce the junction area (SBC) between base layer **105** and collector layer **103** to achieve a reduction in the offset voltage.

[0014] A structure capable of reducing the offset voltage without using ion implantation is a DHBT (Double Heterojunction Bipolar Transistor). **FIG. 6** shows a cross-sectional structure of such a DHBT. The HBT includes collector layer **141** using a semiconductor with a wide energy band gap instead of collector layer **103** in the structure of the aforementioned HBT shown in **FIG. 1**. With the structure, ΔEBE can be equal to ΔEBC to allow a reduction in the offset voltage.

[0015] The aforementioned structures of the respective HBTs capable of reducing the offset voltage, however, present problems as below.

[0016] In the structure of the HBT shown in **FIG. 5**, since collector layer insulation area **131** is formed by ion-implanting an impurity into the portion joined to the outward base area close to a device intrinsic area, it is conceivable that the impurity can be diffused to the device intrinsic area. Such diffusion of the impurity to the device intrinsic area brings about a lower current gain in an HTPT test (high temperature passage test) to contribute to reduce reliability of the device.

[0017] In the structure of the DHBT shown in **FIG. 6**, Δ EBE is equal to ΔEBC and thus ΔEBC causes carriers in operation of the device to be blocked, thereby presenting a problem of reducing collector injection efficiency.

SUMMARY OF THE INVENTION

[0018] It is an object of the present invention to provide a heterojunction bipolar transistor capable of solving the aforementioned problems, providing high reliability of a device, and reducing offset voltage without reducing collector injection efficiency, and a manufacturing method thereof.

[0019] To achieve the aforementioned object, a heterojunction bipolar transistor of the present invention comprises a collector layer, a base layer, and an emitter layer stacked sequentially, wherein the base layer comprises a first base layer joined to the collector layer in an inward base area directly below the emitter layer and a second base layer joined to the collector layer in an outward base area adjacent

to the inward base area. The second base layer is formed of a semiconductor with a wider energy band gap than the collector layer.

[0020] A method of manufacturing a heterojunction bipolar transistor comprises a first step of sequentially stacking a collector layer, a first base layer, and an emitter layer, a second step of removing the first base layer in an outward base area adjacent to an inward base area directly below the emitter layer and a portion of the collector layer directly below the outward base area, and a third step of forming an insulating film made of a predetermined material on the entire surface of the inward base area to sequentially form a second base layer made of a semiconductor with a wider energy band gap than the collector layer and the first base layer on the collector layer from which the portion has been removed in the second step through selective re-growth by using the insulating film.

[0021] Another method of manufacturing a heterojunction bipolar transistor comprises a first step of sequentially stacking a collector layer and a first base layer made of a semiconductor with a wider energy band gap than the collector, a second step of forming an insulating film made of a predetermined material on the entire surface of the first base layer and removing the first base layer in an inward base area directly below an emitter layer to be formed on the first base layer and the insulating film on the inward base area to expose a surface of the collector layer, a third step of re-growing a second collector layer on the surface of the collector layer exposed in the second step, and a fourth step of removing the insulating film and then sequentially forming a second base layer made of a predetermined material and the emitter layer made of a semiconductor with a wider energy band gap than the second base layer through re-growth.

[0022] As described above, in the present invention, since the energy band gap of the second base layer joined to the collector layer in the outward base area is wider than that of the collector layer, the second base layer suppresses current injection from the collector layer in the junction. In this case, the occurrence of offset voltage is determined by the relationship between the junction area (SBE) between the emitter layer and the first base layer and the junction area (SBC) between the first base layer and the collector layer. In this manner, in the present invention, the junction area (SBC) can be reduced by the provision of the second base layer in the outward base area. Thus, the junction area (SBE) can be substantially the same size as the junction area (SBC).

[0023] According to the present invention, the difference in band gaps between the second base layer and the collector layer joined to each other in the outward base area can be larger than the difference in band gaps between the first base layer and the emitter layer joined to each other in the inward base area. With this configuration, collector current in the outward base area is reduced.

[0024] In addition, according to the present invention, since a semiconductor of the same material system is used for the first base layer and the collector layer joined to each other in the inward device area, collector injection efficiency is not reduced due to the wide band gap in these layers.

[0025] Furthermore, according to the present invention, a material with a wide band gap is used for the second base layer in the outward base area in contact with a base electrode, thereby causing no increase in contact resistance.

[0026] As described above, according to the present invention, since ion implantation is not performed near a device intrinsic area, reduced device reliability as conventional is not found. In addition, the use of a semiconductor with a wide band gap only in the outward base area results in no reduction in collector injection efficiency.

[0027] The above and other objects, features, and advantages of the present invention will become apparent from the following description with reference to the accompanying drawings which illustrate examples of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] **FIG. 1** is a schematic cross section showing a device structure of an npn-type heterojunction bipolar transistor with its emitter on the top, which is an example of a conventional heterojunction bipolar transistor;

[0029] **FIG. 2***a* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 1**;

[0030] **FIG. 2***b* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 1**;

[0031] **FIG. 2***c* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 1**;

[0032] **FIG. 2***d* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 1**;

[0033] **FIG. 2***e* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 1**;

[0034] **FIG. 2***f* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 1**;

[0035] **FIG. 3** is a graph schematically illustrating offset voltage in a three-terminal I-V characteristic;

[0036] **FIG. 4** is a diagram showing energy bands in a conventional heterojunction bipolar transistor;

[0037] **FIG. 5** is a schematic cross section showing a structure of an exemplary conventional heterojunction bipolar transistor;

[0038] **FIG. 6** is a schematic cross section showing a structure of a DHBT which is an exemplary conventional heterojunction bipolar transistor;

[0039] **FIG. 7** is a schematic cross section showing a structure of a heterojunction bipolar transistor which is an embodiment of the present invention;

[0040] **FIG. 8***a* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 7**;

[0041] **FIG. 8***b* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 7**;

[0042] **FIG. 8***c* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 7**;

[0043] **FIG. 8***d* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 7**;

[0044] **FIG. 8***e* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 7**;

[0045] **FIG. 8***f* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 7**;

[0046] **FIG. 8***g* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 7**;

[0047] **FIG. 9** is a diagram showing the energy bands in the heterojunction bipolar transistor shown in **FIG. 7**;

[0048] **FIG. 10** is a schematic cross section showing a structure of a heterojunction bipolar transistor of a first example to which the device structure of the heterojunction bipolar transistor shown in **FIG. 7** is applied;

[0049] **FIG. 11***a* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 10**;

[0050] **FIG. 11***b* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 10**;

[0051] **FIG. 11***c* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 10**;

[0052] **FIG. 11***d* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 10**;

[0053] **FIG. 11***e* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 10**;

[0054] **FIG. 11***f* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 10**;

[0055] **FIG. 11***g* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor shown in **FIG. 10**;

[0056] **FIG. 12***a* is a cross section illustrating a step in the manufacturing procedure of a heterojunction bipolar transistor of a second example to which the device structure of the heterojunction bipolar transistor shown in **FIG. 7** is applied;

[0057] **FIG. 12***b* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor of the second example to which the device structure of the heterojunction bipolar transistor shown in **FIG. 7** is applied;

[0058] **FIG. 12***c* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor of the second example to which the device structure of the heterojunction bipolar transistor shown in **FIG. 7** is applied;

[0059] **FIG. 12***d* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor of the second example to which the device structure of the heterojunction bipolar transistor shown in **FIG. 7** is applied; and

[0060] **FIG. 12***e* is a cross section illustrating a step in the manufacturing procedure of the heterojunction bipolar transistor of the second example to which the device structure of the heterojunction bipolar transistor shown in **FIG. 7** is applied.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0061] Next, description is made for embodiments of the present invention with reference to the drawings.

[0062] **FIG. 7** shows a schematic cross-sectional structure of a heterojunction bipolar transistor (HBT) according to an embodiment of the present invention. The HBT is the same as the structure shown in **FIG. 1** except that base layer **104** is newly provided. Base layer **104** is formed of a semiconductor with a wider band gap than base layer **105**, and base layer **104** and base layer **105** constitute a base layer of two-layer structure. Base layer **105** is joined to collector layer **103** in an inward base area (corresponding to a device intrinsic area) directly below emitter layer **106**, and base layer **104** is joined to collector layer **103** in an outward base area (the area on the end of collector layer **103**) adjacent to the inward base area.

[0063] **FIGS. 8***a* to **8***g* are cross sections showing steps in the manufacturing procedure of the aforementioned HBT. In the first place, as shown in **FIG. 8***a*, subcollector layer **102**, collector layer **103**, base layer **105**, and emitter layer **106** are sequentially formed on insulating substrate **101** by using an epitaxial growth method or the like. Then, a metal film which is to serve as emitter electrode **113**, later described, is deposited over the entire surface thereof.

[0064] Next, a photoresist of a predetermined pattern is formed on the metal film and used as a mask to process the metal film through dry etching, thereby providing emitter electrode **113** as shown in **FIG. 8***b*. Emitter electrode **113** may be formed by well-known vapor deposition and lift-off procedures using a photoresist mask. After emitter electrode **113** is formed, the photoresist used as the mask is removed.

[0065] Subsequently, as shown in **FIG. 8***c*, emitter electrode **113** is used as a mask to remove emitter layer **106** until the surface of base layer **105** is exposed through wet etching or dry etching. After SiO_2 film **20** is formed over the entire surface and photoresist **21** of a predetermined pattern is formed, photoresist **21** is used as a mask to partially remove SiO_2 film **20**, base layer **105**, and collector layer **103** as shown in **FIG. 8***d*.

[0066] Next, photoresist **21** is removed, and then base layer **104** of a predetermined material is formed as shown in **FIG. 8***e* by selective regrowth and base layer **105** is formed. The selective regrowth refers to selective growth of GaAs on the surface of a GaAs film by utilizing the fact that a material such as GaAs is not formed on SiO_2.

[0067] Then, base electrode **112** is formed as shown in **FIG. 8***f* on base layer **105** through well-known vapor deposition and lift-off procedures using a photoresist mask. Next, as shown in **FIG. 8***g*, SiO_2 film **20** is removed, and photoresist **22** of a predetermined pattern is formed and used as a mask to sequentially remove base layers **105**, **104**, and collector layer **103**, thereby exposing the surface of subcollector layer **102**.

[0068] After photoresist **22** is removed, a photoresist of a predetermined pattern is formed and used as a mask to remove collector layer **103** until the surface of subcollector layer **102** is exposed. The photoresist used as the mask is removed, and a photoresist of a predetermined pattern is formed and used as a mask to form insulating injection area **114** by injecting a predetermined impurity into subcollector layer **102** with an ion implantation technique.

[0069] Finally, the photoresist used as the mask is removed, and a photoresist of a predetermined pattern is formed on the exposed surface of subcollector layer **102** and used as a mask to form collector electrode **111** through vapor deposition and lift-off procedures, thereby obtaining the npn-type HBT device in **FIG. 7**.

[0070] With the HBT device structure of the embodiment, base layer **104** with a wide band gap joined to collector layer **103** in the outward base area suppresses current injection from collector layer **103** in the junction. Thus, the occurrence of offset voltage is determined by the relationship between the junction area (SBE) between emitter layer **106** and base layer **105** and the junction area (SBC) between base layer **105** and collector layer **103**. Since the junction area (SBE) is substantially the same as the junction area (SBC) in the embodiment, the offset voltage shown in **FIG. 3** described above can be reduced.

[0071] The relationship of band gap widths among respective layers in the HBT device of the embodiment is as follows. **FIG. 9** is a diagram showing the energy bands in the HBT shown in **FIG. 7**. Difference ΔEBBC (=Egc-Egbb) between the band gap (Egbb) of base layer **104** (on the side of the outward base area) with a wide band gap joined to the area on the end of collector layer **103** and the band gap (Egc) of collector layer **103** is larger than difference ΔEBE (=Ege-Egb) between the band gap (Ege) of emitter layer **106** and the band gap (Egb) of base layer **105**. Thus, collector current is small in the outward base area, and as a result, the offset voltage is reduced.

[0072] Next, detailed description is made for the reason of the reduced offset voltage with a specific example in which the HBT device of the embodiment is applied to.

[0073] (First Example)

[0074] **FIG. 10** shows an HBT device structure of a first example to which the HBT device structure shown in **FIG. 7** is applied, and **FIGS. 11***a* to **11***g* illustrate manufacturing steps thereof.

[0075] The example employs an epitaxial wafer, as shown in **FIG. 11***a*, which has n-type subcollector layer **202** made of GaAs, n-type or non-doped collector layer **203** made of GaAs, p-type base layer **204** made of GaAs with a dopant concentration of, for example, 4×10^{19} cm^{-3}, emitter layer **205** made of InGaP, and n-type emitter cap layer **206** made of GaAs or InGaAs, sequentially laminated on semi-insulating GaAs substrate **201**.

[0076] A metal film which is to serve as emitter electrode **211** is formed over the entire surface of emitter cap layer **206** on the aforementioned epitaxial wafer, and photoresist **231** of a predetermined pattern is formed thereon. Next, as shown in **FIG. 11***b*, photoresist **231** is used as a mask to process the metal film, thereby forming emitter electrode **211**. Emitter electrode **211** is formed of, for example, WSi.

[0077] Then, as shown in **FIG. 11***c*, photoresist **231** and emitter electrode **211** are used as a mask to remove emitter cap layer **206** until the surface of emitter layer **205** is exposed. As shown in **FIG. 11***d*, after photoresist **231** is removed, insulating film **221** made of SiO_2 or SiN is deposited on the entire surface with a CVD apparatus, and photoresist **232** of a predetermined pattern is formed thereon. Photoresist **232** is used as a mask to partially remove insulating film **221**, emitter layer **205**, base layer **204**, and collector layer **203**. with the steps, opening **233** is formed.

[0078] Next, as shown in **FIG. 11***e*, after photoresist **232** is removed, a semiconductor (for example, AlGaAs, InGaP, or AlGaAsP) with a wider band gap than collector layer **203** is regrown in opening **233** on the surface of collector layer **203** at a higher concentration (for example, 2×10^{20} cm^{-3}) than base layer **204** through selective re-growth to form base layer **207**. In addition, a semiconductor of the same material as base layer **204** is re-grown on base layer **207** at a higher concentration (for example, 2×10^{20} cm^{-3}) than base layer **204** to form base layer **208**.

[0079] Then, base electrode **212** made of, for example, Pt/Ti/Pt/Au/Ti is formed on base layer **208** through well-known vapor deposition and lift-off procedures using a photoresist mask. In addition, photoresist **234** of a predetermined pattern is formed and used as a mask to sequentially remove insulating film **221**, emitter layer **205**, base layer **204**, and collector layer **203**, thereby exposing the surface of subcollector layer **202** (see **FIG. 11***f*).

[0080] Subsequently, as shown in **FIG. 11***g*, after photoresist **234** is removed, photoresist **235** of a predetermined pattern is formed and used as a mask to form interelement isolation area **222** by ion-implanting a predetermined impurity from the exposed surface of subcollector layer **202**.

[0081] Finally, after photoresist **235** is removed, collector electrode **213** made of, for example, AuGe/Ni/Au is formed on subcollector layer **202** through well-known vapor deposition and lift-off procedures using a photoresist to obtain the HBT device shown in **FIG. 10**.

[0082] In the HBT device of the embodiment configured as described above, the aforementioned offset voltage in the three-terminal I-V characteristic in **FIG. 3** can also be reduced. Detailed description is hereinafter made for the reason of the reduced offset voltage.

[0083] As described in the aforementioned Prior Art, the offset voltage occurs in either of the following two conditions in an npn-type HBT device with its emitter on the top:

[0084] (1) SBE<SBC

[0085] (2) ΔEBC<ΔEBE

[0086] In the HBT device of the example, like the state of the energy bands in **FIG. 9** described above, difference ΔEBBC (=Egc-Egbb) between the band gap (Egc) of col-

lector layer **203** and the band gap (Egbb) of base layer **207** (on the side of the outward base area) with a wide band gap joined to the area on the end of collector layer **203** is larger than difference ΔEBE (=Ege-Egb) between the band gap (Ege) of emitter layer **205** and the band gap (Egb) of base layer **204**. Thus, collector current is reduced in the outward base area, and as a result, the offset voltage is reduced.

[**0087**] Since the semiconductor of the same material is used for base layer **204** corresponding to an intrinsic area and collector layer **203**, no reduction occurs in collector injection efficiency due to the wide band gap.

[**0088**] In addition, a material with a wide band gap is not used for base layer **208** in the outward base area in contact with base electrode **212**, thereby causing no increase in contact resistance.

[**0089**] Since the base layers (**207**, **208**) in the outward base area have great thicknesses and impurity concentrations higher than base layer **204** in the device intrinsic area, sheet resistance of the base layers in the outward base area can be reduced without reducing current gain to produce the effect of improved high-frequency characteristics.

[**0090**] With the aforementioned effects, lower power consumption can be achieved when the HBT of the example is applied to a digital IC, and power added efficiency can be enhanced when it is applied to a power amplifier.

[**0091**] (Second Example)

[**0092**] The base layers with a wide band gap in the outward base area are formed through re-growth in the aforementioned first example. On the other hand, in a second example, base layers with a wide band gap are provided in forming an epitaxial layer.

[**0093**] **FIGS. 12***a* to **12***e* illustrate manufacturing steps of an HBT device structure of the second example to which the HBT device structure shown in **FIG. 7** is applied.

[**0094**] The second example employs an epitaxial wafer as shown in **FIG. 12***a* which comprises semi-insulating GaAs substrate **401**, n-type subcollector layer **402** made of GaAs, n-type or non-doped collector layer **403** made of GaAs, base layer **404** made of a semiconductor with a wider band gap than collector layer **403**, for example, AlGaAs, InGaP, or AlGaAsP, with a dopant concentration of, for example, 2×10^{20} cm^{-3}.

[**0095**] As shown in **FIG. 12***b*, after insulating film **432** made of SiO_2 or SiN is deposited on the entire surface of base layer **404** of the aforementioned epitaxial wafer using a CVD apparatus, the insulating film is opened in an intrinsic area, and collector layer **431** with the same material and same concentration as collector layer **403** is formed in the opening through re-growth.

[**0096**] Next, as shown in **FIG. 12***c*, after insulating film is removed the entire surface, p-type base layer **405** made of GaAs, n-type emitter layer **406** made of a semiconductor with a wider band gap than base layer **405**, for example InGaP or AlGaAs, and n-type emitter cap layer **407** made of GaAs or InGaAs are sequentially formed through re-growth.

[**0097**] Then, as shown in **FIG. 12***d*, emitter electrode **411** is formed of, for example WSi, and base electrode **412** is formed of, for example Pt/Ti/Pt/Au/Ti. Contact is established to base layer **405** through sintering from above emitter **406**.

[**0098**] Finally, as shown in **FIG. 12***e*, collector electrode **413** is formed of, for example AuGe/Ni/Au, and then interelement isolation area **421** is formed with an ion implantation technique.

[**0099**] The HBT of the example also produces effects similar to those of the HBT of the aforementioned first example. Lower power consumption can be achieved when the HBT is applied to a digital IC, and power added efficiency can be enhanced when it is applied to a power amplifier.

[**0100**] As described above, according to the present invention, since the junction area (SBE) between the emitter layer and the base layer can be substantially equal to the junction area (SBC) between the base layer and the collector layer, the offset voltage can be reduced.

[**0101**] In addition, according to the present invention, an HBT can be provided with high device reliability since the collector injection efficiency is not reduced and the ion implantation is not performed near the device intrinsic area.

[**0102**] While preferred embodiments of the present invention have been described using specific terms, such description is for illustrative purposes only, and it is to be understood that changes and variations may be made without departing from the spirit or scope of the following claims.

What is claimed is:

1. A heterojunction bipolar transistor comprising a collector layer, a base layer, and an emitter layer sequentially stacked, wherein said base layer includes a first base layer joined to said collector layer in an inward base area directly below said emitter layer and a second base layer joined to said collector in an outward base area adjacent to said inward base area, said second base layer being formed of a semiconductor with an energy band gap wider than said collector layer.

2. The heterojunction bipolar transistor according to claim 1, wherein the difference in energy band gap width between said second base layer and said collector layer is larger than the difference in energy band gap width between said emitter layer and said first base layer.

3. The heterojunction bipolar transistor according to claim 1, wherein said first base layer and said collector layer are formed of a semiconductor of the same material system.

4. The heterojunction bipolar transistor according to claim 1, wherein said base layer has a two-layer structure including said first and second base layers in said outward base area and said first base layer is provided with a base electrode thereon.

5. A method of manufacturing a heterojunction bipolar transistor comprising:

a first step of sequentially stacking a collector layer, a first base layer, and an emitter layer;

a second step of removing said first base layer in an outward base area adjacent to an inward base area directly below said emitter layer and a portion of said collector layer directly below said outward base area; and

a third step of forming an insulating film made of a predetermined material on the entire surface of said inward base area to sequentially form a second base layer made of a semiconductor with a wider energy band gap than said collector layer and said first base layer on said collector layer from which said portion has been removed in said second step through selective re-growth by using said insulating film.

6. A method of manufacturing a heterojunction bipolar transistor comprising:

a first step of sequentially stacking a collector layer and a first base layer made of a semiconductor with a wider energy band gap than said collector;

a second step of forming an insulating film made of a predetermined material on the entire surface of said first base layer and removing said first base layer in an inward base area directly below an emitter layer to be formed on said first base layer and said insulating film on said inward base area to expose a surface of said collector layer;

a third step of forming a second collector layer on the surface of said collector layer exposed in said second step through re-growth; and

a fourth step of removing said insulating film and then sequentially forming a second base layer made of a predetermined material and said emitter layer made of a semiconductor with a wider energy band gap than said second base layer through re-growth.

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