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LI et al.

(54) **SEMICONDUCTOR DEVICE WITH DOPED REGION BETWEEN GATE AND DRAIN**

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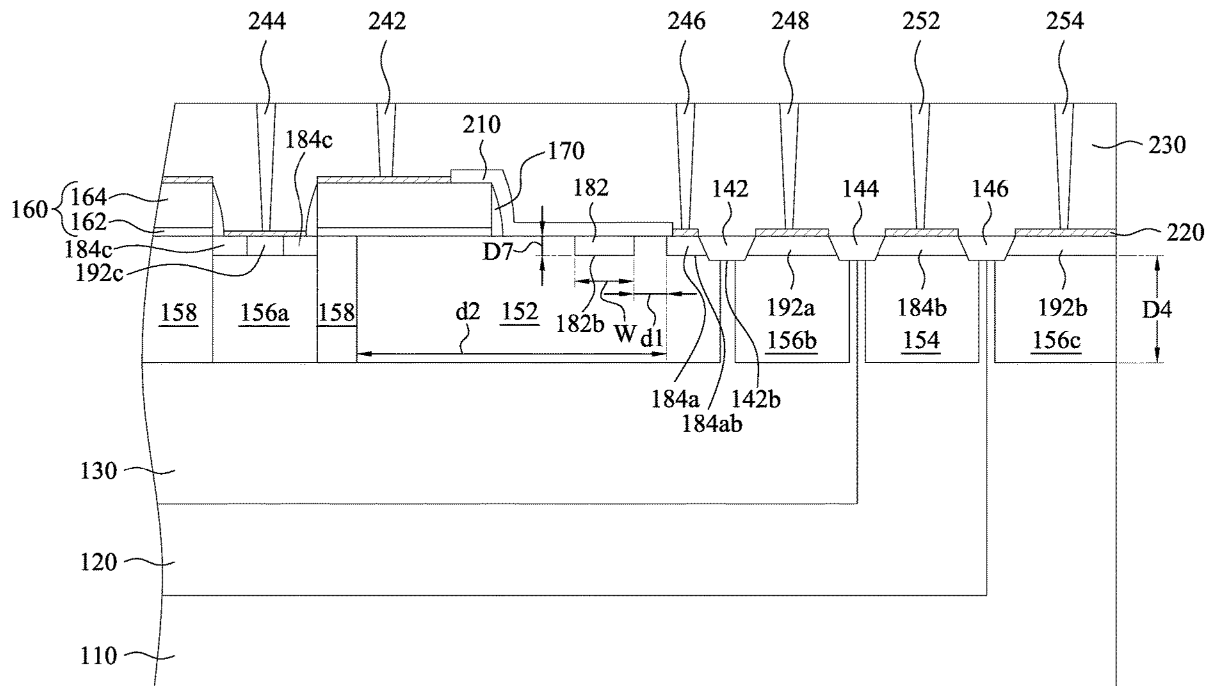
(57) **ABSTRACT**

A semiconductor device includes a gate structure, a drift region, a source region, a drain region, a first doped region, and a second doped region. The gate structure is over a semiconductor substrate. The drift region is in the semiconductor substrate and laterally extends past a first side of the gate structure. The source region is in the semiconductor substrate and adjacent a second side of the gate structure opposite the first side. The drain region is in the drift region. The first doped region is in the drift region and between the drain region and the gate structure. The second doped region is within the drift region. The second doped region forms a P-N junction with the first doped region at a bottom surface of the first doped region.



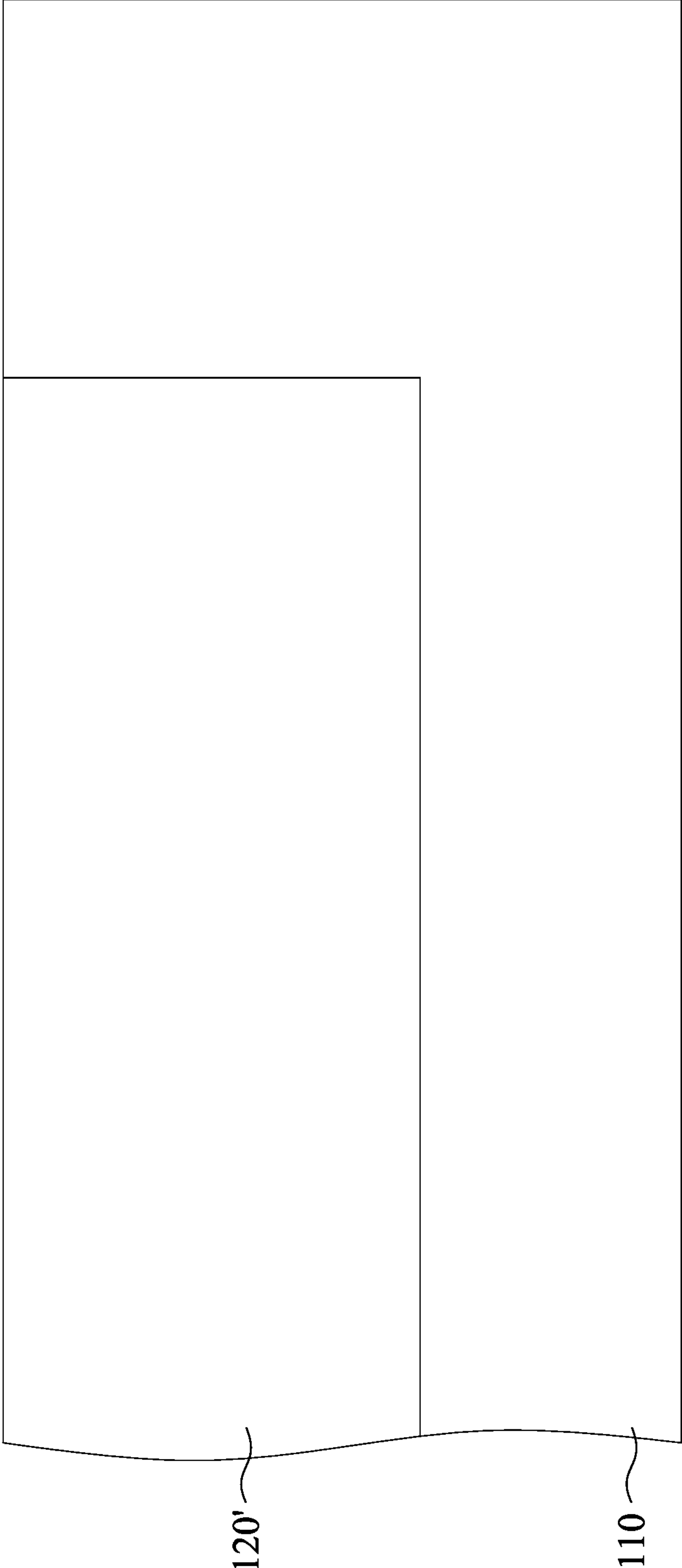


Fig. 1A

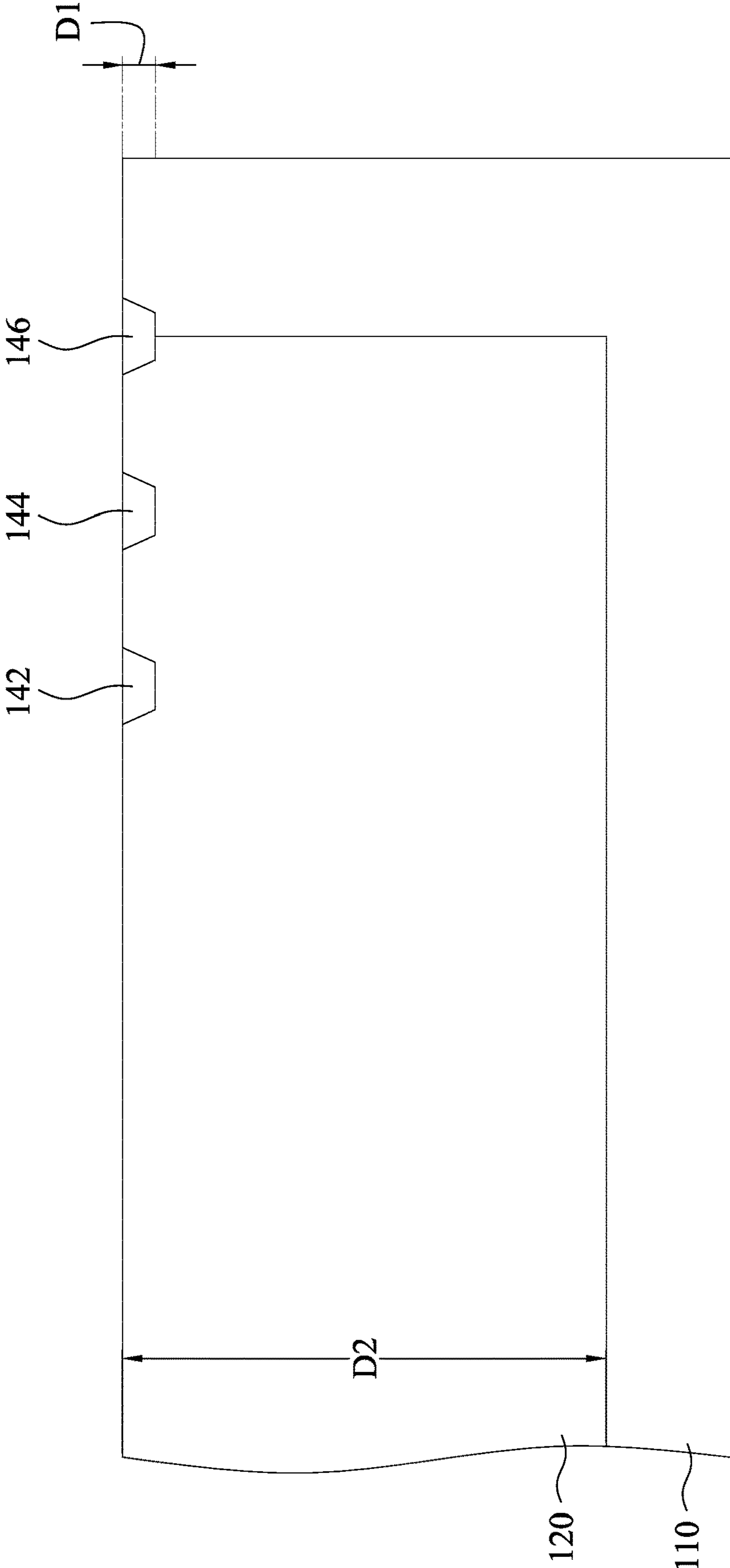


Fig. 1B

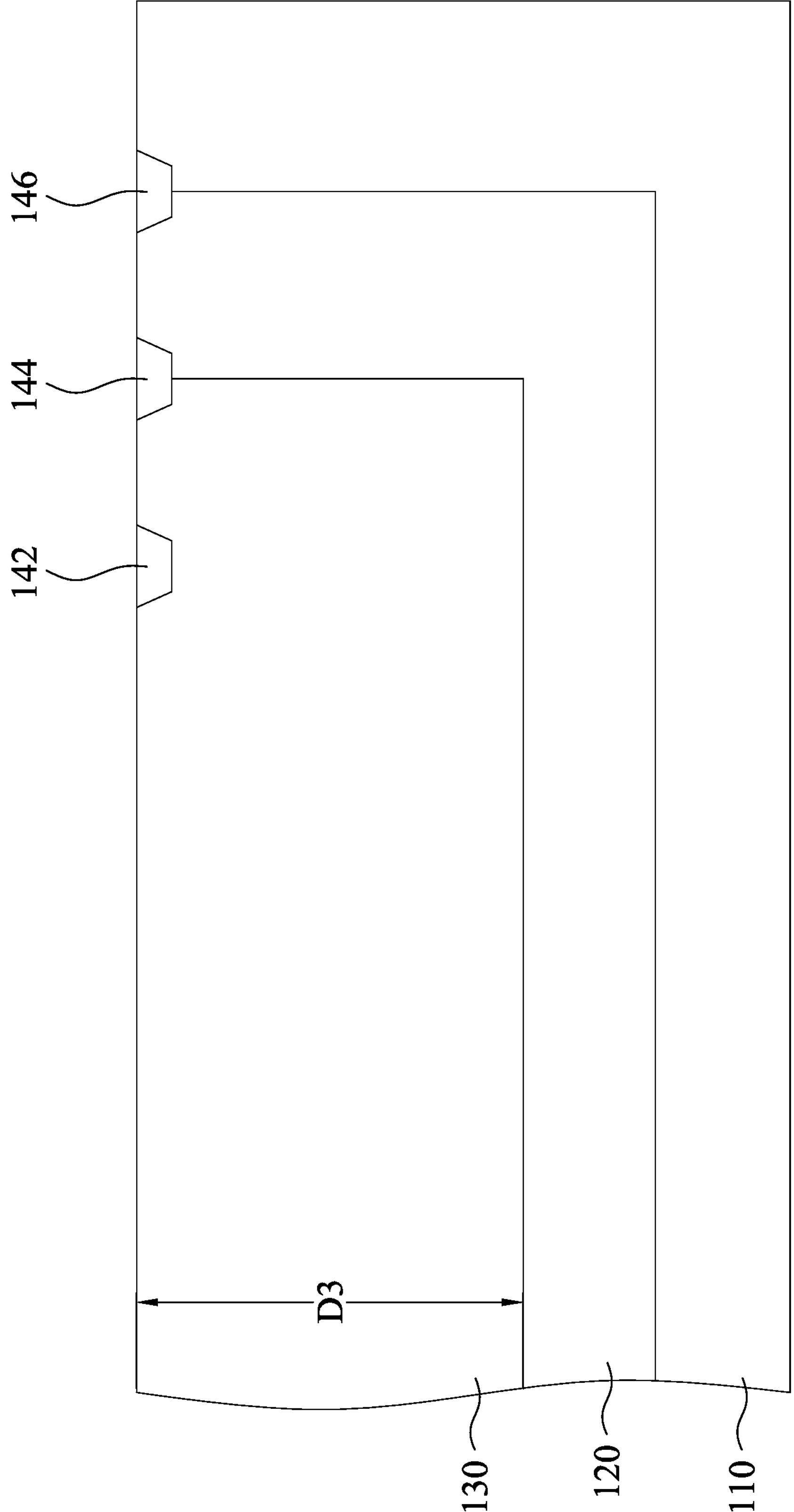


Fig. 1C

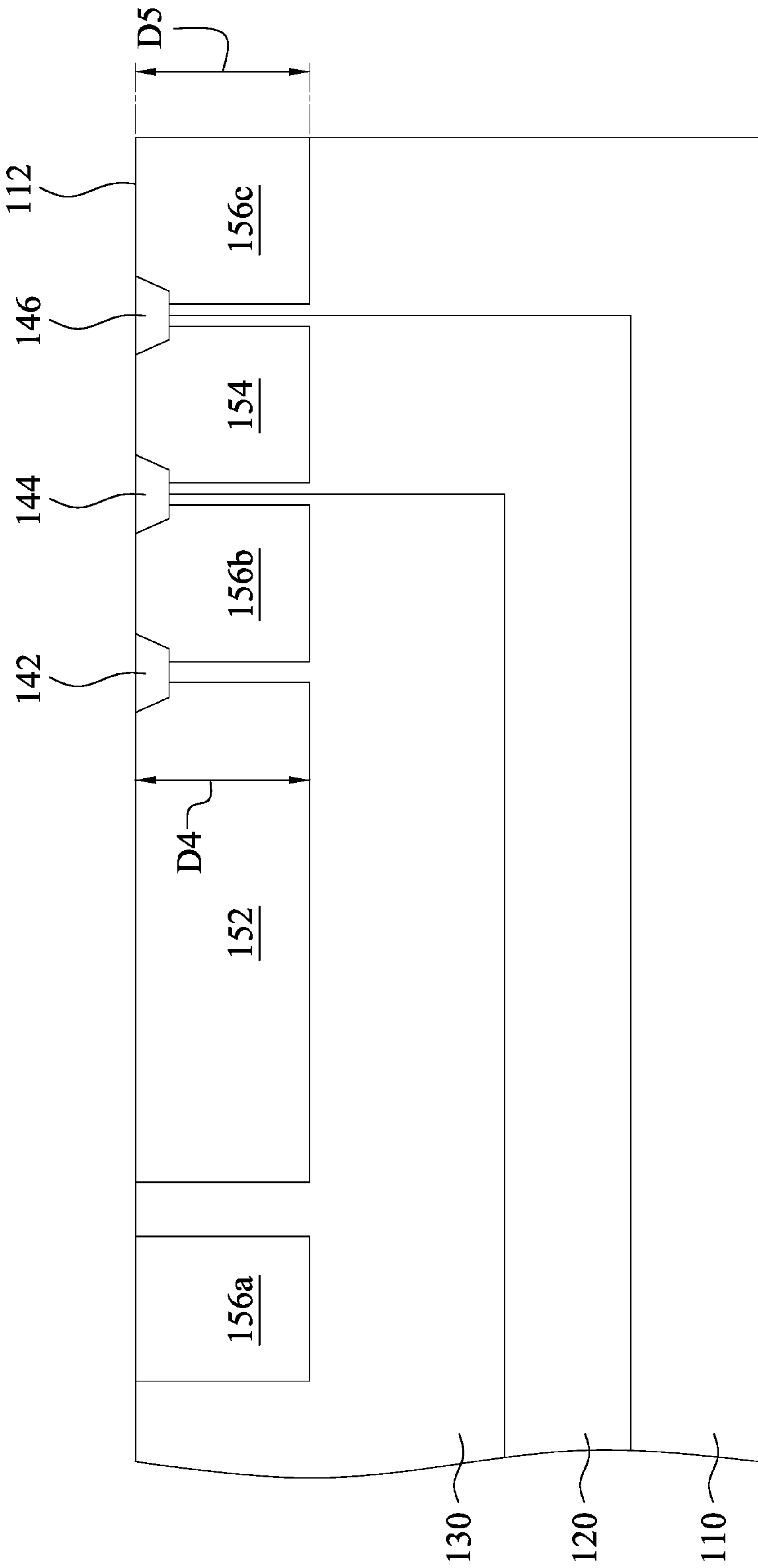


Fig. 1D

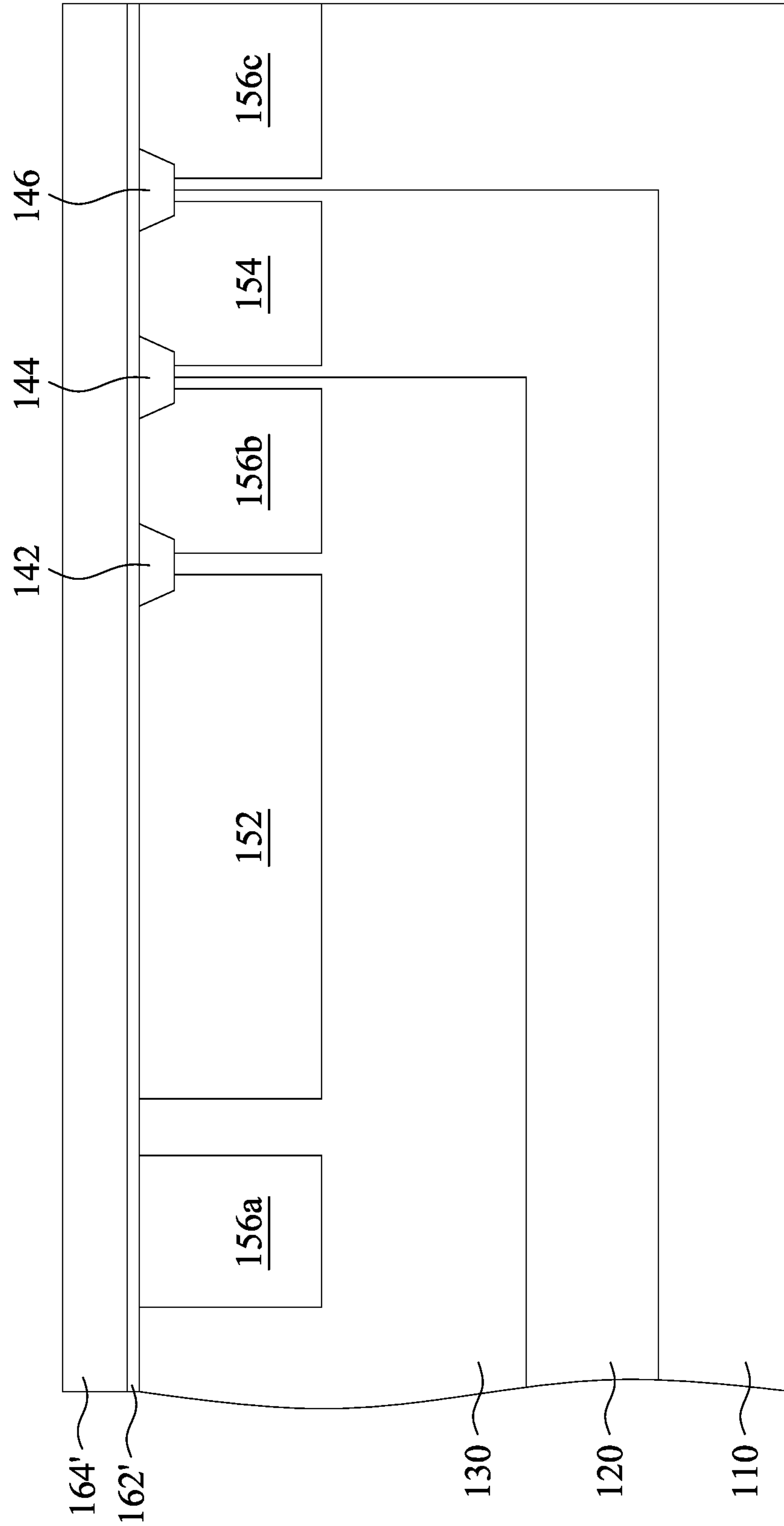


Fig. 1E

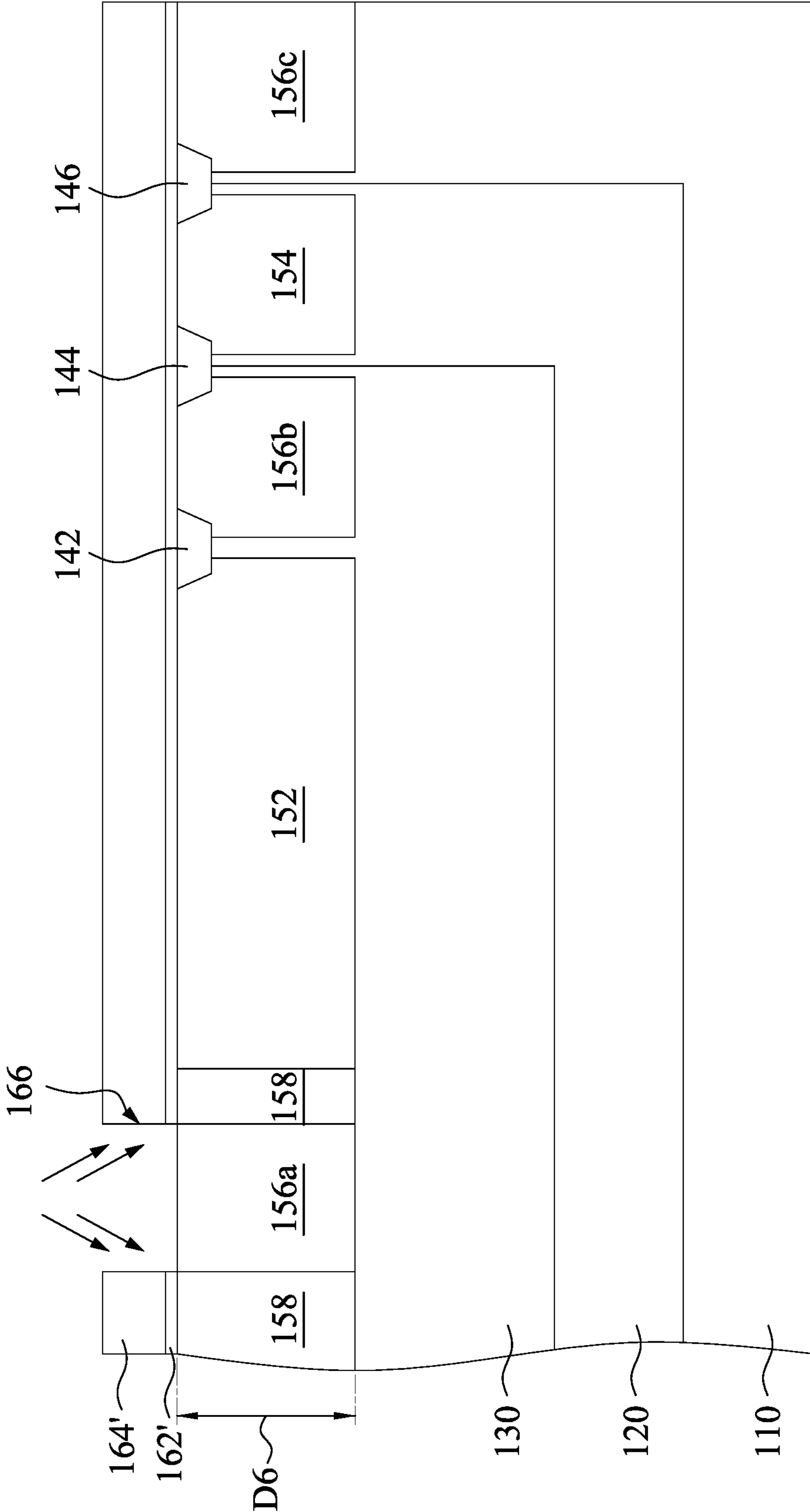


Fig. 1F

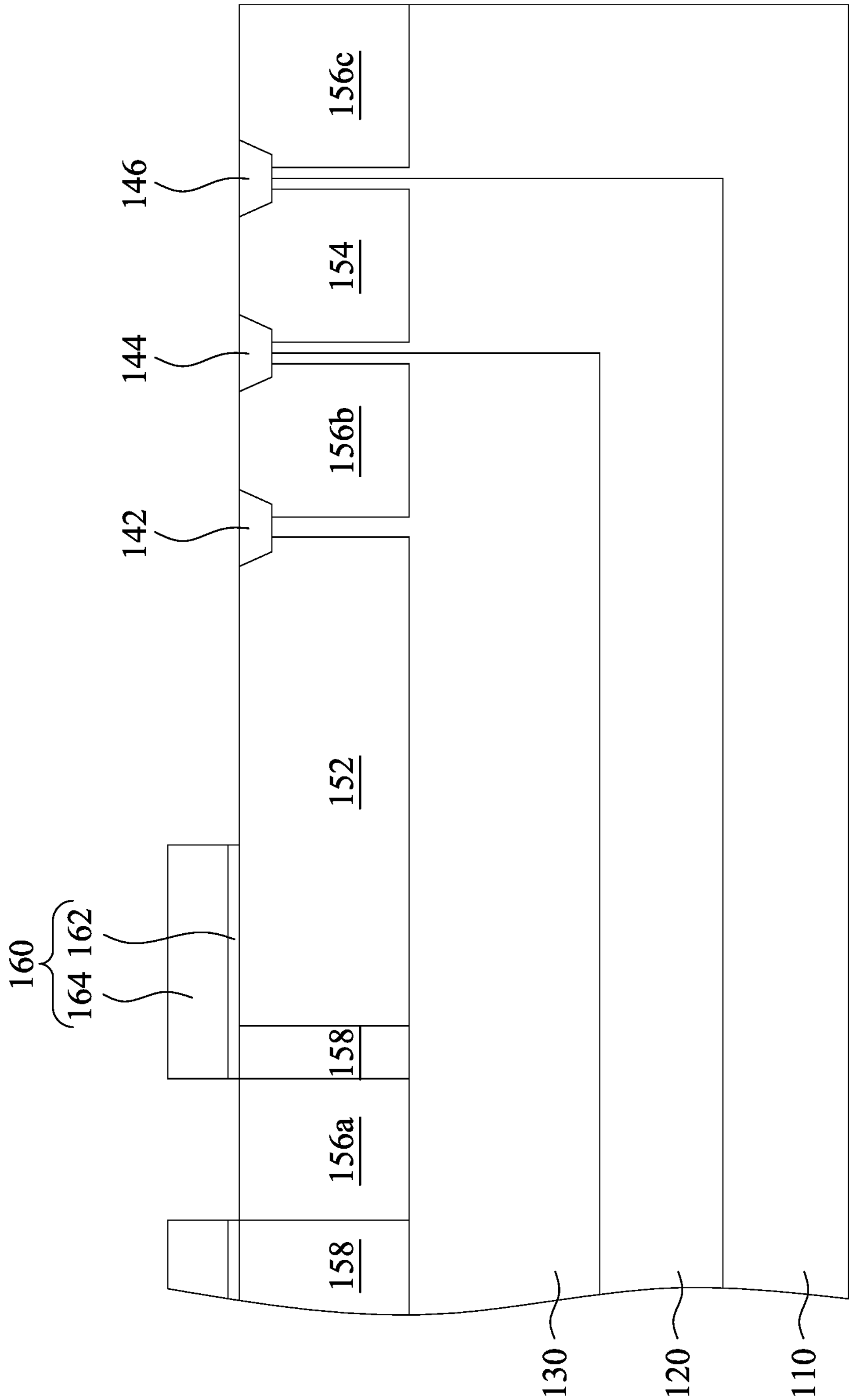


Fig. 1G

Fig. 1H

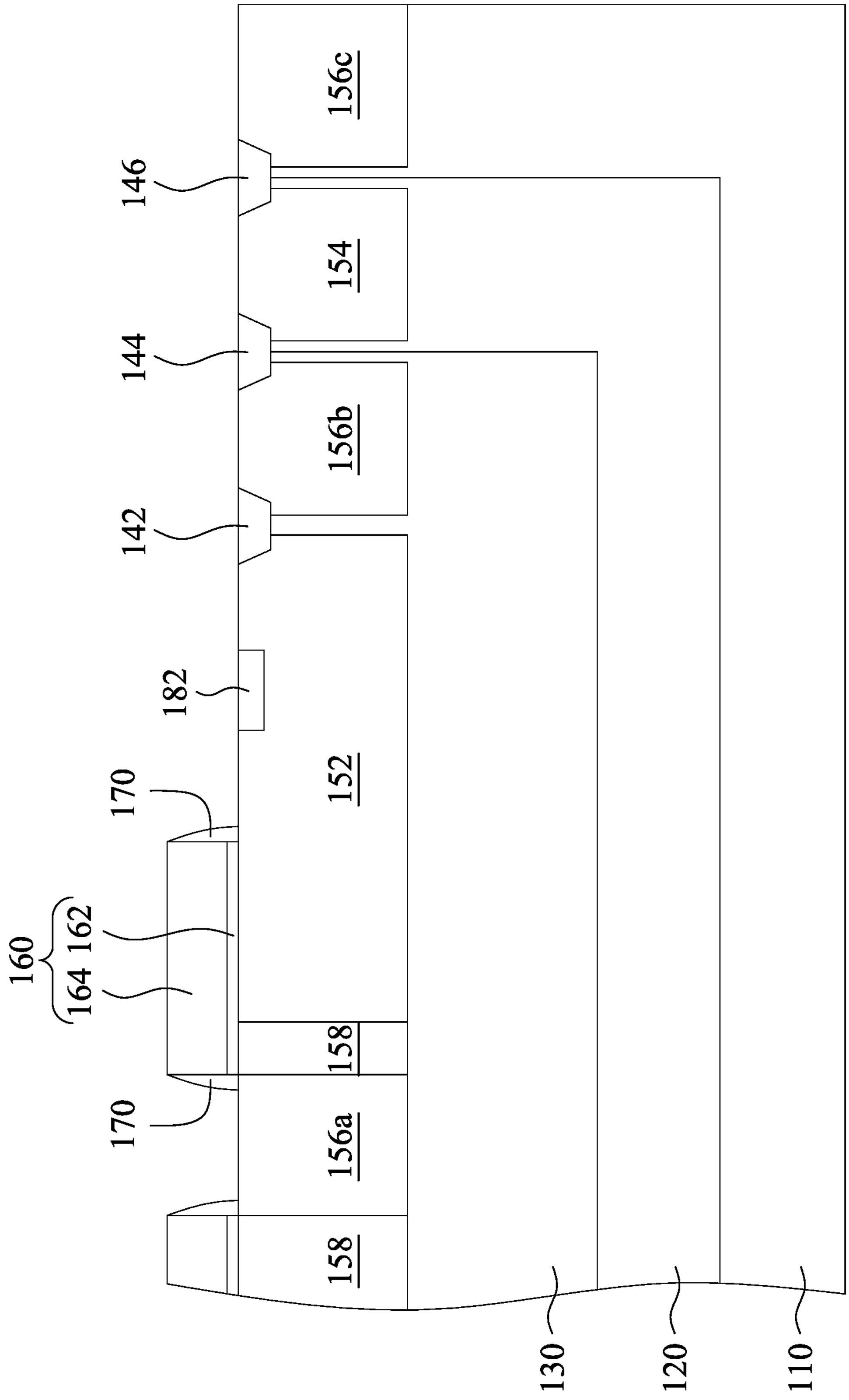


Fig. 1I

Fig. 1J

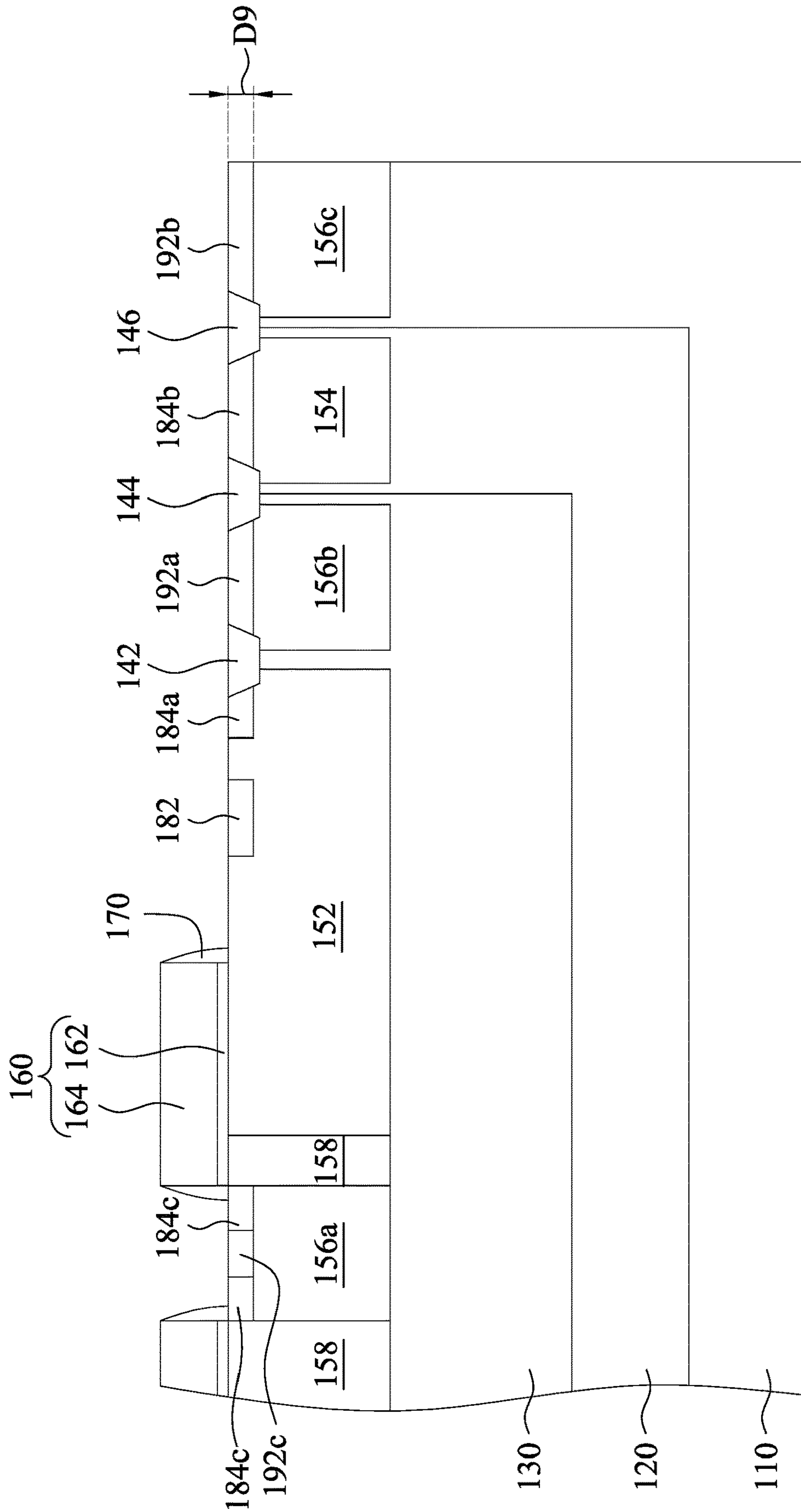


Fig. 1K

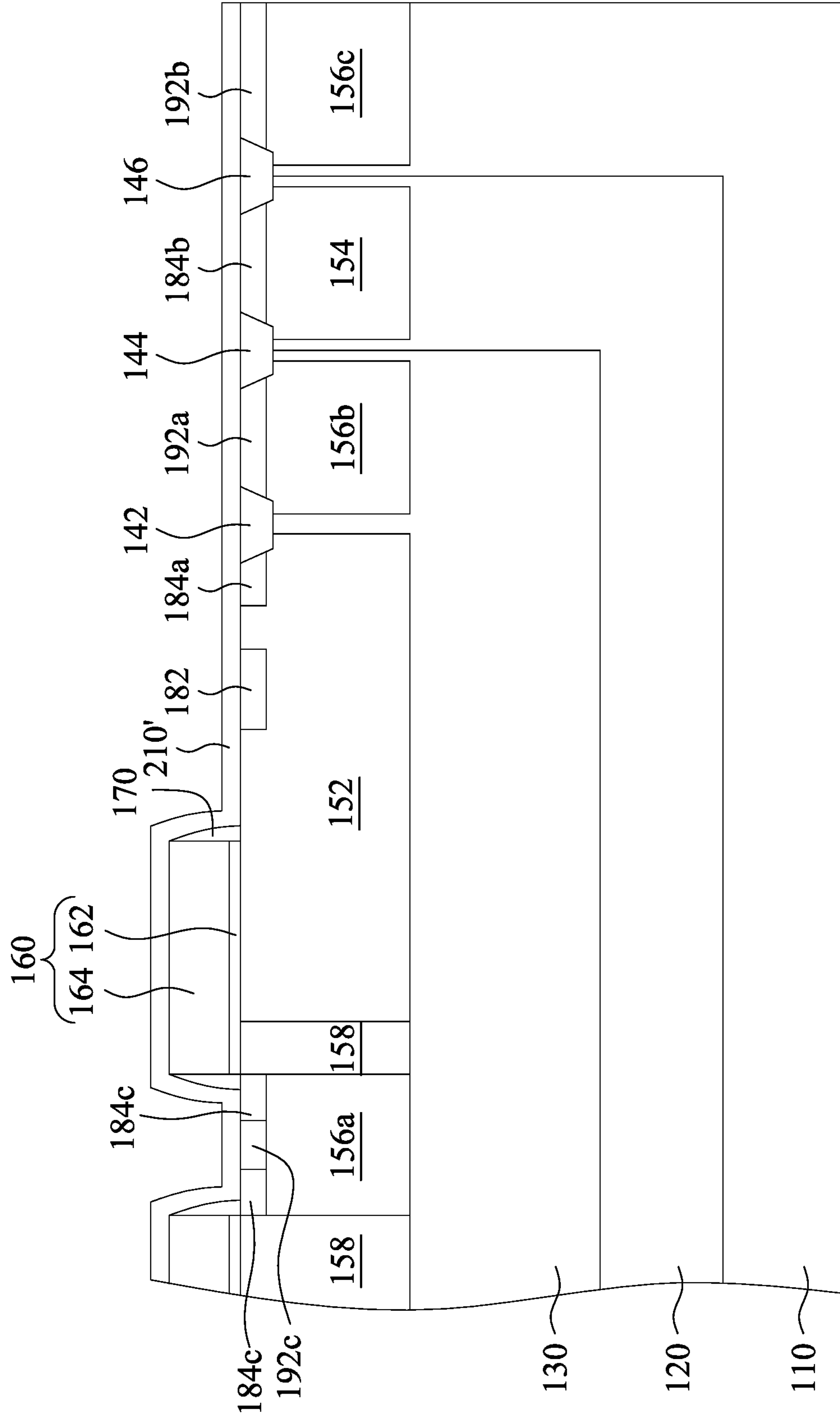


Fig. 1L

192b
146
184b
144
192a
142
184a
182
210
170
160
164
162
184c
184c
156c
154
156b
152
158
156a
158
192c
130
120
110

Fig. 1M

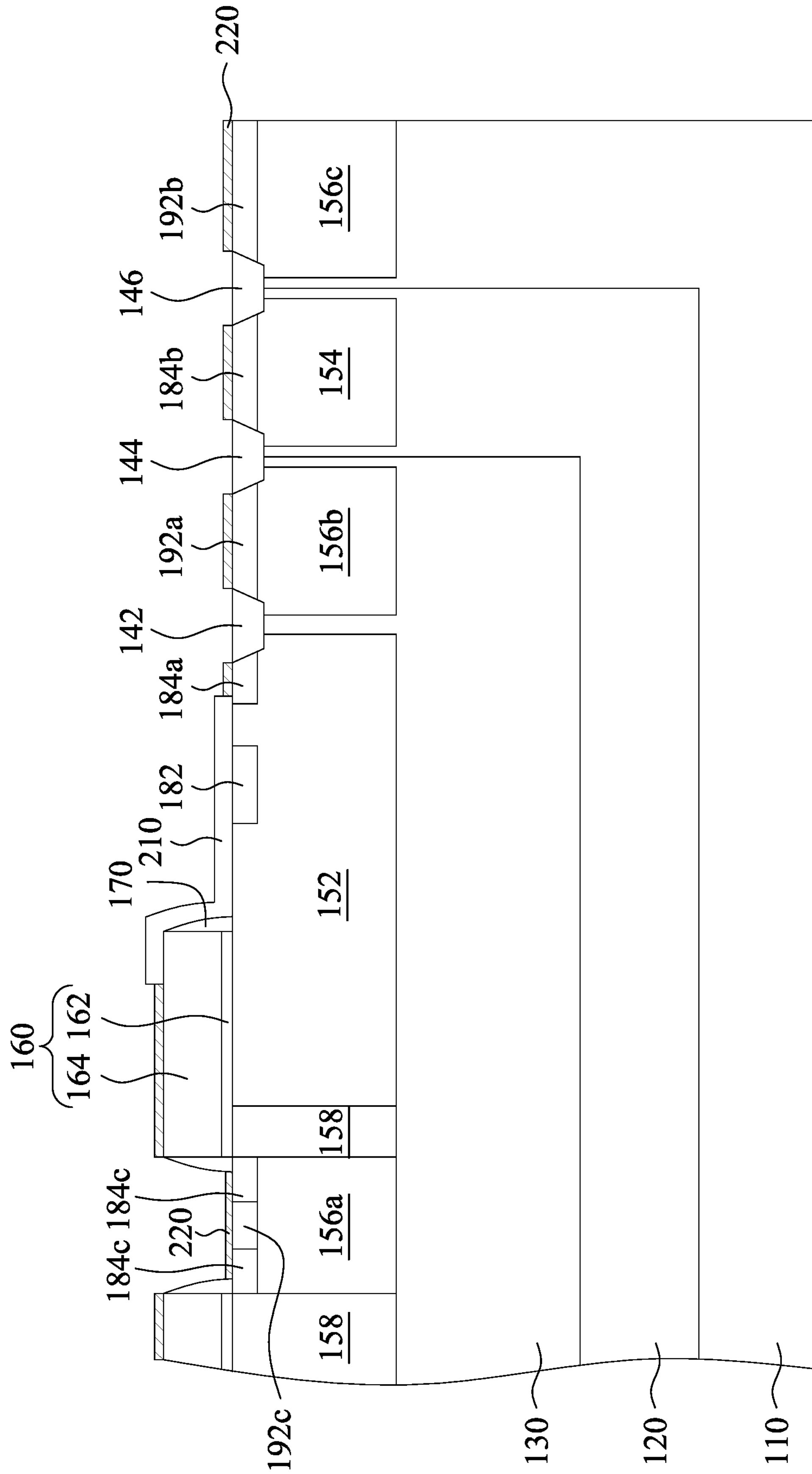


Fig. 1N

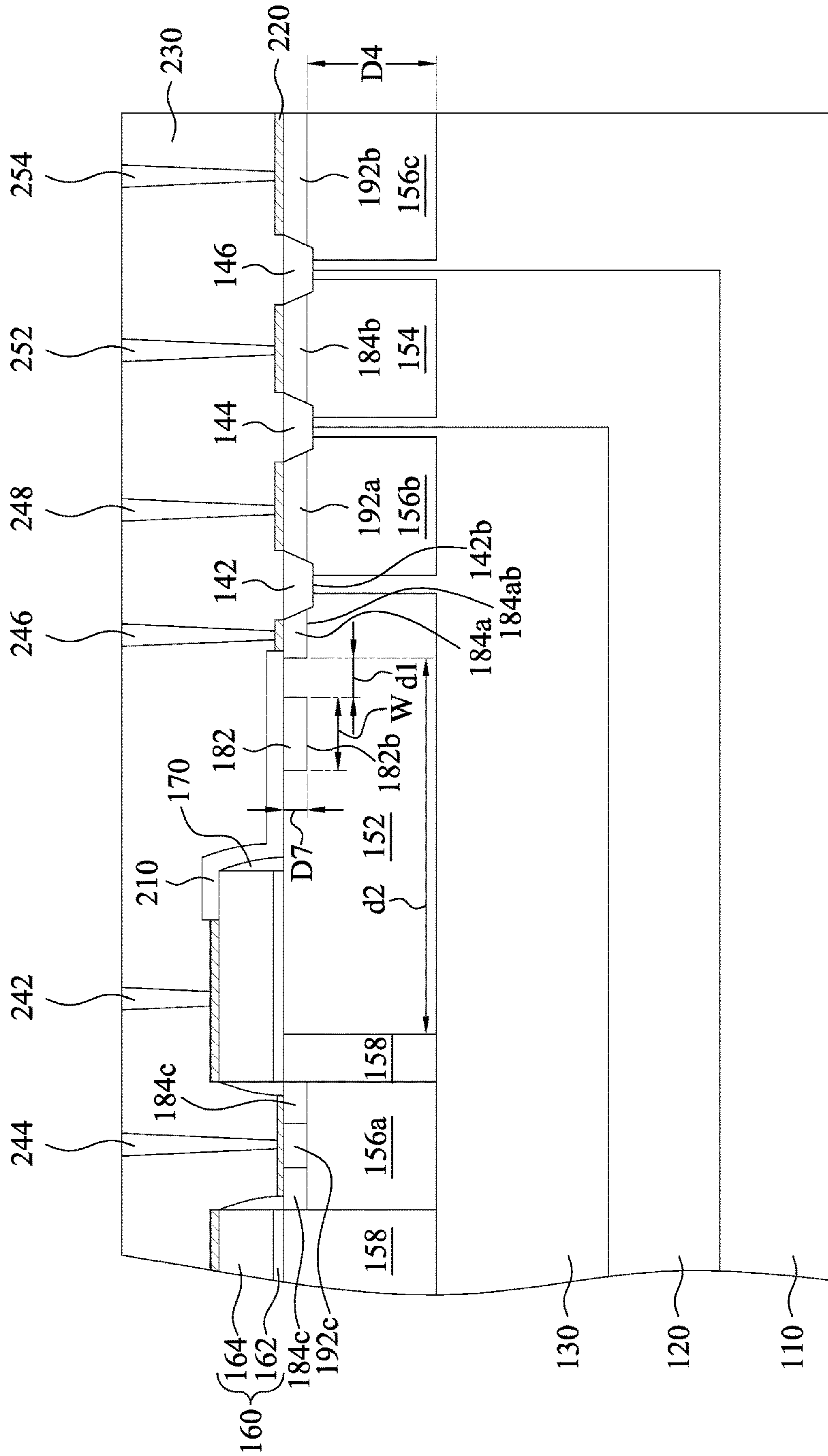


Fig. 1O

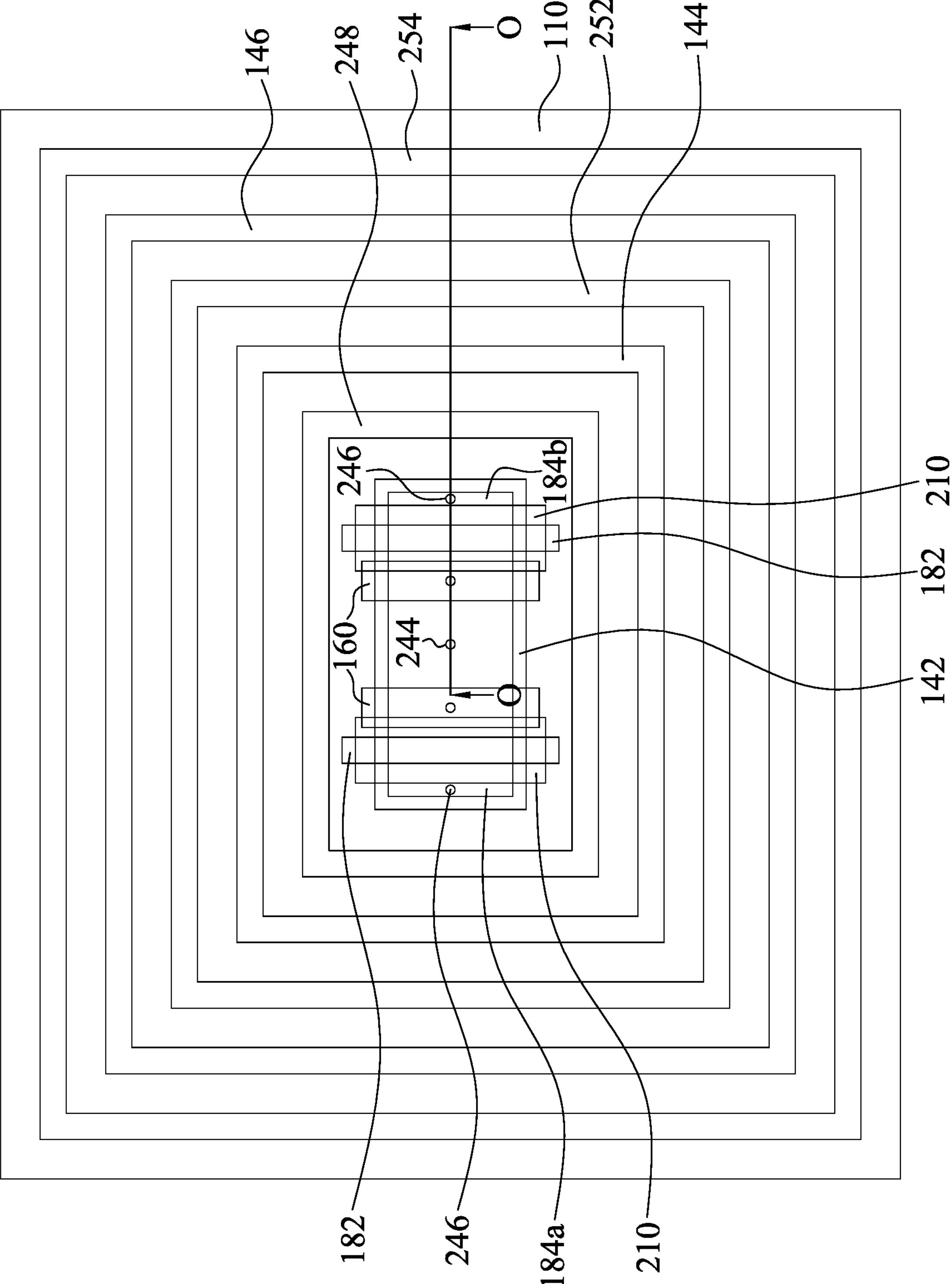


Fig. 2

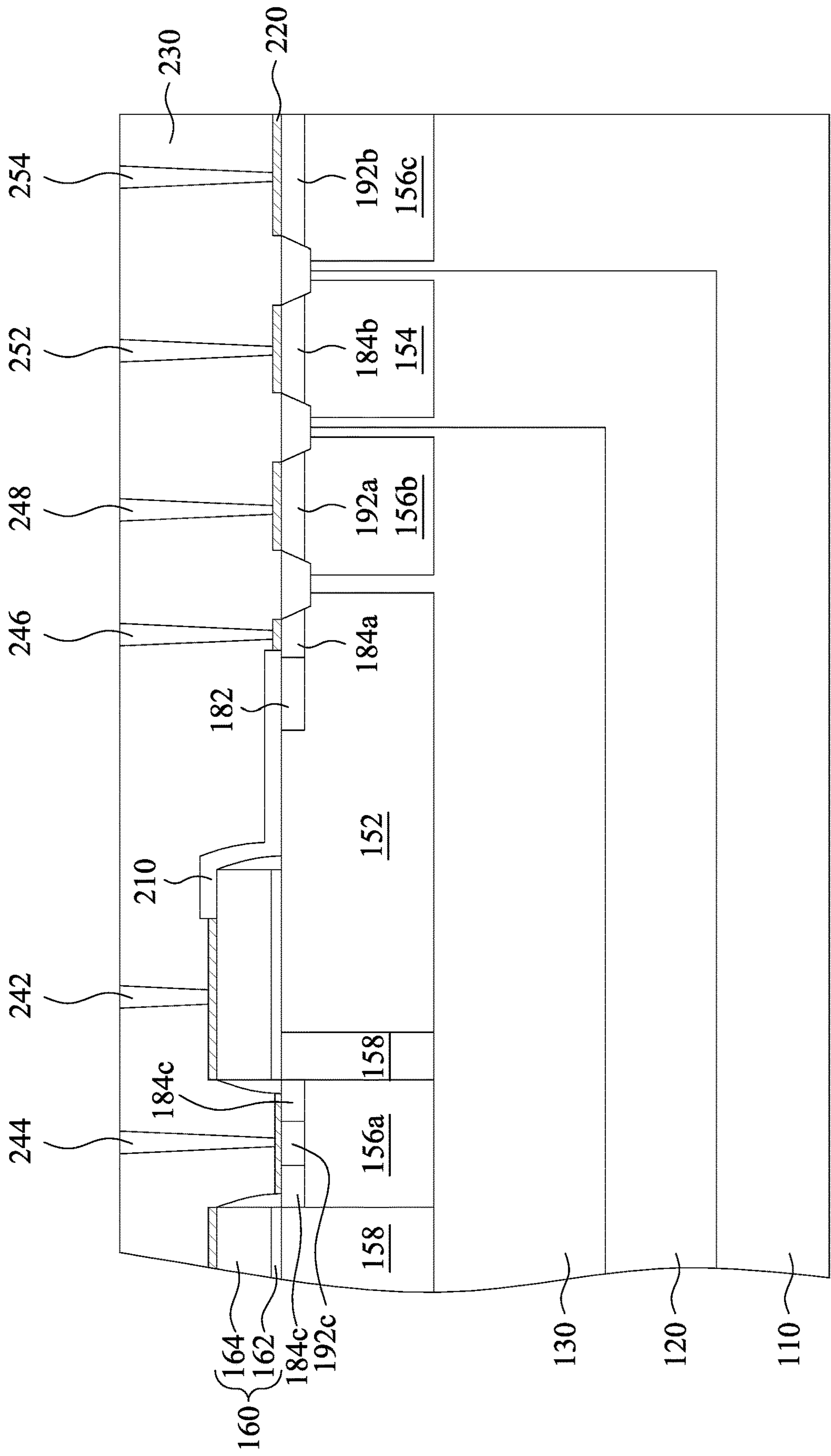


Fig. 3

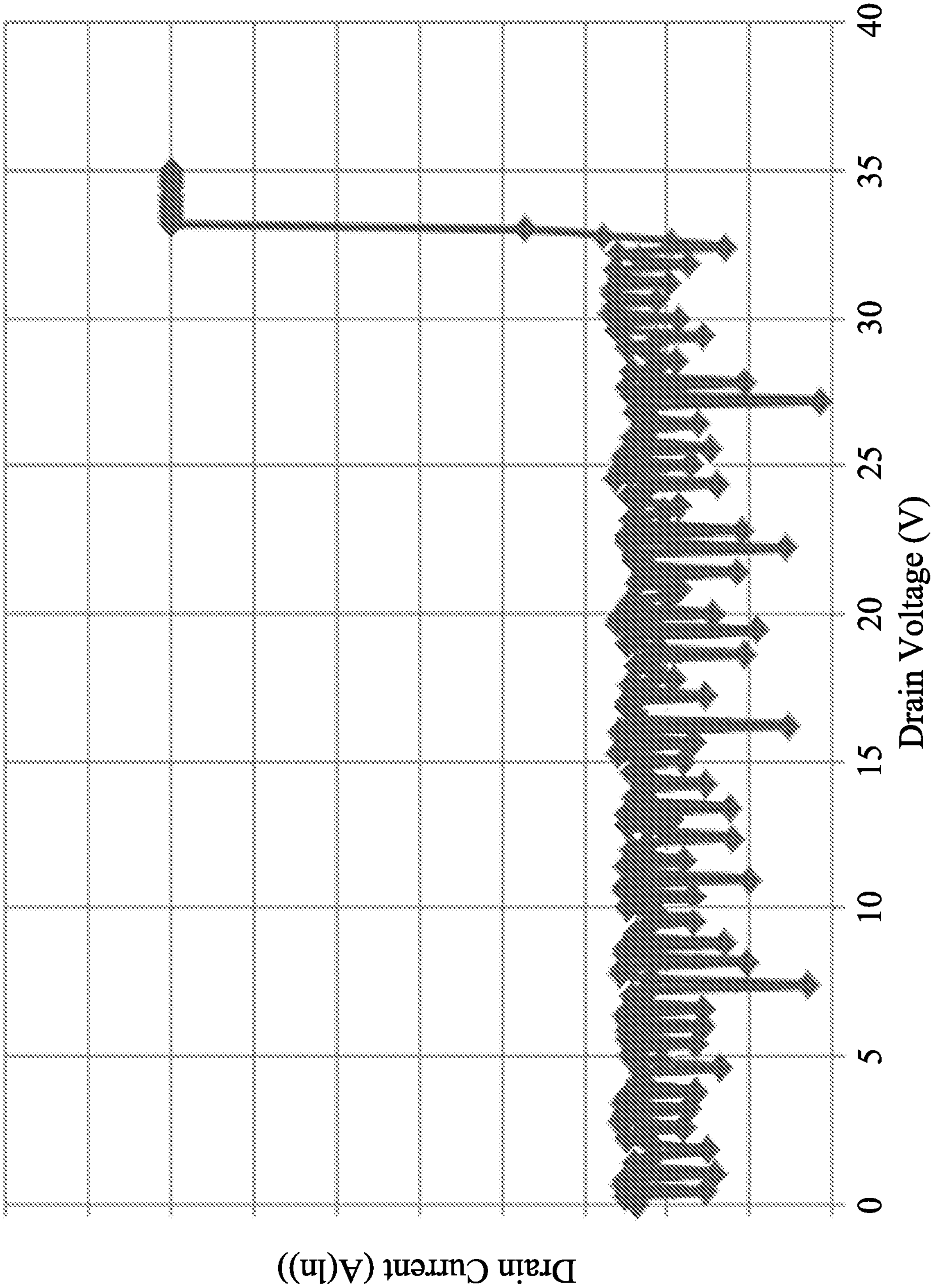


Fig. 4

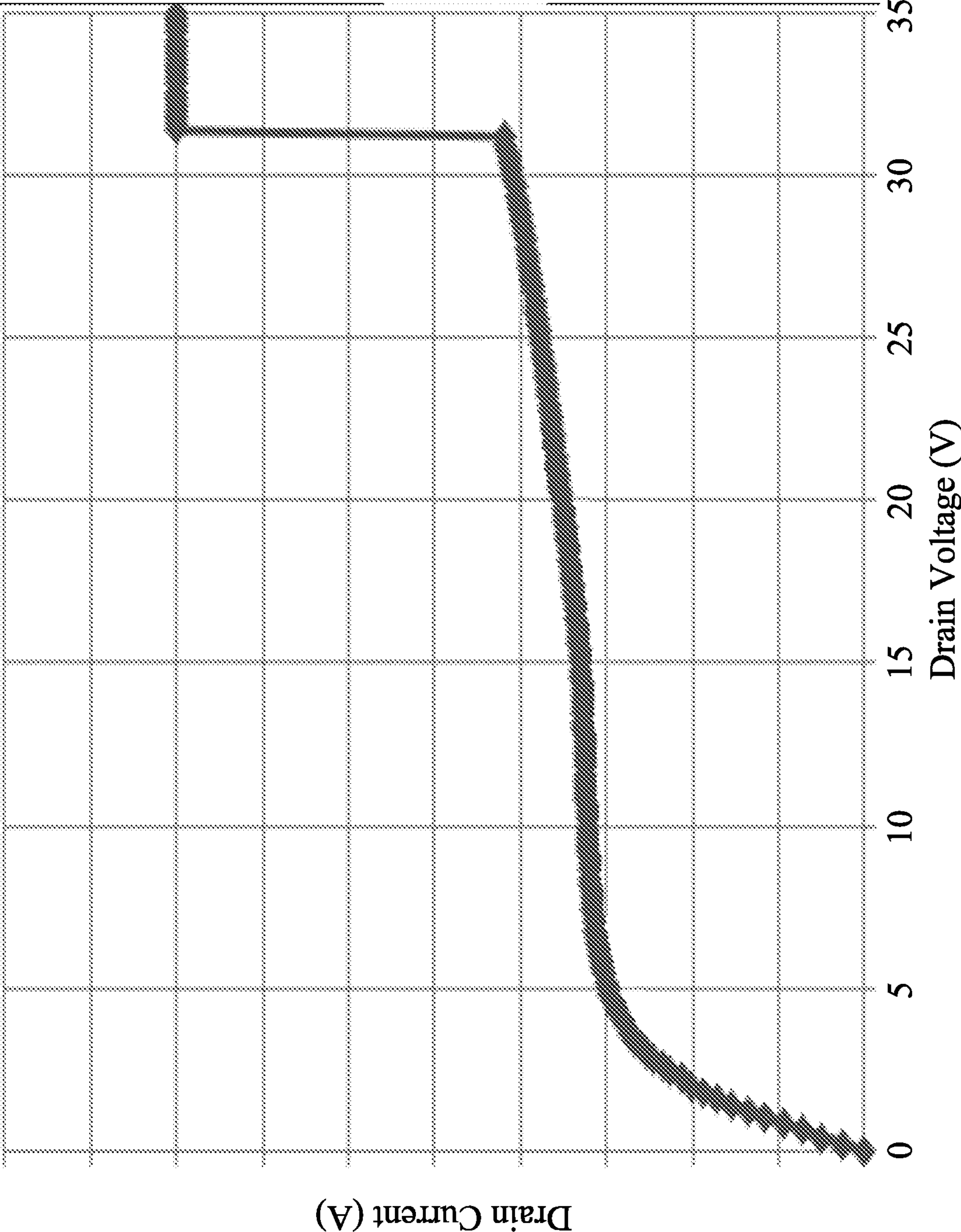


Fig. 5

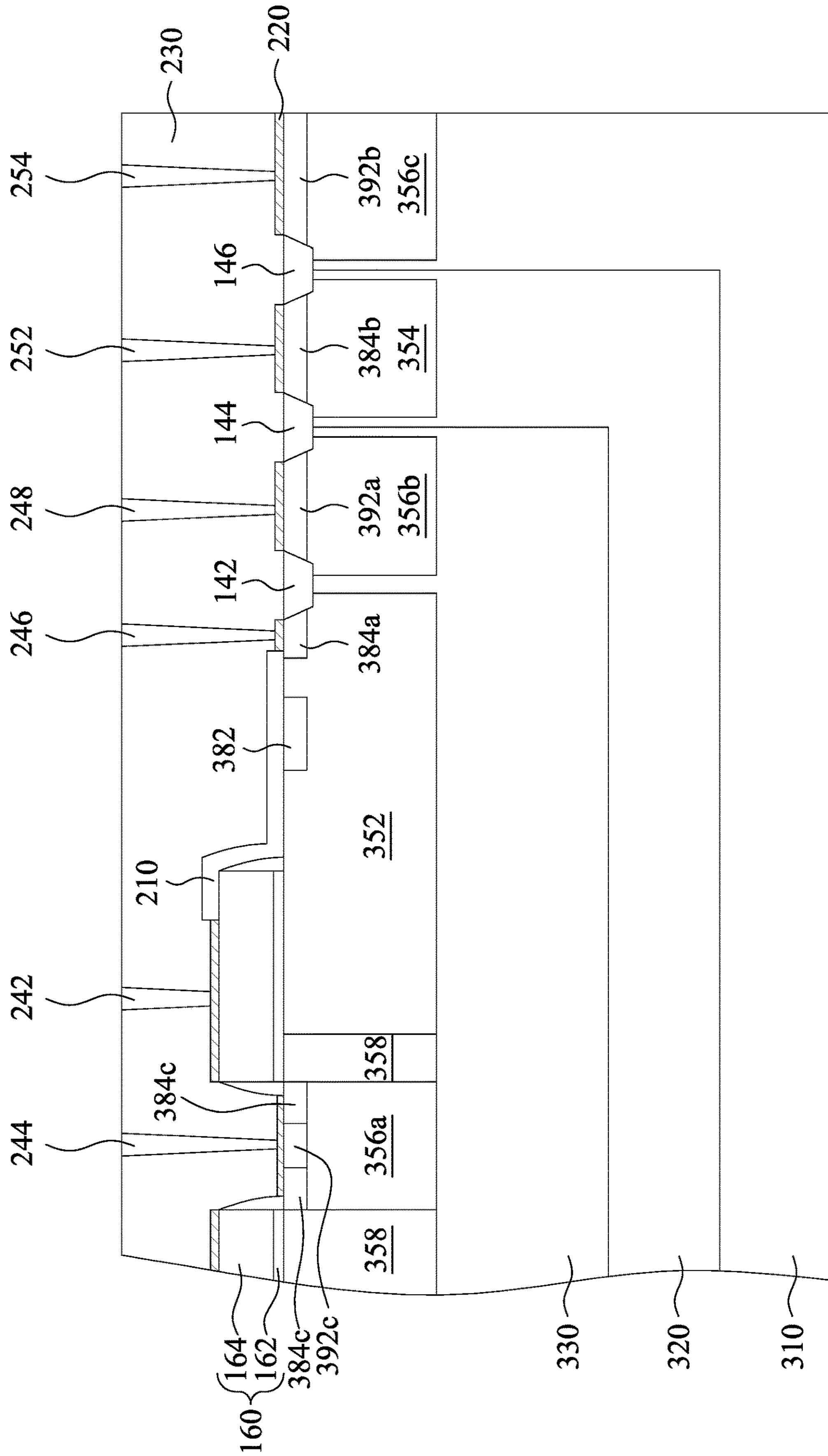


Fig. 6A

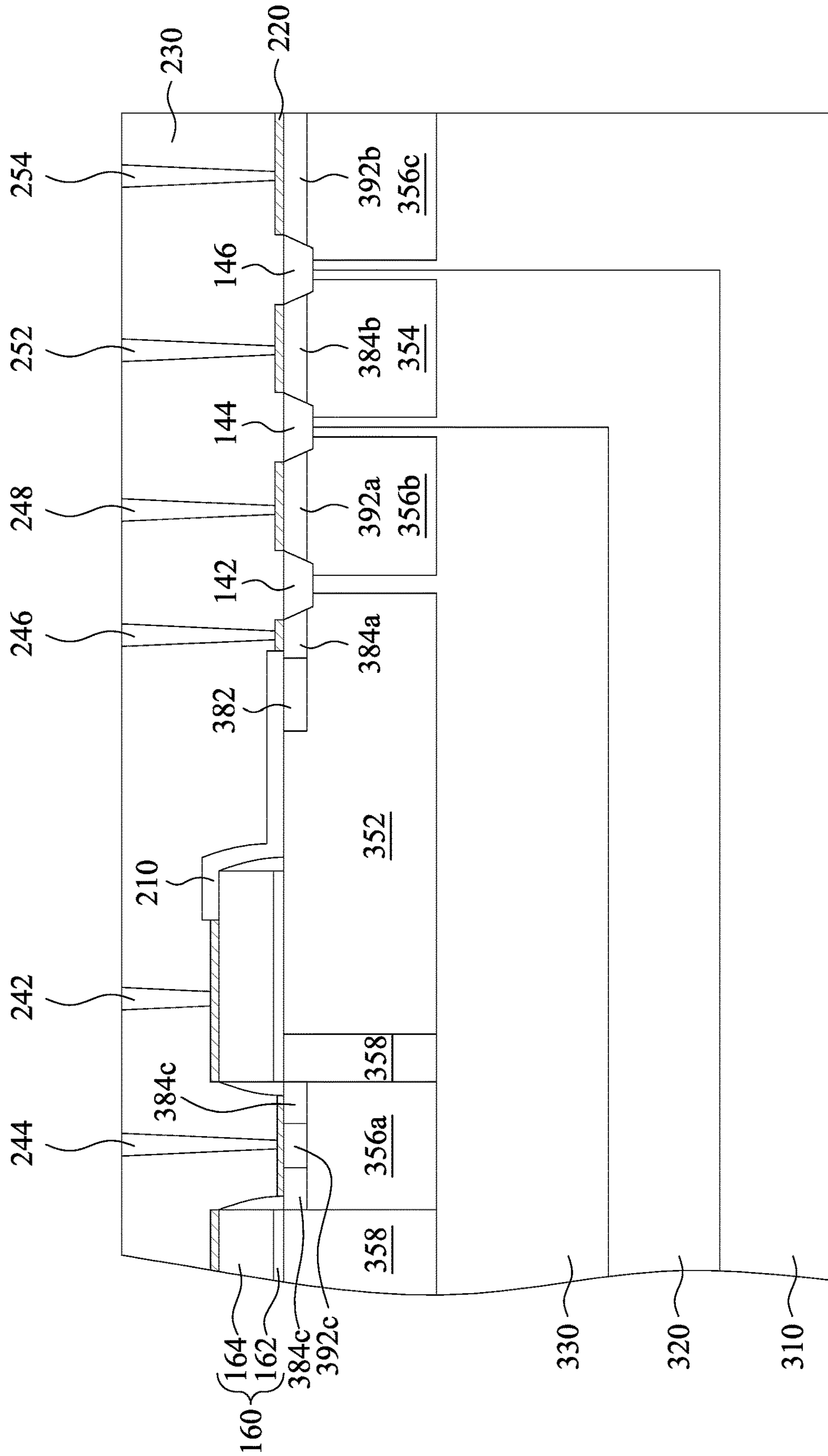


Fig. 6B

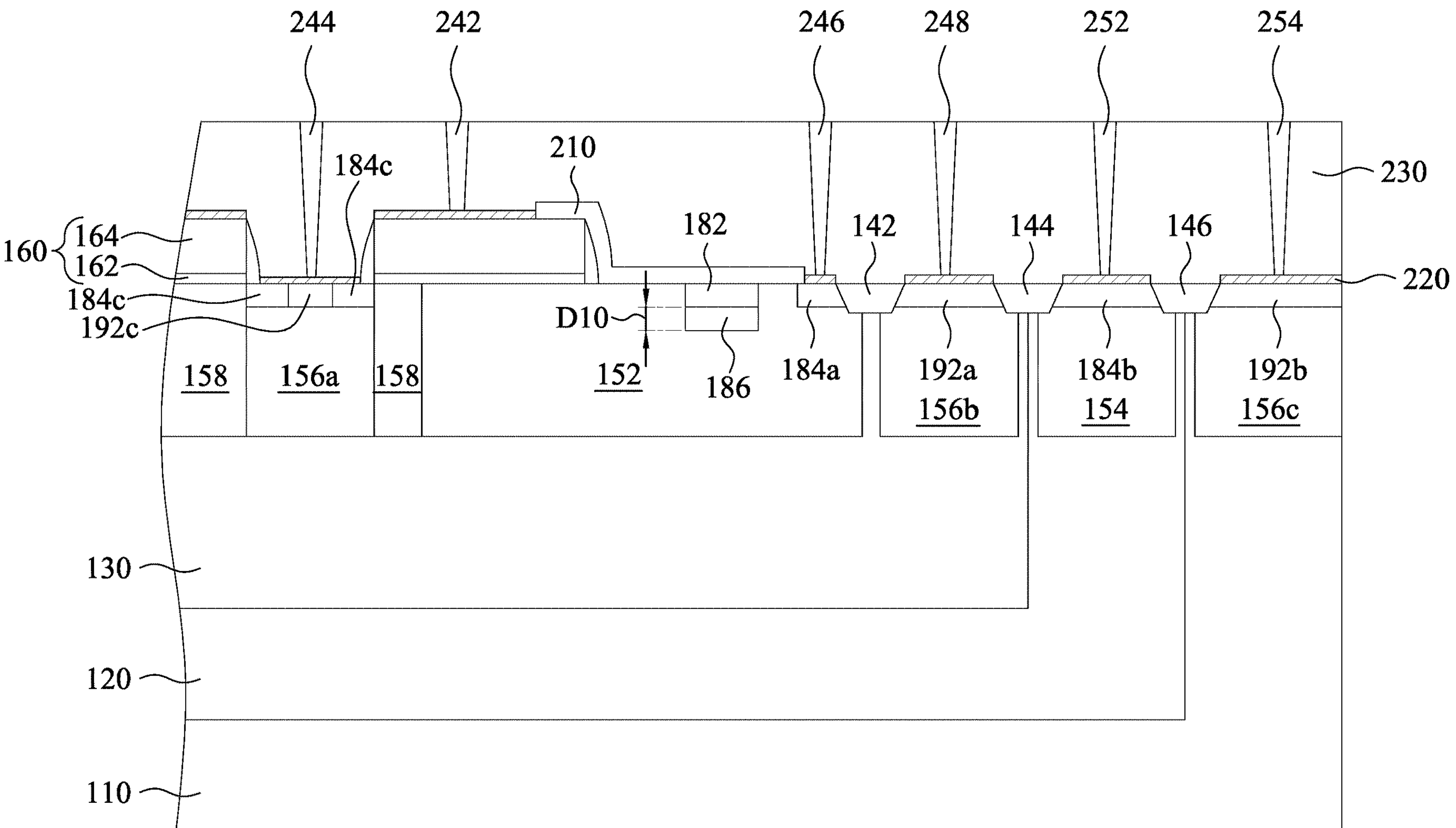


Fig. 7A

230
220
254
252
248
246
242
244
210
182
186
184a
184b
184c
192a
192b
192c
156a
156b
156c
154
152
158
D10
164
162
160
130
120
110

Fig. 7B

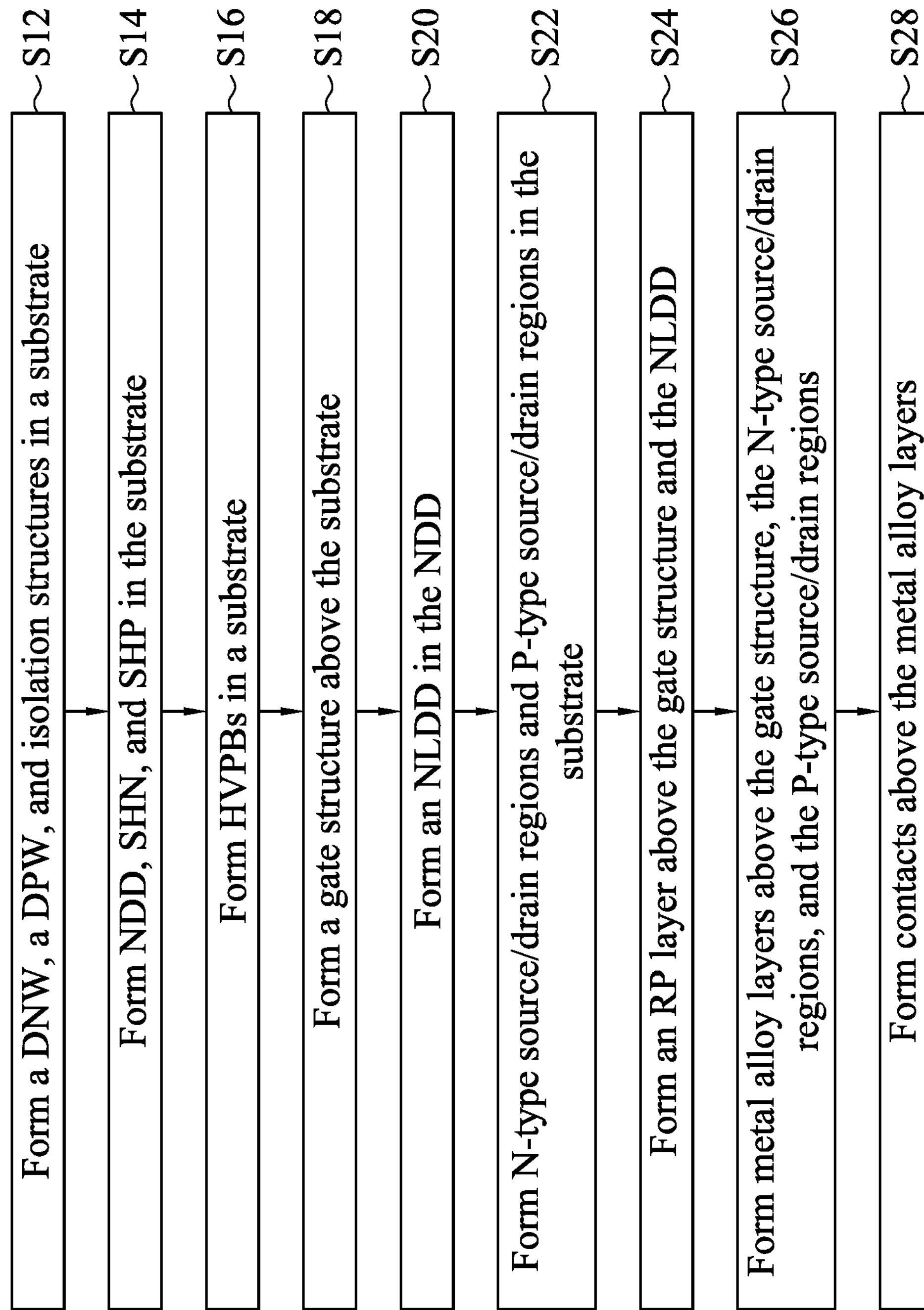


Fig. 8

SEMICONDUCTOR DEVICE WITH DOPED REGION BETWEEN GATE AND DRAIN

PRIORITY CLAIM AND CROSS-REFERENCE

[0001] The present application is a Continuation Application of U.S. Application Ser. No. 17/884,242, filed Aug. 9, 2022, which is a Continuation Application of U.S. application Ser. No. 16/930,565, filed Jul. 16, 2020, now U.S. Pat. No. 11,469,322, issued on Oct. 11, 2022, which claims priority to China Application Ser. No. 202010447490.5, filed May 25, 2020, all of which are herein incorporated by reference.

BACKGROUND

[0002] The semiconductor industry has experienced rapid growth due to improvements in the integration density of a variety of electronic components (e.g., transistors, diodes, resistors, capacitors, etc.). For the most part, this improvement in integration density has come from shrinking the semiconductor process node (e.g., shrink the process node towards the sub-20 nm node). As semiconductor devices are scaled down, new techniques are desired to maintain the electronic components' performance from one generation to the next. For example, low on-resistance and high breakdown voltage of transistors are desirable for various high power applications.

[0003] As semiconductor technologies evolve, metal oxide semiconductor field effect transistors (MOSFET) have been widely used in today's integrated circuits. MOSFETs are voltage controlled devices. When a control voltage is applied to the gate of a MOSFET and the control voltage is greater than the threshold of the MOSFET, a conductive channel is established between the drain and the source of the MOSFET. As a result, a current flows between the drain and the source of the MOSFET. On the other hand, when the control voltage is less than the threshold of the MOSFET, the MOSFET is turned off accordingly.

[0004] According to the polarity difference, MOSFETs may include two major categories. One is n-channel MOSFETs; the other is p-channel MOSFETs. On the other hand, according to the structure difference, MOSFETs can be further divided into three sub-categories, planar MOSFETs, lateral diffused MOS (LDMOS) FETs and vertical diffused MOSFETs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0006] FIGS. **1**A to **1**O illustrate a method for manufacturing a semiconductor device in different stages in accordance with some embodiments.

[0007] FIG. **2** is a top view of the semiconductor device of FIG. **1**O in various embodiments.

[0008] FIG. **3** is a cross-sectional view of a semiconductor device according to various embodiments.

[0009] FIG. **4** is a drain voltage (Vd) vs. drain current (Id) curve of the semiconductor devices at off-state according to some embodiments of the present disclosure.

[0010] FIG. **5** is a Vd vs. Id curve of the semiconductor devices at on-state according to some embodiments of the present disclosure.

[0011] FIGS. **6**A and **6**B are cross-sectional views of semiconductor devices according to various embodiments.

[0012] FIGS. **7**A and **7**B are cross-sectional views of semiconductor devices according to various embodiments.

[0013] FIG. **8** is a flow chart of a method for forming a semiconductor device in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0014] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the puRPse of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0015] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0016] As used herein, "around", "about", "approximately", or "substantially" shall generally mean within 20 percent, or within 10 percent, or within 5 percent of a given value or range. Numerical quantities given herein are approximate, meaning that the term "around", "about", "approximately", or "substantially" can be inferred if not expressly stated.

[0017] The lateral diffused (LD) MOS transistor has advantages. For example, the LDMOS transistor is capable of delivering more current per unit area because its asymmetric structure provides a short channel between the drain and the source of the LDMOS transistor. The present disclosure will be described with respect to embodiments in a specific context, a lateral diffused (LD) metal oxide semiconductor field effect transistor (MOSFET) having a doped region between the drain and the gate structure to improve Kirk effect. The embodiments of the disclosure may also be applied, however, to a variety of metal oxide semiconductor transistors. Hereinafter, various embodiments will be explained in detail with reference to the accompanying drawings.

[0018] FIGS. **1**A to **1**O illustrate a method for manufacturing a semiconductor device in different stages in accordance with some embodiments. It is noted that FIGS. **1**A to

1O have been simplified for a better understanding of the disclosed embodiment. Moreover, the semiconductor device may be configured as a system-on-chip (SoC) device having various PMOS and NMOS transistors that are fabricated to operate at different voltage levels. The PMOS and NMOS transistors may provide low voltage functionality including logic/memory devices and input/output devices, and high voltage functionality including power management devices. For example, transistors that provide low voltage functionality may have operating (or drain) voltages of 1.1 V with standard CMOS technology, or voltages of 1.8/2.5/3.3 V with special (input/output) transistors in standard CMOS technology. In addition, transistors that provide medium/high voltage functionality may have operating (or drain) voltages of 5 V or greater (e.g., 20-35 V). It is understood that the semiconductor device in FIGS. **1**A to **1**O may also include resistors, capacitors, inductors, diodes, and other suitable microelectronic devices that may be implemented in integrated circuits.

[0019] Referring to FIG. **1**A, a semiconductor substrate **110** is provided. The semiconductor substrate **110** may include a semiconductor wafer such as a silicon wafer. Alternatively, the semiconductor substrate **110** may include other elementary semiconductors such as germanium. The semiconductor substrate **110** may also include a compound semiconductor such as silicon carbide, gallium arsenic, indium arsenide, and indium phosphide. Moreover, the semiconductor substrate **110** may include an alloy semiconductor such as silicon germanium, silicon germanium carbide, gallium arsenic phosphide, and gallium indium phosphide. In some embodiments, the semiconductor substrate **110** includes an epitaxial layer (epi layer) overlying a bulk semiconductor. Furthermore, the semiconductor substrate **110** may include a semiconductor-on-insulator (SOI) structure. For example, the semiconductor substrate **110** may include a buried oxide (BOX) layer formed by a process such as separation by implanted oxygen (SIMOX). In various embodiments, the semiconductor substrate **110** may include a buried layer such as an n-type buried layer (NBL), a p-type buried layer (PBL), and/or a buried dielectric layer including a buried oxide (BOX) layer. In the some embodiments, illustrated as an n-type MOS, the semiconductor substrate **110** includes a p-type silicon substrate (p-substrate). For example, p-type dopants are introduced into the semiconductor substrate **110** to form the p-substrate. To form a complementary MOS, an n-type buried layer, i.e., deep n-well (DNW), may be implanted deeply under the active region of the p-type MOS of the p-substrate **110** as described below.

[0020] Specifically, a deep n-type well (DNW) **120'** is formed in the semiconductor substrate **110**. In some embodiments, the DNW **120'** is formed by ion implantation. In some embodiments, arsenic or phosphorus ions are implanted to form the DNW **120'**. In some other embodiments, the DNW **120'** is formed by selective diffusion. The DNW **120'** functions to electrically isolate the p-substrate.

[0021] Reference is made to FIG. **1**B. Isolation structures **142**, **144**, and **146** such as shallow trench isolations (STI) or local oxidation of silicon (LOCOS) (or field oxide, FOX) including isolation features may be formed in the semiconductor substrate **110** to define and electrically isolate various active regions so as to prevent leakage current from flowing between adjacent active regions. As one example, the formation of an STI feature may include dry etching a trench in a substrate and filling the trench with insulator materials such as silicon oxide, silicon nitride, or silicon oxynitride. The filled trench may have a multi-layer structure such as a thermal oxide liner layer filled with silicon nitride or silicon oxide. In some other embodiments, the STI structure may be created using a processing sequence such as: growing a pad oxide, forming a low pressure chemical vapor deposition (LPCVD) nitride layer, patterning an STI opening using photoresist and masking, etching a trench in the substrate, optionally growing a thermal oxide trench liner to improve the trench interface, filling the trench with CVD oxide, using chemical mechanical polishing (CMP) processing to etch back and planarize, and using a nitride stripping process to remove the silicon nitride. In some embodiments, the isolation structures **142**, **144**, and **146** have a depth D**1** in a range of about 200 nm to about 400 nm.

[0022] In some embodiments, an annealing process may be performed during the formation of the isolation structures **142**, **144**, and **146**, and the dopants in the DNW **120'** (see FIG. **1**A) are thus diffused in the annealing process, such that a depth of the DNW **120** is increased. In some embodiments, the DNW **120** has a depth D**2** in a range of about 2 um to about 6 um, and the dopant concentration of the DNW **120** is between about 10^{15} and about 10^{17} per cubic centimeter. The isolation structures **142** and **144** are formed in the DNW **120**. The isolation structure **146** is at the interface of the DNW **120** and the p-substrate **110**.

[0023] Reference is made to FIG. **1**C. In some embodiments, a deep p-type well (DPW) **130** is formed in the DNW **120**. In some embodiments, the DPW **130** is formed by ion implantation. In some other embodiments, boron ions and/or boron difloride (BF_2) ions are implanted to form the DPW **130**. In some other embodiments, the DPW **130** is formed by selective diffusion. The isolation structure **142** is thus deposited in the DPW **130**. The DPW **130** functions to electrically isolate the p-substrate. In some embodiments, the DPW **130** has a depth D**3** in a range of about 2 um to about 3 um, and the dopant concentration of the DPW **130** is between about 10^{15} and about 10^{17} per cubic centimeter. In some embodiments, the DPW **130** and the DNW **120** have substantially the same or similar dopant concentrations.

[0024] Reference is made to FIG. **1**D. An n-type doped region (NDD) (or n-type drift region) **152** is formed in the semiconductor substrate **110** and near the top surface **112** of the semiconductor substrate **110**. Specifically, the NDD **152** is formed in the DPW **130** and adjacent the isolation structure **142**. In FIG. **1**D, a bottom portion of the NDD **152** is enclosed by the DPW **130**. In some embodiments, the NDD **152** is formed by ion-implantation, diffusion techniques, or other suitable techniques. For example, an N-well mask is used to pattern a photoresist layer in a photolithography process or other suitable process. An exemplary photolithography process may include processing steps of photoresist coating, soft baking, mask aligning, exposing, post-exposure baking, developing, and hard baking. An ion implantation utilizing an n-type dopant, such as arsenic or phosphorus, may be performed to form the NDD **152** in the semiconductor substrate **110**. In some embodiments, the dopant concentration of the NDD **152** is between about 10^{16} and about 10^{17} per cubic centimeter. The dopant concentration of the NDD **152** may be greater than the dopant concentration of the DPW **130** (or the DNW **120**). In some embodiments, the NDD **152** has a depth D**4** greater than the

depth D**1** (see FIG. **1**B) of the isolation structures **142**, **144**, and/or **146**. The depth D**4** may be in a range of about 0.5 um to about 1 um.

[0025] Then, a shallow low-voltage n-type well (SHN) **154** is formed in the semiconductor substrate **110** and near the top surface **112** of the semiconductor substrate **110**. Specifically, the SHN **154** is formed in the DNW **120** and between the isolation structures **144** and **146**. In FIG. **1**D, a bottom portion of the SHN **154** is enclosed by the DNW **120**. In some embodiments, the SHN **154** is formed by ion-implantation, diffusion techniques, or other suitable techniques. For example, another N-well mask is used to pattern a photoresist layer in a photolithography process or other suitable process. An exemplary photolithography process may include processing steps of photoresist coating, soft baking, mask aligning, exposing, post-exposure baking, developing, and hard baking. An ion implantation utilizing an n-type dopant, such as arsenic or phosphorus, may be performed to form the SHN **154** in the semiconductor substrate **110**. In some embodiments, the dopant concentration of the SHN **154** is between about 10^{17} and about 10^{18} per cubic centimeter. The dopant concentration of the SHN **154** may be greater than the dopant concentration of the NDD **152**.

[0026] Subsequently, shallow low-voltage p-type wells (SHPs) **156***a*, **156***b*, and **156***c* are formed in the semiconductor substrate **110** and near the top surface **112** of the semiconductor substrate **110**. Specifically, the SHPs **156***a* and **156***b* are formed in the DPW **130** and the SHP **156***c* is formed in the p-substrate **110**. The SHPs **156***a* is configured to suppress the parasitic BJT action. The NDD **152** is formed between the SHPs **156***a* and **156***b*. The SHP **156***b* is formed between the isolation structures **142** and **144**, and the SHP **156***c* is formed adjacent the isolation structure **146**. In FIG. **1**D, bottom portions of the SHPs **156***a* and **156***b* are enclosed by the DPW **130**, and a bottom portion of the SHP **156***c* is enclosed by the p-substrate **110**. In some embodiments, the SHPs **156***a*, **156***b*, and **156***c* are formed by ion-implantation, diffusion techniques, or other suitable techniques. For example, a P-well mask is used to pattern a photoresist layer in a photolithography process or other suitable process. An exemplary photolithography process may include processing steps of photoresist coating, soft baking, mask aligning, exposing, post-exposure baking, developing, and hard baking. An ion implantation utilizing a p-type dopant, such as boron and/or boron difloride (BF_2), may be performed to form the SHPs **156***a*, **156***b*, and **156***c* in the semiconductor substrate **110**. In some embodiments, the dopant concentration of each of the SHPs **156***a*, **156***b*, and **156***c* may be between about 10^{17} and about 10^{18} per cubic centimeter. The dopant concentration of each of the SHPs **156***a*, **156***b*, and **156***c* may be greater than the dopant concentration of the NDD **152**.

[0027] In some embodiments, the SHN **154**, and the SHPs **156***a*, **156***b*, and **156***c* have substantially the same or similar depth D**5**. In some embodiments, the depth D**5** is greater than the depth D**1** (see FIG. **1**B) of the isolation structures **142**, **144**, and/or **146**. The depth D**5** may be in a range of about 1 um to about 2 um. Further, it is noted that the formation sequence of the NDD **152**, the SHN **154**, and the SHPs **156***a*, **156***b*, and **156***c* mentioned above is an example, and should not limit the present disclosure. In some other embodiments, the NDD **152** may be formed after the formation of the SHN **154** and/or the SHPs **156***a*, **156***b*, and **156***c*, and/or the SHN **154** may be formed after the formation of the SHPs **156***a*, **156***b*, and **156***c*.

[0028] Reference is made to FIG. **1**E. A gate dielectric film **162'** and a conductive film **164'** are subsequently formed above the semiconductor substrate **110**. The gate dielectric film **162'** may include a silicon oxide layer. Alternatively, the gate dielectric film **162'** may optionally include a high-k dielectric material, silicon oxynitride, other suitable materials, or combinations thereof. The high-k material may be selected from metal oxides, metal nitrides, metal silicates, transition metal-oxides, transition metal-nitrides, transition metal-silicates, oxynitrides of metals, metal aluminates, zirconium silicate, zirconium aluminate, hafnium oxide, or combinations thereof. The gate dielectric film **162'** may have a multilayer structure such as one layer of silicon oxide and another layer of high k material. The gate dielectric film **162'** may be formed using chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), thermal oxide, other suitable processes, or combinations thereof.

[0029] The conductive film **164'** may include a doped polycrystalline silicon (or polysilicon). Alternatively, the conductive film **164'** may include a metal such as Al, Cu, W, Ti, Ta, TiN, TaN, NiSi, CoSi, other suitable conductive materials, or combinations thereof. The conductive film **164'** may be formed by CVD, PVD, plating, and other proper processes. The conductive film **164'** may have a multilayer structure and may be formed in a multi-step process using a combination of different processes.

[0030] Reference is made to FIG. **1**F. An opening **166** is formed in the gate dielectric film **162'** and the conductive film **164'**, and the opening **166** exposes the SHP **156***a*.The opening **166** may be formed by using a process including photolithography patterning and etching. An exemplary method for patterning the gate dielectric film **162'** and the conductive film **164'** is described below. A layer of photoresist is formed on the conductive film **164'** by a suitable process, such as spin-on coating, and then patterned to form a patterned photoresist feature by a proper lithography patterning method. The pattern of the photoresist may then be transferred by a dry etching process to the underlying conductive film **164'** and the gate dielectric film **162'**, in a plurality of processing operations and various proper sequences. The photoresist layer may be stripped thereafter. In still some other embodiments, a hard mask layer may be used and formed on the conductive film **164'**. The patterned photoresist layer is formed on the hard mask layer. The pattern of the photoresist layer is transferred to the hard mask layer and then transferred to the conductive film **164'**. The hard mask layer may include silicon nitride, silicon oxynitride, silicon carbide, and/or other suitable dielectric materials, and may be formed using a method such as CVD or PVD.

[0031] Then, high-voltage p-type implanted regions (HVPBs) **158** are formed in the DPW **130**, such that each of the HVPBs **158** is formed between the SHP **156***a* and the NDD **152**. That is, the NDD **152** is formed between the HVPB **158** and the isolation structure **142**. The gate dielectric film **162'** and the conductive film **164'** act as implantation masks. The implantation in FIG. **1**F may be tilted, with the tilt angle greater than the tilt angle of the SHP, SHN, and LDD implantations, such that the HVPBs **158** are formed under the gate dielectric film **162'** and the conductive film **164'**. In some embodiments, the HVPBs **158** have a depth

D**6** in a range of about 1.5 um to about 2.5 um. In some embodiments, the dopant concentration of each of the HVPBs **158** may be between about 10^{17} and about 10^{18} per cubic centimeter. The dopant concentration of each of the HVPBs **158** may be greater than the dopant concentration of the SHPs **156***a*, **156***b*, and/or **156***c*.

[0032] Reference is made to FIG. **1**G. The gate dielectric film **162'** and the conductive film **164'** in FIG. **1**F are further patterned to form a gate structure **160** on the semiconductor substrate **110**. In some embodiments, the gate structure **160** includes a gate dielectric layer **162** formed on the semiconductor substrate **110**, and a gate electrode **164** a formed on the gate dielectric layer **162**. Further, the gate structure **160** overlies a portion of the NDD **152** and the HVPB **158**. The gate electrode **164** may be configured to be coupled to metal interconnects and may be disposed overlying the gate dielectric layer **162**. The gate dielectric layer **162** and the gate electrode **164** formed on the semiconductor substrate **110** are then patterned to form a plurality of gate structures using a process including photolithography patterning and etching.

[0033] Reference is made to FIG. **1**H. An N-type light doped region (NLDD) **182** is formed in the NDD **152**. Specifically, the NLDD **182** is formed in the NDD **152** and spaced apart from the isolation structure **142**. In FIG. **1**H, a bottom portion of the NLDD **182** is enclosed by the NDD **152**. A depth D7 of the NLDD **182** is less than the depth D**4** of the NDD **152** and the depth D**1** of the isolation structure **142**, and the depth D**7** is in a range of about 0.2 um to about 0.4 um. Stated in another way, a bottom surface **182***b* of the NLDD **182** is above a bottom surface **142***b* of the isolation structure **142**.

[0034] In some embodiments, the NLDD **182** is formed by ion-implantation, diffusion techniques, or other suitable techniques. For example, another N-well mask **105** is deposited over the structure in FIG. **1**G (i.e., over the NDD **152**, the SHN **154**, the SHPs **156***a*-**156***c*, the gate structure **160**, and the isolation structures **142**, **144**, and **146**). The N-well mask **105** has an opening **106** exposing a portion of the NDD **152**. An ion implantation utilizing an n-type dopant, such as arsenic or phosphorus, may be performed to form the NLDD **182** in the NDD **152**. In some embodiments, the NLDD implantation may be tilted or vertical, with the tilt angle θ between about 0 degree and about 45 degrees. The vertical implantation (i.e., the tilt angle θ is 0 degree) forms an NLDD **182** right under the opening **106**, and the width W of the NLDD **182** is substantially the same as the width of the opening **106**. In some other embodiments, the tilted implantation (i.e., the tilt angle θ is greater than 0 degree) form an NLDD **182** offset from the opening **106**, and the width W of the NLDD **182** is greater than the width of the opening **106**. With the tilted implantation, the size of the opening **106** may be reduced, such that the opening **106** won't expose a region that is supposed to form a drain region of the semiconductor device. Further, the tilt angle of the implantation can be tuned according to the desired width W and/or distance d**1** (see FIG. **1**J) between the NLDD **182** and the following formed drain region (i.e., the N-type source/drain region **184***a* in FIG. **1**J).

[0035] In some embodiments, the dopant concentration of the NLDD **182** is between about 10^{17} and about 10^{19} per cubic centimeter. The dopant concentration of the NLDD **182** is greater than the dopant concentration of the NDD **152**. In some embodiments, the width W of the NLDD **182** is greater than 0 um and equal to or less than about 1 um. The NLDD **182** improves the Kirk effect of the semiconductor device and further improves the drain current (Id)-voltage (Vd) tailing performance, and the detailed description will be discussed in the following paragraphs.

[0036] Reference is made to FIG. **1**I. The N-well mask **105** in FIG. **1**H is removed, and sidewall spacers **170** are formed on opposite sides of the gate structure **160**. The sidewall spacers **170** may include a dielectric material such as silicon oxide. Alternatively, the sidewall spacers **170** may optionally include silicon oxide, silicon nitride, silicon oxynitride, SiCN, $SiC_xO_yN_z$, or combinations thereof. In some embodiments, the sidewall spacers **170** may have a multilayer structure. The sidewall spacers **170** can be formed using a deposition method, such as plasma enhanced chemical vapor deposition (PECVD), low-pressure chemical vapor deposition (LPCVD), sub-atmospheric chemical vapor deposition (SACVD), or the like. The formation of the sidewall spacers **170** may include blanket forming spacer layers and then performing etching operations to remove the horizontal portions of the spacer layers. The remaining vertical portions of the spacer layers form the sidewall spacers **170**.

[0037] Reference is made to FIG. **1**J. N-type source/drain region **184***a*, N-type pick-up region **184***b*, and N-type source/drain region **184***c* are formed in the N-wells or P-wells. The N-type source/drain regions **184***a*, **184***c* and N-type pick-up region **184***b* are N+ or heavily doped regions. In some embodiments, the N-type source/drain regions **184***a*,**184***c* and N-type pick-up region **184***b* include n-type dopants such as P or As. The N-type source/drain regions **184***a*, **184***c* and N-type pick-up region **184***b* may be formed by a method such as ion implantation or diffusion. A rapid thermal annealing (RTA) process may be used to activate the implanted dopant. In various embodiments, the N-type source/drain regions **184***a*, **184***c* and N-type pick-up region **184***b* may have different doping profiles formed by multi-process implantation.

[0038] The N-type source/drain region **184***a* is formed in the NDD **152** and adjacent the isolation structure **142**, and the N-type source/drain region **184***a* is referred to as a drain region of the semiconductor device. Further, the N-type source/drain region **184***a* is formed between the NLDD **182** and the isolation structure **142**. The N-type pick-up region **184***b* is formed in the SHN **154** and between the isolation structures **144** and **146**, and the N-type source/drain regions **184***c* are formed in the SHP **156***a* (outside the NDD **152**) and spaced apart from each other. The N-type source/drain region **184***c* is referred to as a source region of the semiconductor device, in some embodiments. A depth D**8** of each of the N-type source/drain region **184***a*, **184***c* and N-type pick-up region **184***b* is less than the depth D**4** of the NDD **152** and the depth D**1** of the isolation structure **142**, and the depth D**8** is in a range of about 0.2 um to about 0.3 um. In some embodiments, the dopant concentration of each of the N-type source/drain regions **184***a*, **184***c* and N-type pick-up region **184***b* may be between about 10^{20} and about 10^{21} per cubic centimeter. The dopant concentration of each of the N-type source/drain regions **184***a*,**184***c* and N-type pick-up region **184***b* may be greater than the dopant concentration of the NLDD **182**.

[0039] The NLDD **182**, NDD **152**, and N-type source/drain region **184***a* have the same conductivity type (i.e., N-type in this case). The NLDD **182** improves Kirk effect occurred at the surface of drain side. The Kirk effect occurs at the N/N+ junction (i.e., the interface between the NDD

152 and the N-type source/drain region **184***a*) due to a sharper field and an enhanced avalanche multiplication at the junction. The Kirk effect can be suppressed by implementing the NLDD **182** near the N-type source/drain region **184***a*. The NLDD **182** can prevent strong impact ionization near the surface **112** and modifies the electric field near the N-type source/drain region **184***a*, such that the electric field at the drain side is no longer strong/sharpen. Also, the NLDD **182** provides good drain voltage (Vd) vs. drain current (Id) tailing performance (as shown in FIGS. **4** and **5**). Furthermore, the NLDD **182** is not formed under the N-type source/drain region **184***a*, and the NDD **152** surrounds the bottom portion of the NLDD **182**, such that the NLDD **182** won't lower the off-state breakdown voltage of the semiconductor device.

[0040] In some embodiments, the NLDD **182** is spaced apart from the N-type source/drain region **184***a* as shown in FIG. **1**J. A distance d**1** between the NLDD **182** and N-type source/drain region **184***a* may be greater than 0 and equal to or less than about 0.5 um. In some other embodiments, the NLDD **182** is in contact with the N-type source/drain region **184***a* as shown in FIG. **3**, which is a cross-sectional view of a semiconductor device according to various embodiments. Since the drain region (the N-type source/drain region **184***a*) is between the NLDD **182** and the isolation structure **142**, i.e., the NLDD **182** does not diffuse outside the NDD **152**, the NLDD **182** does not lower the off-state breakdown voltage of the semiconductor device.

[0041] Moreover, the dopant concentration of the NLDD **182** is lower than the dopant concentration of the N-type source/drain region **184***a* and higher than the dopant concentration of the NDD **152**. If the dopant concentration of the NLDD **182** is equal to or higher than the N-type source/drain region **184***a*, the NLDD **182** will become the drain region of the semiconductor device, such that the channel length is shorten and the Kirk effect still exists. If the dopant concentration of the NLDD **182** is equal to or lower than the dopant concentration of the NDD **152**, the NLDD **182** does not suppress the Kirk effect.

[0042] Reference is made to FIG. **1**K. P-type pick-up regions **192***a*-**192***c* are formed in the SHPs **156***a*-**156***c*. The P-type pick-up regions **192***a*-**192***c* are P+ or heavily doped regions. In some embodiments, the P-type pick-up regions **192***a*-**192***c* include p-type dopants such as boron or boron difluoride (BF_2). The P-type pick-up regions **192***a*-**192***c* may be formed by a method such as ion implantation or diffusion. A rapid thermal annealing (RTA) process may be used to activate the implanted dopant. A depth D**9** of the P-type pick-up region **192***a*-**192***c* is less than the depth D**4** of the NDD **152** and the depth D**1** of the isolation structure **142**, and the depth D**9** is in a range of about 0.2 um to about 0.3 um. In some embodiments, the dopant concentration of each of the P-type pick-up region **192***a*-**192***c* may be between about 10^{20} and about 10^{21} per cubic centimeter. The dopant concentration of each of the P-type pick-up region **192***a*-**192***c* may be greater than the dopant concentration of the SHPs **156***a*-**156***c* and the dopant concentration of the NLDD **182**.

[0043] The P-type pick-up region **192***a* is formed in the SHP **156***b* and between the isolation structures **142** and **144**, the P-type pick-up region **192***b* is formed in the SHP **156***c* and adjacent the isolation structure **146**, and the P-type pick-up region **192***c* is formed in the SHP **156***a* and between the N-type source/drain regions **184***c*. The P-type pick-up region **192***c* is spaced apart from the HVPB **158**. In some embodiments, the P-type pick-up regions **192***a*-**192***c* may be formed before the formation of the N-type source/drain regions **184***a*, **184***c* and N-type pick-up region **184***b* and/or the NLDD **182**.

[0044] It should be noted that the doping technique used in the previous example is selected purely for demonstration purposes and is not intended to limit the various embodiments to any particular doping technique. One skilled in the art will recognize that alternate embodiment could be employed (such as employing the diffusion technique).

[0045] Reference is made to FIG. **1**L. A resist protective (RP) layer **210'** is formed over the structure in FIG. **1**K, i.e., the gate structure **160**, the sidewall spacers **170**, the N-type source/drain regions **184***a*, **184***c* and N-type pick-up region **184***b*, the NLDD **182**, the P-type pick-up regions **192***a*-**192***c*, and the isolation structures **142**, **144**, and **146**. In some embodiments, the RP layer **210'** is formed of a dielectric layer such as silicon dioxide using chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), other suitable processes, or combinations thereof.

[0046] Reference is made to FIG. **1**M. the RP layer **210'** (see FIG. **1**L) is partially etched away, leaving the RP layer **210** over at least a portion of the gate structure **160** and the sidewall spacers **170**, extending over a portion of the N-type source/drain region **184***a*. That is, the RP layer **210** covers and in contact with the NLDD **182**. The RP layer **210** may function as a silicide blocking layer during a subsequent self-aligned silicide (salicide) process discussed below. The device area that does not use the silicide process is covered with the RP layer **210**. The RP layer **210** can be defined by applying, for example, an oxide wet etch that partially removes the RP layer **210'**. This protects the areas under the RP layer **210** from the silicide formation.

[0047] Reference is made to FIG. **1**N. Metal alloy layers **220** may be formed by silicidation, such as salicide, in which a metal material is formed next to a Si structure, then the temperature is raised to anneal and cause a reaction between underlying silicon and the metal so as to form silicide, and the un-reacted metal is etched away. The salicide material may be self-aligned to be formed on various features such as the N-type source/drain regions **184***a*, **184***c* and N-type pick-up region **184***b*, the P-type pick-up regions **192***a*-**192***c*, and/or the gate electrode **164** to reduce contact resistance. Further, one of the metal alloy layers **220** is in contact with the N-type source/drain region **184***a* and an edge of the RP layer **210**.

[0048] Reference is made to FIGS. **1**O and **2**, where FIG. **2** is a top view of the semiconductor device of FIG. **1**O in various embodiments. The cross-sectional view shown in FIG. **1**O is taken along line O-O in FIG. **2**. For clarity, the metal alloy layers **220** and the wells are omitted in FIG. **2**. An interlayer dielectric (ILD) **230** is formed above the structure in FIG. **1**N. The ILD **230** may include silicon oxide. Alternatively or additionally, the ILD **230** includes a material having a low dielectric constant such as a dielectric constant less than about 3.5. In some embodiments, the dielectric layer **230** includes silicon dioxide, silicon nitride, silicon oxynitride, polyimide, spin-on glass (SOG), fluoride-doped silicate glass (FSG), carbon doped silicon oxide, Black Diamond® (Applied Materials of Santa Clara, Calif.), Xerogel, Aerogel, amorphous fluorinated carbon, Parylene, BCB (bis-benzocyclobutenes), SiLK (Dow Chemical, Mid-

land, Mich.), polyimide, and/or other suitable materials. The dielectric layer **230** may be formed by a technique including spin-on coating, CVD, or other suitable processes.

[0049] Then, a plurality of contacts **242**, **244**, **246**, **248**, **252**, and **254** are formed in the ILD **230**. For example, a plurality of the openings are formed in the ILD **230**, and conductive materials are filled in the openings. The excess portions of the conductive materials are removed to form the contacts **242**, **244**, **246**, **248**, **252**, and **254**. The contacts **242**, **244**, **246**, **248**, **252**, and **254** may be made of tungsten, aluminum, copper, or other suitable materials. In some embodiments, the contact **242** is connected to the gate structure **160**, the contact **244** is connected to the P-type pick-up region **192***c* and the N-type source/drain regions **184***c* (i.e., the source region of the semiconductor device), the contact **246** is connected to the N-type source/drain regions **184***a* (i.e., the drain region of the semiconductor device), the contact **248** is connected to the P-type pick-up regions **192***a,* the contact **252** is connected to the N-type pick-up region **184***b,*and the contact **254** is connected to the P-type pick-up region **192***b.*

[0050] The semiconductor device includes the gate structure **160**, the drain region (i.e., the N-type source/drain region **184***a*), the source region (i.e., the N-type source/drain region **184***c*), the NDD **152**, and the NLDD **182**. The source region and the drain region are on opposite sides of the gate structure **160** and on opposite sides of the NLDD **182**. The NDD **152** is under the gate structure **160**. The NLDD **182** and the drain region are both in the NDD **152**. The depth D**7** of the NLDD **182** is less than the depth D**4** of the NDD **152**, and the depth D**7** is in a range of about 0.2 um to about 0.4 um. In some embodiments, the width W of the NLDD **182** is greater than 0 um and equal to or less than about 1 um. If the width W of the NLDD **182** is greater than about 1 um, the NLDD **182** may be close to the gate structure **160**, such that the off-state breakdown voltage of the semiconductor device may be decreased. In some embodiments, the NLDD **182** does not overlap with the gate structure **160**. That is, the gate structure **160** does not cover the NLDD **182**, and the gate structure **160** is spaced apart from a sidewall **182***s* of the NLDD **182**.

[0051] The NLDD **182** is formed in the NDD **152** and between the N-type source/drain region **184***a* and the gate structure **160**. The NLDD **182**, NDD **152**, and N-type source/drain region **184***a* have substantially coplanar top surfaces (i.e., the top surface **112** of the substrate **110**). In some embodiments, a bottom surface of **182***b* of the NLDD **182** is laterally spaced apart from a bottom surface **184***ab* of the N-type source/drain region **184***a* to define a distance d**1**. The distance d**1** between the NLDD **182** and N-type source/drain region **184***a* may be greater than 0 and equal to or less than about 0.5 um. If the distance d**1** is greater than about 0.5 um, the NLDD **182** is close to the gate structure **160**, and the off-state breakdown voltage of the semiconductor device may be decreased. Since the drain region (the N-type source/drain region **184***a*) is between the NLDD **182** and the isolation structure **142**, i.e., the NLDD **182** does not diffuse outside the NDD **152**, the NLDD **182** does not lower the off-state breakdown voltage of the semiconductor device.

[0052] In some embodiments, a distance d**2**, referred to as a drift region length, is formed between the N-type source/drain region **184***a* and an edge of the NDD **152** adjacent the HVPB **158**. A sum of the width W and the distance d**1** is about 10% to about 50% of the distance d**2**. If the sum (W+d**1**) is lower than about 10%, the NLDD **182** is too short to effectively suppress the Kirk effect; if the sum (W+d**1**) is greater than about 50%, the NLDD **182** may be close to the gate structure **160**, resulting in a low off-state breakdown voltage.

[0053] The semiconductor device further includes an RP layer **210** above the gate structure **160** and the drift region **152**. The RP layer **210** extends over a portion of the gate structure **160** and over the drain region. The RP layer **210** is in contact with the NLDD **182**. Reference is made to FIGS. **1**O and **2**. The substrate device further includes the SHN **154**, the SHPs **156***a*-**156***c,* the HVPBs **158**, and isolation structures **142**, **144**, and **146**. The isolation structures **142**, **144**, and **146**, the SHN **154** and the SHPs **156***a*-**156***c* are ring-shaped. The SHP **156** surrounds the isolation structure **146**, the isolation structure **146** surrounds the SHN **154**, the SHN **154** surrounds the isolation structure **144**, the isolation structure **144** surrounds the SHP **156***b,* SHP **156***b* surrounds the isolation structure **142**, and the isolation structure **142** surrounds the NDD **152**, the SHP **156***a,* the HVPBs **158**, and the structures formed thereon. The drain region is in contact with the isolation structure **142**, and the NLDD **182** is spaced apart from the isolation structure **142**. In some embodiments, the depths of the NLDD **182** and the drain region are both less than the depth of the isolation structure **142**. That is, the bottom surface **182***b* of the NLDD **182** is above the bottom surface **142***b* of the isolation structure **142**.

[0054] Since the NLDD **182** is formed between the gate structure **160** and the N-type source/drain regions **184***a,* the Kirk effect occurred at the drain side can be suppressed. Furthermore, the NLDD **182** also provides good Vd vs. Id tailing performance. Moreover, the NLDD **182** does not complicate the manufacturing process for forming the semiconductor device.

[0055] FIG. **3** is a cross-sectional view of a semiconductor device according to various embodiments. The difference between the semiconductor devices in FIGS. **3** and **1**O pertains to the position of the NLDD **182**. In FIG. **3**, the NLDD **182** is in contact with the N-type source/drain regions **184***a.* That is, the distance d**1** (see FIG. **1**J) is 0. Other relevant structural details of the semiconductor device in FIG. **3** are similar to the semiconductor device in FIG. **1**O, and, therefore, a description in this regard will not be repeated hereinafter.

[0056] FIG. **4** is a drain voltage (Vd) vs. drain current (Id) curve of the semiconductor devices at off-state according to some embodiments of the present disclosure, and FIG. **5** is a Vd vs. Id curve of the semiconductor devices at on-state according to some embodiments of the present disclosure. In FIG. **4**, the breakdown voltage at off-state (BVoff) is about 33 V. In FIG. **5**, the breakdown voltage at on-state (BVon) is about 32 V. Further, FIG. **5** shows a good Id-Vd tailing performance.

[0057] FIGS. **6**A and **6**B are cross-sectional views of semiconductor devices according to various embodiments. The difference between the semiconductor devices in FIGS. **6**A and **1**O pertains to the conductivity types of the wells. Specifically, in FIGS. **6**A and **6**B, the semiconductor device includes a semiconductor substrate **310**, a DPW **320**, and a DNW **330**. The semiconductor substrate **310** is an n-substrate. In some embodiments, the semiconductor device further includes a gate structure **160**, isolation structures **142**, **144**, and **146**, a PDD **352**, a SHP **354**, SHNs **356***a,* **356***b,* and **356***c,* and HVNBs **358**. In some embodiments, the

semiconductor device further includes a PLDD **382**, P-type source/drain regions **384***a* and **384***c*, P-type pick-up region **384***b*, and N-type pick-up regions **392***a*, **392***b*, **392***c*. The semiconductor device further includes an RP layer **210**, metal alloy layers **220**, an ILD **230**, and contacts **242**, **244**, **246**, **248**, **252**, and **254**. In some embodiments, the PLDD **382** is spaced apart from the P-type source/drain regions **384***a* as shown in FIG. **6**A. In some other embodiments, the PLDD **382** is in contact with the P-type source/drain regions **384***a* as shown in FIG. **6**B. Other relevant structural details of the semiconductor device in FIGS. **6**A and **6**B are similar to the semiconductor device in FIG. **1**O, and, therefore, a description in this regard will not be repeated hereinafter.

[0058] FIGS. **7**A and **7**B are cross-sectional views of semiconductor devices according to various embodiments. The difference between the semiconductor devices in FIGS. **7**A and **1**O pertains to the presence of a pocket (doped) region. In FIGS. **7**A and **7**B, a P-type pocket region **186** is formed under the NLDD **182**. That is, the P-type pocket region **186** and the NLDD **182** have different conductivity types. The P-type pocket region **186** is configured for isolating the NLDD **182**. In some embodiments, the P-type pocket region **186** may be formed in the process shown in FIG. **1**H and before the formation of the NLDD **182**. The P-type pocket region **186** and the NLDD **182** may have substantially the same width. In some embodiments, the P-type pocket region **186** has a depth D**10** in a range of about 0.4 um to about 0.6 um, and the dopant concentration of the P-type pocket region **186** is between about 10^{17} and about 10^{19} per cubic centimeter. In some embodiments, the P-type pocket region **186** and the NLDD **182** have substantially the same or similar dopant concentration. Other relevant structural details of the semiconductor device in FIGS. **7**A and **7**B are similar to the semiconductor device in FIG. **1**O, and, therefore, a description in this regard will not be repeated hereinafter. In some other embodiments, an N-type pocket region may be formed under the PLDD **382** in FIGS. **6**A and/or **6**B, and the detailed description will not be repeated hereinafter.

[0059] FIG. **8** is a flow chart of a method M**1** for forming a semiconductor device in accordance with some embodiments of the present disclosure. Although the method M**1** is illustrated and/or described as a series of acts or events, it will be appreciated that the method is not limited to the illustrated ordering or acts. Thus, in some embodiments, the acts may be carried out in different orders than illustrated, and/or may be carried out concurrently. Further, in some embodiments, the illustrated acts or events may be subdivided into multiple acts or events, which may be carried out at separate times or concurrently with other acts or sub-acts. In some embodiments, some illustrated acts or events may be omitted, and other un-illustrated acts or events may be included.

[0060] At block S**12**, DNW, DPW, and isolation structures are formed in a substrate. FIGS. **1**A-**1**C illustrate perspective views and cross-sectional views of some embodiments corresponding to act in block S**12**. At block S**14**, NDD, SHN, and SHP are formed in the substrate. FIG. **1**D illustrates perspective views and cross-sectional views of some embodiments corresponding to act in block S**14**. At block S**16**, HVPBs are formed in a substrate. FIGS. **1**E-**1**F illustrate perspective views and cross-sectional views of some embodiments corresponding to act in block S**16**. At block S**18**, a gate structure is formed above the substrate. FIG. **1**G illustrates perspective views and cross-sectional views of some embodiments corresponding to act in block S**18**. At block S**20**, an NLDD is formed in the NDD. FIG. **1**H illustrates perspective views and cross-sectional views of some embodiments corresponding to act in block S**20**. At block S**22**, N-type source/drain regions and P-type source/drain regions are formed in the substrate. FIGS. **1**J-**1**K illustrate perspective views and cross-sectional views of some embodiments corresponding to act in block S**22**. At block S**24**, an RP layer is formed above the gate structure and the NLDD. FIGS. **1**L-**1**M illustrate perspective views and cross-sectional views of some embodiments corresponding to act in block S**24**. At block S**26**, metal alloy layers are respectively formed above the gate structure, the N-type source/drain regions, and the P-type source/drain regions. FIG. **1**N illustrate perspective views and cross-sectional views of some embodiments corresponding to act in block S**26**. At block S**28**, contacts are respectively formed above the metal alloy layers. FIG. **1**O illustrate perspective views and cross-sectional views of some embodiments corresponding to act in block S**28**. In some embodiments, a process that forming a pocket region in the NDD is performed between the blocks S**18** and S**20**.

[0061] Based on the above discussions, it can be seen that the present disclosure offers advantages. It is understood, however, that other embodiments may offer additional advantages, and not all advantages are necessarily disclosed herein, and that no particular advantages are required for all embodiments. One advantage is that the NLDD improves the Kirk effect occurring at the drain side. As such, the off-state breakdown voltage, the on-state breakdown voltage, and the Id-Vd tailing performances are improved. Another advantage is that the NLDD does not complicate the manufacturing process for forming the semiconductor device.

[0062] According to some embodiments, a semiconductor device includes a substrate, a gate structure, a drift region, a source region, a drain region, and a doped region. The gate structure is above the substrate. The drift region is in the substrate and under the gate structure. The source region and the drain region are on opposite sides of the gate structure. The drain region is in the drift region, and the source region is outside the drift region. The doped region is in the drift region and between the drain region and the gate structure. The doped region is spaced apart from a bottom surface of the drain region.

[0063] According to some embodiments, a semiconductor device includes a substrate, a drift region, a gate structure, a source region, a drain region, an isolation structure, and a doped region. The drift region is in the substrate. The gate structure is above the drift region. The source region and the drain region are on opposite sides of the gate structure. The drain region is in the drift region. The isolation structure is in contact with the drain region and the drift region. The doped region is in the drift region and between the drain region and the gate structure. The doped region and the drain region have the same conductivity type, and a bottom surface of the doped region is above a bottom surface of the isolation structure.

[0064] According to some embodiments, a method for manufacturing a semiconductor device includes forming a drift region in a substrate. A gate structure is formed above the drift region. A doped region is formed in the drift region. A source region and a drain region are formed on opposite

sides of the gate structure and in the drift region. The doped region is formed between the gate structure and the drain region.

[0065] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same puRPses and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A semiconductor device comprising:
- a gate structure over a semiconductor substrate;
- a drift region in the semiconductor substrate and laterally extending past a first side of the gate structure;
- a source region in the semiconductor substrate and adjacent a second side of the gate structure opposite the first side;
- a drain region in the drift region;
- a first doped region in the drift region and between the drain region and the gate structure; and
- a second doped region within the drift region, the second doped region forming a P-N junction with the first doped region at a bottom surface of the first doped region.

2. The semiconductor device of claim **1**, wherein the first doped region is of a same conductivity type as the source region.

3. The semiconductor device of claim **1**, wherein the second doped region is of a different conductivity type from the source region.

4. The semiconductor device of claim **1**, wherein the second doped region is laterally spaced apart from the drain region.

5. The semiconductor device of claim **1**, wherein the second doped region has a width substantially the same as a width of the first doped region.

6. The semiconductor device of claim **1**, wherein the second doped region has a dopant concentration substantially the same as a dopant concentration of the first doped region.

7. The semiconductor device of claim **1**, wherein the second doped region has a bottom surface higher than a bottom surface of the drift region.

8. The semiconductor device of claim **1**, wherein the second doped region has a depth in a range of about 0.4 um to about 0.6 um.

9. The semiconductor device of claim **1**, wherein the second doped region has a dopant concentration between about 10^{17} and about 10^{19} per cubic centimeter.

10. A semiconductor device, comprising:
- a semiconductor substrate;
- a drift region in the semiconductor substrate;
- a gate structure overlapping at least a portion of the drift region;
- a source region and a drain region on opposite sides of the gate structure, wherein the drain region is in the drift region, and the source region is outside the drift region;
- a first doped region in the drift region and between the drain region and the gate structure; and
- a second doped region in the drift region, the second doped region having a conductivity type opposite a conductivity type of the first doped region, wherein the second doped region is in contact with the first doped region and spaced apart from the drain region by the drift region.

11. The semiconductor device of claim **10**, wherein the second doped region is entirely below the first doped region.

12. The semiconductor device of claim **10**, wherein the second doped region has a side surface aligned with a side surface of the first doped region.

13. The semiconductor device of claim **12**, wherein the side surface of the first doped region is spaced apart from the drain region by the drift region.

14. The semiconductor device of claim **12**, wherein the side surface of the first doped region interfaces the drain region.

15. The semiconductor device of claim **10**, wherein the second doped region has a dopant concentration greater than a dopant concentration of the drift region.

16. A semiconductor device, comprising:
- a gate structure over a semiconductor substrate;
- a drift region in the semiconductor substrate extending past a first side of the gate structure;
- a source region in vicinity of a second side of the gate structure opposite the first side;
- a drain region in the drift region;
- an n-type doped region in the drift region and between the drain region and the source region; and
- a p-type doped region in the drift region, the p-type doped region being entirely below the n-type doped region.

17. The semiconductor device of claim **16**, further comprising:
- a p-type implanted region directly below the gate structure, the p-type implanted region abutting the drift region and having a dopant concentration greater than a dopant concentration of the drift region.

18. The semiconductor device of claim **17**, wherein the p-type implanted region is spaced apart from the n-type doped region.

19. The semiconductor device of claim **17**, wherein the p-type implanted region is spaced apart from the p-type doped region.

20. The semiconductor device of claim **16**, wherein the p-type doped region has a same width as the p-type doped region.

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