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(54) **NOISE SIMULATION SYSTEM**

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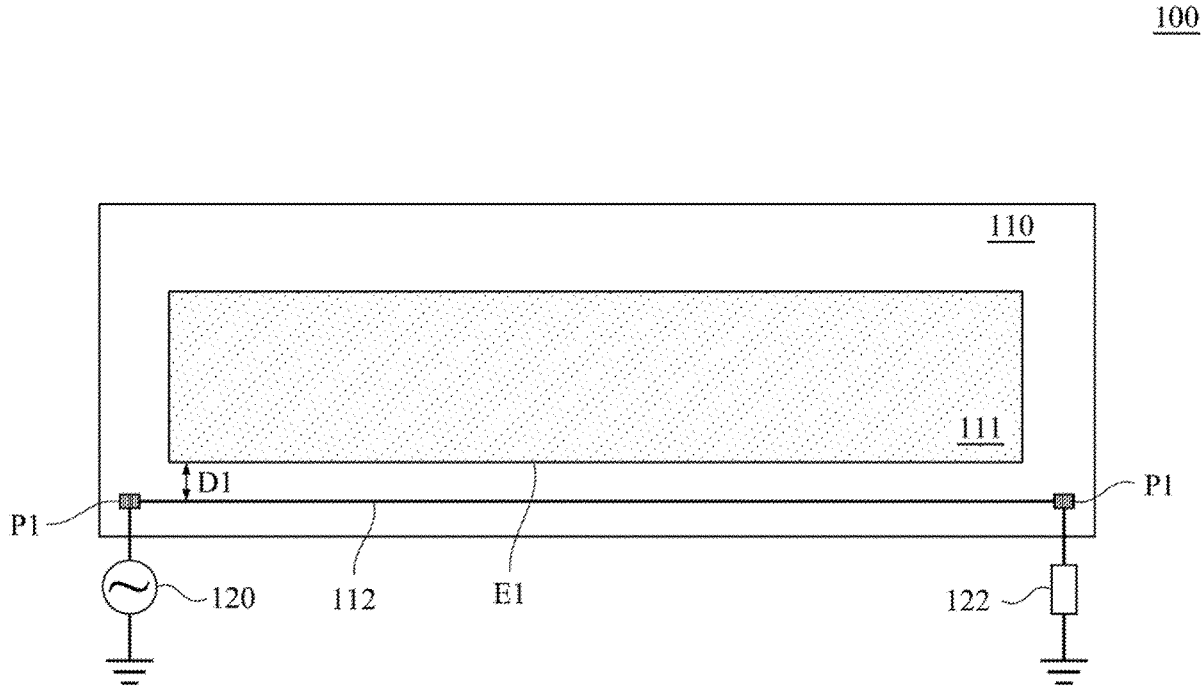
(57) **ABSTRACT**

The disclosure provides a system to simulate a simulated noise on the power zone block of a substrate. The system comprises a signal trace and a signal generating circuit. The signal trace is disposed adjacent to the power zone block. The signal generating circuit is electrically coupled to the signal trace, configured to transmit an alternating current signal over the signal trace. The alternating current signal transmitted over the signal trace is configured to induce a simulated noise on the power zone block, and a waveform of the simulated noise is determined by a frequency of the alternating current signal.



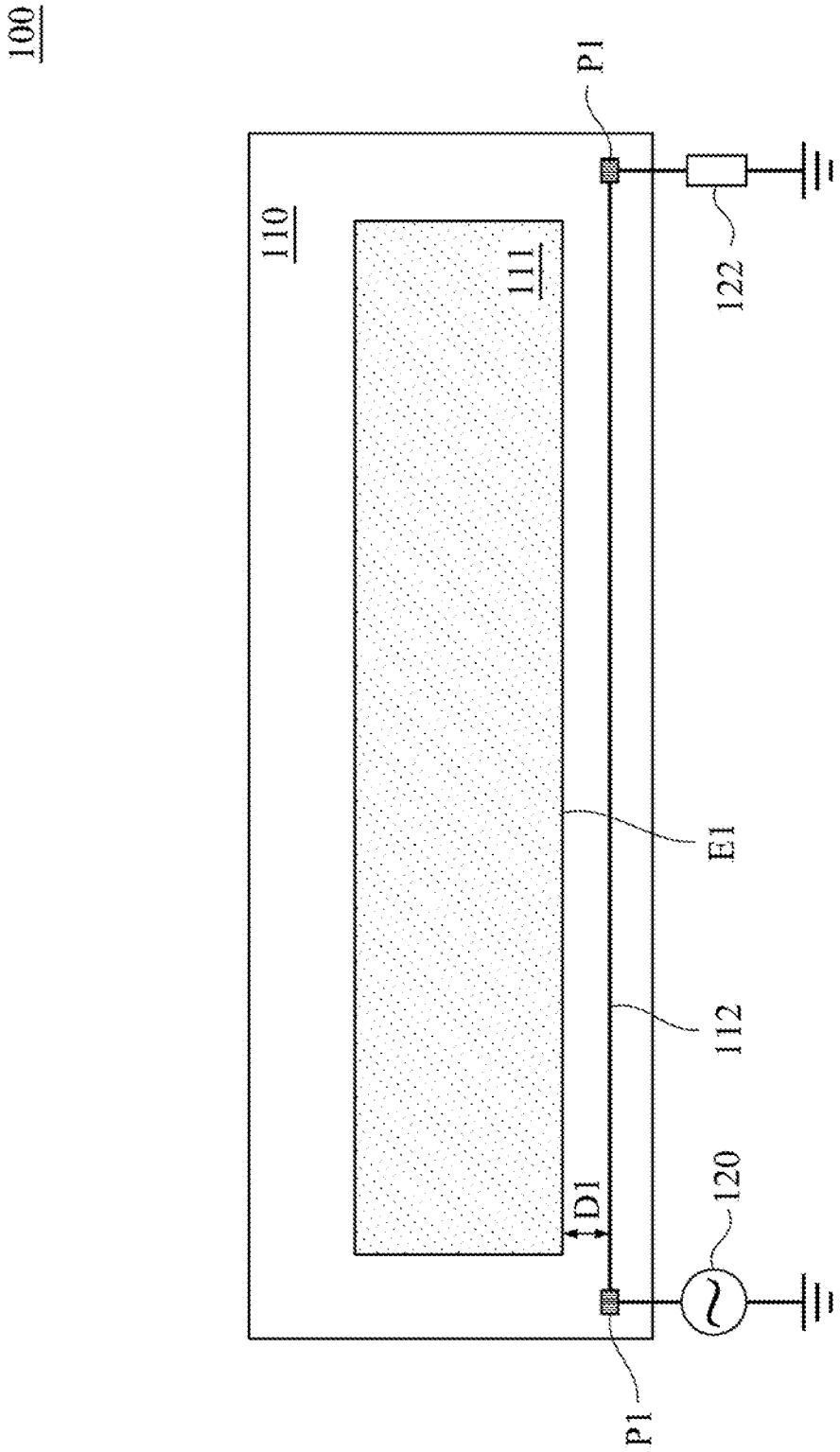


Fig. 1

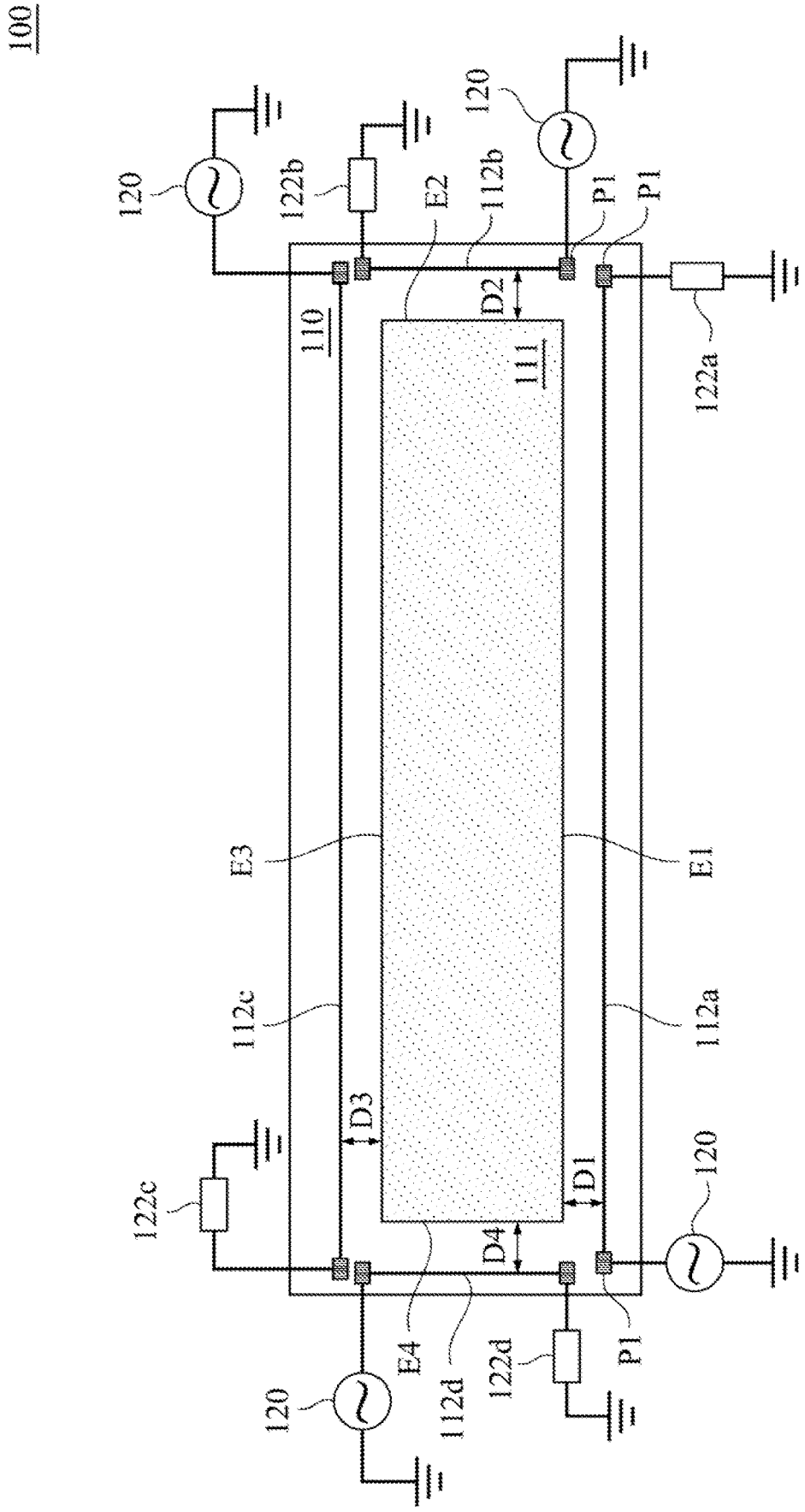

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Fig. 2

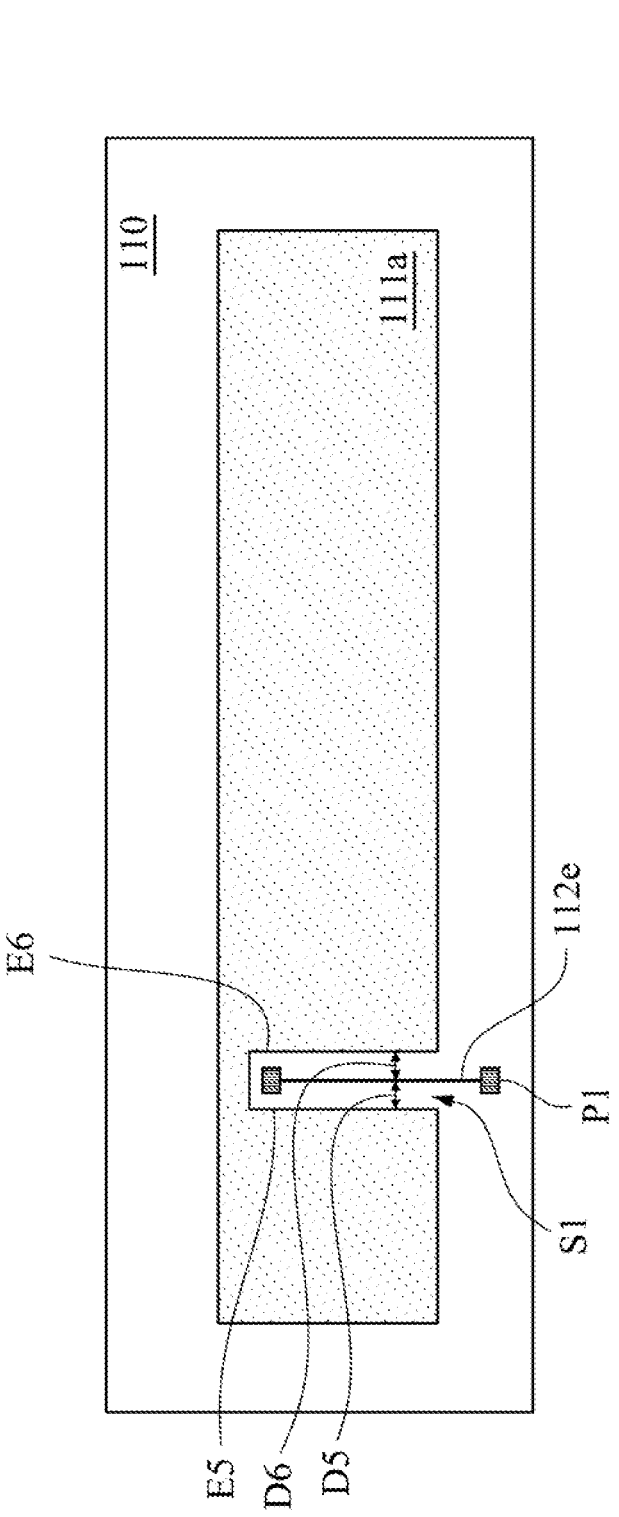

Fig. 3

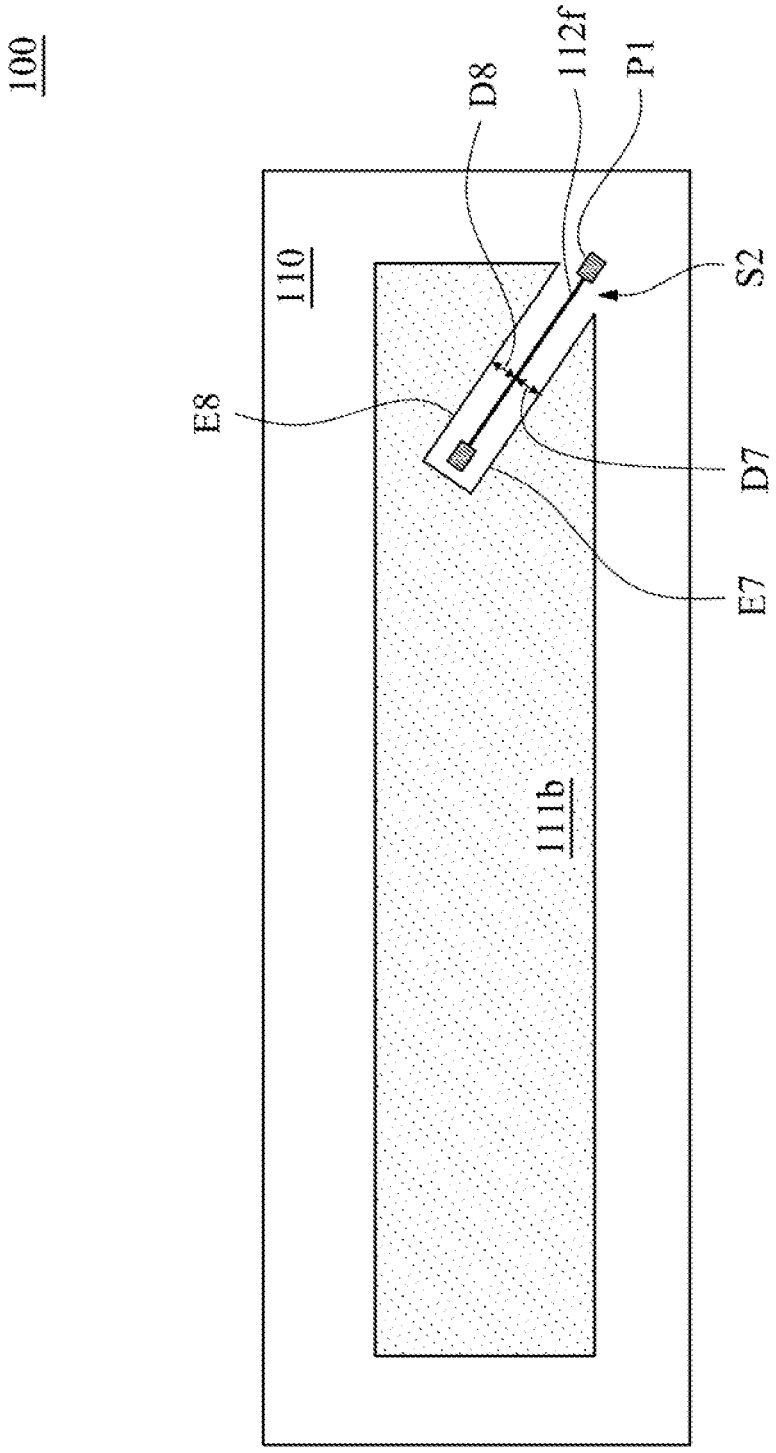

Fig. 4

NOISE SIMULATION SYSTEM

RELATED APPLICATIONS

[0001] This present application is a continuation application of U.S. patent application Ser. No. 17/378,799, filed Jul. 19, 2021, which is herein incorporated by reference in their entirety.

BACKGROUND

Field of Invention

[0002] The present invention relates to a noise simulation technology. More particularly, the present invention relates to a noise simulation system.

Description of Related Art

[0003] With the rapid advancement in high-speed data processing and computing technologies, the operation frequency of the IC chip is higher. In some cases, the design of the power transmit system in the printed circuit, such as the power plane and the ground plane, is associated to a power supply noise (i.e., a simultaneous switching noise) which may cause the IC chip cannot operate normally. Therefore, how to observe and simulate the power supply noise transmitted to the power plane of the designed printed circuit board is important. However, it is hard to directly generate the power supply noise on the power plane of the printed circuit board in a laboratory. Accordingly, what is needed is a noise simulation system to address the issues mentioned above.

SUMMARY

[0004] An aspect of the present invention is to provide a system capable for simulating a noise on the power zone block of a substrate. The system comprises a signal trace and a signal generating circuit. The signal trace is disposed adjacent to the power zone block. The signal generating circuit is electrically coupled to the signal trace, configured to transmit an alternating current signal over the signal trace. The alternating current signal transmitted over the signal trace is configured to induce a simulated noise on the power zone block, and a waveform of the simulated noise is determined by a frequency of the alternating current signal.

[0005] Another aspect of the present invention is to provide a system capable for simulating a noise on the power zone block of a substrate. The system comprises a plurality of signal traces and a signal generating circuit. The signal traces are disposed adjacent to a plurality of edges of the power zone block, respectively. The signal generating circuit is electrically coupled to the signal traces, configured to transmit a plurality of alternating current signals with different frequencies over the signal traces, respectively. The alternating current signals transmitted over the signal trace is configured to induce a simulated noise on the power zone block, wherein a waveform of the simulated noise is determined by the alternating current signals with different frequencies.

[0006] These and other features, aspects, and advantages of the present invention will become better understood with reference to the following description and appended claims.

[0007] In summary, the noise simulation system can generate the simulation noise on the power zone block of the substrate, by transmitting the alternating current signal over the signal trace, to simulate the power supply noise in actual situation.

[0008] It is to be understood that both the foregoing general description and the following detailed description are by examples, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The invention can be more fully understood by reading the following detailed description of the embodiment, with reference made to the accompanying drawings as follows:

[0010] FIG. **1** is a schematic diagram of a noise simulation system in some embodiments of the present disclosure;

[0011] FIG. **2** is a schematic diagram of a noise simulation system in some embodiments of the present disclosure;

[0012] FIG. **3** is a schematic diagram of a noise simulation system in some embodiments of the present disclosure; and

[0013] FIG. **4** is a schematic diagram of a noise simulation system in some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0014] Reference will now be made in detail to the present embodiments of the disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0015] Reference is made to FIG. **1**. FIG. **1** is a schematic diagram of a noise simulation system **100** in some embodiments of the present disclosure. The noise simulation system **100** includes a substrate **110**, a signal trace **112**, a signal generating circuit **120** and a resistor **122**. The substrate **110** may be implemented as a printed circuit board. In some embodiments of the disclosure, memory element, such as any type of random access memory, may be furnished on the substrate **110** (i.e., printed circuit board) to form a memory module (not shown). For example, the memory element may be implemented as static RAM, dynamic RAM, synchronous DRAM, Rambus DRAM, doble data rate RAM, or any other type of RAM.

[0016] The substrate **110**, such as a printed circuit board, often includes planar layers of electrically conductive material separated by layers of dielectric material. One of the conductive layers may be considered as a power plane, and another of the conductive layers may be considered as a ground plane. A portion of the one of the conductive layers which is considered as the power plane can be patterned to form an electrically conductive power zone block **111**. The power zone block **111** typically extends generally parallel to the plane of the substrate **110**.

[0017] In actual computer system, when the memory element (i.e., DRAM) is operating, a noise (i.e., a power supply noise or a simultaneous switching noise) may be transmitted to the power zone block **111**. However, it is hard to directly provide the noise to the power zone block **111** in the lab.

[0018] To consider the noise induced to the power zone block **111** in the actual situation, the signal generating circuit **120** is configured to generate an alternative current signal and transmit the alternative current signal over the signal trace to simulate a simulated noise on the power noise according to the alternative current signal. In other words,

the signal trace **112**, the signal generating circuit **120** and the resistor **122** can be consider as a noise simulation module. How to simulate a noise on the power zone lock will be described in detail in following embodiment.

[0019] In structure, the signal trace **112** is disposed adjacent to an edge E**1** of the power zone block **111**, and the signal trace **112** extends in parallel with the edge E**1** of the power zone block **111**. The signal generating circuit **120** and the resistor **122** are respectively coupled to two terminals of the signal trace **112**. Specifically, a first terminal of the signal generating circuit **120** is electrically coupled to a first terminal of the signal trace **112**. A first terminal of the resistor **122** is electrically coupled to a second terminal of the signal trace **112**. The second terminals of each of the signal generating circuit **120** and the resistor **122** are grounded.

[0020] The signal generating circuit **120** is configured to transmit the alternating current signal, which is a single-end signal, over the signal trace **112**. The alternating current signal transmitted over the signal trace **112** is configured to induce a simulated noise on the power zone block **111**. A waveform of the simulated noise is determined by a frequency of the alternating current signal controlled by the signal generating circuit **120**. In some embodiments, the waveform of the simulated noise can be detected by an EMI scanning device.

[0021] In addition, when the signal generating circuit **120** adjusts the frequency of the alternating current signal, the waveform of the simulated noise is detected by the EMI scanning device, simultaneously, such that a resonance frequency of the power zone block **111** can be determined according to the variety of the waveform of the simulated noise. In some embodiments, the frequency of the alternating current signal can be controlled in a range of 100 kHz~1 MHz. In addition, a resistance of the resistor **122** can be controlled to form a standing wave on the signal trace **112**, according to the alternating current signal, to induce the simulated noise on the power zone block **111**. In some embodiments, resistance of the resistor **122** can be 0 Ohm, 50 Ohm or 10000 Ohm.

[0022] It should be noted that, a distance D**1** between the signal trace **112** and the edge E**1** of the power zone block **111** is less than a threshold value, such that the simulated noise on the power zone block **111** can be induced from the alternating current signal transmitted over the signal trace **112**, wherein the threshold value is less than 10 micrometer.

[0023] In some embodiments, the power zone block **111** and the signal trace **112** may be disposed in the same conductive layer, and each terminal of the signal trace **112** is electrically coupled to a pad P**1** through vertical trace. During the noise simulation operation, the signal generating circuit **120** is electrically coupled to the first terminal of the signal trace **112** through the pad P**1**, and the resistor **122** is electrically coupled to the second terminal of the signal trace **112** through another pad P**1**. After the noise simulation operation, the signal generating circuit **120** and the resistor **122** can be removed from the substrate **110**. In this case, a distance D**1** between an edge E**1** of the power zone block **111** and the signal trace **112** can be set in a range of 1~10 micrometer.

[0024] In other embodiments, the signal trace **112**, the signal generating circuit **120** and the resistor **122** may be disposed on a support, and the support may be controlled to adjust the distance D**1** between the edge E**1** of the power zone block **111** and the signal trace **112** in a range of 1~10 micrometer.

[0025] Reference is made to FIG. **2**. FIG. **2** is a schematic diagram of a noise simulation system **100** in some embodiments of the present disclosure. The noise simulation system **100** includes a substrate **110**, signal traces **112***a*~**112***d*, a signal generating circuit **120** and resistors **122***a*~**122***d*.

[0026] In structure, the signal trace **112***a* is disposed adjacent to an edge E**1** of the power zone block **111**, and the signal trace **112***a* extends in parallel with the edge E**1** of the power zone block **111**. The signal generating circuit **120** and the resistor **122***a* are respectively coupled to two terminals of the signal trace **112***a*. The signal trace **112***b* is disposed adjacent to an edge E**2** of the power zone block **111**, and the signal trace **112***b* extends in parallel with the edge E**2** of the power zone block **111**. The signal generating circuit **120** and the resistor **122***b* are respectively coupled to two terminals of the signal trace **112***b*.

[0027] The signal trace **112***c* is disposed adjacent to an edge E**3** of the power zone block **111**, and the signal trace **112***c* extends in parallel with the edge E**3** of the power zone block **111**. The signal generating circuit **120** and the resistor **122***c* are respectively coupled to two terminals of the signal trace **112***c*. The signal trace **112***d* is disposed adjacent to an edge E**4** of the power zone block **111**, and the signal trace **112***d* extends in parallel with the edge E**4** of the power zone block **111**. The signal generating circuit **120** and the resistor **122***d* are respectively coupled to two terminals of the signal trace **112***d*.

[0028] Specifically, the signal generating circuit **120** is electrically coupled to a first terminal of each of the signal traces **112***a*~**112***d*. The first terminals of each of the resistor **122***a*~**122***d* are electrically coupled to a second terminal of the signal traces **112***a*~**112***d*, respectively. The second terminals of each of the resistor **122** are grounded.

[0029] Similarly, the signal generating circuit **120** is configured to transmit the alternating current signals with different frequencies, which are a single-end signal, over the signal trace **112***a*~**112***d*, respectively. The alternating current signals transmitted over the signal trace **112***a*~**112***d* are configured to induce a simulated noise on the power zone block **111**. A waveform of the simulated noise is determined by the frequencies of the alternating current signals controlled by the signal generating circuit **120**. In some embodiments, the waveform of the simulated noise can be detected by an EMI scanning device.

[0030] In addition, when the signal generating circuit **120** adjusts the frequencies of the alternating current signals, the waveform of the simulated noise is detected by the EMI scanning device, simultaneously, such that a resonance frequency of the power zone block **111** can be determined according to the variety of the waveform of the simulated noise. In some embodiments, the frequency of the alternating current signal can be controlled in a range of 100 kHz~1 MHz. In addition, resistances of the resistor **122***a*~**122***e* can be respectively controlled to form standing waves on the signal trace **112***a*~**112***e* to induce the simulated noise on the power zone block **111** according to the alternating current signals. In some embodiments, resistances of the resistors **122***a*~**122***e* can be 0 Ohm, 50 Ohm or 10000 Ohm.

[0031] It should be noted that, the distances D**1**~D**4** between the signal traces **112***a*~**112***d* and edges E**1**~E**4** of the power zone block **111** is less than a threshold value, such

that the simulated noise on the power zone block **111** can be induced from the alternating current signals transmitted over the signal traces **112**~**112***d*, wherein the threshold value is less than 10 micrometer.

[0032] In some embodiments, the power zone block **111** and the signal traces **112***a*~**112***d* may be disposed in the same conductive layer, and each terminal of the signal traces **112***a*~**112***d* are electrically coupled to a pad P**1** through vertical trace. During the noise simulation operation, the signal generating circuit **120** is electrically coupled to the first terminal of the signal traces **112***a*~**112***d* through the corresponding pad P**1**, and the resistors **122***a*~**122***d* are electrically coupled to the second terminal of the signal traces **112***a*~**112***d* through another corresponding pad P**1**. After the noise simulation operation, the signal generating circuit **120** and the resistors **122***a*~**122***d* can be removed from the substrate **110**. In this case, distances D**1**~D**4** between edges E**1**~E**4** of the power zone block **111** and the signal traces **112***a*~**112***d* can be set in a range of 1~10 micrometer.

[0033] In other embodiments, the signal trace **112***a*~**112***d*, the signal generating circuit **120** and the resistor **122***a*~**122***d* may be disposed on a support, and the support may be controlled to adjust the distances D**1**~D**4** between the edges E**1**~E**4** of the power zone block **111** and the signal trace **112***a*~**112***d* in a range of 1~10 micrometer.

[0034] Reference is made to FIG. **3**. FIG. **3** is a schematic diagram of a noise simulation system **100** in some embodiments of the present disclosure. The noise simulation system **100** includes a substrate **110**, a signal trace **112***e*.

[0035] In structure, the signal trace **112***e* is disposed adjacent to a side E**5** of a slit S**1** on the power zone block **111***a*, and the signal trace **112***e* extends in parallel with the side E**5** of the slit S**1** on the power zone block **111***a*. The signal generating circuit **120** (not shown in FIG. **3**) and the resistor **122** (not shown in FIG. **3**) can be respectively coupled to two terminals of the signal trace **112***e* through the corresponding pad P**1**. The signal generating circuit **120** and the resistor **122** are described in the embodiment of FIG. **1**, thus the description is omitted.

[0036] Similarly, the signal generating circuit **120** (not shown in FIG. **3**) is configured to transmit the alternating current signal which, is a single-end signal, over the signal trace **112***e*. The alternating current signal transmitted over the signal trace **112***e* is configured to induce a simulated noise on the power zone block **111***a*. A waveform of the simulated noise is determined by the frequencies of the alternating current signal controlled by the signal generating circuit **120**. In some embodiments, the waveform of the simulated noise can be detected by an EMI scanning device.

[0037] It should be noted that, the distances D**5**~D**6** between the signal trace **112***e* and sides E**5** and E**6** of the slit S**1** on the power zone block **111***a* is less than a threshold value, such that the simulated noise on the power zone block **111***a* can be induced from the alternating current signal transmitted over the signal traces **112***e*, wherein the threshold value is less than 10 micrometer.

[0038] In this way, no matter what shape the power zone block **111***a* is, the simulated noise can be induced on the power zone block **111***a* by transmitting the alternating current signal over the signal trace **112***e*, so that the waveform of the simulated noise can be detected by the EMI scanning device.

[0039] In some embodiments, the power zone block **111***a* and the signal trace **112***e* may be disposed in the same conductive layer, and each terminal of the signal trace **112***e* is electrically coupled to a pad P**1** through vertical trace. During the noise simulation operation, the signal generating circuit **120** (not shown in FIG. **3**) is electrically coupled to the first terminal of the signal trace **112***e* through the pad P**1**, and the resistor **122** (not shown in FIG. **3**) is electrically coupled to the second terminal of the signal trace **112***e* through another pad P**1**. After the noise simulation operation, the signal generating circuit **120** (not shown in FIG. **3**) and the resistor **122** (not shown in FIG. **3**) can be removed from the substrate **110**. In this case, a distance D**5** between an edge E**5** of the power zone block **111***a* and the signal trace **112***e* can be set in a range of 1~10 micrometer.

[0040] In other embodiments, the signal trace **112***e*, the signal generating circuit **120** (not shown in FIG. **3**) and the resistor **122** (not shown in FIG. **3**) may be disposed on a support, and the support may be controlled to adjust the distance D**5** between the edge E**5** of the power zone block **111** and the signal trace **112***e* in a range of 1~10 micrometer.

[0041] Reference is made to FIG. **4**. FIG. **4** is a schematic diagram of a noise simulation system **100** in some embodiments of the present disclosure. The noise simulation system **100** includes a substrate **110**, a signal trace **112***f*. The substrate **110** has a power zone block **111***b* with a slit S**2** on a corner.

[0042] In structure, the signal trace **112***f* is disposed adjacent to a side E**7** of the slit S**2** on the power zone block **111***b*, and the signal trace **112***f* extends in parallel with the side E**7** of the slit S**2** on the power zone block **111***b*. The signal generating circuit **120** (not shown in FIG. **4**) and the resistor **122** (not shown in FIG. **4**) can be respectively coupled to two terminals of the signal trace **112***f* through the corresponding pad P**1**. The signal generating circuit **120** and the resistor **122** are described in the embodiment of FIG. **1**, thus the description is omitted.

[0043] Similarly, the signal generating circuit **120** (not shown in FIG. **4**) is configured to transmit the alternating current signal, which is a single-end signal, over the signal trace **112***f*. The alternating current signal transmitted over the signal trace **112***f* is configured to induce a simulated noise on the power zone block **111***b*. A waveform of the simulated noise is determined by the frequencies of the alternating current signal controlled by the signal generating circuit **120**. In some embodiments, the waveform of the simulated noise can be detected by an EMI scanning device.

[0044] It should be noted that, the distances D**7**~D**8** between the signal trace **112***f* and sides E**7** and E**8** of the slit S**2** on the power zone block **111***b* is less than a threshold value, such that the simulated noise on the power zone block **111***b* can be induced from the alternating current signal transmitted over the signal traces **112***f*, wherein the threshold value is less than 10 micrometer.

[0045] In some embodiments, the power zone block **111***b* and the signal trace **112***f* may be disposed in the same conductive layer, and each terminal of the signal trace **112***f* is electrically coupled to a pad P**1** through vertical trace. During the noise simulation operation, the signal generating circuit **120** (not shown in FIG. **4**) is electrically coupled to the first terminal of the signal trace **112***f* through the pad P**1**, and the resistor **122** (not shown in FIG. **4**) is electrically coupled to the second terminal of the signal trace **112***f* through another pad P**1**. After the noise simulation opera-

tion, the signal generating circuit **120** (not shown in FIG. **4**) and the resistor **122***f* (not shown in FIG. **4**) can be removed from the substrate **110**. In this case, a distance D**7** between an edge E**7** of the power zone block **111***b* and the signal trace **112***f* can be set in a range of 1~10 micrometer.

[0046] In other embodiments, the signal trace **112***e*, the signal generating circuit **120** (not shown in FIG. **4**) and the resistor **122** (not shown in FIG. **4**) may be disposed on a support, and the support may be controlled to adjust the distance D**5** between the edge E**5** of the power zone block **111** and the signal trace **112***e* in a range of 1~10 micrometer.

[0047] In summary, the noise simulation system **100** can generate the simulation noise on the power zone block **111**, **111***a* and **111***b* of the substrate **110** (i.e. printed circuit board), by transmitting the alternating current signal over the signal trace **112**, **112***a*~**112***f* respectively adjacent to the edge E**1**~E**8** of the power zone block **111**, **111***a* and **111***b*, to simulate the power supply noise in actual situation which is hard to generated by the power supply in lab. Furthermore, when the signal generating circuit **120** of the noise simulation system **100** adjusts the frequency of the alternating current signal, the waveform of the simulation noise on the power zone block **111**, **111***a* and **111***b* can be detected to determine the resonance frequency of the power zone block **111**, **111***a* and **111***b*.

[0048] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims.

What is claimed is:

1. A system capable for simulating a noise on a power zone block of a substrate, wherein the system comprising:

a signal trace, disposed in a slit of the power zone block, wherein the signal trace and the power zone block are disposed in the same conductive layer, and wherein the signal trace extends in parallel with a side of the slit of the power zone block; and

a signal generating circuit, electrically coupled to the signal trace, configured to transmit an alternating current signal over the signal trace,

wherein, the alternating current signal transmitted over the signal trace is configured to induce a simulated noise on the power zone block, wherein a waveform of the simulated noise is determined by a frequency of the alternating current signal.

2. The system of claim **1**, wherein the signal generating circuit is further configured to adjust the frequency of the alternating current signal, according to the waveform of the simulated noise, to determine a resonance frequency of the power zone block.

3. The system of claim **1**, wherein a distance between the signal trace and the side of the slit on the power zone block is less than a threshold value, such that the simulated noise on the power zone block is induced from the alternating current signal transmitted over the signal trace, wherein the threshold value is less than 10 micrometer.

4. The system of claim **1**, further comprising:

a resistor, with a first terminal electrically coupled to the signal trace, and a second terminal is grounded.

5. The system of claim **4**, wherein a resistance of the resistor is controlled to form a standing wave on the signal trace according to the alternating current signal.

6. The system of claim **1**, wherein the power zone block is disposed in a power layer of the substrate.

7. The system of claim **1**, wherein a plurality of memory cell is configured to install on an element interface of the substrate.

8. The system of claim **1**, wherein the alternating current signal is a single-end signal.

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