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(54) **DRIVING METHOD FOR PIXEL CIRCUIT**

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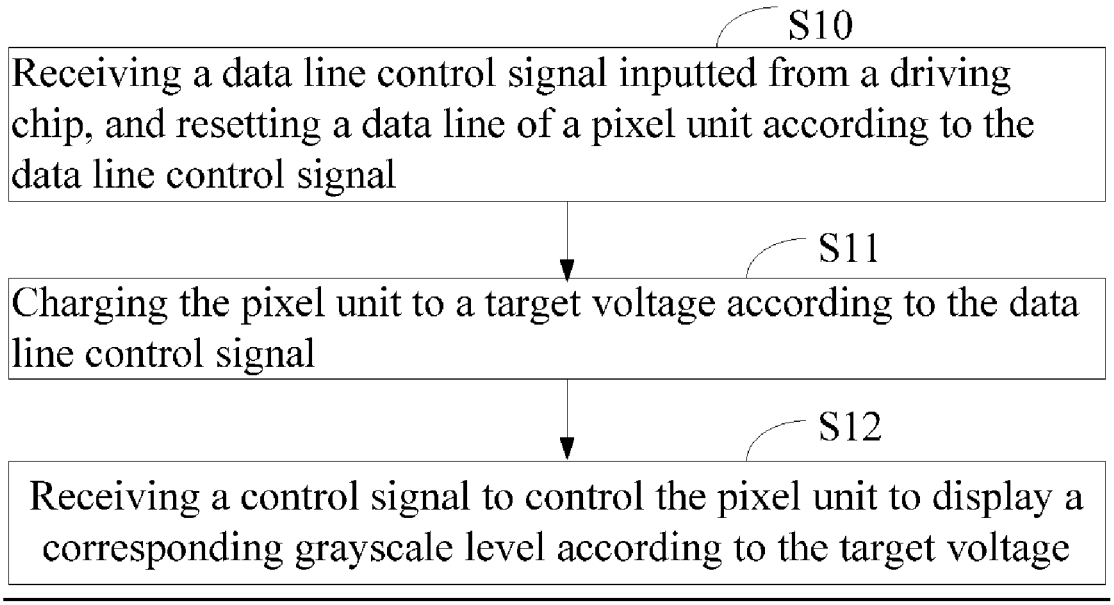
(57) **ABSTRACT**

A driving method for a pixel circuit comprises steps of: receiving a data control signal inputted by a driving chip and resetting a data line of a pixel unit according to the data control signal; charging the pixel unit to a target voltage according to the data line control signal; and receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage. Through above way, the present invention can prevent a wrong charging which will generate an abnormal picture display.



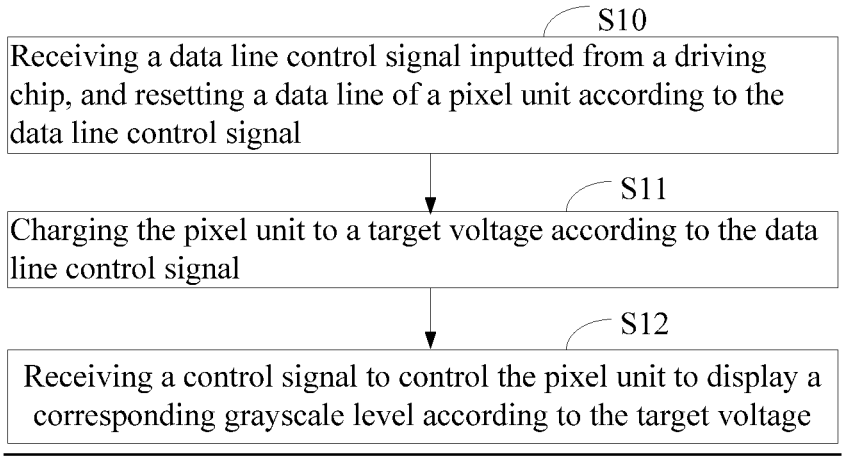

S10
Receiving a data line control signal inputted from a driving chip, and resetting a data line of a pixel unit according to the data line control signal
S11
Charging the pixel unit to a target voltage according to the data line control signal
S12
Receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage

FIG 1

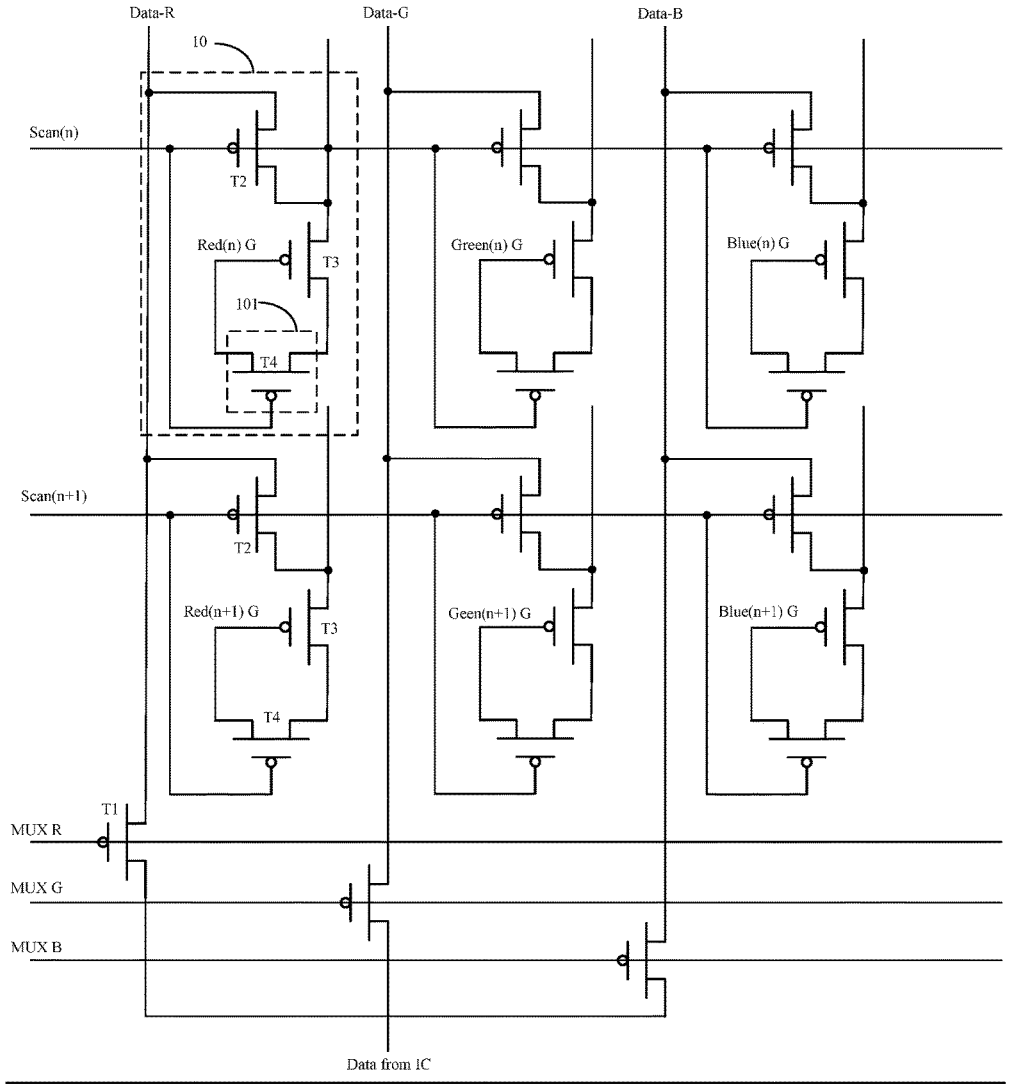

Data-R
Data-G
Data-B
10
Scan(n)
T2
Red(n) G
T3
Green(n) G
Blue(n) G
101
T4
Scan(n+1)
T2
Red(n+1) G
T3
Geen(n+1) G
Blue(n+1) G
T4
T1
MUX R
MUX G
MUX B
Data from IC

FIG 2

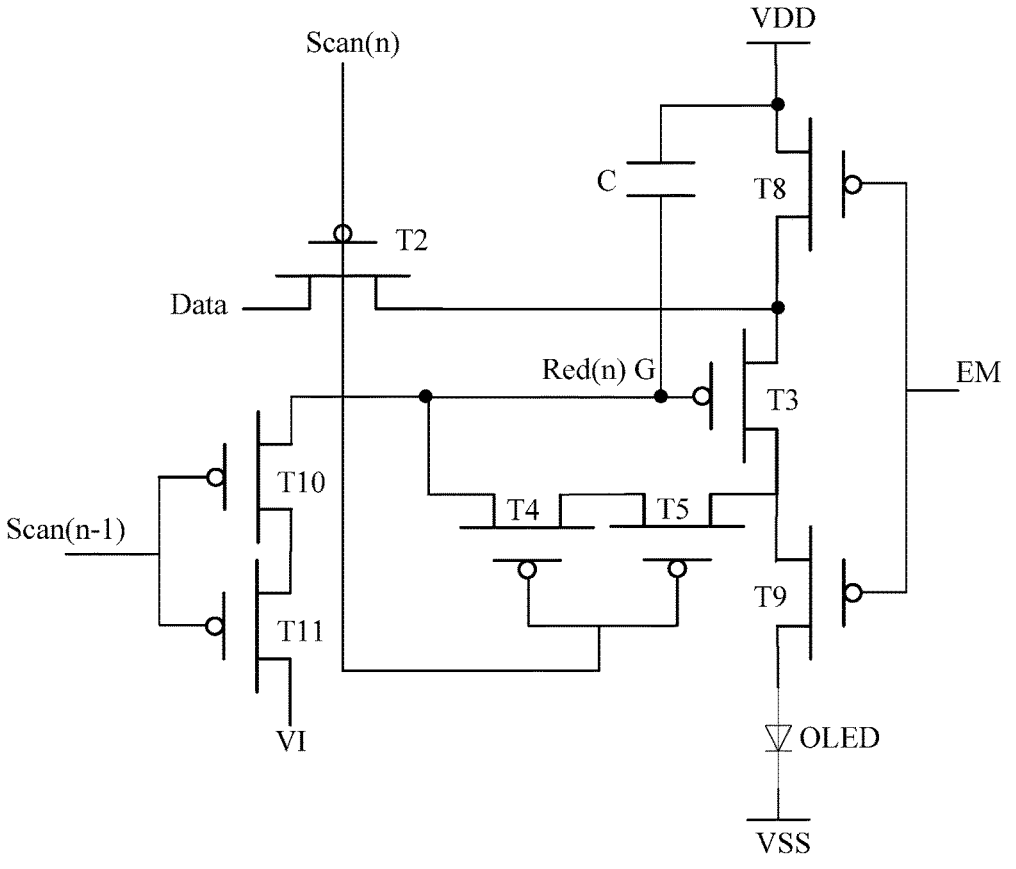

VDD
Scan(n)
C
T8
T2
Data
Red(n) G
T3
EM
T10
T4
T5
Scan(n-1)
T9
T11
VI
OLED
VSS

FIG 3

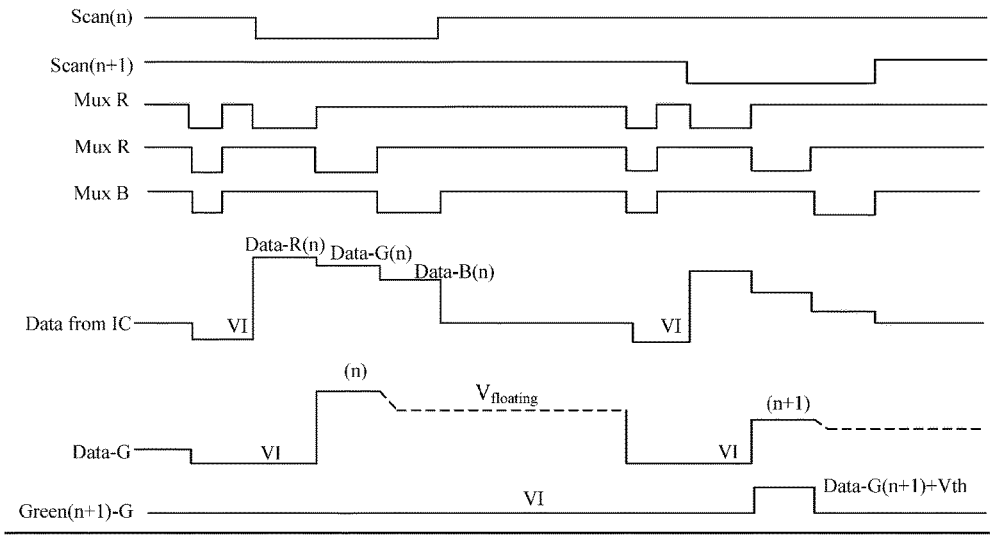

Scan(n)
Scan(n+1)
Mux R
Mux R
Mux B
Data-R(n)
Data-G(n)
Data-B(n)
Data from IC
VI
VI
(n)
$V_{floating}$
(n+1)
Data-G
VI
VI
VI
Data-G(n+1)+Vth
Green(n+1)-G

FIG 4

DRIVING METHOD FOR PIXEL CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a liquid crystal display technology field, and more particularly to a driving method for a pixel circuit.

2. Description of Related Art

[0002] An active-matrix organic light emitting diode (AMOLED) panel has a self-luminous property, and adopting a very thin organic coating layer and a glass substrate. When a current pass through, the organic coating layer will emit light. Because the AMOLED is driven by current so that the AMOLED is very sensitive to the change of the voltage. Specifically, a drift of the threshold voltage easily causes an uneven display of the panel. Accordingly, the pixel compensation circuit of the AMOLED is very important. The pixel circuit of the AMOLED can compensate the drift of the threshold voltage in order to increase the display uniformity of the OLED panel.

[0003] Along with the development of the thin-film transistor of the Low Temperature Poly-silicon (LTPS) semiconductor, because the LTPS semiconductor has a super-high carrier mobility itself, the peripheral integrated circuit of the panel also become the focus of attention, and many people research the related technology of the System on Panel (SOP), and being realized gradually. In the panel design, in order to decrease the cost of the driving chip (IC) and the Chip On Film (COF), a demux circuit design is usually adopted.

[0004] In a general OLED, in the timing diagram that the data line (Data) input a signal through the demux circuit, before a data signal of the data line in inputted, a resetting operation for the data signal of the data line is not executed in a display region (AA region). The data signal in the AA region maintains at a floating voltage before the demux circuit provides a signal. When a scanning signals in inputted, the floating voltage will charge a sub-pixel circuit so as to generate an abnormal picture display.

SUMMARY OF THE INVENTION

[0005] The embodiment of the present invention provides a gate driving circuit, which can effectively prevent an abnormal picture display generated by a wrong charging.

[0006] The present invention provides a driving method for a pixel circuit, comprising steps of: receiving a data control signal inputted by a driving chip and resetting a data line of a pixel unit according to the data control signal, wherein the pixel unit comprises a R sub-pixel, a G sub-pixel and a B sub-pixel, and according the received data control signal, simultaneously resetting the R sub-pixel, the G sub-pixel and the B sub pixel; charging the pixel unit to a target voltage according to the data line control signal; receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage; wherein, pixel circuit comprises a first MOS transistor, a gate of the first MOS transistor is connected with a data line selection signal, a drain of the first MOS transistor receives the data line control signal inputted by a driving chip, a source of the first MOS transistor is connected with the data line; and wherein, the step of receiving a data control signal inputted by a driving chip and resetting a data line of a pixel unit according to the data control signal comprises a step of: the data line selection signal controls the first MOS transistor to be turned on, the data line control signal inputted by the driving chip is inputted to the data line through the first MOS transistor and resetting the data line.

[0007] Wherein, the step of charging the pixel unit to a target voltage comprises a step of: sequentially charging the R sub-pixel, the G sub-pixel and the B sub-pixel to corresponding target voltages.

[0008] Wherein, the pixel circuit includes a R sub-pixel circuit, a G sub-pixel unit and a B sub-pixel unit, each sub-pixel circuit further comprises a second MOS transistor, a third MOS transistor and a first MOS transistor unit; a gate of the second MOS transistor is connected with a first scanning signal, a drain of the second MOS transistor is connected with a drain of the third MOS transistor, a gate and a source of the third MOS transistor are connected with the first MOS transistor unit; the first MOS transistor unit further connects with the first scanning signal, wherein a voltage of the gate of the third MOS transistor is a voltage of the sub-pixel; the step of charging the pixel unit to a target voltage according to the data line control signal comprises a step of: sequentially for the R sub-pixel, the G sub-pixel and the B sub-pixel, the first scanning signal controlling the second MOS transistor and the first MOS transistor unit to be turned on, and the data line selection signal controlling the first MOS transistor to be turned on; and the data line control signal inputted by the driving chip charging the sub-pixel to the target voltage through the first MOS transistor and the second MOS transistor.

[0009] Wherein, the first MOS transistor unit comprises a fourth MOS transistor and a fifth MOS transistor, gates of the fourth MOS transistor and the fifth MOS transistor are connected with the first scanning signal, a drain of the fourth MOS transistor is connected with the gate of the third MOS transistor, a source of the fourth MOS transistor is connected with a drain of the fifth MOS transistor, a source of the fifth MOS transistor is connected with the source of the third MOS transistor; the step of the first scanning signal controlling the first MOS transistor unit to be turned on comprises a step of: the first scanning signal controlling the fourth MOS transistor and the fifth MOS transistor to be turned on simultaneously.

[0010] Wherein, each of the first MOS transistor, the second MOS transistor, the third MOS transistor, the fourth MOS transistor and the fifth MOS transistor is a PMOS transistor.

[0011] Wherein, each of the first MOS transistor, the second MOS transistor, the third MOS transistor, the fourth MOS transistor and the fifth MOS transistor is a NMOS transistor.

[0012] Wherein, each sub-pixel circuit further includes a sixth MOS transistor and a seventh MOS transistor, gates of the sixth MOS transistor and the seventh MOS transistor are connected with the control signal. a drain of the sixth MOS transistor is connected with a first reference voltage, a source of the sixth MOS transistor is connected with the drain of the third MOS transistor, a drain of the seventh MOS transistor is connected with the source of the third MOS transistor, a source of the seventh MOS transistor is connected with a positive electrode of a light-emitting diode, a negative electrode of the light-emitting diode is connected with a second reference voltage; and the step of receiving a control

signal to control the pixel unit to display a corresponding grayscale level according to the target voltage comprises a step of: the control signal controlling the sixth MOS transistor and the seventh MOS transistor to be turned on, and the light-emitting diode emits light according a current formed by the target voltage to display the corresponding grayscale level.

[0013] Wherein, each sub-pixel circuit further includes an eighth MOS transistor and a ninth MOS transistor, gates of the eighth MOS transistor and the ninth MOS transistor are connected with a second scanning signal, a drain of the eighth MOS transistor is connected with the gate of the third MOS transistor, a source of the eighth MOS transistor is connected with a drain of the ninth MOS transistor, a source of the ninth MOS transistor is connected with a reset signal; and before the step of receiving a data control signal inputted by a driving chip, the second scanning signal controls the eighth MOS transistor and the ninth MOS transistor to be turned on, and the reset signal is transmitted to the gate of the third MOS transistor to perform a resetting.

[0014] The present invention also provides a driving method for a pixel circuit, comprising steps of: receiving a data control signal inputted by a driving chip and resetting a data line of a pixel unit according to the data control signal; charging the pixel unit to a target voltage according to the data line control signal; and receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage.

[0015] Wherein, the pixel unit comprises an R sub-pixel, a G sub-pixel and a B sub-pixel, and the step resetting a data line of a pixel unit comprises a step of according the received data control signal, simultaneously resetting the R sub-pixel, the G sub-pixel and the B sub pixel.

[0016] Wherein, the step of charging the pixel unit to a target voltage comprises a step of: sequentially charging the R sub-pixel, the G sub-pixel and the B sub-pixel to corresponding target voltages.

[0017] Wherein, pixel circuit comprises a first MOS transistor, a gate of the first MOS transistor is connected with a data line selection signal, a drain of the first MOS transistor receives the data line control signal inputted by a driving chip, a source of the first MOS transistor is connected with the data line; and wherein, the step of receiving a data control signal inputted by a driving chip and resetting a data line of a pixel unit according to the data control signal comprises a step of: the data line selection signal controls the first MOS transistor to be turned on, the data line control signal inputted by the driving chip is inputted to the data line through the first MOS transistor and resetting the data line.

[0018] Wherein, the pixel circuit includes a R sub-pixel circuit, a G sub-pixel unit and a B sub-pixel unit, each sub-pixel circuit further comprises a second MOS transistor, a third MOS transistor and a first MOS transistor unit; a gate of the second MOS transistor is connected with a first scanning signal, a drain of the second MOS transistor is connected with a drain of the third MOS transistor, a gate and a source of the third MOS transistor are connected with the first MOS transistor unit; the first MOS transistor unit further connects with the first scanning signal, wherein a voltage of the gate of the third MOS transistor is a voltage of the sub-pixel; the step of charging the pixel unit to a target voltage according to the data line control signal comprises a step of: sequentially for the R sub-pixel, the G sub-pixel and the B sub-pixel, the first scanning signal controlling the second MOS transistor and the first MOS transistor unit to be turned on, and the data line selection signal controlling the first MOS transistor to be turned on; and the data line control signal inputted by the driving chip charging the sub-pixel to the target voltage through the first MOS transistor and the second MOS transistor.

[0019] Wherein, the first MOS transistor unit comprises a fourth MOS transistor and a fifth MOS transistor, gates of the fourth MOS transistor and the fifth MOS transistor are connected with the first scanning signal, a drain of the fourth MOS transistor is connected with the gate of the third MOS transistor, a source of the fourth MOS transistor is connected with a drain of the fifth MOS transistor, a source of the fifth MOS transistor is connected with the source of the third MOS transistor; the step of the first scanning signal controlling the first MOS transistor unit to be turned on comprises a step of: the first scanning signal controlling the fourth MOS transistor and the fifth MOS transistor to be turned on simultaneously.

[0020] Wherein, each of the first MOS transistor, the second MOS transistor, the third MOS transistor, the fourth MOS transistor and the fifth MOS transistor is a PMOS transistor.

[0021] Wherein, each of the first MOS transistor, the second MOS transistor, the third MOS transistor, the fourth MOS transistor and the fifth MOS transistor is a NMOS transistor.

[0022] Wherein, each sub-pixel circuit further includes a sixth MOS transistor and a seventh MOS transistor, gates of the sixth MOS transistor and the seventh MOS transistor are connected with the control signal. a drain of the sixth MOS transistor is connected with a first reference voltage, a source of the sixth MOS transistor is connected with the drain of the third MOS transistor, a drain of the seventh MOS transistor is connected with the source of the third MOS transistor, a source of the seventh MOS transistor is connected with a positive electrode of a light-emitting diode, a negative electrode of the light-emitting diode is connected with a second reference voltage; and the step of receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage comprises a step of: the control signal controlling the sixth MOS transistor and the seventh MOS transistor to be turned on, and the light-emitting diode emits light according a current formed by the target voltage to display the corresponding grayscale level.

[0023] Wherein, each sub-pixel circuit further includes an eighth MOS transistor and a ninth MOS transistor, gates of the eighth MOS transistor and the ninth MOS transistor are connected with a second scanning signal, a drain of the eighth MOS transistor is connected with the gate of the third MOS transistor, a source of the eighth MOS transistor is connected with a drain of the ninth MOS transistor, a source of the ninth MOS transistor is connected with a reset signal; and before the step of receiving a data control signal inputted by a driving chip, the second scanning signal controls the eighth MOS transistor and the ninth MOS transistor to be turned on, and the reset signal is transmitted to the gate of the third MOS transistor to perform a resetting.

[0024] Through the above solution, the beneficial effect of the present invention is: the present invention can effectively prevent a wrong charging, which will generate an abnormal picture display through receiving a data control signal inputted by a driving chip and resetting a data line of a pixel

unit according to the data control signal; charging the pixel unit to a target voltage according to the data line control signal; and receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] In order to more clearly illustrate the technical solution in the present invention or in the prior art, the following will illustrate the figures used for describing the embodiments or the prior art. It is obvious that the following figures are only some embodiments of the present invention. For the person of ordinary skill in the art without creative effort, it can also obtain other figures according to these figures. In the figures:

[0026] FIG. **1** is a flow chart of a driving method for a pixel circuit according to an embodiment of the present invention;

[0027] FIG. **2** is a circuit diagram of the pixel circuit according to an embodiment of the present invention;

[0028] FIG. **3** is a circuit diagram of a sub-pixel circuit according to an embodiment of the present invention; and

[0029] FIG. **4** is a timing diagram of the pixel circuit according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0030] The following content combines with the drawings and the embodiment for describing the present invention in detail. It is obvious that the following embodiments are only some embodiments of the present invention. For the person of ordinary skill in the art without creative effort, the other embodiments obtained thereby are still covered by the present invention

[0031] With reference to FIG. **1** to FIG. **3**, FIG. **1** is a flow chart of a driving method for a pixel circuit according to an embodiment of the present invention. FIG. **2** is a circuit diagram of the pixel circuit according to an embodiment of the present invention, and FIG. **3** is a circuit diagram of a sub-pixel circuit according to an embodiment of the present invention. The driving method for the pixel circuit includes:

[0032] Step S**10**: receiving a data line control signal inputted from a driving chip, and resetting a data line of a pixel unit according to the data line control signal.

[0033] In the present embodiment, the pixel unit includes an R sub-pixel, a G sub-pixel and a B sub-pixel. Correspondingly, in the step S**10**, simultaneously resetting the R sub-pixel, the G sub-pixel and the B sub-pixel according to the received data line control signal. Specifically, before the data line charges the pixel unit, resetting the data line by receiving the data line control signal inputted from the driving chip in order to ensure that in a next period, the pixel unit can prevent a wrong charging, which will generate an abnormal display picture.

[0034] Step S**11**: charging the pixel unit to a target voltage according to the data line control signal.

[0035] In the step S**11**, sequentially charging the R sub-pixel, the G sub-pixel and the B sub-pixel to corresponding target voltages. With reference to FIG. **2**, in the embodiment of the present invention, the pixel units are arranged as a matrix, and are connected to scanning lines and data lines. The pixel circuit of each pixel unit includes an R sub-pixel circuit, G sub-pixel circuit and a B sub-pixel unit. The sub-pixel units commonly use one scanning line, and different sub-pixels correspond to different data lines. The pixel circuit includes a first MOS transistor T**1**, a gate of the first MOS transistor T**1** is connected with a data line selection signal. A drain of the first MOS transistor T**1** receives the data line control signal (Data from IC) inputted from the driving chip. A source of the first MOS transistor T**1** is connected with the data line. The data line selection signal controls the first MOS transistor T**1** to be conductive such that the data line control signal (Data from IC) inputted from the driving chip is inputted to the data line through the first MOS transistor T**1** in order to reset the data line.

[0036] With reference to FIG. **2**, the pixel circuit includes an R sub-pixel circuit, a G sub-pixel unit and a B sub-pixel unit. Using the R sub-pixel circuit of one pixel unit as an example. Each sub-pixel circuit **10** further includes a second MOS transistor T**2**, a third MOS transistor T**3** and a first MOS transistor unit **101**. A gate of the second MOS transistor T**2** is connected with a first scanning signal Scan(n), a drain of the second MOS transistor T**2** is connected with a drain of the third MOS transistor T**3**, a gate and a source of the third MOS transistor T**3** are connected with the first MOS transistor unit **101**. The first MOS transistor unit **101** further connects with the first scanning signal Scan(n), wherein, a voltage of the gate of the third MOS transistor T**3** is a voltage of the sub-pixel.

[0037] In the step S**11**, sequentially for the R sub-pixel, the G sub-pixel and the B sub-pixel, the first scanning signal Scan(n) controls the second MOS transistor T**2** and the first MOS transistor unit **101** to be turned on. The data line selection signal controls the first MOS transistor T**1** to be turned on; the data line control signal (Data from IC) inputted by the driving chip charges the sub-pixel to the target voltage through the first MOS transistor T**1** and the second MOS transistor T**2**. Specifically, when the first scanning signal Scan(n) controls the second MOS transistor T**2** in the R sub-pixel, the R sub-pixel and the B sub-pixel to be turned on, firstly, the data line selection signal Mux R controls the first MOS transistor T**1** corresponding to the R sub-pixel to be turned on, the data line control signal (Data from IC) inputted by the driving chip charges the R sub-pixel to a target voltage through the first MOS transistor T**1** and the second MOS transistor T**2** in the R sub-pixel.

[0038] Then, the data line selection signal Mux G controls the first MOS transistor T**1** corresponding to the G sub-pixel to be turned on, the data line control signal (Data from IC) inputted by the driving chip charges the G sub-pixel to a target voltage through the first MOS transistor T**1** and the second MOS transistor T**2** in the G sub-pixel. Finally, the data line selection signal Mux B controls the first MOS transistor T**1** corresponding to the B sub-pixel to be turned on. The data line control signal (Data from IC) charges the B sub-pixel to a target voltage through the first MOS transistor T**1** and the second MOS transistor T**2**. Wherein, the target voltage is a sum of a voltage of the data line control signal (Data from IC) and a threshold voltage Vth of the third MOS transistor.

[0039] In the embodiment of the present invention, the first MOS transistor unit **101** includes a fourth MOS transistor T**4** and a fifth MOS transistor T**5**. Gates of the fourth MOS transistor T**4** and the fifth MOS transistor T**5** are connected with a first scanning signal Scan(n), a drain of the fourth MOS transistor T**4** is connected with a gate of the third MOS transistor T**3**, a source of the fourth MOS

transistor T4 is connected with a drain of the fifth MOS transistor T5. A source of the fifth MOS transistor T5 is connected with a source of the third MOS transistor T3. When the first scanning signal Scan(n) controls the first MOS transistor MOS unit **101** to be turned on, the first scanning signal Scan(n) is required to control the fourth MOS transistor T4 and the fifth MOS transistor T5 to be turned on simultaneously. Of course, in another embodiment of the present invention, the first MOS transistor unit **101** can only include one MOS transistor.

[0040] Besides, in the embodiment of the present invention, each of the first MOS transistor T1, the second MOS transistor T2, the third MOS transistor T3, the fourth MOS transistor T4 and the fifth MOS transistor T5 is a PMOS transistor. However, each of the first MOS transistor T1, the second MOS transistor T2, the third MOS transistor T3, the fourth MOS transistor T4 and the fifth MOS transistor T5 can also be a NMOS transistor.

[0041] Step S12: receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage.

[0042] In the embodiment of the present invention, each sub-pixel circuit further includes a sixth MOS transistor T6 and a seventh MOS transistor T7. Gates of the sixth MOS transistor T6 and the seventh MOS transistor T7 are connected with the control signal EM. A drain of the sixth MOS transistor T6 is connected with a first reference voltage VDD, a source of the sixth MOS transistor T6 is connected with the drain of the third MOS transistor T3. A drain of the seventh MOS transistor T7 is connected with the source of the third MOS transistor T3, a source of the seventh MOS transistor T7 is connected with a positive electrode of a light-emitting diode (OLED), a negative electrode of the light-emitting diode (OLED) is connected with a second reference voltage (VSS).

[0043] In the step S12, the control signal EM controls the sixth MOS transistor T6 and the seventh MOS transistor T7 to be turned on, and the light-emitting diode (OLED) emits light according a current formed by the target voltage to display a corresponding grayscale level.

[0044] In the embodiment of the present invention, each sub-pixel circuit **10** further includes an eighth MOS transistor T8 and a ninth MOS transistor T9, gates of the eighth MOS transistor T8 and the ninth MOS transistor T9 are connected with a second scanning signal Scan(n+1). A drain of the eighth MOS transistor T8 is connected with the gate of the third MOS transistor T3, a source of the eighth MOS transistor T8 is connected with a drain of the ninth MOS transistor T9. A source of the ninth MOS transistor T9 is connected with a reset signal VI. Correspondingly, before the step S10, the second scanning signal Scan(n+1) controls the eighth MOS transistor T8 and the ninth MOS transistor T9 to be turned on, and the reset signal VI is transmitted to the gate of the third MOS transistor T3 to perform a resetting.

[0045] FIG. **4** is a timing diagram of the pixel circuit according to the embodiment of the present invention. The corresponding pixel circuit can refer to FIG. **2** and FIG. **3**. Wherein, the first MOS transistor T1, the second MOS transistor T2, the third MOS transistor T3, the fourth MOS transistor T4, the fifth MOS transistor T5, the sixth MOS transistor T8, the seventh MOS transistor T9, the eight MOS transistor T10 and ninth MOS transistor T11 are all PMOS transistors.

[0046] As shown in FIG. **4**, the working process of timing is as following: First of all, simultaneously turning on the data line selection signals Mux R, Mux G, Mux B, and the data line control signal (data from IC) resets the data lines Data-R, Data-G, Data-B respectively corresponding to the R sub-pixel, the G sub-pixel, the B sub-pixel as the reset signal VI. Then, the first scanning signal Scan(n) becomes a low level. When the data line selection signal Mux R is at a low level, the data line control signal (Data from IC) charges the data line Data-R corresponding to an R sub-pixel of an n-th row. The voltage of the gate Red(n) G of the third transistor T3 in the R sub-pixel becomes $V_{Data\text{-}R}$+Vth. Then, the data line selection signal Mux G becomes a low level, and the data line control signal (Data from IC) charges the data line Data-G corresponding to the G sub-pixel of the n-th row. The voltage of the gate Green(n) G of the third transistor T3 in the G sub-pixel becomes $V_{Data\text{-}G}$+Vth.

[0047] Then, the data line selection signal Mux B becomes a low level, and the data line control signal (Data from IC) charges the data line Data-B corresponding to the B sub-pixel of the n-th row. The voltage of the gate Blue(n) G of the third transistor T3 in the B sub-pixel becomes $V_{Data\text{-}B}$+Vth. Accordingly, charging of the R sub-pixel, the G sub-pixel, the B sub-pixel of the n-th row is finished, and the R sub-pixel, the G sub-pixel, the B sub-pixel are all charged to target voltages. Before charging (n+1)-th row, the data line selection signals Mux R, Mux G, Mux B are simultaneously turned on, the data line control signal (data from IC) resets the data lines Data-R, Data-G, Data-B respectively corresponding to the R sub-pixel, the G sub-pixel, the B sub-pixel to the reset signal VI. Then, the control signal EM controls the sixth MOS transistor T6 and the seventh MOS transistor T7 to be turned on, the light-emitting diode OLED emits light according to a current formed by the target voltage, and displays a corresponding grayscale level.

[0048] At this time, the data lines Data-R, Data-G, Data-B corresponding to the R sub-pixel, the G sub-pixel, the B sub-pixel have a higher floating voltage $V_{floating}$. If in the next period, directly charging the data lines Data-R, Data-G, Data-B corresponding to the R sub-pixel, the G sub-pixel, the B sub-pixel, and if the voltage $V_{Data\text{-}G}$ required to be achieved by charging is less than $V_{floating}$, unable charging phenomenon will occur, the data line Data-G remains at the floating voltage $V_{floating}$ such that the G sub-pixel cannot reach the target voltage $V_{Data\text{-}G}$+Vth at that period so as to maintain at a charging voltage $V_{floating}$+Vth. When the $V_{Data\text{-}G}$ is smaller and the grayscale level is higher, the phenomenon is more obvious.

[0049] Therefore, in the embodiment of the present invention, when the scan(n+1) signal become a low level, the data line selection signal Mux R also becomes a low level, the data line control signal (Data from IC) charges the data line Data-R corresponding to the R sub-pixel of the (n+1)-th row, the voltage of the gate Red(n) G of the third MOS transistor T3 in the R sub-pixel of the (n+1)-th row becomes $V_{Data\text{-}R}$+Vth. At this time, each of the data line Data-G corresponding to the G sub-pixel and the data line Data-B corresponding to the B sub-pixel is the reset signal VI, which is a very low level so that a situation that the gate Green (n+1) G of the third MOS transistor T3 in the G sub-pixel or the gate Blue(n+1) G of the third MOS transistor T3 in the B sub-pixel is incorrectly charged to $V_{floating}$+Vth will be avoided. Accordingly, in the present timing, each sub-pixel can be normally charged to a target voltage in order to

prevent a wrong charging which will generate an abnormal display, and the picture display quality can be greatly improved.

[0050] Wherein, the dotted line portion in FIG. **4** is the floating voltage $V_{floating}$, and the specific value is not determined, and is related to the grayscale level displayed by the sub-pixel in the previous period.

[0051] In summary, the present invention can effectively prevent a wrong charging which will generate an abnormal picture display through receiving a data control signal inputted by a driving chip and resetting a data line of a pixel unit according to the data control signal; charging the pixel unit to a target voltage according to the data line control signal; and receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage.

[0052] The above embodiments of the present invention are not used to limit the claims of this invention. Any use of the content in the specification or in the drawings of the present invention which produces equivalent structures or equivalent processes, or directly or indirectly used in other related technical fields is still covered by the claims in the present invention.

What is claimed is:

1. A driving method for a pixel circuit, comprising steps of:

receiving a data control signal inputted by a driving chip and resetting a data line of a pixel unit according to the data control signal, wherein the pixel unit comprises a R sub-pixel, a G sub-pixel and a B sub-pixel, and according the received data control signal, simultaneously resetting the R sub-pixel, the G sub-pixel and the B sub pixel;

charging the pixel unit to a target voltage according to the data line control signal;

receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage;

wherein, pixel circuit comprises a first MOS transistor, a gate of the first MOS transistor is connected with a data line selection signal, a drain of the first MOS transistor receives the data line control signal inputted by a driving chip, a source of the first MOS transistor is connected with the data line; and

wherein, the step of receiving a data control signal inputted by a driving chip and resetting a data line of a pixel unit according to the data control signal comprises a step of: the data line selection signal controls the first MOS transistor to be turned on, the data line control signal inputted by the driving chip is inputted to the data line through the first MOS transistor and resetting the data line.

2. The driving method according to claim **1**, wherein, the step of charging the pixel unit to a target voltage comprises a step of: sequentially charging the R sub-pixel, the G sub-pixel and the B sub-pixel to corresponding target voltages.

3. The driving method according to claim **1**, wherein, the pixel circuit includes a R sub-pixel circuit, a G sub-pixel unit and a B sub-pixel unit, each sub-pixel circuit further comprises a second MOS transistor, a third MOS transistor and a first MOS transistor unit; a gate of the second MOS transistor is connected with a first scanning signal, a drain of the second MOS transistor is connected with a drain of the third MOS transistor, a gate and a source of the third MOS transistor are connected with the first MOS transistor unit; the first MOS transistor unit further connects with the first scanning signal, wherein a voltage of the gate of the third MOS transistor is a voltage of the sub-pixel;

the step of charging the pixel unit to a target voltage according to the data line control signal comprises a step of: sequentially for the R sub-pixel, the G sub-pixel and the B sub-pixel,

the first scanning signal controlling the second MOS transistor and the first MOS transistor unit to be turned on, and the data line selection signal controlling the first MOS transistor to be turned on; and

the data line control signal inputted by the driving chip charging the sub-pixel to the target voltage through the first MOS transistor and the second MOS transistor.

4. The driving method according to claim **3**, wherein, the first MOS transistor unit comprises a fourth MOS transistor and a fifth MOS transistor, gates of the fourth MOS transistor and the fifth MOS transistor are connected with the first scanning signal, a drain of the fourth MOS transistor is connected with the gate of the third MOS transistor, a source of the fourth MOS transistor is connected with a drain of the fifth MOS transistor, a source of the fifth MOS transistor is connected with the source of the third MOS transistor;

the step of the first scanning signal controlling the first MOS transistor unit to be turned on comprises a step of: the first scanning signal controlling the fourth MOS transistor and the fifth MOS transistor to be turned on simultaneously.

5. The driving method according to claim **4**, wherein, each of the first MOS transistor, the second MOS transistor, the third MOS transistor, the fourth MOS transistor and the fifth MOS transistor is a PMOS transistor.

6. The driving method according to claim **4**, wherein, each of the first MOS transistor, the second MOS transistor, the third MOS transistor, the fourth MOS transistor and the fifth MOS transistor is a NMOS transistor.

7. The driving method according to claim **4**, wherein, each sub-pixel circuit further includes a sixth MOS transistor and a seventh MOS transistor, gates of the sixth MOS transistor and the seventh MOS transistor are connected with the control signal. a drain of the sixth MOS transistor is connected with a first reference voltage, a source of the sixth MOS transistor is connected with the drain of the third MOS transistor, a drain of the seventh MOS transistor is connected with the source of the third MOS transistor, a source of the seventh MOS transistor is connected with a positive electrode of a light-emitting diode, a negative electrode of the light-emitting diode is connected with a second reference voltage; and

the step of receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage comprises a step of: the control signal controlling the sixth MOS transistor and the seventh MOS transistor to be turned on, and the light-emitting diode emits light according a current formed by the target voltage to display the corresponding grayscale level.

8. The driving method according to claim **4**, wherein, each sub-pixel circuit further includes an eighth MOS transistor and a ninth MOS transistor, gates of the eighth MOS transistor and the ninth MOS transistor are connected with a second scanning signal, a drain of the eighth MOS

transistor is connected with the gate of the third MOS transistor, a source of the eighth MOS transistor is connected with a drain of the ninth MOS transistor, a source of the ninth MOS transistor is connected with a reset signal; and

before the step of receiving a data control signal inputted by a driving chip, the second scanning signal controls the eighth MOS transistor and the ninth MOS transistor to be turned on, and the reset signal is transmitted to the gate of the third MOS transistor to perform a resetting.

9. A driving method for a pixel circuit, comprising steps of:

receiving a data control signal inputted by a driving chip and resetting a data line of a pixel unit according to the data control signal;

charging the pixel unit to a target voltage according to the data line control signal; and

receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage.

10. The driving method according to claim **9**, wherein, the pixel unit comprises a R sub-pixel, a G sub-pixel and a B sub-pixel, and the step resetting a data line of a pixel unit comprises a step of according the received data control signal, simultaneously resetting the R sub-pixel, the G sub-pixel and the B sub pixel.

11. The driving method according to claim **10**, wherein, the step of charging the pixel unit to a target voltage comprises a step of: sequentially charging the R sub-pixel, the G sub-pixel and the B sub-pixel to corresponding target voltages.

12. The driving method according to claim **9**, wherein, pixel circuit comprises a first MOS transistor, a gate of the first MOS transistor is connected with a data line selection signal, a drain of the first MOS transistor receives the data line control signal inputted by a driving chip, a source of the first MOS transistor is connected with the data line; and

wherein, the step of receiving a data control signal inputted by a driving chip and resetting a data line of a pixel unit according to the data control signal comprises a step of: the data line selection signal controls the first MOS transistor to be turned on, the data line control signal inputted by the driving chip is inputted to the data line through the first MOS transistor and resetting the data line.

13. The driving method according to claim **12**, wherein, the pixel circuit includes a R sub-pixel circuit, a G sub-pixel unit and a B sub-pixel unit, each sub-pixel circuit further comprises a second MOS transistor, a third MOS transistor and a first MOS transistor unit; a gate of the second MOS transistor is connected with a first scanning signal, a drain of the second MOS transistor is connected with a drain of the third MOS transistor, a gate and a source of the third MOS transistor are connected with the first MOS transistor unit; the first MOS transistor unit further connects with the first scanning signal, wherein a voltage of the gate of the third MOS transistor is a voltage of the sub-pixel;

the step of charging the pixel unit to a target voltage according to the data line control signal comprises a step of: sequentially for the R sub-pixel, the G sub-pixel and the B sub-pixel,

the first scanning signal controlling the second MOS transistor and the first MOS transistor unit to be turned on, and the data line selection signal controlling the first MOS transistor to be turned on; and

the data line control signal inputted by the driving chip charging the sub-pixel to the target voltage through the first MOS transistor and the second MOS transistor.

14. The driving method according to claim **13**, wherein, the first MOS transistor unit comprises a fourth MOS transistor and a fifth MOS transistor, gates of the fourth MOS transistor and the fifth MOS transistor are connected with the first scanning signal, a drain of the fourth MOS transistor is connected with the gate of the third MOS transistor, a source of the fourth MOS transistor is connected with a drain of the fifth MOS transistor, a source of the fifth MOS transistor is connected with the source of the third MOS transistor;

the step of the first scanning signal controlling the first MOS transistor unit to be turned on comprises a step of: the first scanning signal controlling the fourth MOS transistor and the fifth MOS transistor to be turned on simultaneously.

15. The driving method according to claim **14**, wherein, each of the first MOS transistor, the second MOS transistor, the third MOS transistor, the fourth MOS transistor and the fifth MOS transistor is a PMOS transistor.

16. The driving method according to claim **14**, wherein, each of the first MOS transistor, the second MOS transistor, the third MOS transistor, the fourth MOS transistor and the fifth MOS transistor is a NMOS transistor.

17. The driving method according to claim **14**, wherein, each sub-pixel circuit further includes a sixth MOS transistor and a seventh MOS transistor, gates of the sixth MOS transistor and the seventh MOS transistor are connected with the control signal. a drain of the sixth MOS transistor is connected with a first reference voltage, a source of the sixth MOS transistor is connected with the drain of the third MOS transistor, a drain of the seventh MOS transistor is connected with the source of the third MOS transistor, a source of the seventh MOS transistor is connected with a positive electrode of a light-emitting diode, a negative electrode of the light-emitting diode is connected with a second reference voltage; and

the step of receiving a control signal to control the pixel unit to display a corresponding grayscale level according to the target voltage comprises a step of: the control signal controlling the sixth MOS transistor and the seventh MOS transistor to be turned on, and the light-emitting diode emits light according a current formed by the target voltage to display the corresponding grayscale level.

18. The driving method according to claim **14**, wherein, each sub-pixel circuit further includes an eighth MOS transistor and a ninth MOS transistor, gates of the eighth MOS transistor and the ninth MOS transistor are connected with a second scanning signal, a drain of the eighth MOS transistor is connected with the gate of the third MOS transistor, a source of the eighth MOS transistor is connected

with a drain of the ninth MOS transistor, a source of the ninth MOS transistor is connected with a reset signal; and

before the step of receiving a data control signal inputted by a driving chip, the second scanning signal controls the eighth MOS transistor and the ninth MOS transistor to be turned on, and the reset signal is transmitted to the gate of the third MOS transistor to perform a resetting.

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