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(54) METAL OXIDE METAL CAPACITOR WITH SLOT VIAS

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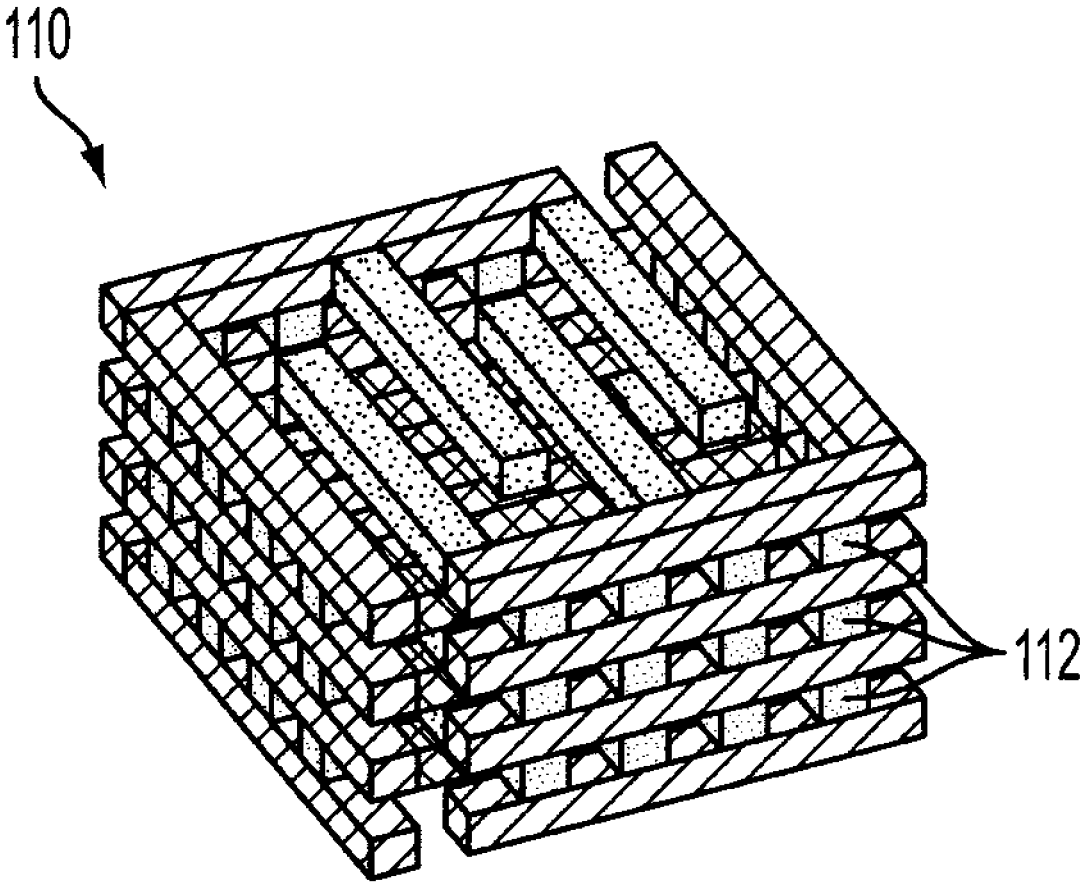
CPC *H01L 29/92* (2013.01)
USPC **257/532**

(57) **ABSTRACT**

A capacitor includes a first electrode including a plurality of first conductive lines, at least one first via, and at least one second via. The first conductive lines are parallel and connected to a first periphery conductive line. The first conductor lines in adjacent layers are coupled by the at least one first and second via. The at least one first via has a first length, and the at least one second via has a second length. The capacitor includes a second electrode opposite to the first electrode. The second electrode includes a plurality of second conductive lines and at least one third via. The second conductive lines are parallel and connected to a second periphery conductive line. The second conductor lines in adjacent layers are coupled by the at least one third via. The capacitor includes at least one oxide layer between the first electrode and the second electrode.



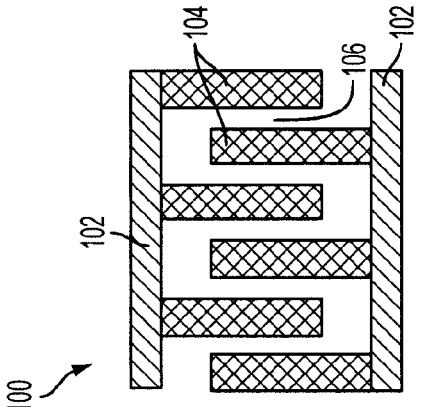


FIG. 1A

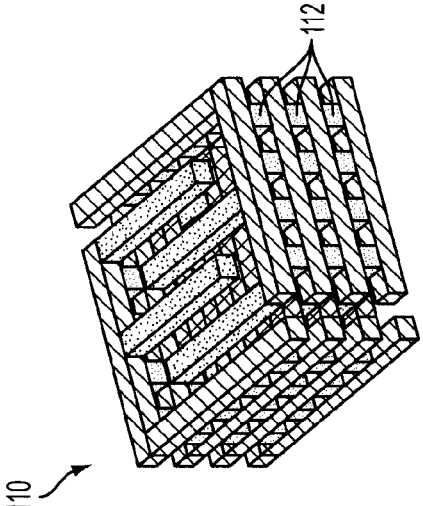


FIG. 1B

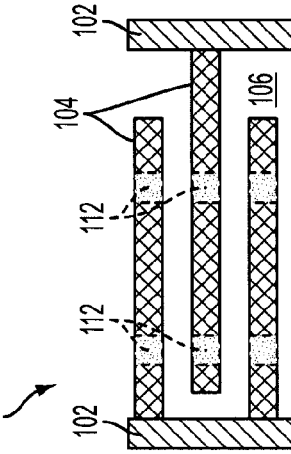


FIG. 2B

FIG. 2A

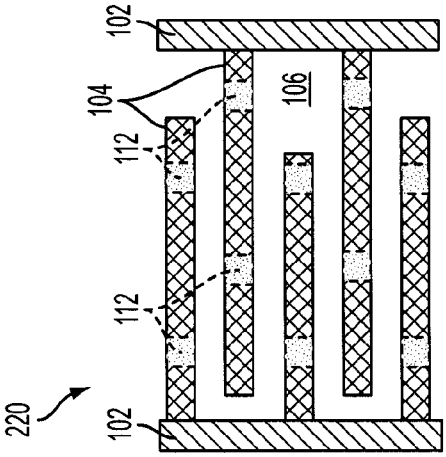


FIG. 2C

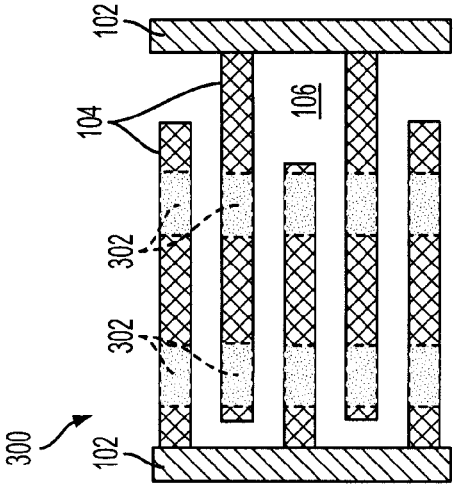


FIG. 3A

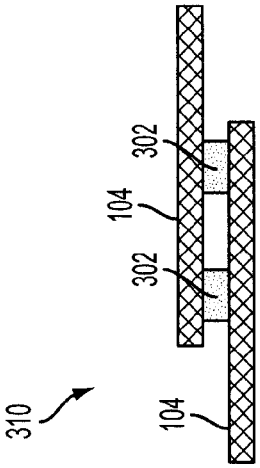


FIG. 3B

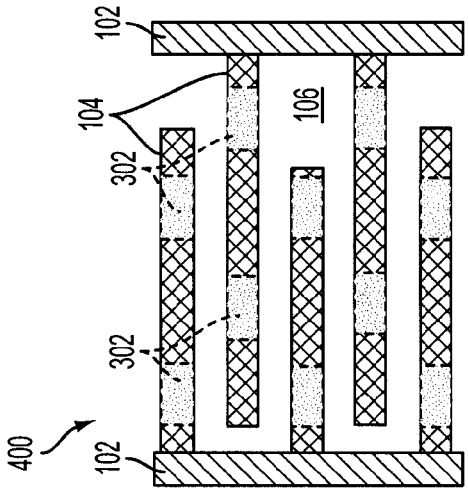


FIG. 4A

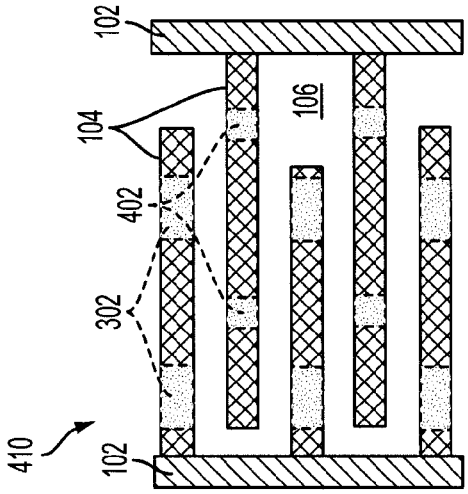


FIG. 4B

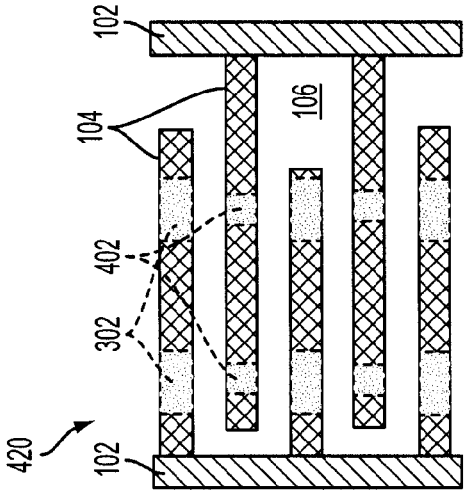


FIG. 4C

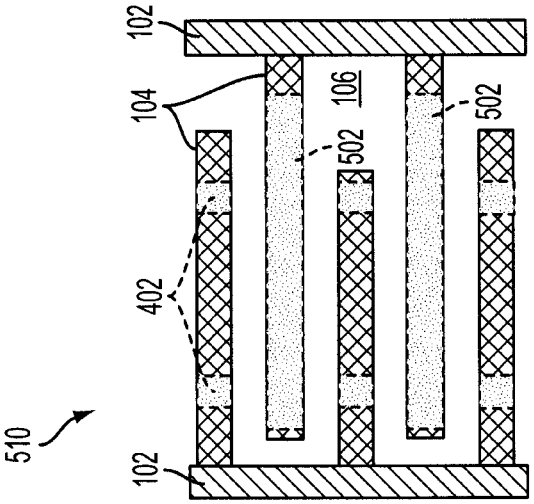

102
104
106
502
502
502
402
510
102

FIG. 5B

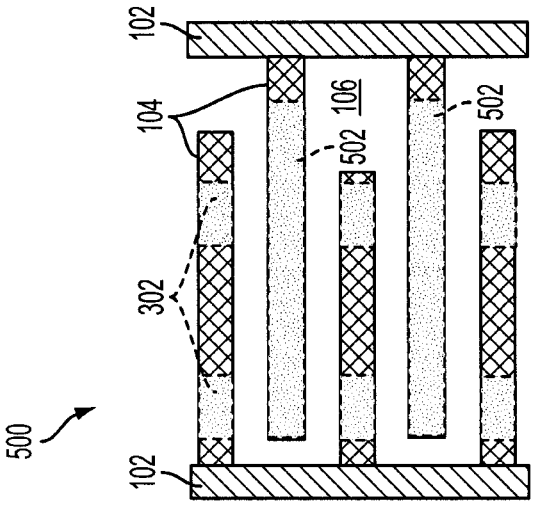

102
104
106
502
502
502
302
500
102

FIG. 5A

METAL OXIDE METAL CAPACITOR WITH SLOT VIAS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application Ser. No. 12/768,001, filed on Apr. 27, 2010, which claims the priority of U.S. Prov. Appl. No. 61/173,439, filed Apr. 28, 2009, which are incorporated herein by reference in their entireties.

TECHNICAL FIELD

[0002] This disclosure relates generally to Metal Oxide Metal (MOM) capacitor, more specifically MOM capacitor with a slot (rectangular) via structure.

BACKGROUND

[0003] An exemplary single layer Metal-oxide-metal (MOM) capacitor structure is shown in FIG. **1**A. The structure **100** has periphery metal **102**, metal lines **104**, and dielectric (oxide) layers **106**. To increase the area usage efficiency, multiple layers of MOM capacitor structures could be vertically stacked together. FIG. **1**B illustrates a stack (multi-layer) MOM capacitor structure, using vias **112** to connect each layer.

[0004] MOM capacitors have been used in the integrated circuits increasingly more often, partly because their minimal capacitive loss to the substrate results in high quality capacitors. Also, MOM capacitors with via have low cost and are easy to implement using a standard logic process. However, conventional MOM capacitors with via tend to have low capacitance and high resistance. Accordingly, important goals in manufacturing MOM capacitors are to increase the capacitance and reduce capacitor resistance, especially for Mixed Signal Radio Frequency (MSRF) product applications. Further, via resistance uniformity and reliable performance are important issues for MOM capacitors with high via density.

[0005] Accordingly, new structures and methods for MOM capacitors are desired to achieve higher capacitance and lower resistance, as well as performance reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] For a more complete understanding of the present disclosure, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0007] FIG. **1**A illustrates an exemplary single layer Metal-oxide-metal (MOM) capacitor structure;

[0008] FIG. **1**B illustrates a stack (multi-layer) MOM capacitor structure, using vias to connect each layer;

[0009] FIG. **2**A illustrates a top view of an example of a conventional multi-layer MOM capacitor structure with vias shown in dotted lines underneath the metal lines;

[0010] FIG. **2**B illustrates a partial side view of a conventional multi-layer MOM capacitor structure with vias between two metal layers;

[0011] FIG. **2**C illustrates a top view of an example of another conventional multi-layer MOM capacitor structure with vias shown in dotted lines underneath the metal lines;

[0012] FIG. **3**A illustrates a top view of an exemplary multi-layer MOM capacitor structure according to one aspect of this disclosure with vias shown in dotted lines underneath the metal lines;

[0013] FIG. **3**B illustrates a partial side view of an exemplary multi-layer MOM capacitor structure according to one aspect of this disclosure with vias between two metal layers;

[0014] FIG. **4**A-FIG. **4**C illustrate a top view of other embodiments of a multi-layer MOM capacitor structure according to one aspect of this disclosure with vias shown in dotted lines underneath the metal lines; and

[0015] FIG. **5**A-FIG. **5**B illustrate a top view of different embodiments of a multi-layer MOM capacitor structure according to another aspect of this disclosure with vias shown in dotted lines underneath the metal lines.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0016] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable novel concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative and do not limit the scope of the disclosure.

[0017] A novel structure for Metal-oxide-metal (MOM) capacitor with slot (rectangular) vias is provided. The structure uses slot (rectangular) vias to lower resistance and increase capacitance due to extended via length and increased sidewall area. Throughout the various views and illustrative embodiments of the present disclosure, like reference numbers are used to designate like elements.

[0018] FIG. **2**A illustrates a top view of an example of a conventional multi-layer MOM capacitor structure **200** with vias shown in dotted lines underneath the metal lines. The structure **200** has periphery metal **102**, metal lines **104**, and dielectric (oxide) layers **106**. The vias **112** are square vias with a fixed size depending on the process (e.g. 0.05 μm×0.05 μm in a 32 nm process). The vias **112** are aligned with each other across multiple metal lines **104** from the top-view shown in FIG. **2**A. The vias **112** connect each metal layer of the multi-layer MOM structure **200**.

[0019] FIG. **2**B illustrates a partial side view of a conventional multi-layer MOM capacitor structure with vias between two metal layers. The vias **112** connect metal lines **104** on different layers.

[0020] FIG. **2**C illustrates a top view of an example of another conventional multi-layer MOM capacitor structure with vias shown in dotted lines underneath the metal lines. The structure **220** has periphery metal **102**, metal lines **104**, and dielectric (oxide) layers **106**. The vias **112** are square vias with a fixed size depending on the process. The vias **112** are staggered across multiple metal lines **104** from the top-view shown in FIG. **2**C. Even though the layout of the structure **220** is different from that of the structure **200**, they both use fixed size square vias **112** to connect metal lines **104** between each layer.

[0021] FIG. **3**A illustrates a top view of an exemplary multi-layer MOM capacitor structure according to one aspect of this disclosure with vias shown in dotted lines underneath the metal lines. The structure **300** has periphery metal **102**, metal lines **104**, and dielectric (oxide) layers **106**. The periphery metal **102** and metal lines **104** could be copper, aluminum, tungsten, etc. The vias **302** are slot (rectangular) vias with a

variable size depending on the process (e.g., 0.05 μm×0.13 μm in a 32 nm process). The vias **302** are aligned with each other across multiple metal lines **104** from the top-view shown in FIG. **3**A. The vias **112** connect each metal layer of the multi-layer MOM structure **300**. MOM capacitor with slot via structure can increase capacitance and reduce resistance by extended via length and increased via sidewall area.

[0022] In one embodiment of the structure **300** using the slot vias **302** with the size of 0.05 μm×0.13 μm, the capacitance increased about 1.6 times (10.34 pF), compared to one embodiment of the structure **200** using square vias **112** with the size of 0.05 μm×0.05 μm (6.477 pF). This capacitance increase is due to extended via length and increased sidewall area from using slot (rectangular) **302** instead of square vias **112**.

[0023] FIG. **3**B illustrates a partial side view of an exemplary multi-layer MOM capacitor structure according to one aspect of this disclosure with vias between two metal layers. The vias **302** connect metal lines **104** on different layers.

[0024] FIG. **4**A-FIG. **4**C illustrate a top view of other embodiments of a multi-layer MOM capacitor structure according to one aspect of this disclosure with vias shown in dotted lines underneath the metal lines. In FIG. **4**A, the structure **400** has periphery metal **102**, metal lines **104**, and dielectric (oxide) layers **106**. The vias **302** are slot (rectangular) vias with a variable size depending on the process (e.g., 0.05 μm×0.13 μm). The vias **302** are staggered across multiple metal lines **104** in the y-direction from the top-view shown in FIG. **4**A. Even though the layout of the structure **400** is different from that of the structure **300**, they both use slot vias **302** to connect metal lines **104** between each layer.

[0025] In FIG. **4**B, the structure **410** has periphery metal **102**, metal lines **104**, and dielectric (oxide) layers **106**. The vias **302** are slot (rectangular) vias with a variable size depending on the process (e.g., 0.05 μm×0.13 μm). The vias **402** are square vias with a variable size depending on the process (e.g. 0.05 μm×0.05 μm). In the structure **410**, the vias **302** and **402** are used together (each on separate metal lines **104**) and staggered across multiple metal lines **104** from the top-view shown in FIG. **4**B. In another embodiment, the vias **302** and **402** can be mixed together in the same metal lines **104**.

[0026] In FIG. **4**C, the structure **420** has periphery metal **102**, metal lines **104**, and dielectric (oxide) layers **106**. Like the structure **410**, the vias **302** and **402** are used together (each on separate metal lines **104**) in the structure **420**, but the vias **302** and **402** are aligned with each other across multiple metal lines **104** from the top-view shown in FIG. **4**C. In another embodiment, the vias **302** and **402** can be mixed together in the same metal lines **104**.

[0027] FIG. **5**A-FIG. **5**B illustrate a top view of different embodiments of a multi-layer MOM capacitor structure according to another aspect of this disclosure with vias shown in dotted lines underneath the metal lines. In FIG. **5**A, the structure **500** has periphery metal **102**, metal lines **104**, and dielectric (oxide) layers **106**. The vias **302** are slot (rectangular) vias with a variable size depending on the process (e.g., 0.05 μm×0.13 μm). The vias **502** are different size (elongated) rectangular vias. The vias **302** and **502** are alternating on different metal lines **104**. The vias **302** are aligned with each other across multiple metal lines **104** from the top-view shown in FIG. **5**A.

[0028] In FIG. **5**B, the structure **510** has periphery metal **102**, metal lines **104**, and dielectric (oxide) layers **106**. The vias **402** are square vias with a variable size depending on the process (e.g. 0.05 μm×0.05 μm). The vias **502** are elongated rectangular vias with a variable size depending on the process. The vias **402** and **502** are alternating on different metal lines **104**. The vias **402** are aligned with each other across multiple metal lines **104** from the top-view shown in FIG. **5**B.

[0029] The advantages of the new structures include increased capacitance and reduced resistance due to extended via lengths and increased via sidewall area. A skilled person in the art will appreciate that there can be many embodiment variations of this disclosure. For example, instead of slot (rectangular) vias, vias with other shapes (e.g. circular, oval, etc.) could be used, and many different size vias could be mixed and arranged in the structures for different embodiments.

[0030] One aspect of this description relates to a capacitor including a first electrode. The first electrode includes a plurality of first conductive lines, at least one first via, and at least one second via. The first conductive lines on the same layer are parallel to each other and connected to a first periphery conductive line. The first conductor lines aligned in adjacent layers are coupled to each other by the at least one first via and the at least one second via. The at least one first via has a first length parallel to the plurality of first conductive lines, and the at least one second via has a second length parallel to the plurality of first conductive lines different from the first length. The capacitor further includes a second electrode aligned opposite to the first electrode. The second electrode includes a plurality of second conductive lines and at least one third via. The second conductive lines on the same layer are parallel to each other and connected to a second periphery conductive line. The second conductor lines aligned in adjacent layers are coupled to each other by the at least one third via. The capacitor further includes at least one oxide layer formed between the first electrode and the second electrode.

[0031] Another aspect of this description relates to a capacitor including a first electrode. The first electrode includes a plurality of first conductive lines and at least one first via. The first conductive lines on the same layer are parallel to each other and connected to a first periphery conductive line. The first conductor lines aligned in adjacent layers are coupled to each other by the at least one first via. The capacitor further includes a second electrode aligned opposite to the first electrode. The second electrode includes a plurality of second conductive lines and a plurality of second vias. The second conductive lines on the same layer are parallel to each other and connected to a second periphery conductive line. The second conductor lines aligned in adjacent layers are coupled to each other by the plurality of second vias. The at least one first via overlaps with at least two of the plurality of second vias across the plurality of first conductive lines and the plurality of second conductive lines on a same layer. The capacitor further includes at least one oxide layer formed between the first electrode and the second electrode.

[0032] Still another aspect of this description relates to a capacitor including a first electrode. The first electrode includes a first periphery conductive line extending in a Y-direction and a plurality of first conductive lines connected to the first periphery conductive line, the each first conductive line of the plurality of first conductive lines extending in an X-direction perpendicular to the Y-direction. The first electrode further includes at least one first via extending in a Z-direction perpendicular to the X-direction and the Y-direction and at least one second via extending in the Z-direction.

Aligned first conductor lines adjacent to each other in the Z-direction are coupled by the at least one first via and the at least one second via. The at least one first via has a first length in the X-direction, and the at least one second via has a second length in the X-direction different from the first length. The capacitor further includes a second electrode aligned opposite to the first electrode. The second electrode includes a second periphery conductive line extending in the Y-direction and a plurality of second conductive lines connected to the second periphery conductive line, wherein each second conductive line of the plurality of second conductive lines extends in the X-direction. The second electrode further includes at least one third via extending in the Z-direction. Aligned second conductor lines adjacent to each other in the Z-direction are coupled by the at least one third via. The capacitor further includes at least one oxide layer formed between the first electrode and the second electrode.

[0033] Although the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized.

What is claimed is:

1. A capacitor comprising:

a first electrode comprising:

a plurality of first conductive lines (**104**)

at least one first via (**302**); and

at least one second via (**302**), wherein the first conductive lines on the same layer are parallel to each other and connected to a first periphery conductive line (**102**), and the first conductor lines aligned in adjacent layers are coupled to each other by the at least one first via and the at least one second via, wherein the at least one first via has a first length parallel to the plurality of first conductive lines, and the at least one second via has a second length parallel to the plurality of first conductive lines different from the first length (paragraphs 0023-0025);

a second electrode aligned opposite to the first electrode, the second electrode comprising:

a plurality of second conductive lines (**104**); and

at least one third via (**402**), wherein the second conductive lines on the same layer are parallel to each other and connected to a second periphery conductive line (**102**), and the second conductor lines aligned in adjacent layers are coupled to each other by the at least one third via; and

at least one oxide layer (**106**) formed between the first electrode and the second electrode.

2. The capacitor of claim **1**, wherein the at least one third via has a third length parallel to the plurality of second conductive lines, and

the second electrode further comprises at least one fourth via (**402**), the fourth via having a fourth length parallel to the plurality of second conductive lines different from the third length (paragraphs 0023-0025).

3. The capacitor of claim **1**, wherein the at least one first via is aligned with the at least one third via across the plurality of first conductive lines and the plurality of second conductive lines on a same layer (FIG. **4**C).

4. The capacitor of claim **1**, wherein the at least one first via is staggered with respect to the at least one third via across the plurality of first conductive lines and the plurality of second conductive lines on a same layer (FIG. **4**B).

5. The capacitor of claim **1**, wherein the at least one third via has a third length parallel to the plurality of second conductive lines, and the first length is equal to the third length (FIG. **4**A; paragraph 0023).

6. The capacitor of claim **1**, wherein the at least one third via has a third length parallel to the plurality of second conductive lines, and the first length is different from the third length (FIG. **5**A; paragraph 0026).

7. The capacitor of claim **1**, wherein one of the at least one first via or the at least one second via has a square shape (FIG. **4**B; paragraph 0024).

8. A capacitor comprising:

a first electrode comprising:

a plurality of first conductive lines (**104**); and

at least one first via (**502**), wherein the first conductive lines on the same layer are parallel to each other and connected to a first periphery conductive line (**102**), and the first conductor lines aligned in adjacent layers are coupled to each other by the at least one first via;

a second electrode aligned opposite to the first electrode, the second electrode comprising:

a plurality of second conductive lines (**104**); and

a plurality of second vias (**302**), wherein the second conductive lines on the same layer are parallel to each other and connected to a second periphery conductive line (**102**), and the second conductor lines aligned in adjacent layers are coupled to each other by the plurality of second vias, wherein the at least one first via overlaps with at least two of the plurality of second vias across the plurality of first conductive lines and the plurality of second conductive lines on a same layer (FIG. **5**A-**5**B; paragraphs 0026-0027); and

at least one oxide layer (**106**) formed between the first electrode and the second electrode.

9. The capacitor of claim **8**, wherein the plurality of second vias comprises:

a third via having a length parallel to the plurality of second conductive lines; and

a fourth via having a length parallel to the plurality of second conductive lines, wherein the length of the third via is different from the length of the fourth via (paragraph 0026).

10. The capacitor of claim **8**, wherein each via of the plurality of second vias has a square shape (FIG. **5**B).

11. The capacitor of claim **8**, wherein each via of the plurality of second vias has a rectangular shape (FIG. **5**A).

12. A capacitor comprising:

a first electrode comprising:

a first periphery conductive line (**102**) extending in a Y-direction;

a plurality of first conductive lines (**104**) connected to the first periphery conductive line, the each first con-

ductive line of the plurality of first conductive lines extending in an X-direction perpendicular to the Y-direction;

at least one first via (**302**) extending in a Z-direction perpendicular to the X-direction and the Y-direction; and

at least one second via (**302**) extending in the Z-direction, wherein aligned first conductor lines adjacent to each other in the Z-direction are coupled by the at least one first via and the at least one second via, wherein the at least one first via has a first length in the X-direction, and the at least one second via has a second length in the X-direction different from the first length (paragraphs 0023-0025);

a second electrode aligned opposite to the first electrode, the second electrode comprising:

a second periphery conductive line (**102**) extending in the Y-direction;

a plurality of second conductive lines (**104**) connected to the second periphery conductive line, wherein each second conductive line of the plurality of second conductive lines extends in the X-direction; and

at least one third via (**402**) extending in the Z-direction, wherein aligned second conductor lines adjacent to each other in the Z-direction are coupled by the at least one third via; and

at least one oxide layer (**106**) formed between the first electrode and the second electrode.

13. The capacitor of claim **12**, wherein the at least one third via has a third length in the X-direction, and the second electrode further comprises at least one fourth via (**402**), the fourth via having a fourth length in the X-direction different from the third length (paragraphs 0023-0025).

14. The capacitor of claim **12**, wherein the at least one first via is aligned with the at least one third via in the Y-direction (FIG. **4**C).

15. The capacitor of claim **12**, wherein the at least one first via is staggered with respect to the at least one third via in the Y-direction (FIG. **4**B).

16. The capacitor of claim **12**, wherein the at least one third via has a third length in the X-direction, and the first length is equal to the third length (FIG. **4**A; paragraph 0023).

17. The capacitor of claim **12**, wherein the at least one third via has a third length in the X-direction, and the first length is different from the third length (FIG. **5**A; paragraph 0026).

18. The capacitor of claim **12**, wherein one of the at least one first via or the at least one second via has a square shape (FIG. **4**B; paragraph 0024).

19. The capacitor of claim **12**, wherein the at least one third via overlaps with the at least one first via and the at least one second via in the Y-direction (FIG. **5**A-**5**B; paragraphs 0026-0027).

20. The capacitor of claim **12**, wherein the second electrode further comprises at least one fourth via (**402**), the at least one first via is aligned with the at least one third via in the Y-direction, and the at least one second via is aligned with the at least one fourth via in the Y-direction. (FIG. **4**C)

* * * * *