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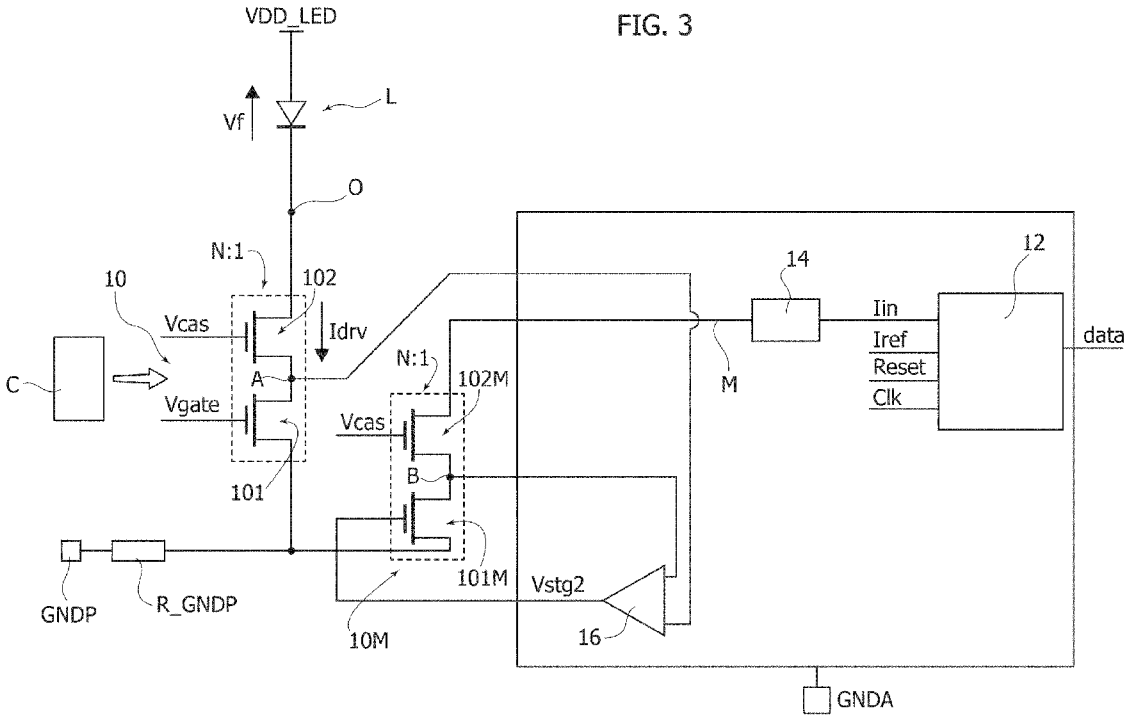
(54) **Title:** MONITORING CIRCUIT AND CORRESPONDING METHOD

FIG. 3



(57) **Abstract:** A current-monitoring circuit (Idrv) through an electrical load (L) (such as a LED source) comprises a first cascode configuration (10) with a first transistor (101) that receives on a control terminal a conduction-control signal (Vgate). The current paths through the first transistor (101) and the second transistor (102) of the cascode are cascaded in a current flow line between the load (O, L) and ground (GNDP). A second cascode configuration (10M) with a third transistor (101M) and a fourth transistor (102M) is coupled in a current-mirror arrangement (N:1) to the first cascode configuration (10). The current paths through the third transistor (101M) and the fourth transistor (102M) are cascaded in a current flow line that replicates the load current (Idrv) between a monitoring node (M) and ground (GNDP). An error amplifier such as an operational amplifier (16) has its inputs coupled, respectively, to a first intermediate node (A) in the current flow line and to a second intermediate node (B) in the replica-current flow line. The error amplifier (16) has an

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output coupled to a control terminal of the third transistor (101M). Circuitry (12, 14) for monitoring the load current (Idrv) coupled to the monitoring node (M) issues a monitoring signal (data) indicative of the intensity of the load current (Idrv).

Monitoring circuit and corresponding method

Technical field

The disclosure relates to techniques for monitoring electrical loads.

One or more embodiments may be applied to driving of solid-state light sources, for example LED sources.

Technological background

Various applications, for example applications in which it is desired to achieve a high level of functional safety, envisage monitoring the output current produced by a driver, for example a circuit used for driving solid-state light sources, such as LED sources.

The corresponding prior art is rather extensive.

For instance, document US 6 734 639 B2 describes a circuit for driving LED arrays in a system having a converter that supplies the biasing voltage for the LED array. The load on the converter is controlled in such a way that conduction at output from the converter occurs only when the LEDs are turned on and supply a load at output from the converter. A sample-and-hold technique is used for storing the information on a previous ON interval and using it for control of the current in a subsequent interval.

Document US 2014/097828 A1 describes a power stage that can be connected to a network cable for carrying power supply and data. The power stage comprises a transistor located in a main current flow path and a current-monitoring circuit for monitoring the flow of current in the main current flow path. Instead of a sensor set in series with the main current flow path, the current-monitoring function uses a stage that mirrors the current in the main current flow path.

In this regard, reference may again be made to the text by T. Regan, *et al.*: "AN-105: Current Sense Circuit Collection Making Sense of Current" (accessible online at the address https://www.analog.com/en/app-notes/an-105fa.html).

In summary, a fair share of the solutions documented in the literature fall into two fundamental categories that envisage detection of the voltage drop across a resistance in series to the load, i.e., mirroring the output device of the driver to obtain a scaled replica of the current, which is then measured directly or converted into a voltage and then measured.

The applications in which it is desired to achieve a high level of functional safety envisage, according to the degree of safety, a given rate of detection of hardware failures. Even though they may be assumed as being random, such failures are generally linked in a proportional way to the area of the semiconductor (silicon) for the integrated circuits and/or to the number and type of parts included in the circuit block of interest.

It is desirable to have available safety mechanisms such as current monitors in order to detect when there occur hardware failures such as to induce significant deviations in the parameters expressed by a hardware block, such as the current at output from the driver.

A safety mechanism may be characterized by a detection rate that indicates the probability associated to detection of a random error or failure in the block.

A series detection resistor is able to afford a high detection rate. This solution is not, however, always practicable, either because, if the currents are high, there is a high dissipation of power, or because a series

resistance requires a low-noise and high-precision read circuit, which is difficult to implement in a context of application affected by noise.

Achievement of a high precision is facilitated by a current driver provided as cascade-current source.

The term "cascode" identifies a particular circuit configuration obtained by setting two transistors (for example, two bipolar transistors or two field-effect transistors - FETs) in series. The cascode combines the positive characteristics of the common-emitter (-source) configuration and of the common-base (-gate) configuration to obtain a good pass band combined with a high output resistance and a relatively high voltage gain.

This effect is obtained because the collector-to-emitter voltage (or the drain-to-source voltage, in the case of use of FETs) of the first transistor is kept practically constant.

In order to achieve adequate levels of functional safety, for example in compliance with specifications such as ASIL-B (detection > 90%) it is desirable to be able to detect possible failures in the cascode-regulation circuits as likewise possible failures in the cascode itself.

The cascode is suited to being regulated so as to obtain a good matching of the current mirror. The monitoring solutions that envisage mirroring the transistor that operates as current source may, however, prove unsatisfactory in so far as the hardware components or the silicon area associated to the cascode and to control thereof are not monitored, which leads to a reduction in the detection rate.

Object and summary

The object of one or more embodiments is to facilitate achievement of a higher detection rate, without this leading to an undesired increase in the hardware associated to the monitored block and/or introduction of hardware components in series with respect to the monitored current.

According to one or more embodiments, the above object is achieved thanks to a circuit having the characteristics recalled in the ensuing claims.

One or more embodiments refer to a corresponding method.

The claims form an integral part of the technical teachings provided herein in relation to embodiments.

Solutions like the ones described herein facilitate the production of current monitors that will not require a further detection element in series, such as a resistor, that might introduce an additional consumption and require a high read sensitivity.

Brief description of the drawings

One or more embodiments will now be described, purely by way of non-limiting example, with reference to the annexed figures, wherein:

Figures 1 and 2 are block diagrams representing the prior art, in the terms already discussed previously;

Figure 3 is a block diagram exemplifying embodiments according to the present disclosure; and

Figure 4 illustrates possible advantageous developments of embodiments according to the present disclosure.

It will be appreciated that, for clarity and simplicity of illustration, the various figures may not be represented at the same scale.

Moreover, for reasons of brevity – and unless the context indicates otherwise – parts or elements that are

similar are denoted in the various figures by the same reference symbols, without a corresponding description being repeated for each figure.

Moreover, throughout this description, one and the same designation may be used, for reasons of brevity, to indicate:

both a certain node or line and a signal that is set up on such node or line, as well as

both a certain component (for example, a capacitor or a resistor) and an electrical parameter thereof (for example, a capacitance or a resistance/impedance).

Detailed description of examples of embodiment

In the ensuing description various specific details are illustrated in order to enable an in-depth understanding of various examples of embodiments according to the description. The embodiments may be obtained without one or more of the specific details, or with other methods, components, materials, etc. In other cases, known structures, materials or operations are not illustrated or described in detail in such a way that the various aspects of the embodiments will not be obscured.

Reference to "an embodiment" or "one embodiment" in the framework of the present description is intended to indicate that a particular configuration, structure, or characteristic described in relation to the embodiment is comprised in at least one embodiment. Hence, phrases such as "in an embodiment" or "in one embodiment" that may be present in various points of the present description do not necessarily refer exactly to one and the same embodiment. Moreover, particular conformations, structures, or characteristics may be combined adequately in one or more embodiments.

The references used herein are provided merely for convenience and hence do not define the sphere of the invention or the scope of the embodiments.

In all of the figures, the reference L designates an electrical load here exemplified in the form of a LED light source, to which a (DC) supply voltage Vf is assumed to be applied.

The load L is to be traversed by a driving current Idrv that is to be monitored.

For this purpose, it is assumed that the load L is set between a supply line or node at a voltage VDD_ LED and a node O (load node) that comes under a driving stage 10 comprising two transistors 101 and 102 (for example, FETs) in a (first) cascode configuration.

It will be appreciated that the load L (as illustrated in all of Figures 1 to 4) usually constitutes an element distinct from the driving stage 10 and the elements associated thereto for monitoring purposes.

The driving stage 10 (to which the load L may hence be associated only at the moment of use) can be rendered selectively conductive and non-conductive so as to drive the current Idrv through the load L.

In particular, the load L is traversed by the current Idrv when the transistors 101, 102 of the stage 10 are conductive, whereas the current Idrv is virtually zero when the transistors 101, 102 of the stage 10 are non-conductive.

Switching of the transistors 101, 102 of the stage 10 between the conductive state and the non-conductive state is obtained as a function of a signal produced (in a way in itself known) by a control circuit denoted as a whole by C.

In this connection, it will be appreciated that the embodiments described herein mainly regard the function of

monitoring (the intensity) of the current Idrv, irrespective of the criteria adopted for driving the current Idrv, dictated by the requirements of application and use (to provide just an example: dimming of the source comprised in the load L to get the intensity of the light radiation emitted by the source to vary).

In the example illustrated herein, it may be assumed that the control circuit C applies an ON/OFF signal Vgate to the control terminal (gate in the case of a FET) of the transistor 101 (current source), while a cascode voltage Vcas (produced in a way in itself known to persons skilled in the sector) is applied to the control terminal (gate in the case of a FET) of the transistor 102.

It is once again recalled that the term "cascode" identifies a particular circuit configuration obtained by setting two transistors (for example two FETs such as 101 and 102) in series with one another in such a way that, when the transistors 101, 102 are conductive, the current Idrv flows in the current paths (source-to-drain in the case of FETs), which may be viewed as cascaded with one another between the node O (to which the load L is to be connected) and ground GNDP.

As has already been said, a fair share of the solutions documented in the literature fall into two fundamental categories that envisage:

as illustrated in Figure 1, detection of the voltage drop across an amperometry resistance R_{AMP} in series to the load L, or else;

as illustrated in Figure 2, replicating (mirroring) with a current-mirror arrangement the output cascode 10 of the driver to obtain a scaled replica (for example, N:1) of

the current Idrv via two further transistors in a (second) cascode configuration 10M.

In the case illustrated in Figure 1, the voltage across the amperometry resistor R_{AMP} is applied between the inputs Vinp and Vinm of an analog-to-digital converter (ADC) 12 to supply a read datum at output, designated by "data", which may be supplied, for example, to the control circuit C for controlling the function of driving of the current Idrv.

As illustrated herein, the converter 12 receives signals Ref (voltage or current reference), Reset, and Clk (clock) that regulate operation thereof (in a way in itself known to persons skilled in the sector).

In the case illustrated in Figure 2, the current Idrv is replicated (for example, in a ratio N:1) by the current mirror 10M (which is also in cascode configuration) that mirrors the current Idrv, then supplying it as current Iin (possibly after passage into another current mirror 14, M:1) to an analog-to-digital converter (ADC) 12 to supply a read datum at output, designated by "data".

It is recalled that by "current mirror" is commonly meant a configuration of electronic devices, such as transistors, that is built so as to reproduce faithfully, in one branch of an electronic circuit, the current circulating in another branch of the same circuit. The current to be reproduced may be constant or variable according to the use.

Also in this case, the output-current read datum ("data") may be supplied to the control circuit C to control the function of driving of the current Idrv.

Consequently, in both cases (Figure 1 and Figure 2), the current Idrv is either measured directly or converted into a voltage that is then to be measured.

Figures 1 and 2 (and also Figures 3 and 4) highlight the fact that the ground of the power stage GNDP is typically characterized by a significant voltage drop (exemplified by a resistor R_GNDP) that is liable to cause a DC shift and noise on the current generated by the current generator.

As has already been noted, the solution that envisages a series detection resistor (R_{AMP} in Figure 1) is able to afford a high detection rate: however, it may not always be practicable, either on account of the possible high power dissipation or on account of the difficulty of implementing the read circuit (basically the converter 12) with characteristics of low noise and high precision.

Also the solutions as exemplified in Figures 3 and 4 (like the solution of Figure 2) point in the direction of obtaining high precision thanks to a current driver provided as cascode current source and of mirroring the cascode current in some way.

Solutions as exemplified in Figures 3 and 4 afford, however, the advantage of "covering" the function of the current-source element and of the cascode biasing circuit, reducing the number of types of failure or fault in the cascode that could not be detected. The corresponding detection rate is hence appreciably higher.

This overcomes the intrinsic drawbacks of traditional current-mirror solutions (see Figure 2), where only a (perhaps negligible) part of the area of the circuitry is monitored, especially when high mirroring ratios are implemented in the driver. It may be noted, in fact, that the diode of the source could be functional, when the gate voltage of the mirror is supplied, with the output circuit that might be faulty.

There could also remain faults in biasing of the cascode that may not be detectable in the current-mirror monitoring solution exemplified in Figure 2.

In the solutions according to Figures 3 and 4 (where – unless the context indicates otherwise – parts or elements similar to parts or elements already described in relation to Figures 1 and 2 are designated by the same reference symbols, without a corresponding detailed description being repeated) it is hence possible to recognize a circuit that comprises:

a load node O configured to be connected to an electrical load L (for example, a LED source),

a first transistor 101 and a second transistor 102 in a first cascode configuration (designated as a whole by 10), with the first transistor 101 having a control terminal (gate, in the case of a FET) configured to receive, for example from the circuit C, a conduction-control signal with the current paths (source-to-drain, in the case of FETs) through the first transistor 101, and the second transistor 102 cascaded in a current flow line between the load node O and ground GNDP.

With the first transistor 101 (current source) conductive, a load current Idrv flows in the current flow line through the transistors 101 and 102 (and hence through the load L).

In the solutions according to Figures 3 and 4, there are likewise present a third transistor 101M and a fourth transistor 102M in a (second) cascode configuration (designated as a whole by 10M) that is coupled in a current-mirror arrangement (for example, with a mirroring ratio N:1) to the first cascode configuration 10 comprising the transistors 101 and 102.

It is once again recalled that by "current mirror" is commonly meant a configuration of electronic devices, such as (bipolar or field-effect) transistors, provided for replicating faithfully, for example in a ratio N:1, in one branch of an electronic circuit the current circulating in another branch of the same circuit. The current to be reproduced may be constant or variable according to the use.

Current mirrors, as likewise cascode configurations, are suited to being implemented both with bipolar transistors and with field-effect transistors. The fact that the present description and the annexed figures refer to field-effect transistors has hence merely an exemplary nature and in no way limits the scope of the embodiments.

In the solutions according to Figures 3 and 4, the current paths (source-to-drain in the case of FETs) through the third transistor 101M and the fourth transistor 102M are cascaded in a current flow line that is to be traversed by a current that replicates (for example, with a scaling ratio of N:1) the current Idrv through the load L, which is to be monitored.

As illustrated, the aforesaid replica-current flow line extends between a monitoring node or line M (for monitoring the load current Idrv) and ground GNDP.

In the solutions according to Figures 3 and 4 a differential stage 16 (for example, a high-gain operational amplifier – OpAmp) is used as error amplifier.

The stage 16 receives at input the voltages at the intermediate nodes, designated by A and B, of the two cascodes 10 and 10M, and then detects the difference between:

the voltage at the node A between the two transistors 101 and 102 of the cascode 10, and

the voltage at the node B between the two transistors 101M and 102M of the cascode 10M.

In the solutions according to Figures 3 and 4 an error amplifier 16 (for example, an OpAmp) is hence present with inputs coupled, respectively:

to a first intermediate node (node A) of the current flow line (through the cascode 10), with a transistor of the first cascode configuration (for example, the second transistor 102) set between the load node O and the first intermediate node A, and

to a second intermediate node (node B) of the replica-current flow line (through the cascode 10M), with a transistor of the second cascode configuration (for example, the fourth transistor 102M) set between the monitoring node M and the second intermediate node B.

In the solutions according to Figures 3 and 4, the error amplifier 16 has the output coupled to the control terminal (gate, in the case of a FET) of the third transistor 101M.

At the same time, the control terminal (gate, in the case of a FET) of the first transistor 101 continues to be configured to receive (as signal Vgate) the signal for driving in conduction, starting from the circuit C, and the control terminals (gates, in the case of FETs) of the second transistor 102 and of the fourth transistor 102M receive a cascode voltage Vcas, produced in a way in itself known to persons skilled in the sector.

The output (voltage) signal of the stage 16, Vstg2, is applied to the control terminal – gate in the case of a FET – of the third transistor 101M of the cascode 10M.

As illustrated, the stage 16 is thus used for regulating the current source (transistor 101M) of the cascode replica

circuit 10M, whilst the gate of the transistor 102M is biased at the same gate voltage Vcas as the homologous transistor 102 in the main cascode device 10.

The voltage of the replica source is then fed back to the operational amplifier 16 in negative feedback so that the voltage of the current source (transistor 101M) of the cascode replica device 10M is forced to be equal (or almost equal) to that of the main cascode 10.

Immunity in regard to ground shifts within the bandwidth of the regulation circuit is facilitated by the fact that the ground voltage of the replica cascode 10M is the same as that of the final power stage 10.

The current produced by the replica cascode 10M is applied (possibly after passage in another current mirror 14, M:1) as current Iin to an analog-to-digital converter (ADC) 12 to supply at output the read datum, denoted by "data", which, again, can be supplied to the control circuit C for controlling the function of driving of the current Idrv.

In the solutions according to Figures 3 and 4 there is hence present circuitry (the converter 12 and, possibly, the further current mirror 14) for monitoring the load current Idrv. This circuitry is coupled to the monitoring node M and is consequently configured to issue a monitoring signal (for example, the signal "data", in digital format) indicative of the intensity of the current Idrv that is driven in the load L thanks to the current flow line through the first cascode 10 comprising the transistors 101 and 102.

Figure 4 (where, once again and unless the context indicates otherwise, parts or elements that are similar to parts or elements already described in relation to Figures 1 and 3 are designated by the same reference symbols, without

a corresponding detailed description being repeated) exemplifies the possibility of extending the solution exemplified in Figure 3 to monitoring of the current Idrv in a plurality of N output driver stages (assumed to be the same as one another for simplicity) via multiplexers designated as a whole by 18.

The output drivers that are currently not selected for the purposes of current monitoring may be off or else be kept connected to the control loop in so far as the output current can be selected by a multiplexer.

In the case of a number of drivers (DRV), the ground connection reaches each driver, so that in Figure 4 is indicated a respective resistive value R_GNDP_DRV, coming under the resistance R_GNDP. The total voltage drop will be distributed between R_GNDP and R_GNDP_DRV and each replica continues to "see" the same ground voltage of the corresponding driver.

In summary, a solution as exemplified in Figure 4 comprises a plurality of N load nodes (such as the node O) configured to be connected to respective electrical loads L.

In a solution as exemplified in Figure 4, the aforesaid load nodes have coupled to them, according to the criteria discussed previously with reference to Figure 3:

respective first cascode configurations 10;

respective second cascode configurations 10M, with replica-current flow lines between respective load-current monitoring nodes M1, …, MN and ground GNDP; as well as

respective error amplifiers 16.

In the solution as exemplified in Figure 4, the load-current monitoring circuitry 12, 14 is a common circuitry, and the multiplexers 18 are configured to couple selectively to the aforesaid common monitoring circuitry (converter 12

and, possibly, scaling circuit 14) the aforesaid respective current-monitoring nodes M1, …, MN.

The above common circuitry is thus able to issue as signals "data" N monitoring signals (e.g., in digital format) indicative of the intensity of the load current in N respective electrical loads.

A solution as exemplified in Figure 4 is suited to being used with a routine of reading of the corresponding monitoring data implemented as sequence of steps in which a multiplexer selects a certain configuration, a corresponding measurement is obtained (for example, via the converter 12), a new multiplexer configuration is selected, a corresponding measurement is obtained, and so forth.

This embodiment facilitates a scaling of functionality with a reduced overhead at a hardware level.

Solutions as illustrated in Figures 3 and 4 afford the advantage represented by the fact that monitoring is carried out on the last element of the chain for supply of the load L so that detection of the cascode current provides a coverage of detection of hardware failures that is wider than solutions (like that of Figure 2) that are based upon a current-source detection.

In solutions like the ones illustrated in Figures 3 and 4, the output stage 10 of the driver comprises a current-source element (transistor 101) and a cascode element (transistor 102) in combination with a replica-cascode stage 10M, with a scale factor of N.

The replica stage 10M is driven (on the gate of the transistor 101M) by an operational amplifier 16 in closed-loop configuration, where the corresponding error signal (given by the difference between the voltages at the nodes A and B, i.e., between the voltage on the current source of

the main cascode driver 10 and the voltage on the current source of the replica cascode driver 10M) tends to be cancelled out by the gain of the loop in which the operational amplifier 16 is inserted.

The output current of the replica driver 10M is optionally again scaled by a factor M in block 14.

The resulting current is digitalized in the converter 12 to supply the reading "data" of the current scaled by the gain of the converter 12 and by the factor N×M.

Since the ground of the power stage GNDP is typically characterized by a significant voltage drop that causes a DC shift and noise, the proposed solution provides a high degree of immunity in regard to ground shifts.

This is obtained by the regulation circuit, which forces the voltages at the nodes A and B of the main-cascode current source 10 and of the replica-cascode current source 10M to be the same.

The control loop can be assigned to a separate ground-voltage supply (denoted by GNDA in Figures 3 and 4) so that the analog circuit is thus decoupled from the switching noise and from the ground shifts in the supply (GNDP).

In other words, the circuitry 12, 14 that monitors the load current Idrv is referenced to a respective ground GNDA that is distinct from the ground GNDP of the first cascode configuration 10 and of the second cascode configuration 10M.

The immunity to noise is further improved using an oversampling converter 12, with a bandwidth narrower than the bandwidth of the control loop.

Without prejudice to the underlying principles, the details of construction and the embodiments may vary, even significantly, with respect to what has been illustrated

herein, purely by way of non-limiting example, without thereby departing from the scope of the invention, said scope being specified by the annexed claims.

LIST OF THE REFERENCE SYMBOLS

Load (LED source)	L
Load supply	VDD_LED
Load voltage	Vf
Load current	Idrv
Load node	O
Control circuit	C
Main cascode	10
First main cascode transistor	101
Second main cascode transistor	102
Cascode ground	GNDP
Cascode-ground shift	R_GNDP
	R_GNDP_DRV
Replica cascode	10M
First replica-cascode transistor	101M
Second replica-cascode transistor	102M
Intermediate nodes	A, B
Monitoring node	M; M1, …, MN
Analog-to-digital converter	12
Current mirror	14
Operational amplifier	16
Ground of monitoring circuit	GNDA

CLAIMS

1. A circuit, comprising:

a load node (O) configured to be connected to an electrical load (L),

a first transistor (101) and a second transistor (102) in a first cascode configuration (10), the first transistor (101) having a control terminal configured to receive a conduction control signal (Vgate), with current paths through the first transistor (101) and the second transistor (102) cascaded in a current flow line between said load node (O) and ground (GNDP), wherein, with the first transistor (101) conductive, a load current (Idrv) flows in said current flow line,

a third transistor (101M) and a fourth transistor (102M) in a second cascode configuration (10M), the second cascode configuration (10M) coupled in a current mirror arrangement (N:1) to the first cascode configuration (10), with current flow paths through the third transistor (101M) and the fourth transistor (102M) cascaded in a replica current flow line configured to be traversed by a replica of said load current (Idrv), said replica current flow line being between a load current (Idrv) monitoring node (M) and ground (GNDP),

an error amplifier (16) having inputs coupled, respectively, to a first intermediate node (A) in the current flow line with a transistor (102) of the first cascode configuration between said load node (O) and said first intermediate node (A) and to a second intermediate node (B) in the replica current flow line with a transistor (102M) of the second cascode configuration (10M) between said monitoring node (M) and said second intermediate node (B),

the error amplifier (16) having an output coupled to a control terminal of the third transistor (101M), and

load current (Idrv) monitoring circuitry (12, 14) coupled to said monitoring node (M) and configured to produce a monitoring signal (data) indicative of the intensity of the load current (Idrv) in said current flow line.

2. The circuit of claim 1, wherein the load current (Idrv) monitoring circuitry (12, 14) comprises an analog-to-digital converter (12), wherein said monitoring signal (data) is a digital signal.

3. The circuit of claim 2, wherein the load current (Idrv) monitoring circuitry (12, 14) comprises an oversampling analog-to-digital converter (12).

4. The circuit of any of the preceding claims, wherein the load current (Idrv) monitoring circuitry (12, 14) comprises a scaling circuit (14) coupled to said monitoring node (M), wherein said monitoring signal (data) is a function of a scaled replica of the signal at said monitoring node (M).

5. The circuit of any of the preceding claims, wherein the first (101), second (102), third (101M) and fourth (102M) transistors comprise field effect transistors.

6. The circuit of any of the preceding claims, wherein the error amplifier (16) comprises an operational amplifier.

7. The circuit of any of the preceding claims, wherein the load current (Idrv) monitoring circuitry (12, 14) is

referred to a respective ground (GNDA) distinct from the ground (GNDP) of the first cascode configuration (10) and of the second cascode configuration (10M).

8. The circuit of any of the preceding claims, comprising:

a plurality of load nodes (O) configured to be connected to respective electrical loads (L), wherein the load nodes in said plurality of load nodes (O) have coupled therewith respective said first cascode configurations (10), respective said second cascode configurations (10M) with replica current flow lines between respective load current (Idrv) monitoring nodes (M1, ..., MN) and ground (GNDP), as well as respective said error amplifiers (16), and

a common load current (Idrv) monitoring circuitry (12, 14) comprising multiplexer circuitry (18) configured to selectively couple said common monitoring circuitry (12, 14) to said respective load current (Idrv) monitoring nodes (M1, ..., MN) and to issue respective monitoring signals (data) indicative of the intensity of the load current (Idrv) in said respective electrical loads (L).

9. A method, comprising:

connecting an electrical load (L) to a load node (O),

cascading a first transistor (101) and a second transistor (102) in a first cascode configuration (10) in a current flow line between said load node (O) and ground (GNDP) and applying to a control terminal of the first transistor (101) a conduction control signal (Vgate), wherein, with the first transistor (101) conductive, a current (Idrv) flows in the electric load (L) connected to the load node (O) through said current flow line,

coupling in a current mirror arrangement (N:1) the first cascode configuration (10) to a second cascode configuration (10M) with a third transistor (101M) and a fourth transistor (102M) having current paths through the third transistor (101M) and the fourth transistor (102M) cascaded in a replica current flow line traversed by a replica of said load current (Idrv), said replica current flow line being between a load current (Idrv) monitoring node (M) and ground (GNDP),

coupling the inputs of an error amplifier (16), respectively, to a first intermediate node (A) in the current flow line with a transistor (102) of the first cascode configuration between said load node (O) and said first intermediate node (A) and to a second intermediate node (B) in the replica current flow line with a transistor (102M) of the second cascode configuration (10M) between said monitoring node (M) and said second intermediate node (B), also coupling an output of the error amplifier (16) to a control terminal of the third transistor (101M), and

monitoring the load current (Idrv) with monitoring circuitry (12, 14) which is coupled to said monitoring node (M) and which outputs a monitoring signal (data) indicative of the intensity of the load current (Idrv) in said current flow line.

FIG. 1

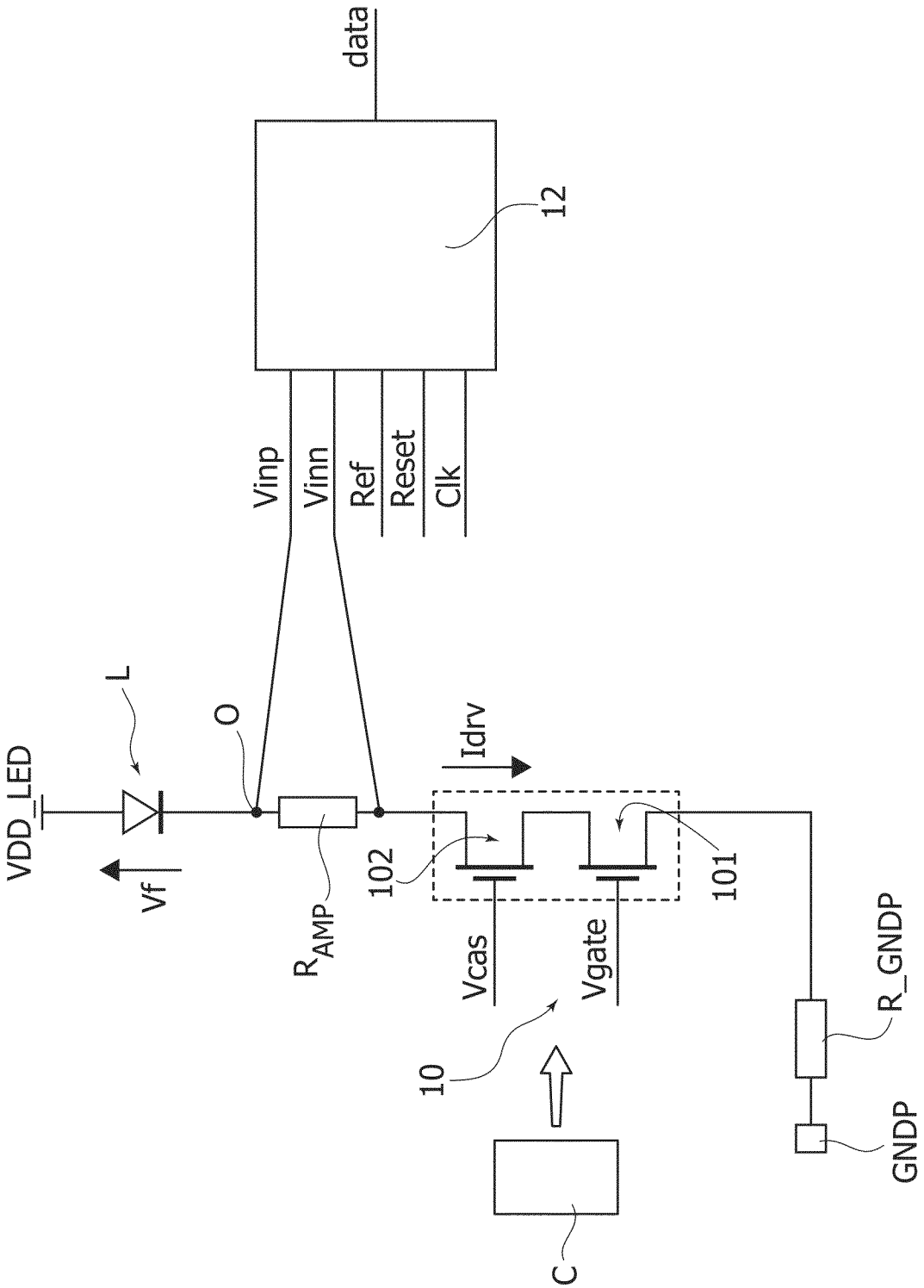

data
12
Vinp
Vinn
Ref
Reset
Clk
L
O
Idrv
VDD_LED
Vf
R_{AMP}
102
101
Vcas
Vgate
R_GNDP
10
GNDP
C

FIG. 2

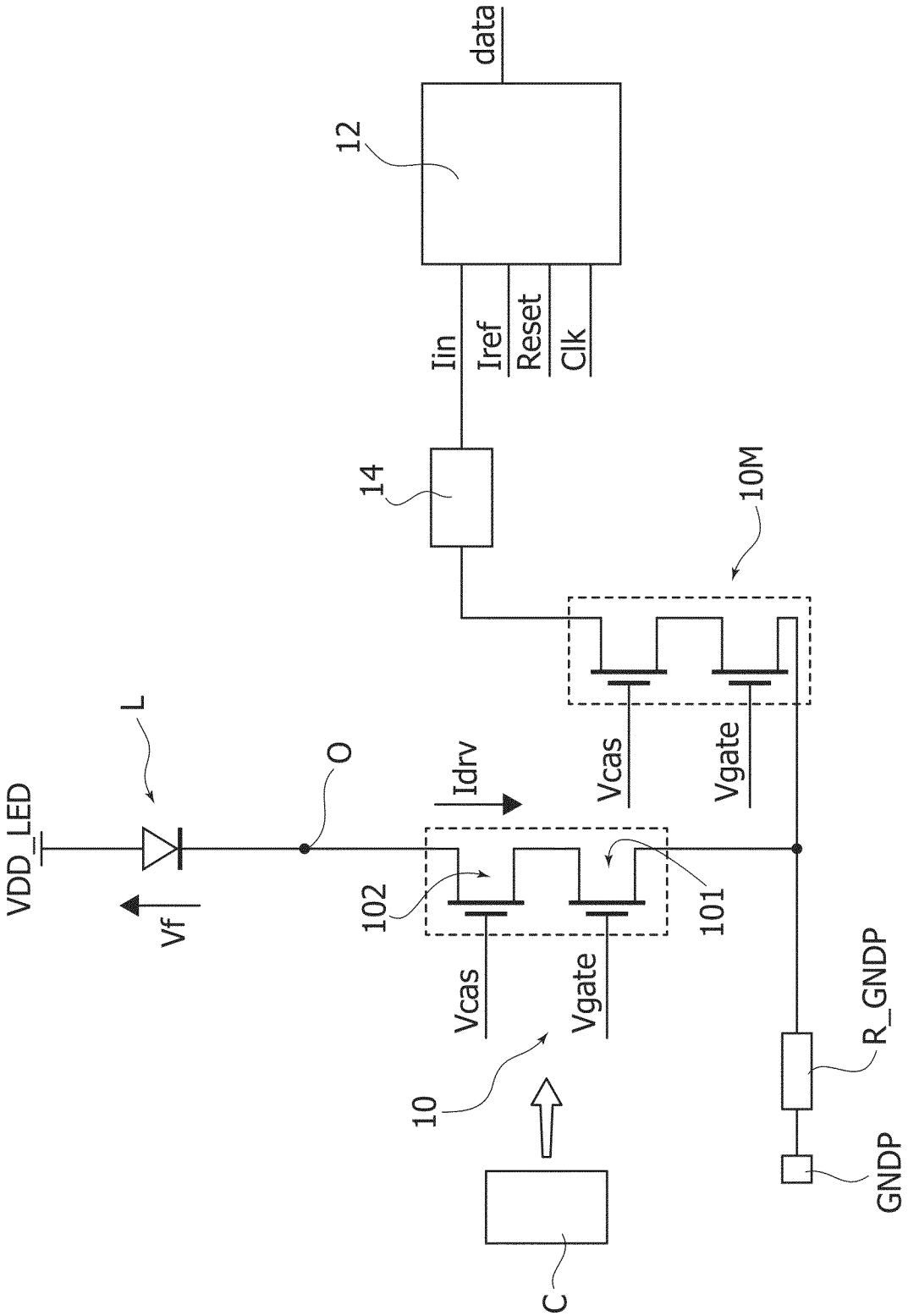
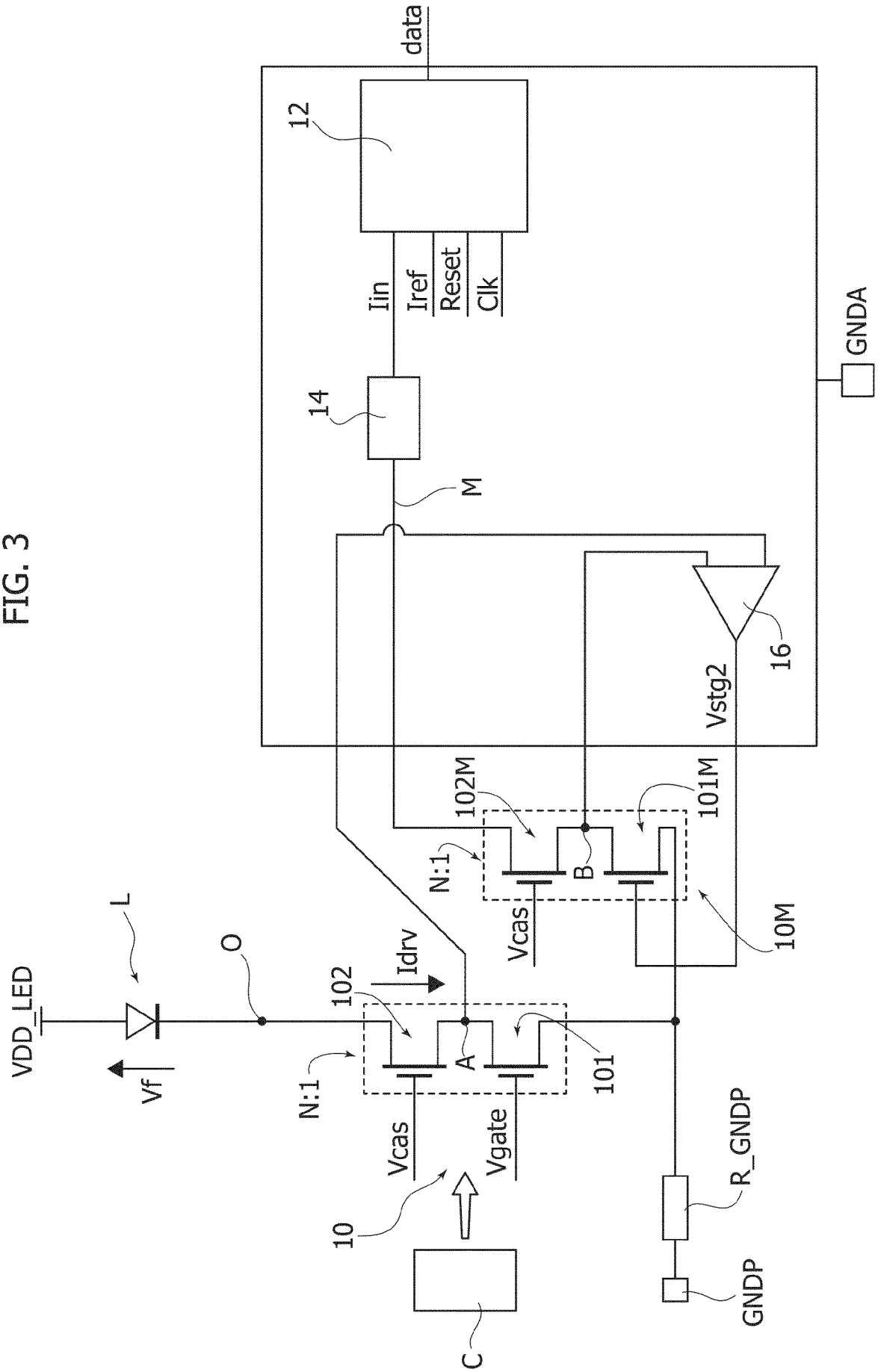

data
12
Iin
Iref
Reset
Clk
14
10M
L
O
Idrv
Vcas
Vgate
VDD_LED
Vf
102
101
Vcas
Vgate
R_GNDP
10
GNDP
C

FIG. 3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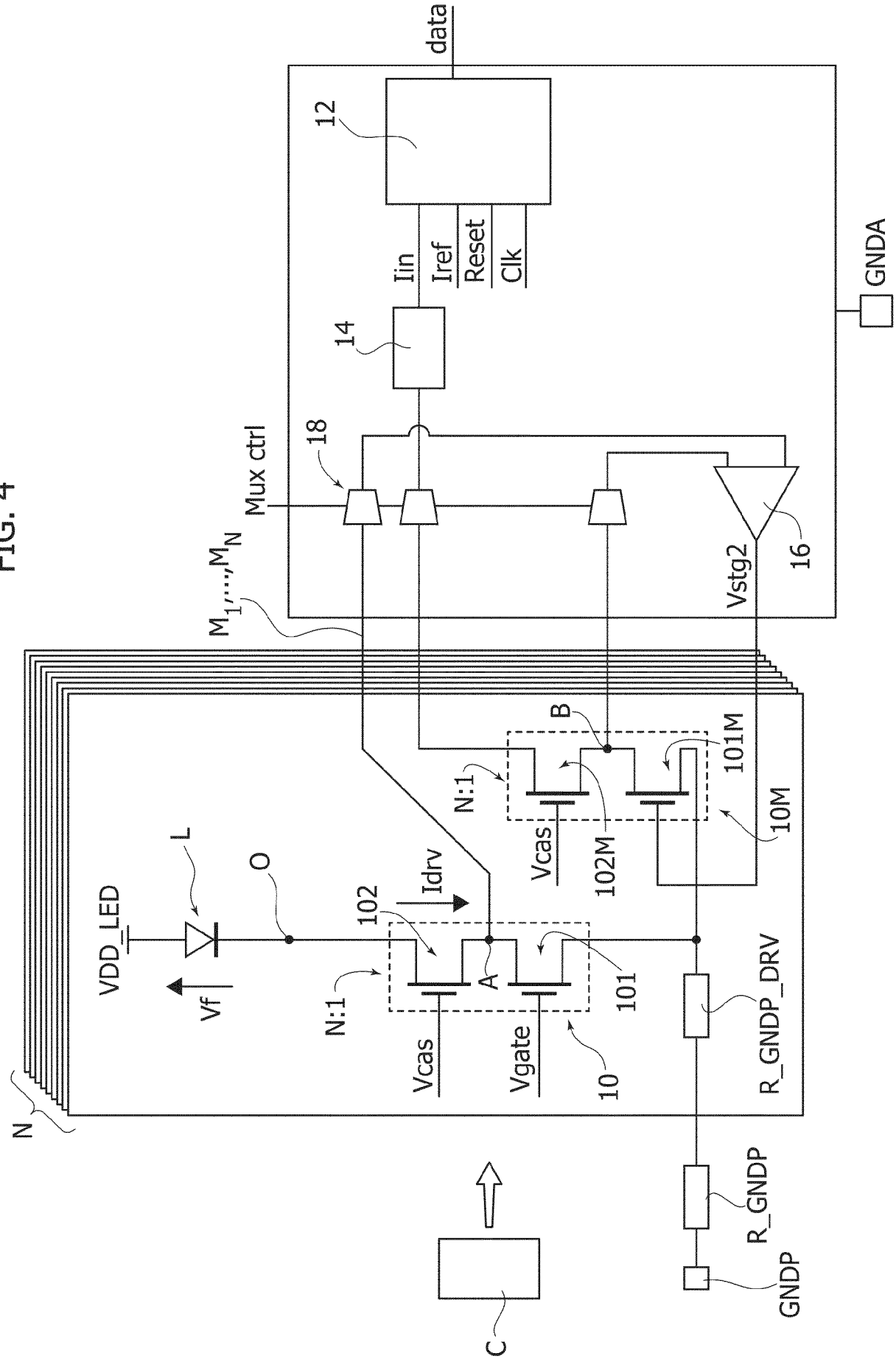
Iin
Iref
Reset
Clk
GNDA
14
M
16
Vstg2
102M
101M
N:1
B
Vcas
10M
L
O
Idrv
102
VDD_LED
Vf
N:1
A
101
Vcas
Vgate
R_GNDP
10
GNDP
C

FIG. 4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12
Iin
Iref
Reset
Clk
GNDA
14
18
Mux ctrl
$M_1,\ldots,M_N$
Vstg2
16
B
101M
N:1
10M
Vcas
102M
L
O
Idrv
102
VDD_LED
Vf
N:1
A
101
R_GNDP_DRV
Vcas
Vgate
10
N
C
R_GNDP
GNDP

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2024/054910

A. CLASSIFICATION OF SUBJECT MATTER
INV. H05B45/345 H05B45/50 H05B45/397 H02M1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H05B H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MOHAMMAD HOSSEIN MAGHAMI ET AL: "Analysis and design of a high-compliance ultra-high output resistance current mirror employing positive shunt feedback", INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, JOHN WILEY & SONS, INC, HOBOKEN, USA, vol. 43, no. 12, 5 December 2014 (2014-12-05), pages 1935-1952, XP071448064, ISSN: 0098-9886, DOI: 10.1002/CTA.2049 the whole document -----	1-9
A	US 8 947 008 B2 (CHUANG YU-CHUN [TW]; PU RUEI-IUN [TW]; SILICON TOUCH TECH INC [TW]) 3 February 2015 (2015-02-03) figure 2 -----	1,9
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 May 2024	27/05/2024

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Alberti, Carine

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2024/054910

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2019/387588 A1 (GREENWOOD JOHN DAVID [GB]) 19 December 2019 (2019-12-19) figures 5-6,8-9	1,9
A	US 6 194 967 B1 (JOHNSON LUKE A [US] ET AL) 27 February 2001 (2001-02-27) figures	1,9
X	US 9 961 729 B1 (NARAYANAN SHYAM [DE] ET AL) 1 May 2018 (2018-05-01) figure 6	1-9

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2024/054910

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 8947008 B2	03-02-2015	CN 102970789 A	13-03-2013
		EP 2597931 A2	29-05-2013
		JP 5328964 B2	30-10-2013
		JP 2013055657 A	21-03-2013
		TW 201313060 A	16-03-2013
		US 2013057175 A1	07-03-2013
US 2019387588 A1	19-12-2019	CN 110619853 A	27-12-2019
		JP 7455458 B2	26-03-2024
		JP 2019220182 A	26-12-2019
		TW 202006492 A	01-02-2020
		US 2019387588 A1	19-12-2019
		US 2021059028 A1	25-02-2021
US 6194967 B1	27-02-2001	NONE	
US 9961729 B1	01-05-2018	DE 102017204718 A1	27-09-2018
		US 9961729 B1	01-05-2018