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Chang et al.

(54) PIXEL STRUCTURE AND MANUFACTURING METHOD THEREOF BACKGROUND

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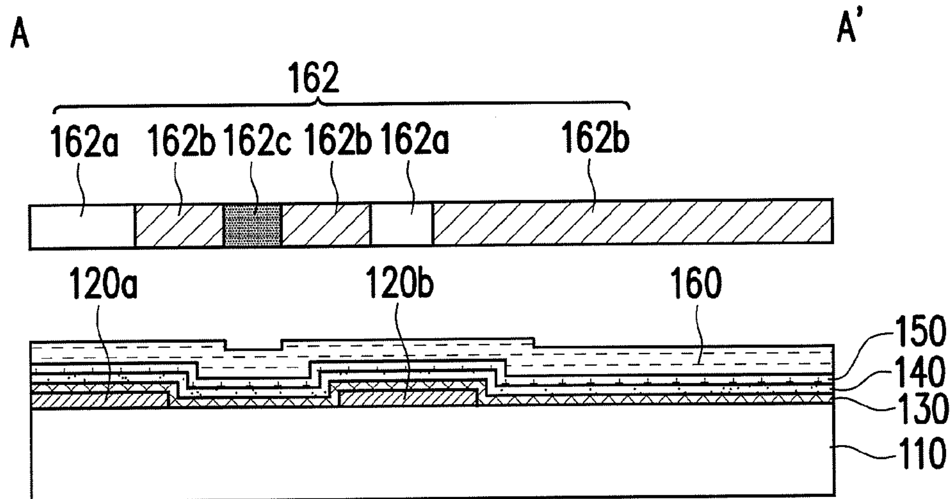
(57) **ABSTRACT**

A method for manufacturing a pixel structure is provided. A patterned semiconductor material layer, an insulation material layer, and a gate electrode material layer are formed in sequence on a substrate to form a stacked structure. A patterned photoresist layer is formed on the stacked structure by using a photomask. A portion of the stacked structure is removed to pattern the patterned semiconductor material layer into a patterned semiconductor layer by using the patterned photoresist layer as a mask. Another portion of the stacked structure is etched by using a portion of the patterned photoresist layer as a mask until a portion of the semiconductor layer in the stacked structure is exposed. Then, an exposed portion of the semiconductor layer is modified to increase a conductivity of the exposed portion of the semiconductor layer. Finally, the patterned photoresist layer is removed. A pixel structure manufactured by the method is provided.



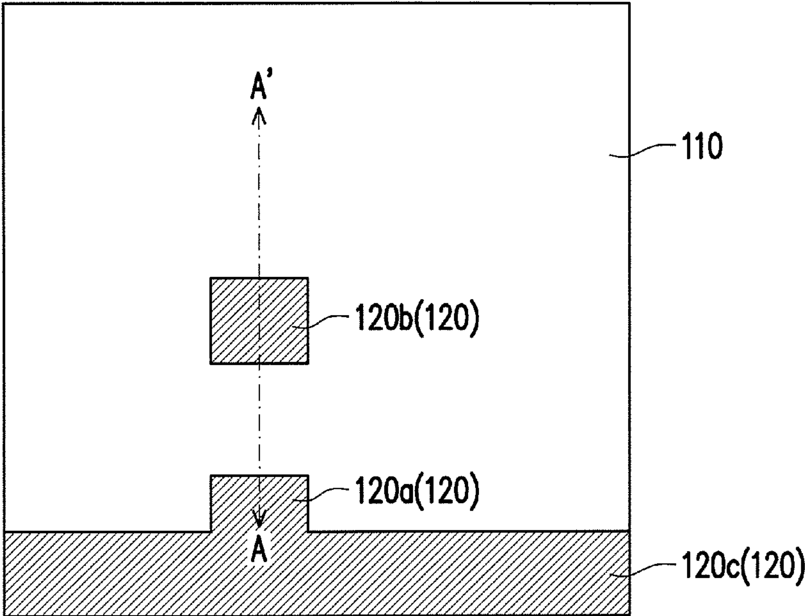


FIG. 1A

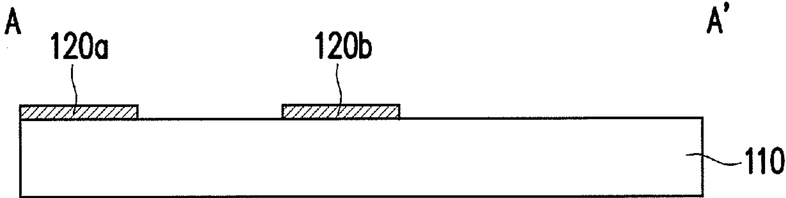


FIG. 1B

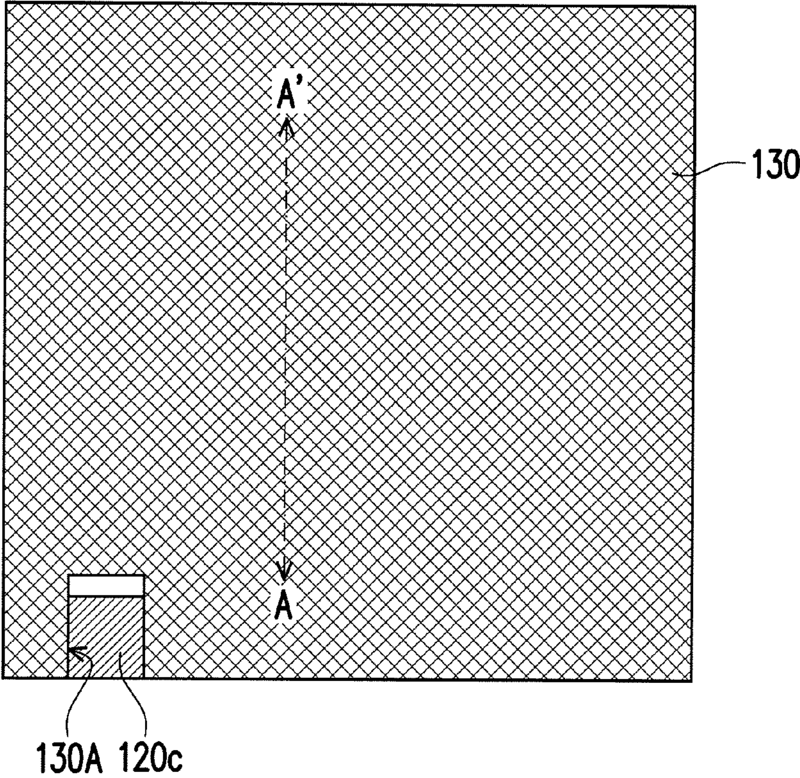


FIG. 2A

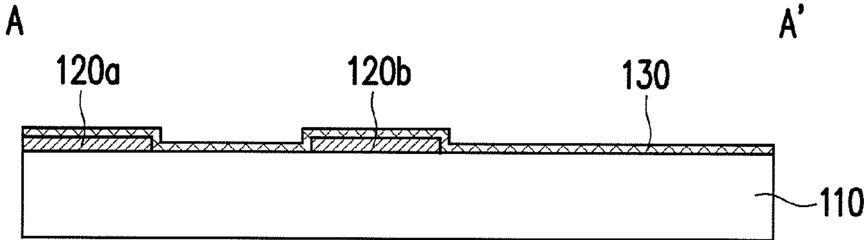


FIG. 2B

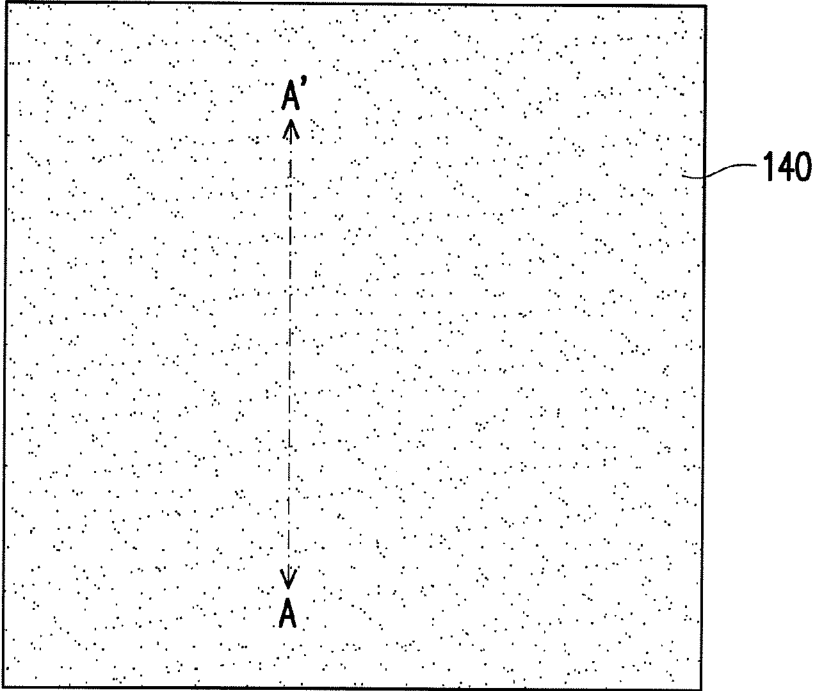


FIG. 3A

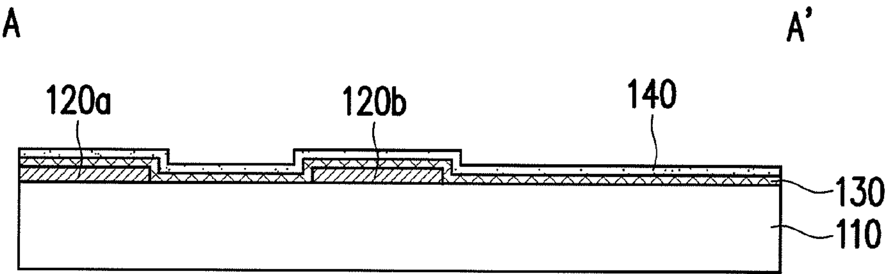


FIG. 3B

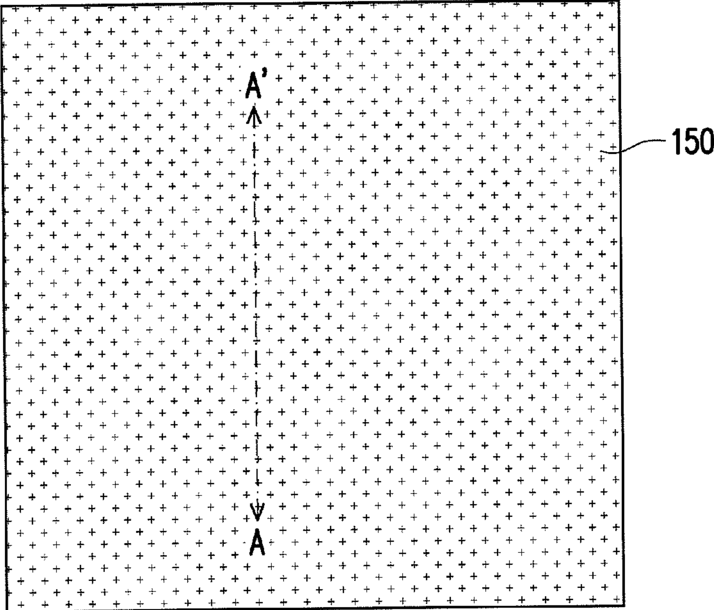


FIG. 4A

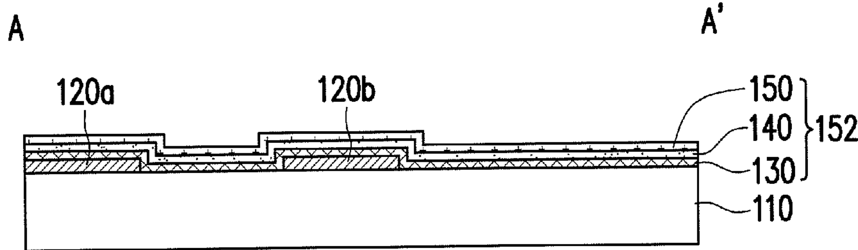


FIG. 4B

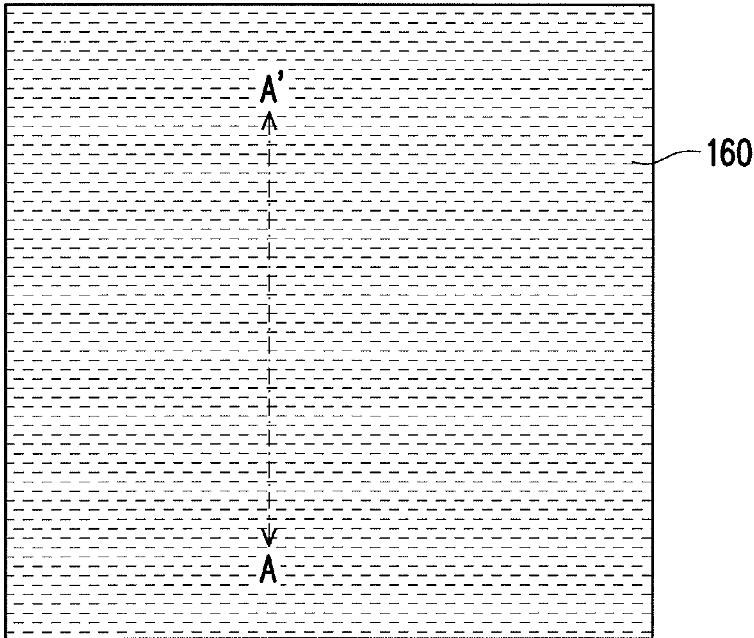


FIG. 5A

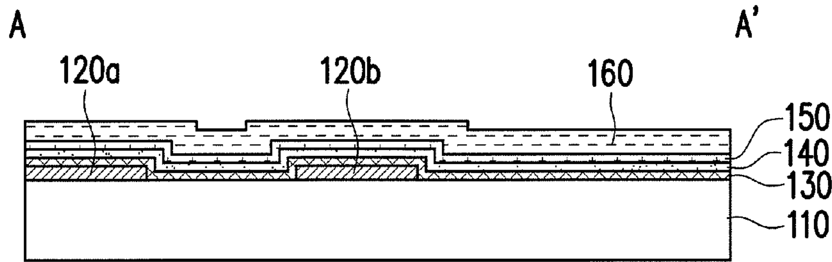


FIG. 5B

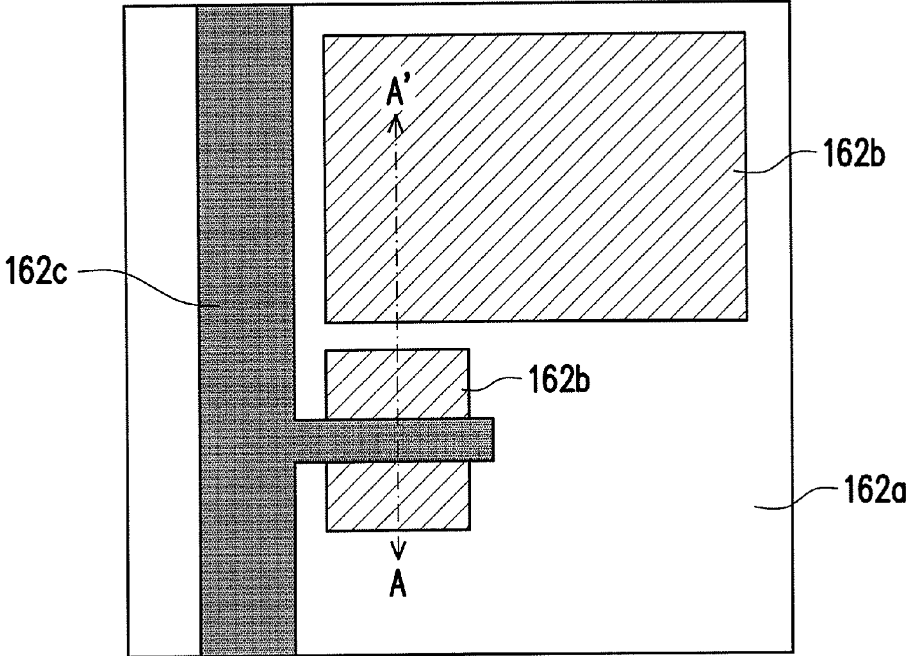


FIG. 6A

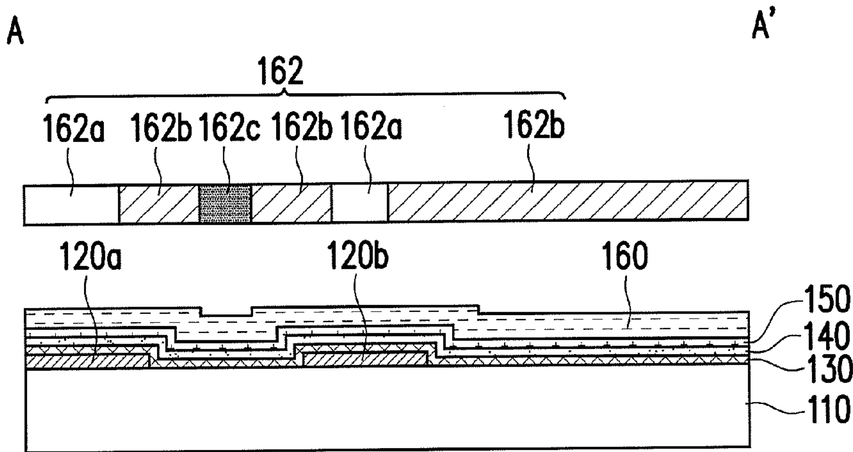


FIG. 6B

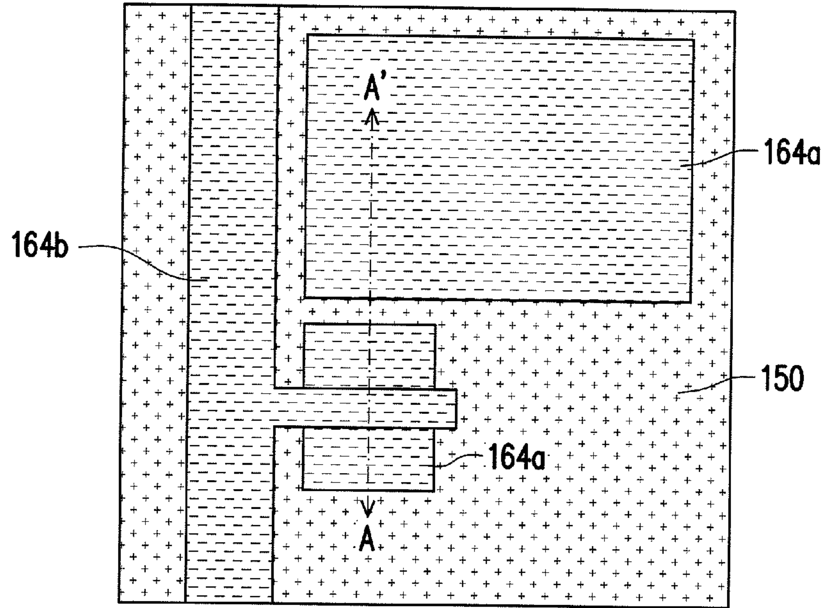


FIG. 7A

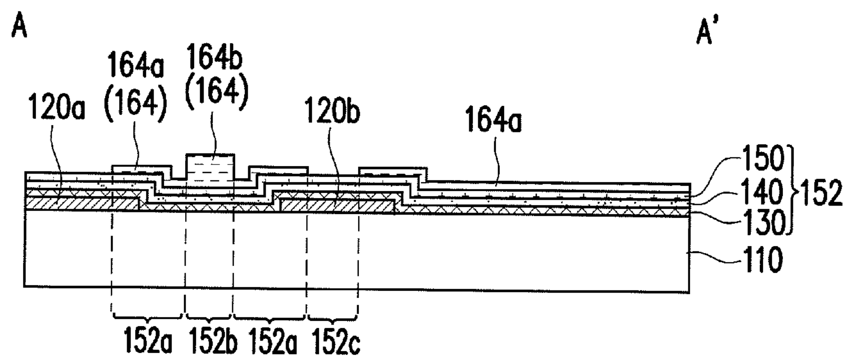


FIG. 7B

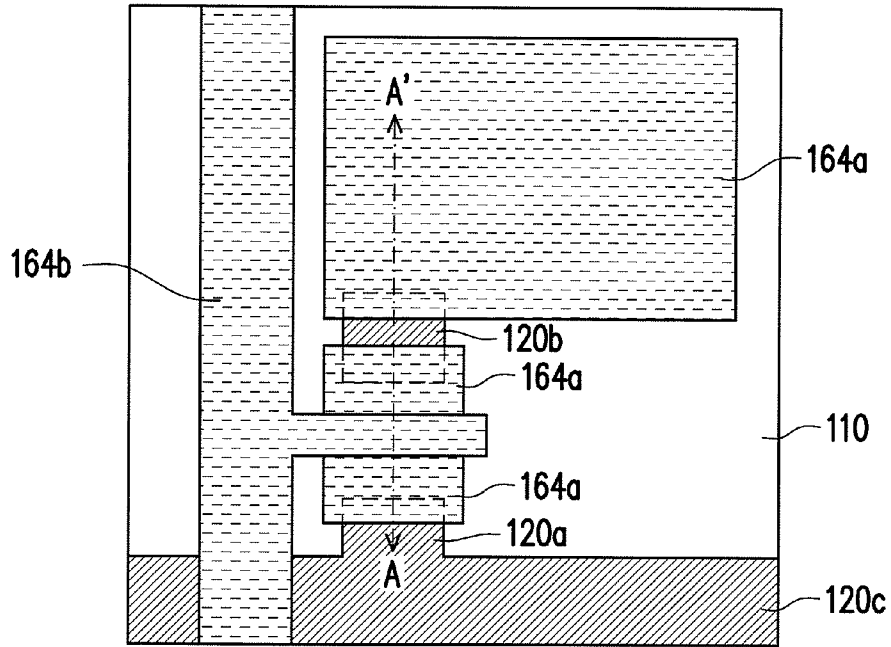


FIG. 8A

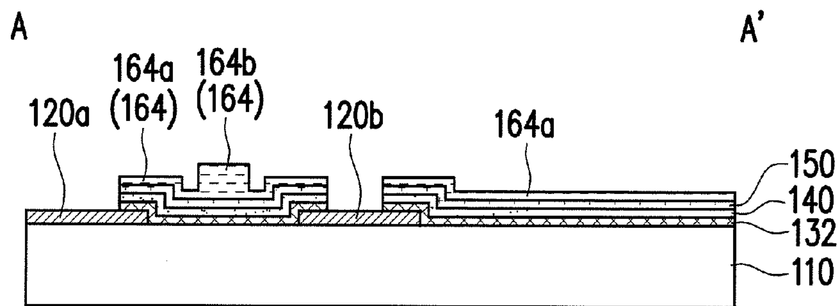


FIG. 8B

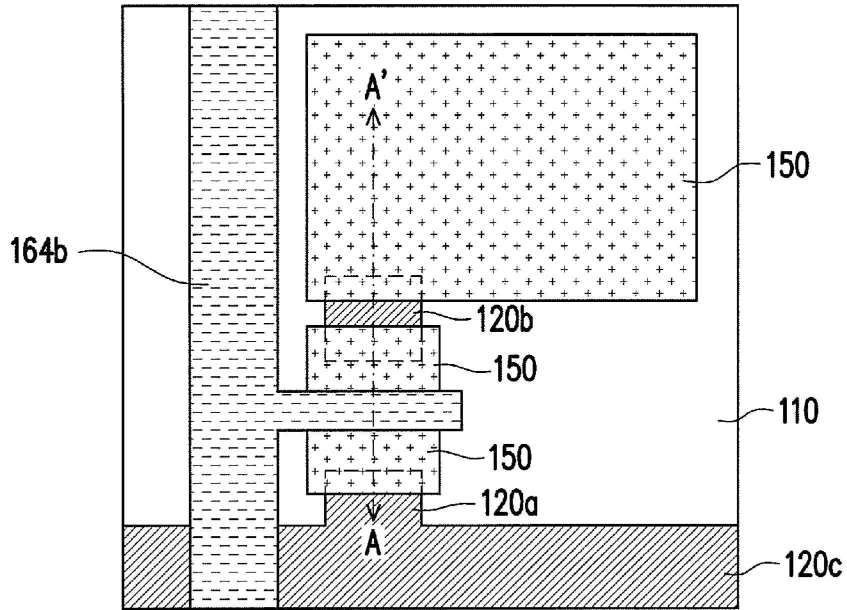


FIG. 9A

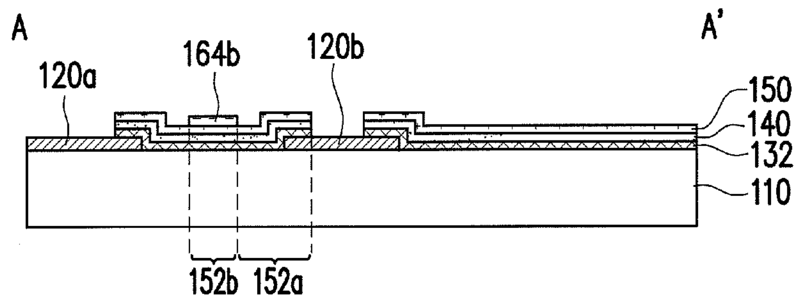


FIG. 9B

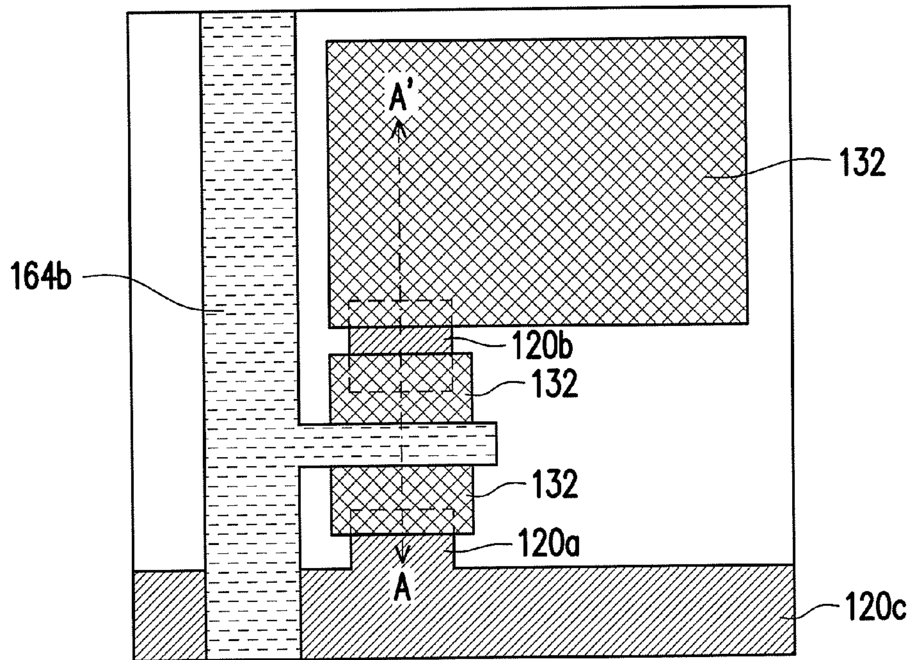


FIG. 10A

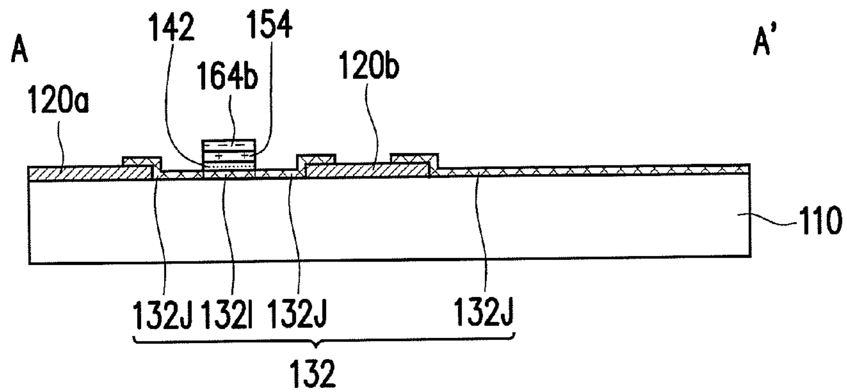


FIG. 10B

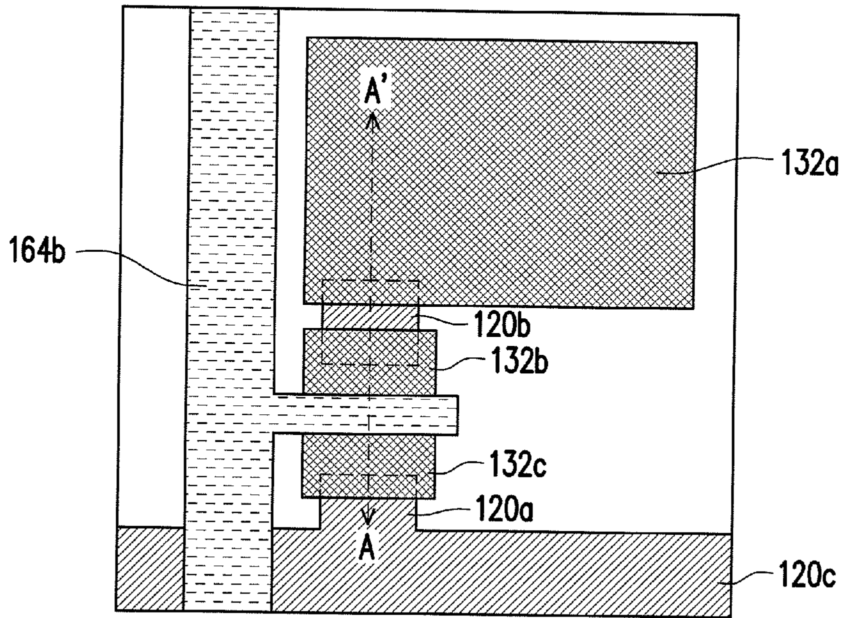


FIG. 11A

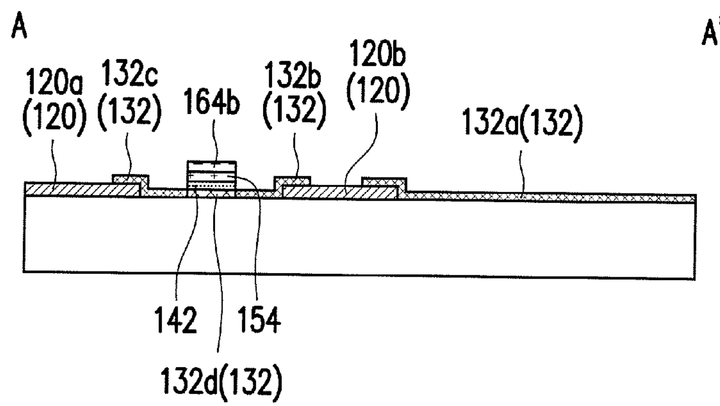


FIG. 11B

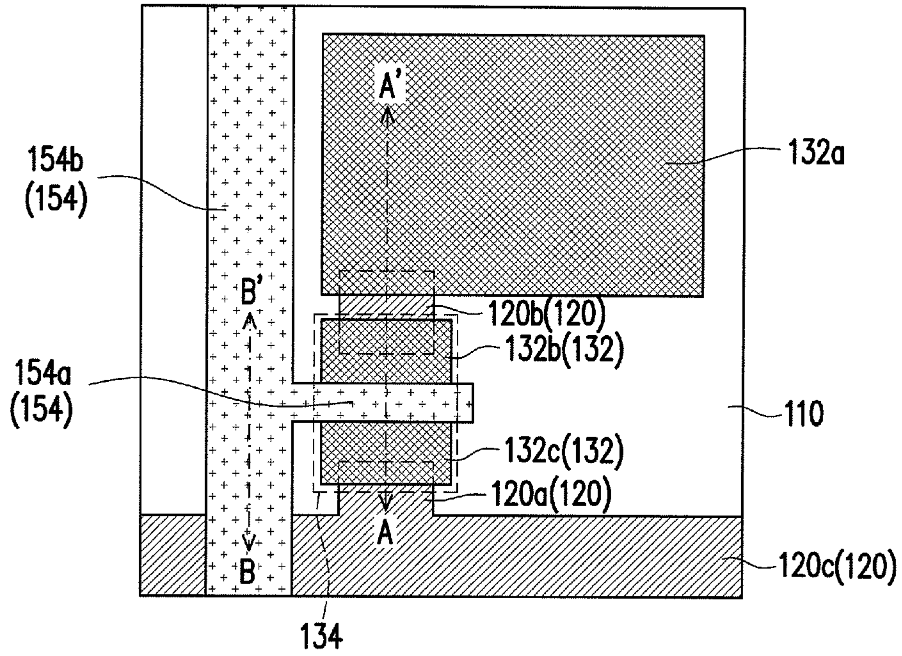


FIG. 12A

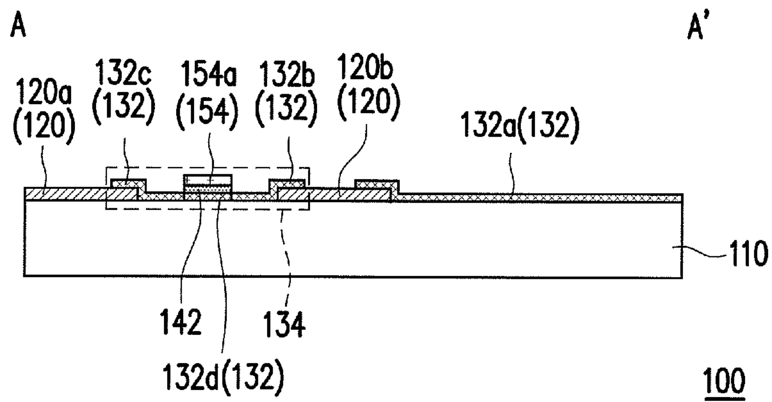


FIG. 12B

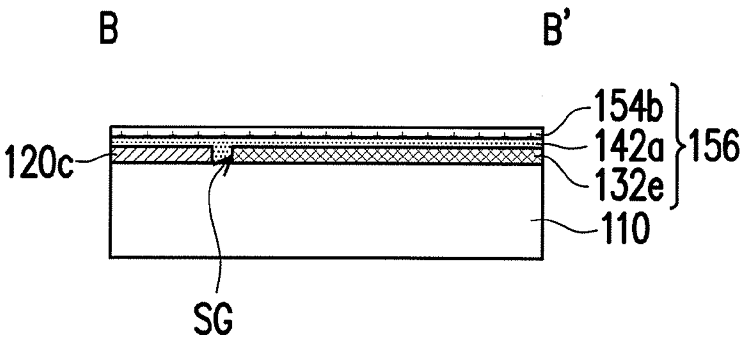


FIG. 12C

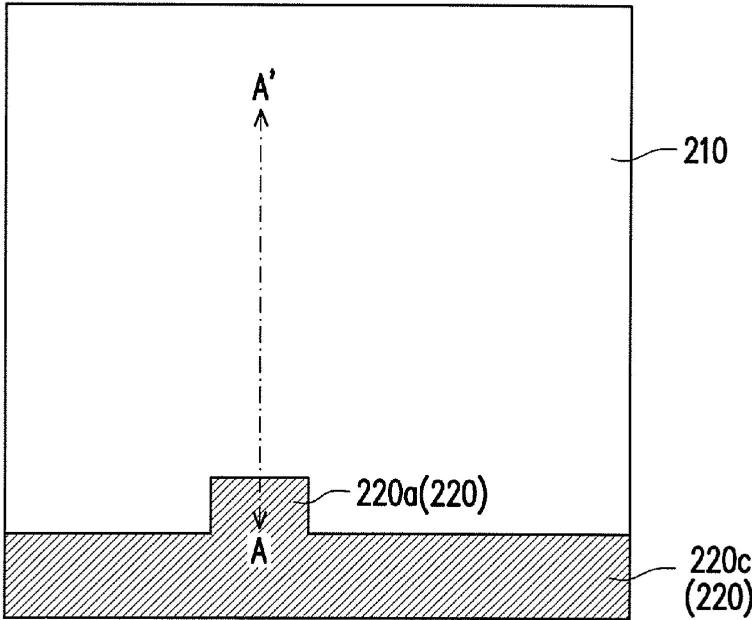


FIG. 13A

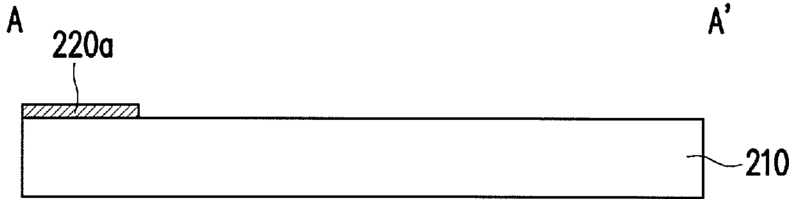


FIG. 13B

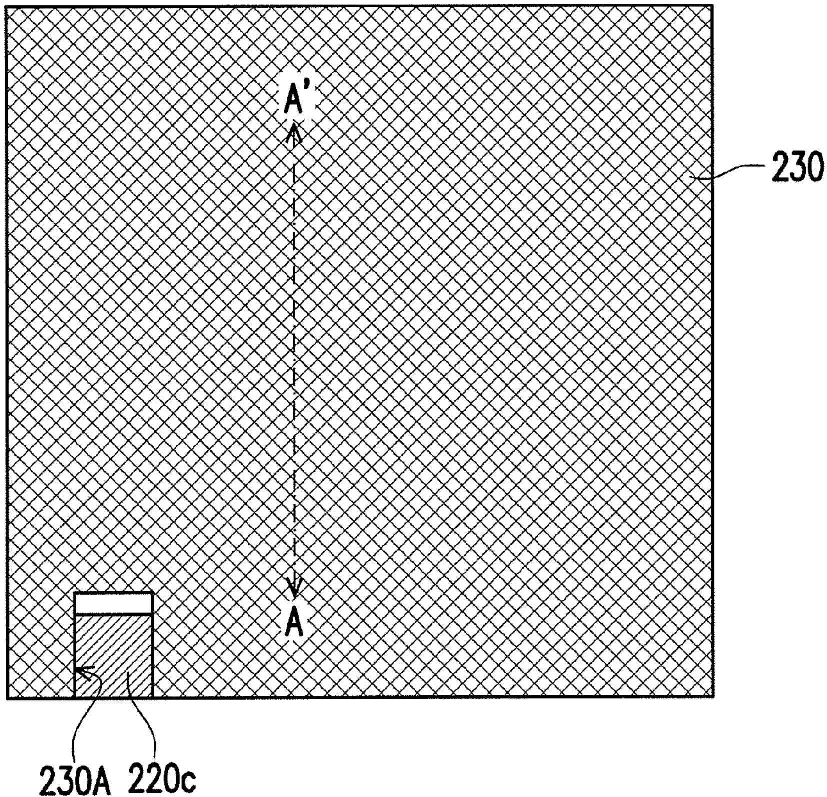


FIG. 14A

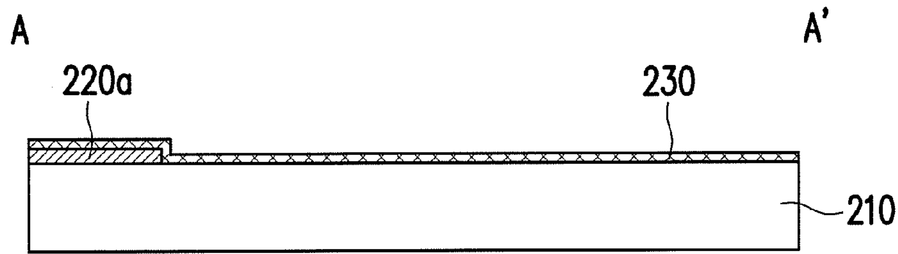


FIG. 14B

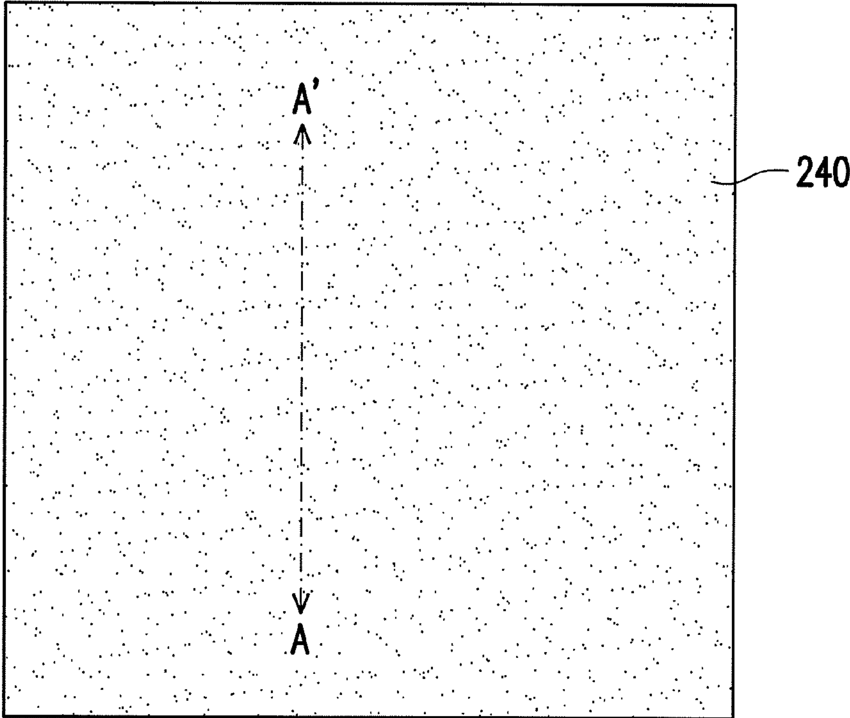


FIG. 15A

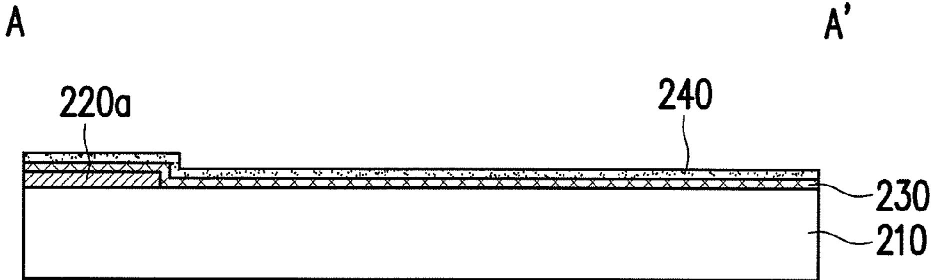


FIG. 15B

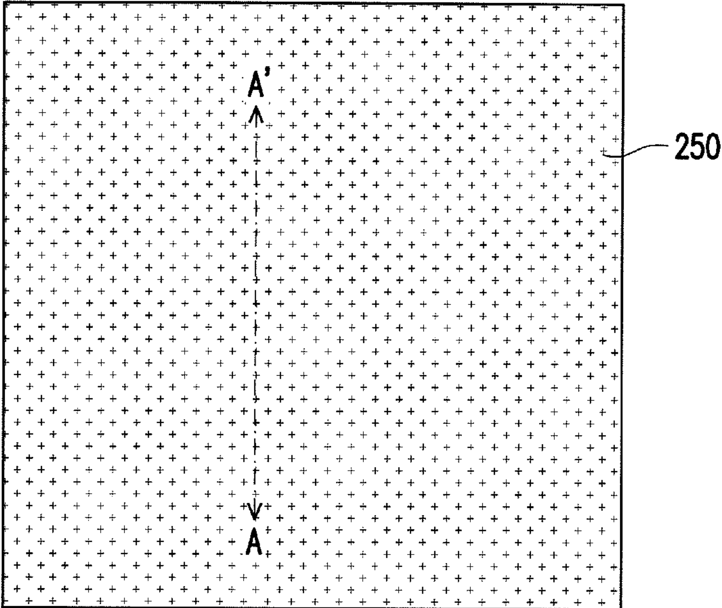


FIG. 16A

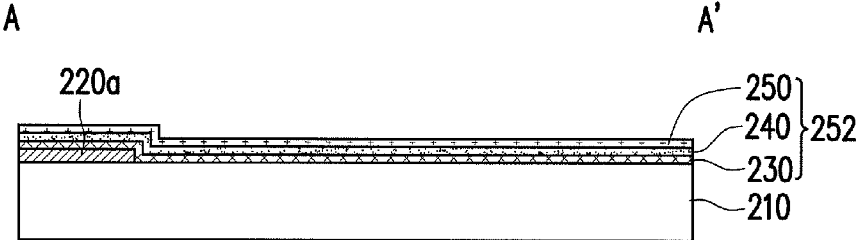


FIG. 16B

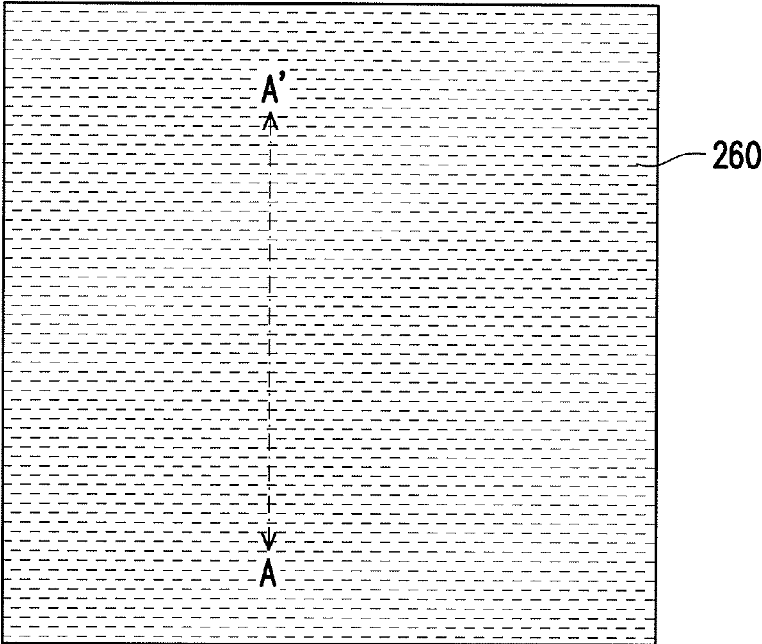


FIG. 17A

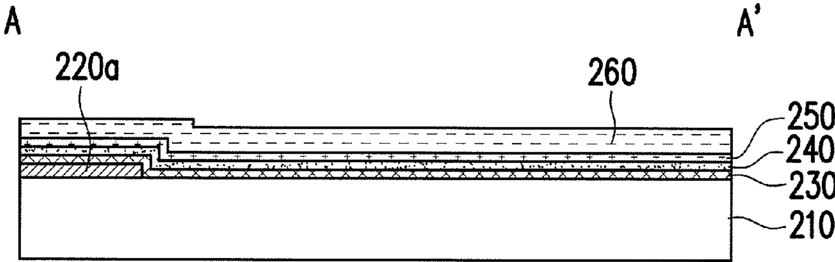


FIG. 17B

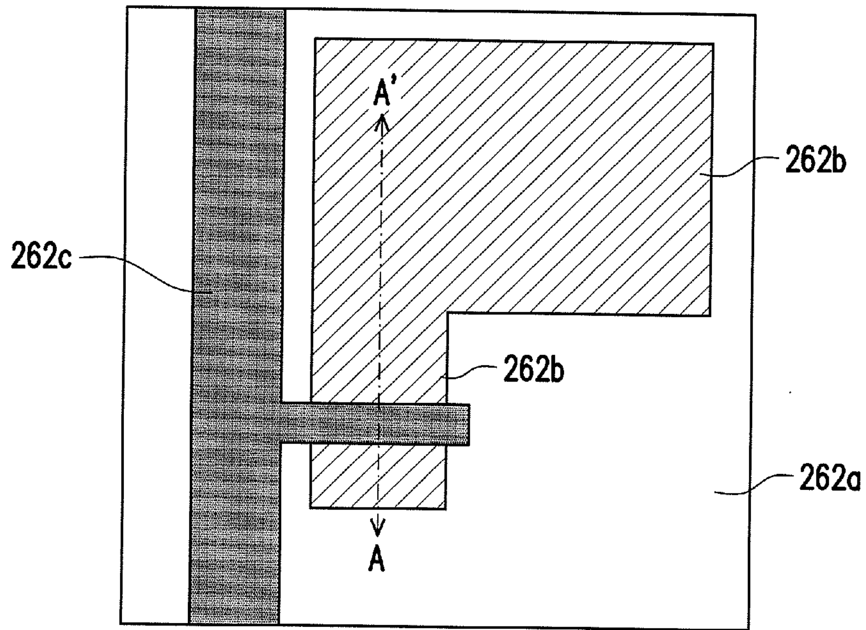


FIG. 18A

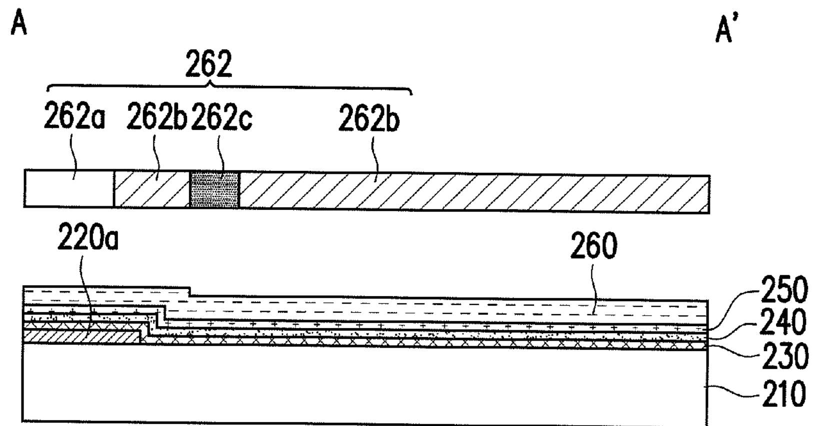


FIG. 18B

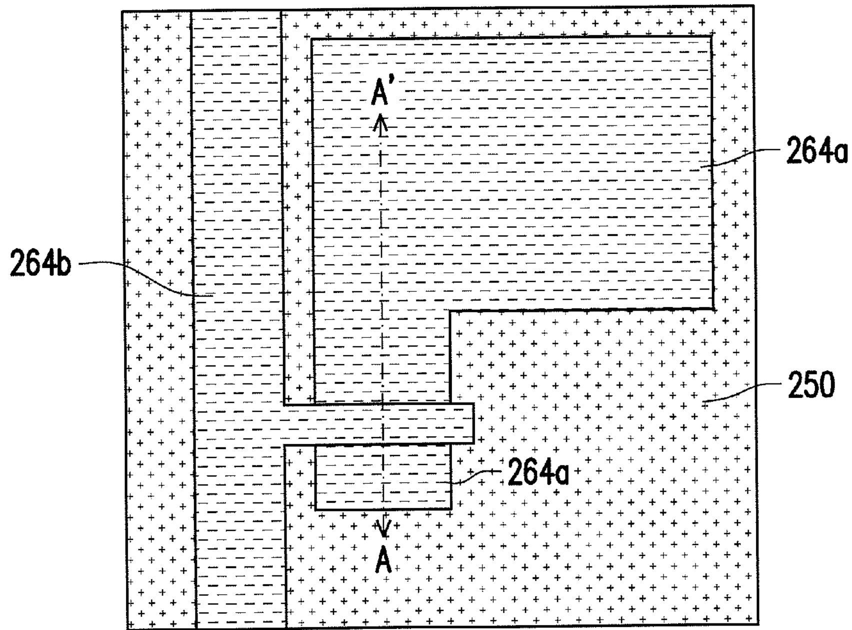


FIG. 19A

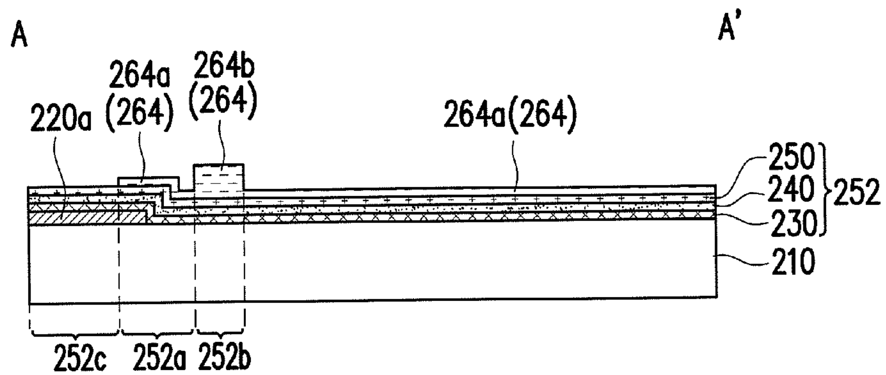


FIG. 19B

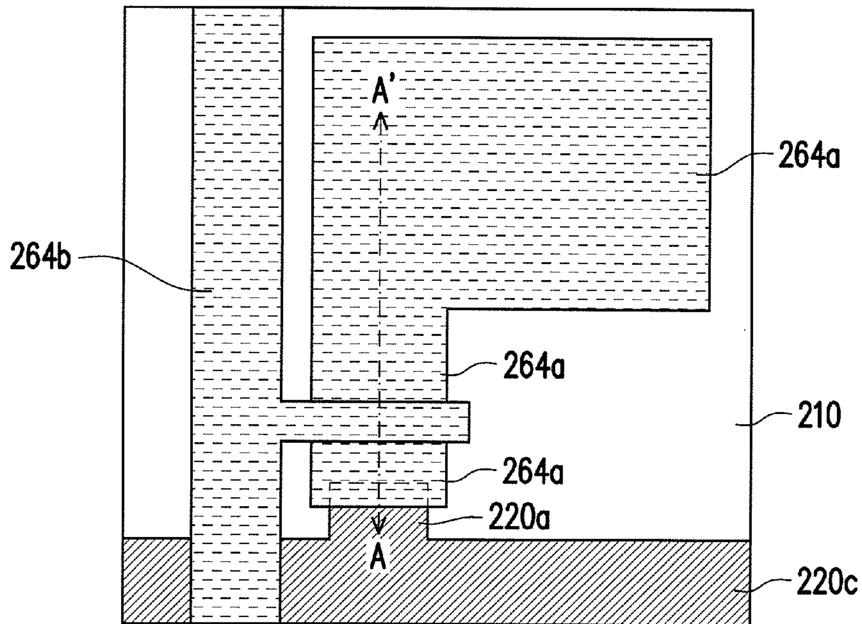


FIG. 20A

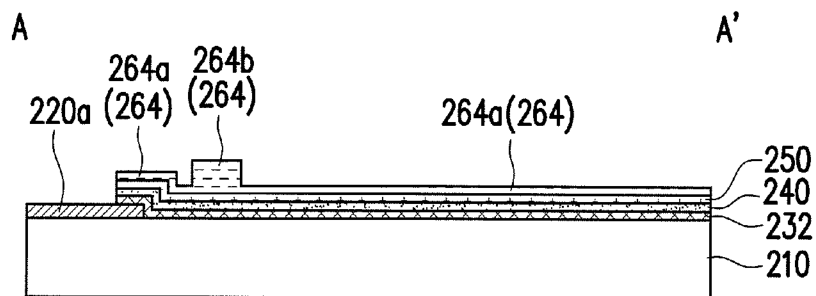


FIG. 20B

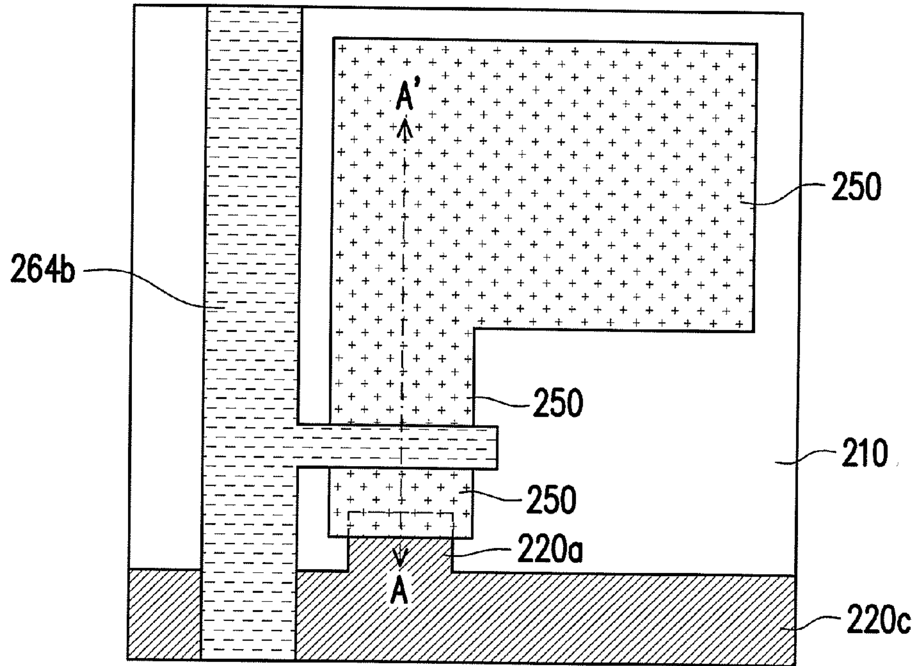


FIG. 21A

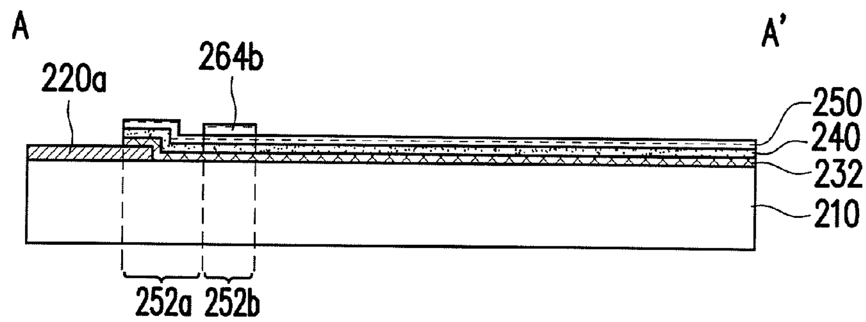


FIG. 21B

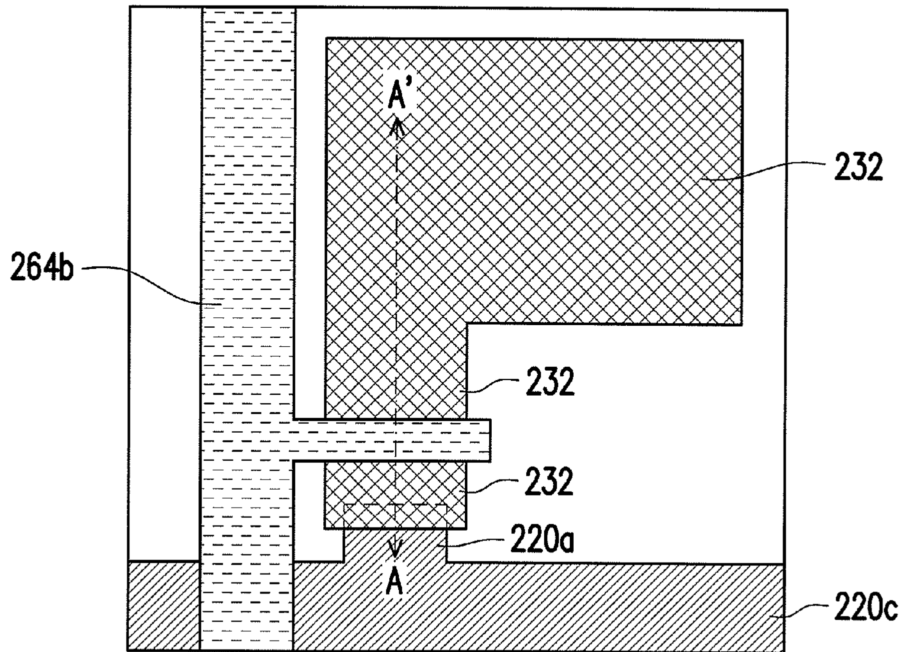


FIG. 22A

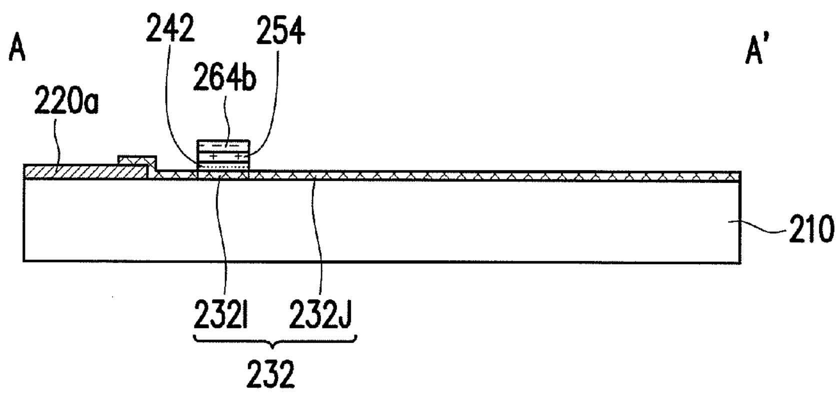


FIG. 22B

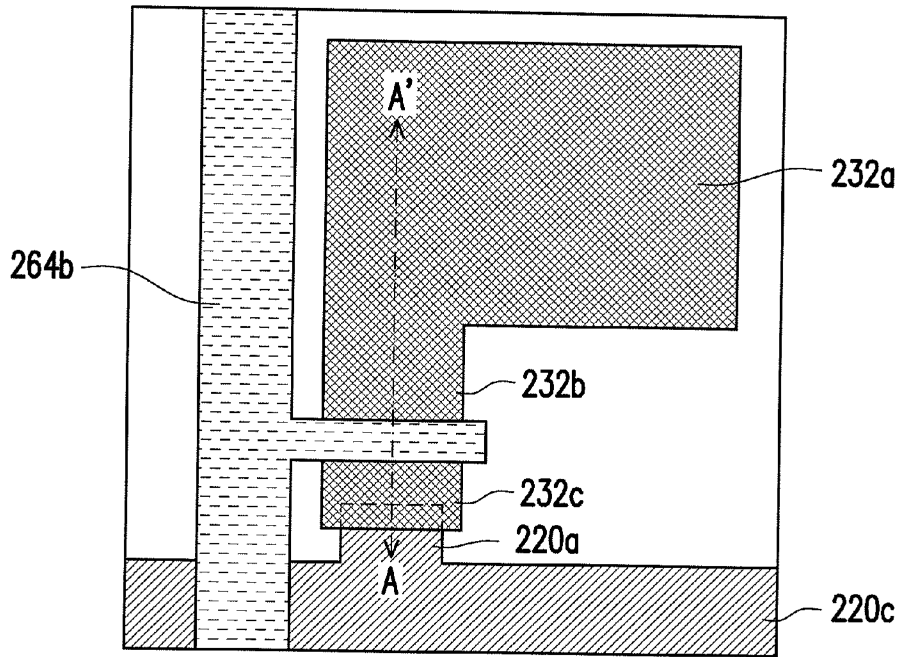


FIG. 23A

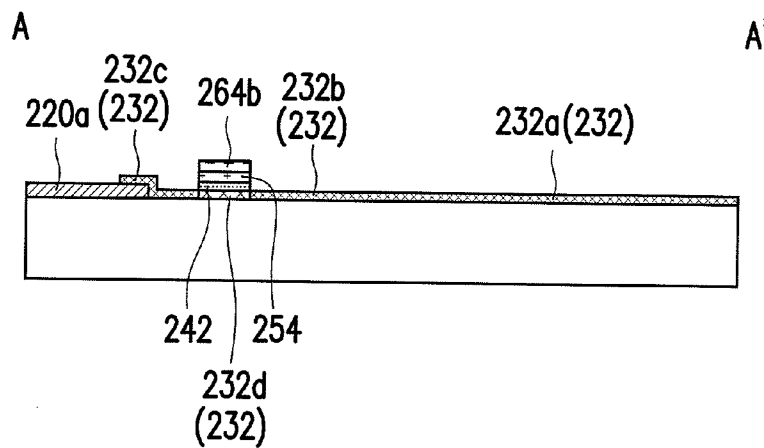


FIG. 23B

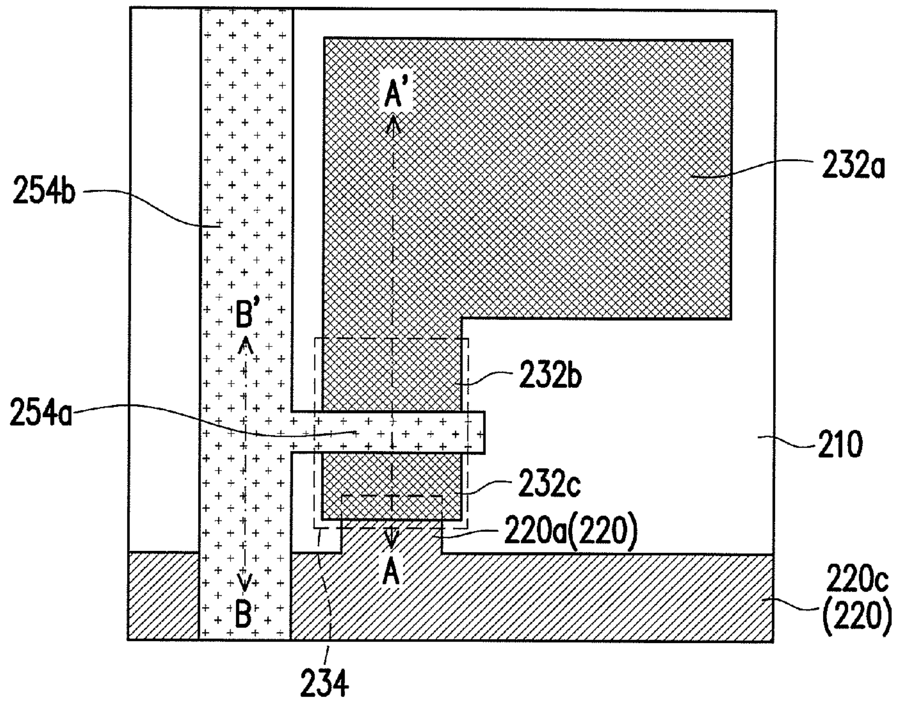


FIG. 24A

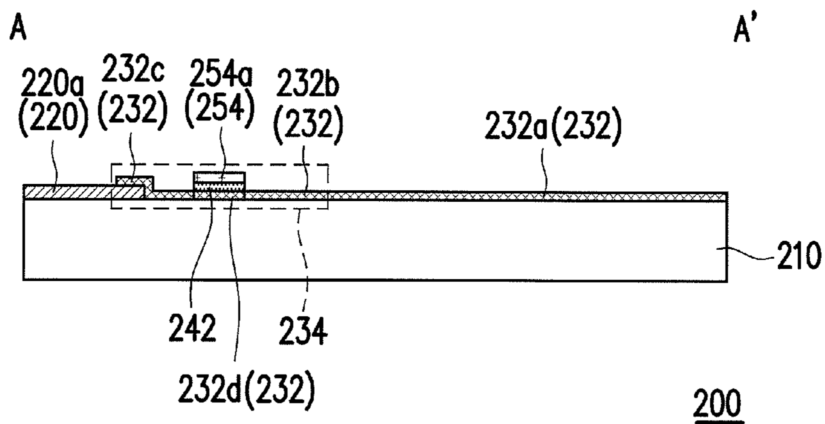


FIG. 24B

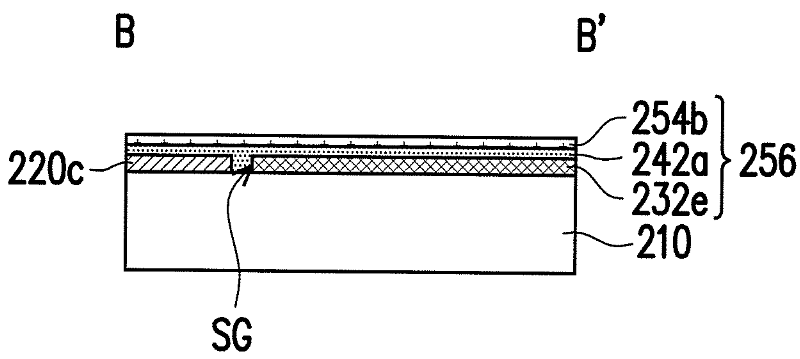


FIG. 24C

PIXEL STRUCTURE AND MANUFACTURING METHOD THEREOF BACKGROUND

BACKGROUND

[0001] Field of the Invention

[0002] The invention relates to a pixel structure and a manufacturing method thereof. In particular, the invention relates to a pixel structure with a patterned oxide semiconductor layer.

[0003] Description of Related Art

[0004] In general, the conventional manufacturing process of a pixel structure having an oxide semiconductor layer substantially involves six masking steps. With the first masking step, a gate electrode is formed on a substrate. Then, a gate insulating layer is comprehensively formed on the substrate for covering the gate electrode. Next, with the second masking step, an oxide semiconductor layer is formed on the gate insulating layer above the gate electrode. Furthermore, with the third masking step, an etching stop layer is formed on a portion of the oxide semiconductor layer. Afterward, a metal layer is formed on the etching stop layer; and with the fourth masking step, a source electrode and a drain electrode, which are electrically insulated with each other, are separately defined on two sides of the etching stop layer. Then, an insulating layer is formed on the substrate for covering the source electrode and the drain electrode. After that, with the fifth masking step, a contact window is formed on the insulating layer in order to expose the drain electrode. Finally, with the sixth masking step, a pixel electrode is formed on the substrate, and this pixel electrode fills up the contact window and is electrically connected with the drain electrode. At this point, the manufacturing of the pixel structure having the oxide semiconductor layer is completed. Nevertheless, the abovementioned manufacturing process of the pixel structure is complicated, and has high production costs.

SUMMARY OF THE INVENTION

[0005] The invention is to provide a pixel structure and a manufacturing method thereof, capable of reducing production costs and simplifying the manufacturing process by reducing the number of masks.

[0006] The invention provides a method of forming a pixel structure. The method includes the following steps. A patterned semiconductor material layer, an insulation material layer, and a gate electrode material layer are formed in sequence on a substrate to form a stacked structure. Next, a patterned photoresist layer is formed on the stacked structure by using a photomask. The patterned photoresist layer comprises a first thickness portion covering a first portion of the stacked structure and a second thickness portion covering a second portion of the stacked structure, and the patterned photoresist layer exposes a third portion of the stacked structure. The third portion of the stacked structure is removed to pattern the patterned semiconductor material layer into a patterned semiconductor layer by using the patterned photoresist layer as a mask. The first thickness portion of the patterned photoresist layer is then removed and the second thickness portion of the patterned photoresist layer is thinned to expose the first portion of the stacked structure previously covered by the first thickness portion of the patterned photoresist layer. Next, the first portion of the stacked structure is etched by using the thinned second thickness portion of the patterned photoresist layer as a mask until an exposed portion of the patterned semiconductor layer in the first portion of the stacked structure is exposed. The gate electrode material layer is patterned into a gate electrode layer, and the insulation material layer is patterned into an insulation layer having a shape substantially conformal to the gate electrode layer and covering a covered portion of the patterned semiconductor layer. Then, the exposed portion of the patterned semiconductor layer is modified to increase a conductivity of the exposed portion of the patterned semiconductor layer. The thinned second thickness portion of the patterned photoresist layer is then removed. The covered portion of the patterned semiconductor layer includes a channel, and the exposed portion of the patterned semiconductor layer includes a source and a drain. The gate electrode layer includes a gate above the channel, and the gate, the channel, the source and the drain form a thin film transistor structure.

[0007] In an embodiment of the invention, the method further includes forming a patterned metal layer on the substrate prior to forming the stacked structure. The patterned metal layer includes a data line electrically connected to the source.

[0008] In an embodiment of the invention, the patterned semiconductor material layer has an opening exposing a portion of the data line and the patterned semiconductor layer patterned from the patterned semiconductor material layer includes a semiconductor portion and has a separating gap corresponding to the opening, such that the insulation layer patterned from the insulation material layer has a insulation portion filling the separating gap and contacting the portion of the data line and the semiconductor portion is electrically insulating to the data line.

[0009] In an embodiment of the invention, removing the first thickness portion of the patterned photoresist layer and the thinning the second thickness portion of the patterned photoresist layer includes performing an ashing process.

[0010] In an embodiment of the invention, the forming the patterned photoresist layer on the stacked structure includes using one half-tone photomask or one gray-tone photomask to form the first thickness portion and the second thickness portion.

[0011] In an embodiment of the invention, modifying the exposed portion of the patterned semiconductor layer includes performing a plasma treatment, an ion implanting, or a combination thereof.

[0012] In an embodiment of the invention, a processing gas of the plasma treatment includes hydrogen gas.

[0013] In an embodiment of the invention, removing the second thickness portion includes performing a stripping process.

[0014] In an embodiment of the invention, the method further includes forming a pixel electrode electrically connected to the drain.

[0015] In an embodiment of the invention, the formation of the pixel electrode is simultaneous to the formation of the source and the drain.

[0016] In an embodiment of the invention, the pixel electrode is formed by modifying the exposed portion of the patterned semiconductor layer.

[0017] The invention further provides a pixel structure. The pixel structure includes a pixel electrode, disposed on a substrate, a thin film transistor structure, and an insulation

layer. The thin film transistor structure is disposed on the substrate and connected to the pixel electrode. The thin film transistor structure includes a source, a drain and a channel formed by a patterned semiconductor layer and a gate formed by a gate electrode layer. The source and the drain are located on two opposite sides of the channel, and the gate is located above the channel. The insulation layer is interposed between the patterned semiconductor layer and the gate electrode layer and has a shape substantially conformal to the gate electrode layer. The insulation layer covers an covered portion of the patterned semiconductor layer to form the channel and exposes an exposed portion of the patterned semiconductor layer to form the source and the drain.

[0018] In an embodiment of the invention, a material of the patterned semiconductor layer includes an oxide semiconductor material.

[0019] In an embodiment of the invention, the covered portion of the patterned semiconductor layer has a first conductivity type and the exposed portion of the patterned semiconductor layer has a second conductivity type more conductive than the first conductivity type.

[0020] In an embodiment of the invention, the exposed portion of the patterned semiconductor layer further includes the pixel electrode.

[0021] In an embodiment of the invention, the pixel structure further includes a data line disposed on the substrate, located between the patterned semiconductor layer and the substrate, and electrically connected to the source of the thin film transistor structure.

[0022] In an embodiment of the invention, the gate electrode layer further includes a gate line electrically connected to the gate of the thin film transistor structure. The insulation layer includes a insulation portion underlying the gate line. The patterned semiconductor layer further includes a semiconductor portion underlying the gate line, and the gate line, the insulation portion and the semiconductor portion form a gate line structure crossing over the data line.

[0023] In an embodiment of the invention, the patterned semiconductor layer has a separating gap exposing a portion of the data line, and the insulation portion fills the separating gap and contacts the portion of the data line. In addition, the semiconductor portion is electrically insulating to the data line.

[0024] In an embodiment of the invention, a portion of the source is in direct contact with the data line to electrically connect to the data line.

[0025] In an embodiment of the invention, the pixel structure further includes a patterned metal portion disposed on the substrate, located and electrically connected between the drain and the pixel electrode. A material of the patterned metal portion and the data line is the same.

[0026] Based on the above, in the manufacturing process of the pixel structure of the invention, the patterned photoresist layer is patterned to have a first thickness portion and a second thickness portion by using a photomask, and the following processes of forming the pixel structure use the patterned photoresist layer as a mask for forming multiple elements, such as the channel, the source, the drain, the gate and the gate insulation layer. Therefore, this allows the manufacture of the pixel structure of the invention to reduce the amount of photomasks required. Thus, the manufacturing cost of the pixel structure of the invention can be effectively lowered. Furthermore, in the pixel structure, the source and drain are electrically contacted with the channel without contact holes. In addition, the drain is electrically contacted with the pixel electrode without contact holes. The pixel structure according to the embodiment of the present invention has an improved resolution or aperture ratio. In addition, not requiring contact holes also saves space in the thin film transistor layout that utilizes the pixel structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0028] FIG. **1**A to FIG. **12**A are schematic top views illustrating the manufacture process of a pixel structure according to an embodiment of the invention.

[0029] FIG. **1**B to FIG. **12**B are schematic cross-sectional views respectively taken along line A-A' in the corresponding FIG. **1**A to FIG. **12**A.

[0030] FIG. **12**C is a schematic cross-sectional view taken along line B-B' in the corresponding FIG. **12**A.

[0031] FIG. **13**A to FIG. **24**A are schematic top views illustrating the manufacture process of a pixel structure according to another embodiment of the invention.

[0032] FIG. **13**B to FIG. **24**B are schematic cross-sectional views respectively taken along line A-A' in the corresponding FIG. **13**A to FIG. **24**A.

[0033] FIG. **24**C is a schematic cross-sectional view taken along line B-B' in the corresponding FIG. **24**A.

DESCRIPTION OF THE EMBODIMENTS

[0034] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0035] FIG. **1**A to FIG. **12**A are schematic top views illustrating the manufacture process of a pixel structure according to an embodiment of the invention. FIG. **1**B to FIG. **12**B are schematic cross-sectional views respectively taken along line A-A' in the corresponding FIG. **1**A to FIG. **12**A. It should be noted that in FIG. **1**A to FIG. **12**A, if a boundary of a layer substantially overlaps with another layer, the schematic top views only label the top most layer. Thus, FIG. **1**A to FIG. **12**A have omitted the references for some of the components. Please refer to the corresponding schematic cross-sectional views (i.e., FIG. **1**B to FIG. **12**B) at the same time. The following uses FIG. **1**A to FIG. **12**A and FIG. **1**B to FIG. **12**B to describe the manufacture process of the pixel structure of an embodiment of the invention.

[0036] Referring to FIG. **1**A and FIG. **1**B, a metal layer (not shown) is first formed on a substrate **110**. Next, the metal layer is patterned to form a patterned metal layer **120** on the substrate **110**. The patterned metal layer includes a first metal portion **120***a*, a second metal portion **120***b*, and a data line **120***c*. The first metal portion **120***a* branches off of the data line **120***c*. A material of the patterned metal layer **120** is, for example, molybdenum, aluminum, titanium, indium tin oxide, or a combination thereof. However, the invention is not limited thereto.

[0037] Referring to FIG. **2**A and FIG. **2**B, a patterned semiconductor material layer **130** is formed on the substrate **110**. Particularly, the patterned semiconductor material layer **130** has an opening **130**A exposing a portion of the data line **120***c*. A material of the patterned semiconductor material layer **130** is an oxide semiconductor material. For example, the material of the patterned semiconductor material layer **130** may be indium gallium zinc oxide, indium zinc oxide, indium gallium oxide, zinc oxide, tin oxide, gallium zinc oxide, zinc tin oxide, or indium tin oxide. However, the invention is not limited thereto. In addition, the opening **130**A can be formed by performing a lithography-etching process.

[0038] Referring to FIG. **3**A and FIG. **3**B, an insulation material layer **140** is formed on the patterned semiconductor material layer **130**. A material of the insulation material layer **140** is for example, silicon dioxide. However, the invention is not limited thereto.

[0039] Referring to FIG. **4**A and FIG. **4**B, a gate electrode material layer **150** is formed on the insulation material layer **140**. A material of the gate electrode material layer **150** is for example, molybdenum, aluminum, titanium, or a combination thereof. However, the invention is not limited thereto.

[0040] Thus, it can be seen that the patterned semiconductor material layer **130**, the insulation material layer **140**, and the gate electrode material layer **150** are formed in sequence on the substrate **110** to form a stacked structure **152**.

[0041] Referring to FIG. **5**A and FIG. **5**B, a photoresist layer **160** is formed on the gate electrode material layer **150** by using a photosensitive material.

[0042] Referring to FIG. **6**A and FIG. **6**B, a photomask **162** is used to pattern the photoresist layer **160**. The photomask **162** includes a first mask pattern **162***a*, a second mask pattern **162***b*, and a third mask pattern **162***c* with different transparencies. The transparency of the second mask pattern **162***b* is, for example, between the transparencies of the first mask pattern **162***a* and the third mask pattern **162***c*. In further detail, the first mask pattern **162***a* is, for example, completely transparent, the third mask pattern **162***c* is, for example, not transparent, and the second mask pattern **162***b* has a transparency between the first mask pattern **162***a* and the third mask pattern **162***c*. The photomask **162** may be a half-tone photomask or a gray-tone photomask. However, the invention is not limited thereto. Any suitable type of photomask to pattern the photoresist layer **160** can be utilized.

[0043] Referring to FIG. **7**A and FIG. **7**B, the photoresist layer **160** is patterned to form a patterned photoresist layer **164**. The patterned photoresist layer **164** includes a first thickness portion **164***a* and a second thickness portion **164***b*. The first thickness portion **164***a* corresponds to the second mask pattern **162***b* of the photomask **162** and covers a first portion **152***a* of the stacked structure **152**. The second thickness portion **164***b* corresponds to the third mask pattern **162***c* of the photomask **162** and covers a second portion **152***b* of the stacked structure **152**. A third portion **152***c* of the stacked structure **152** is exposed by the patterned photoresist layer **164**, wherein the third portion **152***c* of the stacked structure **152** corresponds to the first mask pattern **162***a* of the photomask **162**. In the present embodiment, owing to transparency difference of the second mask pattern **162***b* and the third mask pattern **162***c*, the second thickness portion **164***b* is thicker than the first thickness portion **164***a*.

[0044] Referring to FIG. **8**A and FIG. **8**B, the third portion **152***c* of the stacked structure **152** is removed to pattern the patterned semiconductor material layer **130** into a patterned semiconductor layer **132** by using the patterned photoresist layer **164** as a mask. The patterned semiconductor layer **132** has the same shape as the first thickness portion **164***a* and the second thickness portion **164***b* of the patterned photoresist layer **164**. The third portion **152***c* of the stacked structure **152** is removed by etching from the gate electrode material layer **150** until the patterned metal layer **120** is exposed. Thus, parts of the first metal portion **120***a*, the second metal portion **120***b*, and the data line **120***c* are exposed.

[0045] Referring to FIG. **9**A and FIG. **9**B, the first thickness portion **164***a* of the patterned photoresist layer **164** is then removed and the second thickness portion **164***b* of the patterned photoresist layer **164** is thinned to expose the first portion **152***a* of the stacked structure **152** previously covered by the first thickness portion **164***a* of the patterned photoresist layer **164**. In the embodiment, an ashing process is performed to remove the first thickness portion **164***a* of the patterned photoresist layer **164** and thin the second thickness portion **164***b* of the patterned photoresist layer **164**.

[0046] Referring to FIG. **10**A and FIG. **10**B, the first portion **152***a* of the stacked structure **152** is etched by using the thinned second thickness portion **164***b* of the patterned photoresist layer **164** as a mask until an exposed portion **132**J of the patterned semiconductor layer **132** in the first portion **152***a* of the stacked structure **152** is exposed. The gate electrode material layer **150** is patterned into a gate electrode layer **154**, and the insulation material layer **140** is patterned into an insulation layer **142** having a shape substantially conformal to the gate electrode layer **154** and covering a covered portion **1321** of the patterned semiconductor layer **132**.

[0047] Referring to FIG. **11**A and FIG. **11**B, the exposed portion **132**J of the patterned semiconductor layer **132** is then modified to increase a conductivity of the exposed portion **132**J of the patterned semiconductor layer **132**. The process for modifying the exposed portion **132**J of the patterned semiconductor layer **132** includes performing a plasma treatment, an ion implanting, or a combination thereof. Particularly, in the plasma treatment, a processing gas includes hydrogen gas. However, the invention is not limited thereto. Other suitable method of modifying the exposed portion **132**J of the patterned semiconductor layer **132** can be performed for increasing the conductivity of the exposed portion **132**J of the patterned semiconductor layer **132**.

[0048] By modifying the exposed portion **132**J of the patterned semiconductor layer **132** by the insulation layer **142** to increase conductivity, the modified portion of the patterned semiconductor layer **132** includes and forms a pixel electrode **132***a*, a drain **132***b*, and a source **132***c*. The pixel electrode **132***a* is electrically connected to the drain **132***b* through the second metal portion **120***b*. That is to say the pixel electrode **132***a* is electrically connected to the second metal portion **120***b*, and the second metal portion **120***b* is electrically connected to the drain **132***b*.

[0049] In the embodiment, the pixel electrode **132***a* is formed simultaneously with the formation of the source **132***c* and the drain **132***b* by using the same film layer. In addition, the covered portion **1321** of the patterned semi-

conductor layer **132**, that was covered by the insulation layer **142** and not modified to increase conductivity, forms is a channel **132***d*.

[0050] Referring to FIG. **12**A and FIG. **12**B, the thinned second thickness portion **164***b* of the patterned photoresist layer **164** is then removed. The process for removing the second thickness portion **164***b* includes performing a stripping process. However, the invention is not limited thereto. Other suitable method of removing the second thickness portion **164***b* can also be selected. After removing the second thickness portion **164***b*, the gate electrode layer **154** is exposed, and a pixel structure **100** of the embodiment is completely manufactured. In the present embodiment, the gate electrode layer **154** includes a gate **154***a* above the channel **132***d*, and a gate line **154***b* electrically connected to the gate **154***a*. The gate **154***a*, the channel **132***d*, the source **132***c* and the drain **132***b* form a thin film transistor structure **134**. Based on the method described above, it can be seen that the thin film transistor structure **134** is self-aligned during formation, wherein the channel **132***d* and the gate **154***a* are defined by using the thinned second thickness portion **164***b* of the patterned photoresist layer **164**. Thus, the thin film transistor structure **134** is a self-aligned thin film transistor structure. Particularly, in the present embodiment, the channel **132***d*, the source **132***c*, the drain **132***b* and the gate **154***a* are formed by using the same patterned photoresist layer **160** and the patterned photoresist layer **160** is formed by using one photomask. Therefore, the required amount of photomask for forming the thin film transistor structure **134** is reduced for saving the manufacture cost.

[0051] FIG. **12**C is a schematic cross-sectional view taken along line B-B' in the corresponding FIG. **12**A. Referring to FIG. **12**A, FIG. **12**B, and FIG. **12**C, the pixel structure **100** includes the pixel electrode **132***a* disposed on a substrate **110**, the thin film transistor structure **134**, and the insulation layer **142**. The thin film transistor structure **134** is disposed on the substrate **110** and connected to the pixel electrode **132***a*. The thin film transistor structure **134** includes the source **132***c*, the drain **132***b* and the channel **132***d* formed by the same patterned semiconductor layer **132** and the gate **154***a* formed by the gate electrode layer **154**. The source **132***c* and the drain **132***b* are located at two opposite sides of the channel **132***d*, and the gate **154***a* is located above the channel **132***d*. The insulation layer **142** is interposed between the patterned semiconductor layer **132** and the gate electrode layer **154** and has a shape substantially conformal to the gate electrode layer **154**. The insulation layer **142** covers a portion of the patterned semiconductor layer **132** to form the channel **132***d* and exposes another portion of the patterned semiconductor layer **132** to form the source **132***c* and the drain **132***b*.

[0052] According to the step depicted in FIG. **11**A and FIG. **11**B, the covered portion **1321** of the patterned semiconductor layer **132** has a first conductivity type and the exposed portion **132**J of the patterned semiconductor layer **132** has a second conductivity type more conductive than the first conductivity type. Therefore, the exposed portion **132**J of the patterned semiconductor layer **132** can form the source **132***c*, the drain **132***b* and the pixel electrode **132***a* which are the elements predetermined to be electrically conductive.

[0053] For transmitting the electric signals, the pixel structure **100** further includes the data line **120***c* disposed on the substrate **110**, and electrically connected to the source **132***c* of the thin film transistor structure **134**, wherein the first metal portion **120***a* of the data line **120***c* is located between the semiconductor layer **132** and the substrate **110**. In addition, the gate electrode layer **154** further includes the gate line **154***b* electrically connected to the gate **154***a* of the thin film transistor structure **134**. The gate line **154***b* and the data line **120***c* extends in different directions for respectively transmitting a control signal to the gate **154***a* and transmitting a data signal to the source **132***c*. Therefore, the thin film transistor structure **134** can be turned on by the control signal and the data signal can be transmitted to the pixel electrode **132***a* through the turned-on thin film transistor structure **134**.

[0054] In the present embodiment, the gate line **154***b* is formed by using the same method of forming the gate **154***a*. Therefore, the insulation layer **142** includes an insulation portion **142***a* underlying the gate line **154***b*. The insulation portion **142***a* conforms in shape to the gate line **154***b*. The patterned semiconductor layer **132** further includes a semiconductor portion **132***e* underlying the gate line **154***b* and has a separating gap SG corresponding to the opening **130**A shown in FIG. **2**A and exposing a portion of the data line **120***c*. The semiconductor portion **132***e* partially conforms in shape to the gate line **154***b*. The gate line **154***b*, the insulation portion **142***a* and the semiconductor portion **132***e* form a gate line structure **156**, where the gate line **154***b* and the insulation portion **142***a* of the gate line structure **156** cross over the data line **120***c* at the separating gap SG such that the semiconductor portion **132***e* is not in contact with the data line **120***c* and the insulation portion **142***a* of the insulation layer **142** fills in the separating gap SG and contacts the data line **120***c* for isolating the data line **120***c* from the gate line **154***b*. In other words, the semiconductor portion **132***e* of the gate line structure **156** is electrically insulating to the data line **120***c* so that a short circuit would not generate between the semiconductor portion **132***e* and the data line **120***c*.

[0055] In the embodiment, a portion of the source **132***c* is in direct contact with the data line **120***c* by being in direct contact with the first metal portion **120***a* that branches off of the data line **120***c*, to electrically connect to the data line **120***c*. In addition, the pixel structure **100** further includes the second metal portion **120***b* disposed on the substrate **110**, located and electrically connected between the drain **132***b* and the pixel electrode **132***a*. A material of the second metal portion **120***b* and the data line **120***c* is the same. However, in an alternative embodiment, the first metal portion **120***a* and the second metal portion **120***b* can be selectively omitted.

[0056] FIG. **13**A to FIG. **24**A are schematic top views illustrating the manufacture process of a pixel structure according to another embodiment of the invention. FIG. **13**B to FIG. **24**B are schematic cross-sectional views respectively taken along line A-A' in the corresponding FIG. **13**A to FIG. **24**A. It should be noted that in FIG. **13**A to FIG. **24**A, if a boundary of a layer substantially overlaps with another layer, the schematic top views only label the top most layer. Thus, FIG. **13**A to FIG. **24**A have omitted the references for some of the components. Please refer to the corresponding schematic cross-sectional views (i.e., FIG. **13**B to FIG. **24**B) at the same time. The following uses FIG. **13**A to FIG. **24**A and FIG. **13**B to FIG. **24**B to describe the manufacturing process of the pixel structure of another embodiment of the invention.

[0057] The difference between the embodiment of FIG. **13**A to FIG. **24**A, FIG. **13**B to FIG. **24**B, and FIG. **24**C and the embodiment of FIG. **1**A to FIG. **12**A, FIG. **1**B to FIG. **12**B, and FIG. **12**C, is that the second metal portion **120***b* is not included in the embodiment of FIG. **13**A to FIG. **24**A, FIG. **13**B to FIG. **24**B, and FIG. **24**C. Similar elements will use the same names, and processes that are the same both embodiments will not be repeated herein. The materials used are also similar in both embodiments, and the description will not be repeated herein.

[0058] Referring to FIG. **13**A and FIG. **13**B, a metal layer (not shown) is first formed on a substrate **210**. Next, the metal layer is patterned to form a patterned metal layer **220** on the substrate **210**. The patterned metal layer includes a first metal portion **220***a* and a data line **220***c*. The first metal portion **220***a* branches off of the data line **220***c*.

[0059] Referring to FIG. **14**A and FIG. **14**B, a patterned semiconductor material layer **230** is formed on the substrate **210**. Particularly, the patterned semiconductor material layer **230** has an opening **230**A exposing a portion of the data line **220***c*. Referring to FIG. **15**A and FIG. **15**B, an insulation material layer **240** is formed on the patterned semiconductor material layer **230**. Referring to FIG. **16**A and FIG. **16**B, a gate electrode material layer **250** is formed on the insulation material layer **240**. Thus, it can be seen that the patterned semiconductor material layer **230**, the insulation material layer **240**, and the gate electrode material layer **250** are formed in sequence on the substrate **210** to form a stacked structure **252**.

[0060] Referring to FIG. **17**A and FIG. **17**B, a photoresist layer **260** is formed on the gate electrode material layer **250** by using a photosensitive material. Referring to FIG. **18**A and FIG. **18**B, a photomask **262** is used to pattern the photoresist layer **260**. The photomask **262** includes a first mask pattern **262***a*, a second mask pattern **262***b*, and a third mask pattern **262***c* with different transparencies. The description of the photomask **262** is similar to the photomask **162**, and will not be repeated herein.

[0061] Referring to FIG. **19**A and FIG. **19**B, the photoresist layer **260** is patterned to form a patterned photoresist layer **264**. The patterned photoresist layer **264** includes a first thickness portion **264***a* and a second thickness portion **264***b*. The first thickness portion **264***a* corresponds to the second mask pattern **262***b* of the photomask **262** and covers a first portion **252***a* of the stacked structure **252**. The second thickness portion **264***b* corresponds to the third mask pattern **262***c* of the photomask **262** and covers a second portion **252***b* of the stacked structure **252**. A third portion **252***c* of the stacked structure **252** is exposed by the patterned photoresist layer **264**. The third portion **252***c* of the stacked structure **252** that is exposed by the patterned photoresist layer **264** corresponds to the first mask pattern **262***a* of the photomask **262**. In the present embodiment, owing to transparency difference of the second mask pattern **262***b* and the third mask pattern **262***c*, the second thickness portion **264***b* is thicker than the first thickness portion **264***a*.

[0062] Referring to FIG. **20**A and FIG. **20**B, the third portion **252***c* of the stacked structure **252** is removed to pattern the patterned semiconductor material layer **230** into a patterned semiconductor layer **232** by using the patterned photoresist layer **264** as a mask. The patterned semiconductor layer **232** has the same shape as the first thickness portion **264***a* and the second thickness portion **264***b* of the patterned photoresist layer **264** in the top view as shown in FIG. **20**A. The third portion **252***c* of the stacked structure **252** is removed by etching from the gate electrode material layer **250** until the patterned metal layer **220** is exposed. Thus, parts of the first metal portion **220***a* and the data line **220***c* are exposed.

[0063] Referring to FIG. **21**A and FIG. **21**B, the first thickness portion **264***a* of the patterned photoresist layer **264** is then removed and the second thickness portion **264***b* of the patterned photoresist layer **264** is thinned to expose the first portion **252***a* of the stacked structure **252** previously covered by the first thickness portion **264***a* of the patterned photoresist layer **264**. In the embodiment, an ashing process is performed to remove the first thickness portion **264***a* of the patterned photoresist layer **264** and thin of the second thickness portion **264***b* of the patterned photoresist layer **264**.

[0064] Referring to FIG. **22**A and FIG. **22**B, the first portion **252***a* of the stacked structure **252** is etched by using the thinned second thickness portion **264***b* of the patterned photoresist layer **264** as a mask until an exposed portion **232**J of the patterned semiconductor layer **232** in the first portion **252***a* of the stacked structure **252** is exposed. The gate electrode material layer **250** is patterned into a gate electrode layer **254**, and the insulation material layer **240** is patterned into an insulation layer **242** having a shape substantially conformal to the gate electrode layer **254** and covering a covered portion **2321** of the patterned semiconductor layer **232**.

[0065] Referring to FIG. **23**A and FIG. **23**B, the exposed portion **232**J of the patterned semiconductor layer **232** is then modified to increase a conductivity of the exposed portion **232**J of the patterned semiconductor layer **232**. This step is similar to the description of the step in FIG. **11**A and FIG. **11**B, and will not be repeated herein.

[0066] By modifying the exposed portion **232**J of the patterned semiconductor layer **232** exposed by the insulation layer **242** to increase conductivity, the modified exposed portion **232**J of the patterned semiconductor layer **232** includes and forms a pixel electrode **232***a*, a drain **232***b*, and a source **232***c*. The pixel electrode **232***a* is electrically connected to the drain **232***b*. In the embodiment, there is no a metal portion to electrically connect the pixel electrode **232***a* and the drain **232***b*. Rather, the pixel electrode **232***a* and the drain **232***b* are of the same patterned semiconductor layer **232**, and branch off of each other to be in direct contact and electrically connected.

[0067] In the embodiment, the pixel electrode **232***a* is formed simultaneously with the formation of the source **232***c* and the drain **232***b* by using the same film layer. In addition, the covered portion **2321** of the patterned semiconductor layer **232** covered by the insulation layer **242** that was not modified to increase conductivity forms a channel **232***d*. Accordingly, in the present embodiment, the pixel electrode **232***a*, the source **232***c*, the drain **232***b* and the channel **232***d* can be formed by using the same film layer, the patterned semiconductor material layer **230**.

[0068] Referring to FIG. **24**A and FIG. **24**B, the thinned second thickness portion **264***b* of the patterned photoresist layer **264** is then removed. The process for removing the second thickness portion **264***b* includes performing a stripping process. However, the invention is not limited thereto. Any suitable method of removing the second thickness portion **264***b* can be used. After removing the second thickness portion **264***b*, the gate electrode layer **254** is exposed,

and a pixel structure **200** of the embodiment is completely manufactured. In the present embodiment, the gate electrode layer **254** includes a gate **254***a* above the channel **232***d*, and a gate line **254***b* electrically connected to the gate **254***a*. The gate **254***a*, the channel **232***d*, the source **232***c* and the drain **232***b* form a thin film transistor structure **234**. Based on the method described above, it can be seen that the thin film transistor structure **234** is self-aligned during formation, wherein the channel **232***d* and the gate **254***a* are defined by using the thinned second thickness portion **264***b* of the patterned photoresist layer **264**. Thus, the thin film transistor structure **234** is a self-aligned thin film transistor structure. Particularly, in the present embodiment, the channel **232***d*, the source **232***c*, the drain **232***b* and the gate **254***a* are formed by using the same patterned photoresist layer **260** and the patterned photoresist layer **260** is formed by using one photomask. Therefore, the required amount of photomask for forming the thin film transistor structure **234** is reduced for saving the manufacture cost.

[0069] FIG. **24**C is a schematic cross-sectional view taken along line B-B' in the corresponding FIG. **24**A. Referring to FIG. **24**A, FIG. **24**B, and FIG. **24**C, the pixel structure **200** includes the pixel electrode **232***a* disposed on the substrate **210**, the thin film transistor structure **234**, and the insulation layer **242**. The thin film transistor structure **234** is disposed on the substrate **210** and connected to the pixel electrode **232***a*. The thin film transistor structure **234** includes the source **232***c*, the drain **232***b* and the channel **232***d* formed by a patterned semiconductor layer **232** and a gate **254***a* formed by a gate electrode layer **254**. The source **232***c* and the drain **232***b* are located on two opposite sides of the channel **232***d*, and the gate **254***a* is located above the channel **232***d*. The insulation layer **242** is interposed between the patterned semiconductor layer **232** and the gate electrode layer **254** and has a shape substantially conformal to the gate electrode layer **254**. The insulation layer **242** covers a portion of the patterned semiconductor layer **232** to form the channel **232***d* and exposes another portion of the patterned semiconductor layer **232** to form the source **232***c* and the drain **232***b*.

[0070] According to the step depicted in FIG. **23**A and FIG. **23**B, the covered portion **2321** of the patterned semiconductor layer **232** has a first conductivity type and the exposed portion **232**J of the patterned semiconductor layer **232** has a second conductivity type more conductive than the first conductivity type. Therefore, the exposed portion **232**J of the patterned semiconductor layer **232** can from the source **232***c*, the drain **232***b*, and the pixel electrode **232***a* which are elements predetermined to be electrically conductive.

[0071] For transmitting the electric signals, the pixel structure **200** further includes the data line **220***c* disposed on the substrate **210**, located between the patterned semiconductor layer **232** and the substrate **210**, and electrically connected to the source **232***c* of the thin film transistor structure **234**. In addition, the gate electrode layer **254** further includes the gate line **254***b* electrically connected to the gate **254***a* of the thin film transistor structure **234**. The gate line **254***b* and the data line **220***c* extends in different directions for respectively transmitting a control signal to the gate **254***a* and transmitting a data signal to the source **232***c*. Therefore, the thin film transistor structure **234** can be turned on by the control signal and the data signal can be transmitted to the pixel electrode **232***a* through the turned-on thin film transistor structure **234**.

[0072] In the present embodiment, the gate line **254***b* is formed by using the same method of forming the gate **254***a*. Therefore, the insulation layer **242** includes a insulation portion **242***a* underlying the gate line **254***b*. The insulation portion **242***a* conforms in shape to the gate line **254***b*. The patterned semiconductor layer **232** further includes a semiconductor portion **232***e* underlying the gate line **254***b* and has a separating gap SG corresponding to the opening **230**A shown in FIG. **14**A and exposing a portion of the data line **220***c*. The semiconductor portion **232***e* partially conforms in shape to the gate line **154***b*. The gate line **254***b*, the insulation portion **242***a* and the semiconductor portion **232***e* form a gate line structure **256**, where the gate line **254***b* and the insulation portion **242***a* of the gate line structure **256** cross over the data line **220***c* at the separating gap SG such that the semiconductor portion **232***e* is not in contact with the data line **220***c* and the insulation portion **242***a* of the insulation layer **242** fills in the separating gap SG and contacts the data line **220***c* for isolating the data line **220***c* from the gate line **254***b*. In other words, the insulation layer **242** patterned from the insulation material layer **240** fills the separating gap SG such as the semiconductor portion **232***e* of the gate lines structure **256** is electrically insulating to the data line **220***c* for preventing the short circuit between the data lines **220***c* and the semiconductor portion **232***e* of the gate lines structure **256**. In the embodiment, a portion of the source **232***c* is in direct contact with the data line **220***c* by being in direct contact with the first metal portion **220***a* that branches off of the data line **220***c*, to electrically connect to the data line **220***c*. In addition, the pixel structure **200** is different from the pixel structure **100** in that it does not further include a second metal portion between the drain **232***b* and the pixel electrode **232***a*. The drain **232***b* and the pixel electrode **232***a* are connected to each other and made from the same patterned semiconductor layer **232**.

[0073] Based on the above, it should be noted that, in the manufacturing process of the pixel structure of the embodiments, the photoresist layer is patterned by the photomask to form the patterned photoresist layer that includes the first thickness portion and the second thickness portion. This allows that patterned photoresist layer to act as a mask when etching different portions of the stacked structure. This further allows the manufacture of the pixel structure to require fewer masks. Thus, the manufacturing cost of the pixel structure of the invention can be effectively lowered.

[0074] In addition, when performing etching to expose the source and the drain, the channel is covered by the insulation layer. Thus, the channel of the semiconductor layer will not be damaged during the etching process. This allows the thin film transistor structure to have better reliability.

[0075] Furthermore, it can be seen that since the source, the drain, and the channel are of the same patterned semiconductor layer, the source, the drain, and the channel are electrically connected without requiring contact holes. In addition, the drain is electrically contacted with the pixel electrode without contact holes. This improves resolution or aperture ratio of the pixel structure. In addition, not requiring contact holes also saves space in the layout of the thin film transistor structure.

[0076] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications

and variations of this invention provided they fall within the scope of the following claims and their equivalents.

1. A manufacturing method of a pixel structure, the method comprising:

forming a patterned semiconductor material layer, an insulation material layer, and a gate electrode material layer in sequence on a substrate to form a stacked structure;

forming a patterned photoresist layer on the stacked structure by using a photomask, wherein the patterned photoresist layer comprises a first thickness portion covering a first portion of the stacked structure and a second thickness portion covering a second portion of the stacked structure, and the patterned photoresist layer exposes a third portion of the stacked structure;

removing the third portion of the stacked structure to pattern the patterned semiconductor material layer into a patterned semiconductor layer by using the patterned photoresist layer as a mask;

removing the first thickness portion of the patterned photoresist layer and thinning the second thickness portion of the patterned photoresist layer to expose the first portion of the stacked structure previously covered by the first thickness portion of the patterned photoresist layer;

etching the first portion of the stacked structure by using the thinned second thickness portion of the patterned photoresist layer as a mask until an exposed portion of the patterned semiconductor layer in the first portion of the stacked structure is exposed, wherein the gate electrode material layer is patterned into a gate electrode layer, and the insulation material layer is patterned into an insulation layer having a shape substantially conformal to the gate electrode layer and covering a covered portion of the patterned semiconductor layer;

modifying the exposed portion of the patterned semiconductor layer to increase a conductivity of the exposed portion of the patterned semiconductor layer; and

removing the thinned second thickness portion of the patterned photoresist layer, wherein the covered portion of the patterned semiconductor layer comprises a channel, the exposed portion of the patterned semiconductor layer comprises a source and a drain, the gate electrode layer comprises a gate above the channel, and the gate, the channel, the source and the drain form a thin film transistor structure.

2. The method as claimed in claim **1**, further comprising forming a patterned metal layer on the substrate prior to forming the stacked structure, wherein the patterned metal layer comprises a data line electrically connected to the source.

3. The method as claimed in claim **2**, wherein the patterned semiconductor material layer has an opening exposing a portion of the data line and the patterned semiconductor layer patterned from the patterned semiconductor material layer comprises a semiconductor portion and has a separating gap corresponding to the opening, such that the insulation layer patterned from the insulation material layer comprises an insulation portion filling the separating gap and contacting the portion of the data line and the semiconductor portion is electrically insulating to the data line.

4. The method as claimed in claim **1**, wherein the removing the first thickness portion of the patterned photoresist layer and the thinning the second thickness portion of the patterned photoresist layer comprises performing an ashing process.

5. The method as claimed in claim **1**, wherein the forming the patterned photoresist layer on the stacked structure comprises using one half-tone photomask or one gray-tone photomask to form the first thickness portion and the second thickness portion.

6. The method as claimed in claim **1**, wherein the modifying the exposed portion of the patterned semiconductor layer comprises performing a plasma treatment, an ion implanting, or a combination thereof.

7. The method as claimed in claim **6**, wherein the plasma treatment uses hydrogen gas as a processing gas.

8. The method as claimed in claim **1**, wherein the removing the second thickness portion comprises performing a stripping process.

9. The method as claimed in claim **1**, further comprising forming a pixel electrode electrically connected to the drain.

10. The method as claimed in claim **9**, wherein the formation of the pixel electrode is simultaneous to the formation of the source and the drain.

11. The method as claimed in claim **9**, wherein the pixel electrode is formed by modifying the exposed portion of the patterned semiconductor layer.

12. A pixel structure, comprising:

a pixel electrode, disposed on a substrate;

a thin film transistor structure, disposed on the substrate and connected to the pixel electrode, the thin film transistor structure comprising a source, a drain, and a channel formed by a patterned semiconductor layer and a gate formed by a gate electrode layer, wherein the source and the drain are located at two opposite sides of the channel, and the gate is located above the channel; and

an insulation layer interposed between the patterned semiconductor layer and the gate electrode layer and having a shape substantially conformal to the gate electrode layer, wherein the insulation layer covers a covered portion of the patterned semiconductor layer to form the channel and exposes an exposed portion of the patterned semiconductor layer to form the source and the drain, the exposed portion of the patterned semiconductor layer further comprises the pixel electrode, and the pixel electrode, the source and the drain are belonged to a same film.

13. The pixel structure as claimed in claim **12**, wherein a material of the patterned semiconductor layer comprises an oxide semiconductor material.

14. The pixel structure as claimed in claim **12**, wherein the covered portion of the patterned semiconductor layer has a first conductivity type and the exposed portion of the patterned semiconductor layer has a second conductivity type more conductive than the first conductivity type.

15. The pixel structure as claimed in claim **14**, wherein the exposed portion of the patterned semiconductor layer further comprises the pixel electrode.

16. The pixel structure as claimed in claim **12**, further comprising a data line disposed on the substrate, located between the patterned semiconductor layer and the substrate, and electrically connected to the source of the thin film transistor structure.

17. The pixel structure as claimed in claim **16**, wherein the gate electrode layer further comprises a gate line electrically

connected to the gate of the thin film transistor structure, the insulation layer comprises a insulation portion underlying the gate line, the patterned semiconductor layer further comprises a semiconductor portion underlying the gate line, and the gate line, the insulation portion and the semiconductor portion form a gate line structure.

18. The pixel structure as claimed in claim **17**, wherein the patterned semiconductor layer has a separating gap exposing a portion of the data line, the insulation portion fills the separating gap and contacts the portion of the data line, and the semiconductor portion of the gate line structure is electrically insulating to the data line.

19. The pixel structure as claimed in claim **16**, wherein a portion of the source is in direct contact with the data line to electrically connect to the data line.

20. The pixel structure as claimed in claim **16**, further comprising a patterned metal portion disposed on the substrate, located and electrically connected between the drain and the pixel electrode, wherein a material of the patterned metal portion and the data line is the same.

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