

### (54) DUAL CHANNEL STRUCTURES WITH MULTIPLE THRESHOLD VOLTAGES

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### References Cited

### U.S. PATENT DOCUMENTS



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### ( 57 ) ABSTRACT

A method of forming a semiconductor structure includes depositing a first work function metal layer in nanosheet channel stacks for first and second CMOS structure each including a first nanosheet channel stack for an nFET and a second nanosheet channel stack for a pFET. The method also includes patterning to remove the first work function metal layer surrounding nanosheet channels in the first nanosheet channel stack of the first CMOS structure and nanosheet channels in the second nanosheet channel stack of the second CMOS structure. The method further includes depositing a second work function metal layer to surround the nanosheet channels in the first nanosheet channel stack of the first CMOS structure and the nanosheet channels in the second nanosheet channel stack of the second CMOS structure . The first CMOS structure has a first threshold voltage and the second CMOS structure has a second threshold voltage.

### 20 Claims, 13 Drawing Sheets



# ( 56 ) References Cited

## U.S. PATENT DOCUMENTS



\* cited by examiner





























structures. Semiconductor devices, such as those utilizing and the second CMOS structure comprises a first nanosheet semiconductor fin field-effect transistors (FinFETs), are an channel stack for a negative-channel field-e evolution of complementary metal-oxide-semiconductor <sup>10</sup> (nFET) comprising two or more nanosheet channels of a first (CMOS) devices. In some semiconductor devices utilizing channel material and a second nanosheet channel nology is used to form a device channel comprising one or<br>more nanosheet channels of a second channel mate-<br>more layers of nanosheets. In nanosheet technology, each  $\frac{1}{15}$  rial different than the first channel material more layers of nanosheets. In nanosheet technology, each  $\frac{1}{15}$ nanosheet has a vertical thickness substantially less than the function metal layer surrounds the two or more nanosheet width of that nanosheet. Gate structures may be formed channels of the second nanosheet channel stack in the first above and below each nanosheet.<br>CMOS structure and the two or more nanosheet channels of

For example, in one embodiment a method of forming a 25<br>miconductor structure comprises depositing a first work BRIEF DESCRIPTION OF THE DRAWINGS semiconductor structure comprises depositing a first work function metal layer surrounding nanosheet channels in nanosheet channel stacks for a first complementary metal-<br>
oxide-semiconductor (CMOS) structure and at least a sec-<br>
voltage dual channel device, according to an embodiment of ond CMOS structure, each of the first CMOS structure and <sup>30</sup> the present invention.<br>the second CMOS structure comprising a first nanosheet FIG. 2A illustrates a cross-sectional view of a negative the second CMOS structure comprising a first nanosheet channel stack for a negative-channel field-effect transistor channel stack for a negative-channel field-effect transistor channel portion of CMOS structures resulting from deposi-<br>(nFET) comprising two or more nanosheet channels of a first tion of a first work function material, acc (nFET) comprising two or more nanosheet channels of a first tion of a first work function material, according to an channel material and a second nanosheet channel stack for embodiment of the present invention. channel material and a second nanosheet channel stack for embodiment of the present invention . a positive - channel field - effect transistor ( PFET ) comprising » FIG . 2B illustrates a cross - sectional view of a positive two or more nanosheet channels of a second channel mate-<br>
rial different than the first channel material. The method also<br>
sition of a first work function material, according to an rial different than the first channel material. The method also sition of a first work function material, according to an comprises patterning to remove the first work function metal embodiment of the present invention. layer surrounding the two or more nanosheet channels in the  $_{40}$  FIG. 3A illustrates a cross-sectional view of the FIG. 2A first nanosheet channel stack of the first CMOS structure and structure following removal of the first nanosheet channel stack of the first CMOS structure and structure following removal of the first work function matetion remove the first work function metal layer surrounding rial from a portion of the structure, acc to remove the first work function metal layer surrounding rial from a portion of the structure, according to an embodi-<br>the two or more nanosheet channels in the second nanosheet ment of the present invention. channel stack of the second CMOS structure. The method FIG. 3B illustrates a cross-sectional view of the FIG. 2B further comprises depositing a second work function metal 45 structure following removal of the first work fu further comprises depositing a second work function metal 45 laver to surround the two or more nanosheet channels in the layer to surround the two or more nanosheet channels in the rial from a portion of the structure, according to an embodi-<br>first nanosheet channel stack of the first CMOS structure and ment of the present invention. first to surround the two or more nanosheet channels in the FIG. 4A illustrates a cross-sectional view of the FIG. 3A second nanosheet channel stack of the second CMOS structure following deposition of a second work functi

prises a first complementary metal-oxide-semiconductor structure following deposition of a second work function<br>(CMOS) structure and at least a second CMOS structure, material, according to an embodiment of the invention. each of the first CMOS structure and the second CMOS FIG. 5A illustrates a cross-sectional view of the FIG. 3A structure comprising a first nanosheet channel stack for a 55 structure following deposition of a second work f structure comprising a first nanosheet channel stack for a 55 structure following deposition of a second work function<br>negative-channel field-effect transistor (nFET) comprising material different than the first work funct two or more nanosheet channels of a first channel material according to an embodiment of the invention.<br>and a second nanosheet channel stack for a positive-channel FIG. 5B illustrates a cross-sectional view of the FIG. 3B<br> field-effect transistor (pFET) comprising two or more structure following deposition of a second work function nanosheet channels of a second channel material different 60 material different than the first work function ma than the first channel material. A first work function metal according to an embodiment of the invention.<br>
layer surrounds the two or more nanosheet channels of the FIG. 6A illustrates a top-down view of first and second<br> second nanosheet channel stack in the first CMOS structure CMOS structures, according to an embodiment of the inven-<br>and the two or more nanosheet channels of the first tion. nanosheet channel stack in the second CMOS structure. A  $65$  FIG. 6B illustrates a cross-sectional view taken along the second work function metal layer surrounds the two or more line A-A in FIG. 6A, according to an embod nanosheet channels of the first nanosheet channel stack in

DUAL CHANNEL STRUCTURES WITH first CMOS structure and the two or more nanosheet channel Stack in the second nanosheet channel stack in the second nanosheet channel stack in the second nels of the second nanosheet channel stack in the second CMOS structure.

BACKGROUND In another embodiment, an integrated circuit comprises a<br>Superior of the comprising a first complementary semiconductor structure comprising a first complementary The present application relates to semiconductors, and metal-oxide-semiconductor (CMOS) structure and at least a<br>more specifically, to techniques for forming semiconductor second CMOS structure. Each of the first CMOS stru more specifically, to techniques for forming semiconductor second CMOS structure. Each of the first CMOS structure structures. Semiconductor devices, such as those utilizing and the second CMOS structure comprises a first semiconductor fin field-effect transistors (FinFETs), are an channel stack for a negative-channel field-effect transistor evolution of complementary metal-oxide-semiconductor  $10$  (nFET) comprising two or more nanosheet c ( CMOS ) devices. In some semiconductor devices utilizing channel material and a second nanosheet channel stack for FinFETs, gate around device nanosheet or nanowire tech-<br>
a positive-channel field-effect transistor (pFET) CMOS structure and the two or more nanosheet channels of the first nanosheet channel stack in the second CMOS SUMMARY 20 structure. A second work function metal layer surrounds the two or more nanosheet channels of the first nanosheet Embodiments of the invention provide techniques for channel stack in first CMOS structure and the two or more<br>forming dual channel structures with multiple threshold nanosheet channels of the second nanosheet channel stack forming dual channel structures with multiple threshold nanosheet channels of the second nanosheet channel stack in voltages.

voltage dual channel device, according to an embodiment of the present invention.

structure following deposition of a second work function  $50$  material, according to an embodiment of the invention.

ture.<br>In another embodiment, a semiconductor structure com-<br>prises a first complementary metal-oxide-semiconductor<br>structure following deposition of a second work function<br>tion

line A-A in FIG. 6A, according to an embodiment of the invention.

line B-B in FIG. 6A, according to an embodiment of the WF2, between formation of IL and high-k dielectric invention.

line C-C in FIG. 6A, according to an embodiment of the <sup>5</sup> invention.

forming dual channel structures with multiple threshold FIGS 2A and 2B illustrate cross-sectional views 200 and voltages, along with illustrative apparatus, systems and 250, respectively, of the nFET and pFET portions of a voltages, along with illustrative apparatus, systems and devices having dual channel structures formed using such devices having dual channel structures formed using such CMOS structures resulting from deposition of the first work methods. However, it is to be understood that embodiments 15 function, or WF1, material. of the invention are not limited to the illustrative methods, As shown in FIGS. 2A and 2B, the structure includes apparatus, systems and devices but instead are more broadly portions of two regions 201 and 201' for both nF apparatus, systems and devices but instead are more broadly portions of two regions 201 and 201' for both nFET and applicable to other suitable methods, apparatus, systems and pFET. The first region 201 represents an area applicable to other suitable methods, apparatus, systems and pFET. The first region 201 represents an area where WF1 devices.

sistors (nFETs) and positive channel field-effect transistors a second CMOS structure. For clarity of illustration, the (pFETs). Dual channel CMOS devices utilize different chan-regions for only two CMOS structures are sho (pFETs). Dual channel CMOS devices utilize different chan-<br>negions for only two CMOS structures are shown. It is to be<br>nel materials in the nFETs and pFETs, such as using silicon<br>appreciated, however, that a plurality of C nel materials in the nFETs and pFETs, such as using silicon appreciated, however, that a plurality of CMOS structures (Si) for nFET channels and silicon germanium (SiGE) for may be formed, including two or more CMOS struct pFET channels. Multiple threshold voltage (Vt) CMOS 25 using WF1 and/or WF2. In addition, in some embodiments devices are desired in structures such as nanosheet CMOS more than two WFs may be used to form more than two devices are desired in structures such as nanosheet CMOS more than two WFs may be used to form more than two devices. Described herein are techniques for ensuring Vt CMOS structures. In some embodiments, the channel dopuniformity in both nFETs and pFETs of a nanosheet CMOS ing may be used to fine tune the Vts for two or more CMOSs.<br>device for dual work function (WF) metal gates and multi-<br>The FIG. 2A structure includes a substrate 202, a Vt with the same patterning to provide more Vts. In some 30 layer 204 formed over the substrate 202, a high-k dielectric<br>embodiments, it is desired to provide a multi-Vt scheme layer 206 formed over the isolator layer 204, embodiments, it is desired to provide a multi-Vt scheme with dual channel nanosheet CMOS devices without dipole with dual channel nanosheet CMOS devices without dipole 208 formed over the high-k dielectric layer 206, and a<br>like lanthanum oxide to define multi-Vt due to two reasons. scavenging metal layer 210 formed over the barrier First, additional patterning required in dipole is challenging 208.<br>and reliable packaging is not available. Second, the dipole 35 The substrate 202 may be formed of Si. The substrate 202 method reduces the mobility thus i method reduces the mobility thus impacting the final per-<br>formance. The horizontal width of the substrate 202

FIG. 1 illustrates a band diagram 100 for a multi-Vt (in direction X-X') may vary as desired, such as based on the CMOS device utilizing a first work function (WF1) and number of CMOS structures. second work function (WF2) material for the gate. The band 40 Isolator layer 204 may be formed of silicon dioxide diagram 100 illustrates the conduction band edge (Ec), the  $(SiO<sub>2</sub>)$ . The isolator layer 204 may have a diagram 100 illustrates the conduction band edge (Ec), the ( $SiO<sub>2</sub>$ ). The isolator layer 204 may have a vertical thickness valence band edge (Ev), and the band offset between Si and (in direction Y-Y') ranging from 5 valence band edge (Ev), and the band offset between Si and (in direction Y-Y') ranging from 5 nanometers (nm) to 20 SiGe, where Si is used as the channel material for nFET and nm. The horizontal width of the isolator layer Sige, where Si is used as the channel material for nFET and nm. The horizontal width of the isolator layer 204 (in Sige is used as the channel material for pFET. The nFET has direction X-X') may match that of the underlyin SiGe is used as the channel material for pFET. The nFET has direction X-X') may match that of the underlying substrate two threshold voltages—a first threshold voltage nVt1 asso- 45 202. ciated with WF2 and a second threshold voltage nVt2 High-k dielectric layer 206 may be formed of hafnium associated with WF1. The pFET similarly has two threshold dioxide (HfO2). The high-k dielectric layer 206 may have a associated with WF1. The pFET similarly has two threshold dioxide (HfO2). The high-k dielectric layer 206 may have a<br>voltages—a first threshold voltage pVt1 associated with vertical thickness (in direction Y-Y') ranging fr voltages — a first threshold voltage pVt1 associated with vertical thickness (in direction Y-Y') ranging from 1 nm to WF1 and a second threshold voltage pVt2 associated with 3 nm. The horizontal width (in direction X-X') WF2. The n-channel threshold voltages, nVt1 and nVt2, are 50 dielectric layer 204. related such that nVt1<nVt2. The p-channel threshold volt-<br>isolator layer 204.

devices formed using the techniques described herein can 55 provide increased performance by reducing doping in the channels. In addition, fabrication is simplified by reducing width of the barrier layer 208 (in direction X-X') may match the masks and patterning steps required to define multiple that of the underlying high-k dielectric Vts. In addition, drawbacks caused by multi-Vt via lantha-<br>num oxide  $(La_2O_3)$ , such as reduced mobility, may be 60 (Ti), aluminum (Al), titanium aluminum (TiAl), tantalum num oxide ( $La_2O_3$ ), such as reduced mobility, may be 60 avoided.

In a general process flow for forming a nanosheet CMOS (TiAIC), or any combination of Ti and Al alloys aforemen-<br>device, nanosheet release is followed by formation of an tioned. The scavenging metal layer 210 may have a ve device, nanosheet release is followed by formation of an tioned. The scavenging metal layer 210 may have a vertical interfacial layer (IL) and a high-k dielectric layer. WF thickness (in direction Y-Y') ranging from 1 nm t deposition is then performed, followed by an optional metal 65 The horizontal width (in direction X-X') of the scavenging electrode deposition step and gate chemical mechanical metal layer 210 may match that of the underly electrode deposition step and gate chemical mechanical metal layer 210 may match that of the underlying barrier planarization (CMP). Methods are described below for layer 208. In some embodiment, the scavenging metal layer

FIG. 6C illustrates a cross-sectional view taken along the facilitating deposition of first and second WFs, WF1 and he B-B in FIG. 6A. according to an embodiment of the WF2, between formation of IL and high-k dielectric la

FIG. 6D illustrates a cross-sectional view taken along the More particularly, WF1 metal deposition to be used for the C-C in FIG. 6A, according to an embodiment of the  $5 \text{ nVt2}$  (e.g., the higher Vt for nFET) and pVt1 ( Vt for pFET) is performed first, followed by patterning to remove WF1 material from one or more regions or areas of the device where WF2 material is to be formed. WF2 metal DETAILED DESCRIPTION<br>the device where WF2 material is to be formed. WF2 metal<br>deposition is then performed in such regions for nVt1 (e.g.,<br>lllustrative embodiments of the invention may be 10 the lower Vt for nFET) and pVt1

will be used for a first CMOS structure, while the second<br>CMOS devices include negative channel field-effect tran- 20 region 201' represents an area where WF2 will be used for CMOS devices include negative channel field-effect tran- 20 region 201' represents an area where WF2 will be used for sistors (nFETs) and positive channel field-effect transistors a second CMOS structure. For clarity of il may be formed, including two or more CMOS structures using WF1 and/or WF2. In addition, in some embodiments

Formance.<br>FIG. 1 illustrates a band diagram 100 for a multi-Vt (in direction X-X') may vary as desired, such as based on the

3 nm. The horizontal width (in direction X-X') of the high-k dielectric layer  $206$  may match that of the underlying

ages, pVt1 and pVt2, are related such that pVt1<pVt2. Barrier layer 208 may be formed of titanium nitride (TiN),<br>Embodiments provide a number of advantages for utiliz-<br>ing multiple WFs. For example, multi-Vt nanosheet CMOS nitride (TiSiN) and titanium carbide (TiC) may be used. The barrier layer 208 may have a vertical thickness (in direction  $Y-Y'$ ) ranging from 2 angstrom (A) to 20A. The horizontal

oided.<br>In a general process flow for forming a nanosheet CMOS (TiAIC), or any combination of Ti and Al alloys aforemenlayer 208. In some embodiment, the scavenging metal layer 210 is not pinched off between the nanosheet channels 214 FIG. 2A, described above, illustrates the regions 201 and so that both inner sheet regions (e.g., regions between two 201' in an nFET structure. FIG. 2B illustrates so that both inner sheet regions (e.g., regions between two 201' in an nFET structure. FIG. 2B illustrates the regions 201 of the nanosheet channels 214, an example of which is and 201' for a pFET structure. As will be des of the nanosheet channels 214, an example of which is and 201' for a pFET structure. As will be described in further labeled 203 in FIG. 2A) and outer sheet regions (e.g., detail below with respect to FIGS. 6A-6D, the nFET labeled 203 in FIG. 2A) and outer sheet regions (e.g., detail below with respect to FIGS.  $6A-6D$ , the nFET in regions of the nanosheet channels 214 which are not sur-  $\frac{1}{2}$  region 201 the pFET in region 201 are conne regions of the nanosheet channels 214 which are not sur- 5 region 201 the pFET in region 201 are connected in a first<br>rounded by another nanosheet channel, an example of which CMOS structure while the nFET in region 201' a rounded by another nanosheet channel, an example of which CMOS structure while the nFET in region 201' and the pFET is labeled 205 in FIG. 2A) have the same work function and in region 201' are connected in a second CMOS s same Vt so that the nanosheets have the uniform Vt in each FIGS. 2A and 2B show the same layers with the same<br>region 201, 201'. By pinched off, it is meant that the layer sizing formed of the same materials as indicated by region 201, 201'. By pinched off, it is meant that the layer sizing formed of the same materials as indicated by the use 222 (described in further detail below), is not contacted by 10 of the same reference numerals in FIG 222 (described in further detail below), is not contacted by 10 of the same reference numerals in FIGS. 2A and 2B. FIGS.<br>itself but is rather separated by layer 212 (described in 2A and 2B differ, however, in the material further detail below). If both inner sheet regions and outer sheet regions have the same Vt, the structure is treated as sheet regions have the same Vt, the structure is treated as NFET structure of FIG. 2A is different than the material of having uniform Vt, meaning that the surface around each the nanosheet channels 215 in the PFET structu

The top capping layer 212 may be formed of TiN, although 2A. For example, if the nanosheet channels 214 are formed other suitable materials such as TiC may be used. The sizing of Si, the nanosheet channels 215 may be forme of the top capping layer 212 will vary based on the size of 20 where the germanium (Ge) concentration may range from<br>the regions 201, 201' (e.g., such as based on the number of  $10\%$  to 40%. In other embodiments, the nFE the regions 201, 201' (e.g., such as based on the number of 10% to 40%. In other embodiments, the nFET may utilize a nanosheet channels 214 which are formed. The top capping group III-V semiconductor for nanosheet channels nanosheet channels 214 which are formed. The top capping group III-V semiconductor for nanosheet channels 214 layer 212 may generally have a thickness surrounding the while the pFET utilizes pure Ge for nanosheet channels nanosheet channels 214 (and the layers 216, 218, 220 and FIGS. 3A and 3B show cross sectional view 300 and 350, 222 described below) ranging from 0.5 nm to 2 nm. In some 25 respectively, of the nFET and pFET structures of

arrangement. In other embodiments, more or fewer than 30 three nanosheet channels may be used in the regions 201, nFET and pFET structures of FIGS. 2A and 2B, followed by 201'. The nanosheet channels 214 may be formed of Si, removal of layers 208, 210, 212, 220 and 222 from the 201'. The nanosheet channels 214 may be formed of Si, removal of layers 208, 210, 212, 220 and 222 from the although other suitable materials such as group III-V semi-<br>respective regions left exposed by the mask (e.g., reg although other suitable materials such as group III-V semi-<br>conductors such as gallium arsenide (GaAs), indium phos-<br>for the nFET structures and region 201 for the pFET phide (InP), gallium phosphide (GaP), gallium nitride (GaN) 35 structures). The layers 208, 210, 212, 220 and 222 may be and indium gallium arsenide (InGaAs) may be used. Each removed using wet etchants such as sulfur chlo and indium gallium arsenide (InGaAs) may be used. Each removed using wet etchants such as sulfur chloride (SCI) nanosheet 214 may have a horizontal width (in direction and hydrogen peroxide ( $H_2O_2$ ), or other suitable p  $X-X'$  ) ranging from 10 nm to 60 nm, and a vertical thickness (in direction  $Y-Y$ ) ranging from 5 nm to 12 nm.

which may be formed of  $Si_xO_{1-x}$  or  $Si_xN_{1-x}, O_y$ . In  $Si_xO_{1-x}$ , FIGS. 3A and 3B following deposition of the second work the value of x may range from 0.3 to 0.5. In  $\sin N_{1-x}$ ,  $\sin N_{1-x}$ ,  $\sin N_{2x}$  material. For the nFET structures, the value of x may range from 0.3 to 0.5 and the value of y may WF2 material is deposited in region 201'. For value of x may range from 0.3 to 0.5 and the value of y may WF2 material is deposited in region 201'. For the pFET range from 0.1 to 0.5. The concentrate of N may range from structures, the WF2 material is deposited in re 0.01 to 0.2. The IL 216 may have a thickness (in both 45 Bottom barrier layer 224 is deposited to surround the direction X-X' and direction Y-Y') ranging from 0.8 nm to nanosheet channels 214/215, the IL 216 and the high-k direction X-X' and direction Y-Y') ranging from 0.8 nm to nanosheet channels  $214/215$ , the IL 216 and the high-k 1.5 nm. The IL 216 is surrounded by high-k dielectric layer dielectric layer 218. For the nFET structures s 218, which may be formed of the same material and at the 4A, deposition of the material for the bottom barrier layer same time as the high-k dielectric layer 206 described above. 224 also results in a bottom barrier layer

A bottom barrier layer 220, which may be formed of the 50 ited over the nFET structure in region 201 and over the same material and at the same time as the barrier layer 208, high-k dielectric layer 206 in region 201'. For same material and at the same time as the barrier layer 208, high-k dielectric layer 206 in region 201'. For the pFET<br>surrounds the high-k dielectric layer 218. WF1 metal layer structures shown in FIG. 4B, deposition of th surrounds the high-k dielectric layer 218. WF1 metal layer structures shown in FIG. 4B, deposition of the material for 222, which may be formed of the same material and at the the bottom barrier layer 224 also results in b 222, which may be formed of the same material and at the the bottom barrier layer 224 also results in bottom barrier same time as scavenging metal layer 210, surrounds the layer 224' being deposited over the pFET structure same time as scavenging metal layer 210, surrounds the layer 224' being deposited over the pFET structure in region bottom barrier layer 220.

and 201', respectively, may be achieved in various ways. In bottom barrier layer 224. For the nFET structures shown in some embodiments, the materials used for WF1 in region FIG. 4A, deposition of the material for the WF2 201 and WF2 in region 201' may be the same, but have 226 also results in formation of a layer 226' over the layer varying thicknesses in one or both of the scavenging metal 60 224' in region 201. For the pFET structures sh layer 210 and in WF1 metal layer 222. In some embodi-<br>ments, the different work functions may be achieved by also results in formation of the layer 226' over the layer 224' ments, the different work functions may be achieved by also results in formation of the layer 226' over the layer 224' using different top capping layers 212 for the different in region 201'. regions 201 and 201'. In other embodiments, the materials Top capping layer 228 is formed over the WF2 metal layer used for WF1 metal layer 222 may be different than the 65 226. For the nFET structures shown in FIG. 4A, de material used for forming WF2 metal layer 226 described of the material for the top capping layer 228 also results in below.

having unanosheet channel 214 has the same Vt . 15 2B. The material of the nanosheet channels 215 in the PFET A top capping layer 212 is formed over the scavenging structure of FIG. 2B may be based on the material used for A top capping layer 212 is formed over the scavenging structure of FIG. 2B may be based on the material used for metal layer 210 and surrounding nanosheet channels 214. the nanosheet channels 214 in the NFET structure of F

and 2B following patterning and removal of WF1 metal pinch off the nanosheet to provide uniform Vt.<br>Although FIG. 2A illustrates a structure with three is removed from region 201'. For the pFET structures, the Although FIG. 2A illustrates a structure with three is removed from region 201'. For the pFET structures, the nanosheet channels 214, embodiments are not limited to this WF1 metal layer 222 is removed from region 201. A ma WF1 metal layer  $222$  is removed from region  $201$ . A mask may be patterned over the regions  $201$ ,  $201'$  in both the and hydrogen peroxide  $(H_2O_2)$ , or other suitable processing such as selective reactive-ion etching (ME).

FIGS. 4A and 4B show cross-sectional views 400 and 450, respectively, of the nFET and pFET structures shown in Each nanosheet channel 214 is surrounded by IL 216, 40 450, respectively, of the nFET and pFET structures shown in hich may be formed of  $Si_2O_{1-x}$  or  $Si_2O_{1-x}$  In  $Si_2O_{1-x}$ . FIGS. 3A and 3B following deposition of the 224 also results in a bottom barrier layer 224' being depos-

bottom barrier layer 220.<br>
Differing work functions WF1 and WF2 for regions 201 Next, WF2 metal layer 226 is deposited to surround the and 201', respectively, may be achieved in various ways. In bottom barrier layer 224. F

formation of a layer  $228'$  over the layer  $226'$  in region 201.

top capping layer 228 in region 201' may be formed of the  $5$  WF2 metal stack provides nVt1 for the nFET and WF1 same materials as the bottom barrier layer 220, WF1 metal stack provides pVt1 for the pFET. same materials as the bottom barrier layer 220, WF1 metal metal stack provides pVt1 for the pFET.<br>layer 222 and top capping layer 212 in region 201, respec-<br>Although FIG. 6A shows the first and second CMOS layer 222 and top capping layer 212 in region 201, respectively. In some embodiments, each layer stack is formed of tively. In some embodiments, each layer stack is formed of structures as being next to one another, this is not a require-<br>TiN/TiAlC/TiN, with the thickness of the TiAlC differing for ment. One or more other CMOS structure WF1 and WF2. For the nFET structures shown in FIG. 4A, 10 the WF2 metal layer 226 in region 201' is thicker than the the WF2 metal layer 226 in region 201' is thicker than the FIG. 6A. For example, multiple instances of the first CMOS WF1 metal layer 222 in region 201. Similarly, for the PFET structure and the second CMOS structure may b WF1 metal layer 222 in region 201. Similarly, for the PFET structure and the second CMOS structure may be formed as structures shown in FIG. 4B, the WF2 metal layer 226 in desired. Fins 604 provide source/drain regions bet structures shown in FIG. 4B, the WF2 metal layer 226 in desired. Fins 604 provide source/drain regions between the region 201 is thicker than the WF1 metal layer 222 in region first CMOS structure and the second CMOS struc region 201 is thicker than the WF1 metal layer 222 in region first CMOS structure and the second CMOS structure sur-<br>201'. 15 rounding the gates 602-1 and 602-2.

As described above, the thickness (in both direction X-X' FIG. 6B shows a cross-sectional view 625 of the first and Y-Y') of the WF1 metal layer 222 surrounding the CMOS structure, taken along line A-A in FIG. 6A. FIG. 6C and Y-Y') of the WF1 metal layer 222 surrounding the CMOS structure, taken along line A-A in FIG. 6A. FIG. 6C nanosheet channels 214/215 in regions 201 and 201' (for the shows a cross-sectional view 650 of the second CMOS nanosheet channels 214/215 in regions 201 and 201' (for the shows a cross-sectional view 650 of the second CMOS<br>NFET structures and PFET structures, respectively) may be structure, taken along the line B-B in FIG. 6A. FIGS NFET structures and PFET structures, respectively) may be structure, taken along the line B-B in FIG. 6A. FIGS. 6B and<br>in the range of 1 nm to 3 nm. The thickness of the WF2 metal 20 6C illustrate the gate electrode 230 fo layer  $224$  surrounding the nanosheet channels  $214/215$  in regions 201' and 201 (for the nFET structures and the pFET FIG. 6D shows a cross-sectional view 675 taken along<br>structures, respectively) may be in the range of 2 nm to 6 nm. line C-C in FIG. 6A. FIG. 6D illustrates spacer

materials but differing thicknesses for WF1 and WF2. In 30 may match to ther embodiments, different materials may be used for WF1 channels 214. and WF2. FIGS. 5A and 5B illustrate such an arrangement. The source/drain regions  $234$  may be formed of silicon FIGS. 5A and 5B show cross sectional views 500 and 550, phosphorus (Si,P,) or silicon carbon phosphorus (SiC FIGS. 5A and 5B show cross sectional views 500 and 550, phosphorus  $(Si_xP_y)$  or silicon carbon phosphorus (SiCP) for respectively, of the nFET and pFET structures of FIGS. 3A nFET, and  $Si_xCe_y$  for PFET. The horizontal widt and 3B following deposition of the second work function, or 35 WF2, material, where the WF2 material differs from the WF2, material, where the WF2 material differs from the the source/drain regions 234 may match that of the sur-<br>WF1 material. Bottom barrier layer 224 is re-deposited to rounding regions as illustrated. surround the nanosheet channels 214/215, the IL 216 and the The spacers 236 may be formed of SiN, SiBCN, SiCON, high-k dielectric layer 218. Next, WF2 metal layer 227 is SiCO or another suitable material, and may have a ho capping layer 228 is formed over the WF2 metal layer 227. Device isolation may be achieved using shallow trench<br>Formation of the bottom barrier layer 224, WF2 metal layer insulator (STI) and/or deep trench insulator (DTI) 227 and capping layer 228 in region 201' also results in the FIG. 6D shows STIs 238, which may be formed of  $Si_xO_y$  or deposition of such materials over region 201 as illustrated in  $Si_xN_y$ . The sizing of the STIs 238 may m deposition of such materials over region 201 as illustrated in  $Si_xN_y$ . The sizing of the STIs 238 may match that of the FIGS. 5A and 5B and as denoted by corresponding element 45 surrounding structure as illustrated.

The WF2 metal layer 227 is formed of a different material source and drains of the devices. The contacts in layer 240 than the WF1 metal layer 222. For example, while the WF1 may be formed of a silicide, such as titanium s than the WF1 metal layer 222. For example, while the WF1 may be formed of a silicide, such as titanium silicide (TiS) metal layer 222 is formed of TiAlC, the WF2 metal layer 227 although other suitable materials may be use may be formed of TiAl or TaAlC. In some embodiments, the  $50$  connects in layer 240 may be formed of tungsten (W), cobalt bottom barrier layer 224 and top capping layer 228 may be (Co) or another low resistance metal such formed of the same materials as bottom barrier layer 220 and ruthenium (Ru), etc. Each of the layers 240 may have a top capping layer 212, respectively. In other embodiments, horizontal width (in direction X-X') and a vert top capping layer 212, respectively. In other embodiments, horizontal width (in direction X-X') and a vertical thickness different materials may be used for at least one of the bottom (in direction Y-Y') which matches that different materials may be used for at least one of the bottom (in direction Y-Y') which matches that of the surrounding barrier layer  $224$  and the top capping layer  $228$ . For  $55$  structure as illustrated. example, the bottom barrier layer 220 and top capping layer 1 some embodiments, a method of forming a semicon-<br>212 may be formed of TiN while the bottom barrier layer ductor structure comprises depositing a first work func 212 may be formed of TiN while the bottom barrier layer ductor structure comprises depositing a first work function 224 and top capping layer 228 may be formed of TiC or TaN. metal layer surrounding nanosheet channels in n 224 and top capping layer 228 may be formed of TiC or TaN. metal layer surrounding nanosheet channels in nanosheet The thicknesses of the WF1 metal layer 222 and the WF2 channel stacks for a first CMOS structure and at lea

FIG. 6A shows a top down view 600 of a structure, illustrating how the regions  $201$  and  $201'$  described above illustrating how the regions 201 and 201' described above channel stack for an nFET comprising two or more with respect to FIGS. 2-5 are connected to form first and nanosheet channels of a first channel material and a seco with respect to FIGS. 2-5 are connected to form first and nanosheet channels of a first channel material and a second second CMOS structures.

pFET structure in region 201 in to form a first CMOS than the first channel material. The method also includes structure. In the first CMOS structure, WF1 metal stack patterning to remove the first work function metal laye

For the pFET structures shown in FIG. 4B, deposition of the provides nVt2 for the nFET and WF2 metal stack provides material for the top capping layer 228 also results in for-<br>mation of the layer 228' over the layer 226' i ation of the layer 228' over the layer 226' in region 201'. connected with the pFET structure in region 201' to form a<br>The bottom barrier layer 224, WF2 metal layer 226 and second CMOS structure. In the second CMOS structu

ment. One or more other CMOS structures may be formed between the first and second CMOS structures shown in

6C illustrate the gate electrode 230 formed over the tops of the nFET and pFET structures.

pinched off between the sheets so that in an outer region the The spacers 232 may be formed of SiN, SiBCN, SiCON, thickness of WF2 metal layer 224 is about the same total SiCO or another suitable material, and may have a h Embodiments, however, are not limited to using the same The vertical thickness (in direction Y-Y') of the spacers 232 aterials but differing thicknesses for WF1 and WF2. In 30 may match that of the spacing between the nano

nFET, and  $\text{Si}_{x}\text{Ge}_{y}$  for PFET. The horizontal width (in direction X-X') and the vertical thickness (in direction Y-Y') of

Figure 1 and 5 and 58 and 47 and 47 and 58 and although other suitable materials may be used. The inter-<br>connects in layer  $240$  may be formed of tungsten (W), cobalt

channel stacks for a first CMOS structure and at least a second CMOS structure, each of the first CMOS structure metal layer 227 may be the same or may vary as desired. 60 second CMOS structure, each of the first CMOS structure FIG. 6A shows a top down view 600 of a structure, and the second CMOS structure comprising a first nanoshee second CMOS structures.<br>The nFET structure in region 201 is connected with the 65 nanosheet channels of a second channel material different The nFET structure in region 201 is connected with the 65 nanosheet channels of a second channel material different pFET structure in region 201 in to form a first CMOS than the first channel material. The method also incl patterning to remove the first work function metal layer

surrounding the two or more nanosheet channels in the first nanosheet channel stack of the first CMOS structure and to nanosheet channel stack of the first CMOS structure and to nanosheet channel stack in the second CMOS structure. The remove the first work function metal layer surrounding the nFET and the pFET of the first CMOS structure remove the first work function metal layer surrounding the nFET and the pFET of the first CMOS structure each have<br>two or more nanosheet channels in the second nanosheet a first threshold voltage and the nFET and the pFET channel stack of the second CMOS structure. The method 5 further includes depositing a second work function metal further includes depositing a second work function metal age different than the first threshold voltage. In some layer to surround the two or more nanosheet channels in the embodiments, an integrated circuit comprises the layer to surround the two or more nanosheet channels in the embodiments, an integrated circuit comprises the semicon-<br>first nanosheet channel stack of the first CMOS structure and ductor structure. for the first work function metal layer<br>second nanosheet channel stack of the second CMOS struc- 10 comprises a first thickness and the second work function second nanosheet channel stack of the second CMOS struc- 10 comprises a first thickness and the second work function<br>ture. The nFET and the pFET of the first CMOS structure metal layer comprises a second thickness differen ture. The nFET and the pFET of the first CMOS structure metal layer comprises a second thickness different than the each have a first threshold voltage and the nFET and the first thickness. In other embodiments, the first each have a first threshold voltage and the nFET and the first thickness. In other embodiments, the first work function pFET of the second CMOS structure each have a second metal layer comprises a first work function metal pFET of the second CMOS structure each have a second metal layer comprises a first work function metal material threshold voltage different than the first threshold voltage. and the second work function metal layer compris

comprises a first thickness and the second work function work function metal material. The first work function metal metal layer comprises a second thickness different than the material and the second work function metal m first thickness. In other embodiments, the first work function each comprise one of Ti, Al, TiAl, TaAlC, TiAlC, or a metal layer comprises a first work function metal material combination of Ti and Al alloys. In some embod and the second work function metal layer comprises a 20 second work function metal material different than the first work function metal material. The first work function metal second work function metal layer comprises a second thick-<br>material and the second work function metal material may ness different than the first thickness and a each comprises one of Ti, Al, TiAl, TaAlC, TiAlC, or a combination of Ti and Al alloys. In some embodiments, the 25 combination of Ti and Al alloys. In some embodiments, the 25 metal material.<br>
first work function metal layer comprises a first thickness The semiconductor structure may further comprise a<br>
and a first work function metal and a first work function metal material, and the second capping layer surrounding the first work function metal layer vork function metal layer comprises a second thickness between the two or more nanosheet channels in th work function metal layer comprises a second thickness between the two or more nanosheet channels in the second<br>different than the first thickness and a second work function nanosheet channel stack of the first CMOS struct different than the first thickness and a second work function nanosheet channel stack of the first CMOS structure and metal material different than the first work function metal naterial different than the first work funct

layer surrounding the first work function metal layer between the two or more nanosheet channels in the second between the two or more nanosheet channels in the second material and the capping layer may comprise a non-scav-<br>nanosheet channel stack of the first CMOS structure and 35 enging metal. nanosheet channels in the first the first compute and 35 engine in the description above, various materials and dimenture or more nanosheet channels in the first nanosheet sions for different elements are provided. Unless two or more nanosheet channels in the first nanosheet sions for different elements are provided. Unless otherwise channel stack of the second CMOS structure. The first work noted, such materials are given by way of example channel stack of the second CMOS structure. The first work noted, such materials are given by way of example only and function metal layer may comprise a scavenging metal embodiments are not limited solely to the specific material and the capping layer may comprise a non-scav- 40

pinches off between the two or more nanosheet channels in Semiconductor devices and methods for forming same in the second nanosheet channel stack of the first CMOS accordance with the above-described techniques can be structure but does not pinch off between the two or more 45 nanosheet channels in the first nanosheet channel stack of nanosheet channels in the first nanosheet channel stack of tronic systems. Suitable hardware and systems for imple-<br>the first CMOS structure. The two or more nanosheet menting embodiments of the invention may include, but the first CMOS structure. The two or more nanosheet menting embodiments of the invention may include, but are channels in the first nanosheet channel stack of the first not limited to, personal computers, communication net channels in the first nanosheet channel stack of the first not limited to, personal computers, communication net-<br>CMOS structure and the two or more nanosheet channels in works, electronic commerce systems, portable commun CMOS structure and the two or more nanosheet channels in works, electronic commerce systems, portable communica-<br>the second nanosheet channel stack of the first CMOS 50 tions devices (e.g., cell and smart phones), solid-st the second nanosheet channel stack of the first CMOS 50 tions devices (e.g., cell and smart phones), solid-state media<br>structure may have a uniform threshold voltage.<br>Storage devices, functional circuitry, etc. Systems and

In some embodiments, a semiconductor structure com-<br>prises a first CMOS structure and at least a second CMOS plated embodiments of the invention. Given the teachings prises a first CMOS structure and at least a second CMOS plated embodiments of the invention. Given the teachings structure, each of the first CMOS structure and the second provided herein, one of ordinary skill in the art CMOS structure comprising a first nanosheet channel stack 55 to contemplate other impleme<br>for an nFET comprising two or more nanosheet channels of embodiments of the invention. a first channel material and a second nanosheet channel In some embodiments, the above-described techniques stack for a pFET comprising two or more nanosheet chan-<br>net used in connection with semiconductor devices that may nels of a second channel material different than the first require, for example, CMOSs, metal-oxide-semiconductor channel material. The semiconductor structure further com- 60 field-effect transistors (MOSFETs), and/or Fin channel material. The semiconductor structure further com- 60 field-effect transistors (MOSFETs), and/or FinFETs. By way<br>prises a first work function metal layer surrounding the two of non-limiting example, the semiconduct prises a first work function metal layer surrounding the two of non-limiting example, the semiconductor devices can<br>or more nanosheet channels of the second nanosheet channel include, but are not limited to CMOS, MOSFET, a or more nanosheet channels of the second nanosheet channel include, but are not limited to CMOS, MOSFET, and stack in the first CMOS structure and the two or more FinFET devices, and/or semiconductor devices that use stack in the first CMOS structure and the two or more FinFET devices, and/or semiconductor devices that use nanosheet channels of the first nanosheet channel stack in CMOS, MOSFET, and/or FinFET technology. the second CMOS structure, and a second work function 65 Various structures described above may be implemented<br>metal layer surrounding the two or more nanosheet channels in integrated circuits. The resulting integrated cir

10<br>and the two or more nanosheet channels of the second a first threshold voltage and the nFET and the pFET of the second CMOS structure each have a second threshold volt-

threshold voltage different than the first threshold voltage. and the second work function metal layer comprises a<br>In some embodiments, the first work function metal layer 15 second work function metal material different t In some embodiments, the first work function metal layer 15 second work function metal material different than the first comprises a first thickness and the second work function work function metal material. The first work combination of Ti and Al alloys. In some embodiments, the first work function metal layer comprises a first thickness and a first work function metal material, and wherein the ness different than the first thickness and a second work function metal material different than the first work function

surrounding the first work function metal layer between the material.<br>The method may further comprise forming a capping channel stack of the second CMOS structure. The first work channel stack of the second CMOS structure. The first work function metal layer may comprise a scavenging metal

embodiments are not limited solely to the specific examples given. Similarly, unless otherwise noted, all dimensions are enging metal.<br>In some embodiments, the first work function metal layer solely to the specific dimensions or ranges given.

accordance with the above-described techniques can be employed in various applications, hardware, and/or elecstorage devices, functional circuitry, etc. Systems and hard-<br>In some embodiments, a semiconductor structure com-<br>ware incorporating the semiconductor devices are contemprovided herein, one of ordinary skill in the art will be able<br>to contemplate other implementations and applications of

can be distributed by the fabricator in raw wafer form (that

is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher 5. The method of claim 4, wherein the first work function level carrier) or in a multichip package (such as a ceramic 5 metal material and the second work functi level carrier ) or in a multichip package (such as a ceramic 5 carrier that has either or both surface interconnections or carrier that has either or both surface interconnections or each comprises one of titanium (Ti), aluminum (Al), tita-<br>buried interconnections). In any case the chip is then inte-<br>mium aluminum (TiAl), tantalum aluminum car grated with other chips, discrete circuit elements, and/or<br>other signal processing devices as part of either (a) an and Al alloys. intermediate product, such as a motherboard, or (b) an end 10 6. The method of claim 1, wherein the first work function product. The end product can be any product that includes metal layer comprises a first thickness and product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end integrated circuit chips, ranging from toys and other low-end function metal material, and wherein the second work func-<br>applications to advanced computer products having a dis-<br>tion metal layer comprises a second thicknes play, a keyboard or other input device, and a central pro-<br>the first thickness and a second work function metal material.<br>15 different than the first work function metal material.

illustration, but are not intended to be exhaustive or limited between the two or more nanosheet channels in the second to the embodiments disclosed. Many modifications and nanosheet channel stack of the first CMOS structu to the embodiments disclosed. Many modifications and nanosheet channel stack of the first CMOS structure and variations will be apparent to those of ordinary skill in the 20 surrounding the first work function metal layer variations will be apparent to those of ordinary skill in the 20 art without departing from the scope and spirit of the art without departing from the scope and spirit of the two or more nanosheet channels in the first nanosheet described embodiments. The terminology used herein was channel stack of the second CMOS structure. chosen to best explain the principles of the embodiments, the **8**. The method of claim 1, wherein the first work function practical application or technical improvement over tech-<br>metal layer pinches off between the two or nologies found in the marketplace, or to enable others of 25 ordinary skill in the art to understand the embodiments ordinary skill in the art to understand the embodiments CMOS structure but does not pinch off between the two or<br>more nanosheet channels in the first nanosheet channel stack

- ( CMOS) structure and at least a second CMOS structure, each of the first CMOS structure and the second 35 ture, each of the first CMOS structure and the second 35 a first complementary metal-oxide-semiconductor CMOS structure comprising a first nanosheet channel (CMOS) structure and at least a second CMOS struc-(nFET) comprising two or more nanosheet channels of a first channel material and a second nanosheet channel (pFET) comprising two or more nanosheet channels of a second channel material different than the first chan-
- patterning to remove the first work function metal layer a second channel material material material: surrounding the two or more nanosheet channels in the 45 first nanosheet channel stack of the first CMOS strucfirst nanosheet channel stack of the first CMOS struc-<br>a first work function metal layer annosheet channels of the second nanosheet chan-<br>ture and to remove the first work function metal layer<br>more nanosheet channels of th surrounding the two or more nanosheet channels in the second nanosheet channel stack of the second CMOS second nanosheet channel stack of the second CMOS more nanosheet channels of the first nanosheet channel<br>stack in the second CMOS structure: and<br>stack in the second CMOS structure: and structure; and<br>depositing a second work function metal layer to surround<br>a second work function metal layer surround<br>a second work function metal layer surround 50
- positing a second work function metal layer to surround a second work function metal layer surrounding the two<br>the two or more nanosheet channels in the first or more nanosheet channels of the first nanosheet and to surround the two or more nanosheet channels in more nanosheet channels of the second nanosheet channel stack of the second 55 mel stack in the second CMOS structure.

2. The method of claim 1, wherein the nFET and the pFET first work function metal layer comprises a first thickness of the first CMOS structure each have a first threshold and the second work function metal layer comprises of the first CMOS structure each have a first threshold and the second work function metal layer comprises a voltage and the nFET and the pFET of the second CMOS second thickness different than the first thickness. structure each have a second threshold voltage different than 60 12. The semiconductor structure of claim 10, wherein the the first threshold voltage.<br>
first work function metal layer comprises a first work

metal layer comprises a first thickness and the second work layer comprises a second work function metal material material. function metal layer comprises a second thickness different than the first thickness.

is, as a single wafer that has multiple unpackaged chips), as and the second work function metal layer comprises a a bare die, or in a packaged form. In the latter case the chip second work function metal material differen second work function metal material different than the first<br>work function metal material.

tion metal layer comprises a second thickness different than<br>the first thickness and a second work function metal material

The descriptions of the various embodiments of the 7. The method of claim 1, further comprising forming a present invention have been presented for purposes of capping layer surrounding the first work function metal layer capping layer surrounding the first work function metal layer

metal layer pinches off between the two or more nanosheet channels in the second nanosheet channel stack of the first sclosed herein.<br>
What is claimed is:<br>
What is claimed is:<br>
What is claimed is:<br>  $\frac{d}{dt}$  of the first CMOS structure.

1. A method of forming a semiconductor structure, com-<br>1. The method of claim 1, wherein the two or more<br>prising:<br>1. A method of claim 1, wherein the two or more<br>prising: ising:<br>30 nanosheet channels in the first nanosheet channel stack of<br>4 depositing a first work function metal layer surrounding the first CMOS structure and the two or more nanosheet positing a first work function metal layer surrounding the first CMOS structure and the two or more nanosheet nanosheet channels in nanosheet channels in the second nanosheet channel stack of the first nanosheet channels in nanosheet channel stacks for a channels in the second nanosheet channel stack of the first first complementary metal-oxide-semiconductor CMOS structure have a uniform threshold voltage. First comprise comprise to comprise the comprise of the semiconductor structure, comprising:

- CMOS structure comprising a first nanosheet channel (CMOS) structure and at least a second CMOS structure and the second<br>stack for a negative-channel field-effect transistor ture, each of the first CMOS structure and the s ture, each of the first CMOS structure and the second CMOS structure comprising a first nanosheet channel stack for a negative-channel field-effect transistor (nFET) comprising two or more nanosheet channels of stack for a positive-channel field-effect transistor 40 (nFET) comprising two or more nanosheet channels of a first channel material and a second nanosheet channel a second channel material different than the first chan-<br>
tack for a positive-channel field-effect transistor<br>
(pFET) comprising two or more nanosheet channels of (pFET) comprising two or more nanosheet channels of<br>a second channel material different than the first chan
	- more nanosheet channels of the second nanosheet channel stack in the first CMOS structure and the two or
- the two or more nanosheet channels in the first or more nanosheet channels of the first nanosheet channel stack of the first CMOS structure channel stack in first CMOS structure and the two or nanosheet channel stack of the first CMOS structure channel stack in first CMOS structure and the two or and to surround the two or more nanosheet channels in more nanosheet channels of the second nanosheet chan-

the semiconductor structure of claim 10, wherein the second 55 nel state in the semiconductor structure of claim 10, wherein the semiconductor structure of claim 10, wherein the nFET and the pFET first work function metal

the first threshold voltage.<br> **the first work function** function metal material and the second work function metal<br> **3**. The method of claim 1, wherein the first work function function metal material and the second work fu function metal material and the second work function metal layer comprises a second work function metal material

than the first thickness.<br>
4. The method of claim 1, wherein the first work function first work function metal material and the second work 4. The method of claim 1, wherein the first work function first work function metal material and the second work metal layer comprises a first work function metal material function metal material each comprises one of tita function metal material each comprises one of titanium (Ti), 25

aluminum (Al), titanium aluminum (TiAl), tantalum alumi (pFET) comprising two or more nanosheet channels of num carbon (TaAlC), titanium aluminum carbon (TiAlC), or a second channel material different than the first chana combination of Ti and Al alloys.<br>14. The semiconductor structure of claim 10, wherein the

14. The semiconductor structure of claim 10, wherein the wherein a first work function metal layer surrounds the first work function metal layer comprises a first thickness 5 two or more nanosheet channels of the second first work function metal layer comprises a first thickness 5 two or more nanosheet channels of the second and a first work function metal material, and wherein the second panosheet channel stack in the first CMOS structur and a first work function metal material, and wherein the nanosheet channel stack in the first CMOS structure<br>second work function metal layer comprises a second thick-<br>and the two or more nanosheet channels of the first second work function metal layer comprises a second thick-<br>ness different than the first thickness and a second work<br>nanosheet channel stack in the second CMOS structure;

more nanosheet channels of the second nanosheet channels of the second nanosheet channels in the second nanosheet channels of the second nanosheet channels of the second nanosheet channels of the second CMOS structure.<br> **1** between the two or more nanosheet channels in the first **18.** The integrated circuit of claim 17, wherein the first papechoet channel stock of the second CMOS structure

16. The semiconductor structure of claim 15, wherein the second work function metal layer comprises a second metal layer comprises a second metal layer comprises a second metal in mess different than the first thickness. first work function metal layer comprises a scavenging metal<br>metal und the compilered circuit of claim 17, wherein the first<br>metal and the compilered comprises a non-convenience and the first material and the capping layer comprises a non-scavenging 20

- tary metal-oxide-semiconductor (CMOS) structure and than the first work function metal material.<br>at least a second CMOS structure;<br> $\frac{25}{\sqrt{10}}$  at least a second CMOS structure;
- ( $nFET$ ) comprising two or more nanosheet channels of carbon ( $14A1C$ ), titanium aluminum aluminum carbon ( $n$  and  $A1$  alloys. stack for a positive-channel field-effect transistor  $* * *$

a second channel material different than the first channel material:

- 
- The metal material different than the first the second work<br>
function metal material different than the first work function<br>
the first work function<br>
therein a second work function metal layer surrounds the<br>
two or more na

nanosheet channel stack of the second CMOS structure.<br>16 The second work function metal layer comprises a first thick-<br>16 The secondwitter structure of claim 15 wherein the

metal.<br>
The metal work function metal layer comprises a first work function<br>
17. An integrated circuit comprising:<br>
The metal material and the second work function metal layer<br>
17. An integrated circuit comprising: metal material and the second work function metal layer comprises a second work function metal material different a semiconductor structure comprising a first complemen-<br>than the first work function metal material

work function metal material and the second work function work function metal material and the second work function wherein each of the first CMOS structure and the second<br>CMOS structure arguments a first perceptical changed metal material each comprises one of titanium (Ti), alu CMOS structure comprises a first nanosheet channel metal material each comprises one of titanium (11), alumin-<br>ethelic for a possible channel field offert transister num (Al), titanium aluminum (TiAl), tantalum aluminum stack for a negative-channel field-effect transistor num (AI), titanium aluminum (TIAI), tantalum aluminum<br>(nEET) comprising two or more papocheet channels of carbon (TaAlC), titanium aluminum carbon (TiAlC), or a

\* \* \* \* \*