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(54) LOW POWER COHERENT RECEIVER FOR SHORT-REACH OPTICAL COMMUNICATION

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Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation of U.S. Patent Application No. 16/421,666, filed May 24, 2019.

BACKGROUND

[0002] An ever-growing bandwidth demand continues to drive a need for higher-speed optical interconnection networks, such as intra-datacenter links. To scale the interconnection interface bandwidth beyond lTb/s (1.6Tb/s, 3.2bit/s and beyond), more bandwidth-efficient coherent optical transmission technologies are likely needed. A "coherent" optical transmission system is characterized by its capability to do "coherent detection," meaning that an optical receiver can track the phase of an optical transmitter to extract any phase and frequency information carried by a transmitted signal, and therefore allow encoding and decoding information over both the amplitude and phase dimension of a light (for each polarization). Coherent technology has the potential to achieve higher link budget, require less active optical components such as lasers, and is also more tolerant toward several optical transmission impairments, such as the in-band optical interference, fiber dispersion, as well as laser relative intensity noise (RIN). Fiber dispersion is still not a problem until 800Gb/s, but could become a problem for future multi-Tb/s systems if current intensity modulation with direct detection (IM/DD) based coarse wavelength division multiplexing (CWDM) technologies are used. The impact of laser RIN also increases with baud rate and the modulation level. Increasing baud rate to beyond current 56Gbaud and modulation level beyond 4 levels would likely require scaling bandwidth beyond 1Tb/s for intra-datacenter links.

[0003] Coherent optical transmission technology, which is predominantly used in long-haul (LH) and metro networks, still faces several challenges for intra-datacenter applications. The first is power-hungry coherent digital signal processing (DSP). The second is the need for lasers with higher phase stability and modulators with higher extinction ratio (ER). The third is the backward compatibility requirement for certain applications. Regarding the first challenge, although significant progress has been made in recent years, the state-of-the-art coherent DSP power is still prohibitively high for intra-datacenter applications. For example, at a 7nm node, 400G coherent ZR, which represents the lowest-power 400G coherent DSP, is still about 70% higher than IM/DD-based 400G solutions. Accordingly, there is a need for solutions capable of further reducing coherent DSP power for intra-datacenter reach applications.

[0004] Up to present, three types of methods have been used or proposed to reduce coherent receiver DSP power. The first is to move to more advanced CMOS node. The second is to use fractional (non-integer) oversampling technique to reduce oversampling rate from traditional 2 to about 1.2. The third is to simplify the coherent equalizer design. For example, DSP power saving can be achieved by combining the conventional frequency-domain fiber chromatic dispersion (CD) equalizer and the time-domain polarization mode dispersion (PMD) multiple input multiple output (MIMO) equalizer into a single frequency-domain equalizer (FDE). But this method is effective only for metro or LH systems where the required equalizer length is significantly larger than that required by the intra-datacenter systems. As another example, a single-tap 2x2 complex-valued MIMO equalizer can be used for polarization recovery, while CD and bandwidth equalization is achieved by two complex-valued single-input single output (SISO) linear feedforward equalizers (FFEs). However, this method is very sensitive to coherent receiver path delays or skews. To address this coherent skew problem, an additional 3-tap 4x4 MIMO equalizer can be used for coherent skew correction, at the expense of increased power consumption. Up to present, all the proposed simplified coherent equalization methods still require analog-to-digital conversion (ADC) oversampling and fractionally-spaced equalization for practical implementation.

[0005] US 9,240,843 B1 discloses an apparatus that includes a coherent optical receiver that can receive during a first time period a set of in-phase signals and a set of quadrature signals having a skew from the set of in-phase signals. The coherent receiver can blindly determine a delay between the set of in-phase signals and the set of quadrature signals based on the set of in-phase signals and the set of quadrature signals. The delay includes an intersymbol portion and an intrasymbol portion. The coherent optical receiver can apply the delay at a second time after the first time period such that a skew after the second time is less than the skew at the first time period.

[0006] US 9,036,751 B1 discloses a receiver that applies a calibration method to compensate for skew between input channels. The receiver skew is estimated by observing the coefficients of an adaptive equalizer which adjusts the coefficients based on time-varying properties of the multi-channel input signal. The receiver skew is compensated by programming the phase of the sampling clocks for the different channels. Furthermore, during real-time operation of the receiver, channel diagnostics is performed to automatically estimate differential group delay and/or other channel characteristics based on the equalizer coefficients using a frequency averaging or polarization averaging approach.

[0007] WO 2014/194940 A1 discloses a coherent optical receiver, comprising: analog-to-digital conversion means configured for sampling an analog coherent optical signal into a digital coherent optical signal; channel equalization means configured for equalizing the digital coherent optical signal; channel transfer function calculation means configured for calculating a channel transfer function based on the digital coherent optical signal and

the equalized digital coherent optical signal interpolated by interpolation means and configured for adjusting the channel equalization means based on the calculated channel transfer function; phase detection means configured for providing a timing error detection characteristic, TEDC, signal, based on the equalized digital coherent optical signal; feed-backward timing recovery means configured for adjusting the sampling of the analog-to-digital conversion means based on the TEDC signal with respect to a frequency offset compensation criterion; and feed-forward timing recovery means configured for adjusting the interpolation means with respect to a phase offset compensation criterion.

BRIEF SUMMARY

[0008] The invention is defined by the independent claims. Dependent claims specify embodiments thereof.

[0009] The system and method described herein further reduce coherent receiver DSP power by using baud-rate ADC sampling and baud-rate spaced coherent equalization. The present disclosure proposes a power-efficient dual-DSP architecture to enhance coherent receiver performance for short reach coherent systems.

[0010] Several techniques are described herein to enable a low-power coherent receiver with enhanced performance for intra-datacenter reach optical interconnection applications. The first is a coherent skew adjustment technique which enables lower-power baud-rate ADC sampling and baud-rate-spaced coherent equalization. The second is a real-valued low-power coherent equalization technique, where a single-tap real-valued 4x4 MIMO equalizer plus four real-valued single-input single-out (SISO) equalizers are used for simultaneous polarization recovery, in-phase and quadrature (I/Q) phase error correction, and bandwidth equalization. The third is a power-efficient dual-DSP architecture to enhance coherent receiver performance, in which a complementary low-speed (non-streaming) coherent DSP is introduced for optimal I/Q phase error correction and constellation decision parameters determination through more sophisticated algorithms that are too power hungry to be implemented in the primary (streaming) high-speed DSP. Combined use of these three techniques not only enables overall coherent receiver power reduction, but also improves overall receiver performance for short reach optical communication.

[0011] One aspect of the disclosure provides a method of processing received optical signals at a coherent receiver. The method includes receiving, at a plurality of analog-to-digital converter ADC sampling clocks, a plurality of separate signals based on the received optical signals , performing baud-rate ADC sampling at each of the plurality of ADC sampling clocks, providing the plurality of signals output by the plurality of ADC sampling clocks to a high-speed digital signal processor, performing, at the high-speed digital signal processor high-speed processing of each of the plurality of signals, wherein the high-speed processing provides bandwidth equalization and polarization recovery by: processing the signals using two different types of real-valued or mixed-value equalizers, said processing comprises: inputting each of the plurality of signals to one of a plurality of real-valued or mixed value multi-tap single input single output SISO equalizers, and inputting the plurality of signals into a real-valued single tap multiple input multiple output MIMO equalizer, and directly introducing different time delays to each of the plurality of ADC sampling clocks, comprising: detecting, by a baud rate clock phase error detector in a clock recovery loop, phase errors, directly introducing different time delays to each of the plurality of ADC sampling clocks, and inputting an output of the high-speed digital signal processor into the baud rate clock phase error detector.

[0012] In other examples, it may include using a separate voltage controlled oscillator (VCO) in a clock recovery loop for each ADC sampling clock, each VCO using information from a common baud rate clock phase error detector.

[0013] In some examples, a low-speed DSP in parallel with the high-speed DSP, the low-speed DSP performing block by block DSP, such as to find at least one of optical constellation decision parameters, I/Q phase error compensation parameters, or optimal equalizer tap coefficients for input to the high-speed DSP.

[0014] Another aspect of the disclosure provides a low-power coherent optical receiver, including a plurality of analog-to-digital converter ADC sampling clocks adapted to receive a plurality of separate signals based on the received optical signals , wherein each ADC sampling clock is configured to perform baud-rate ADC sampling, a high-speed digital signal processor configured to perform high-speed processing of each of the plurality of signals output by the ADC sampling clocks, wherein the high-speed processor is configured to provide bandwidth equalization and polarization recovery, wherein the high-speed digital signal processor further comprises two different types of real-valued or mixed-value equalizers connected to each other, comprising: a plurality of multi-tap single input single output SISO equalizers, and a single-tap multiple input multiple output MIMO equalizer, and a baud rate clock phase error detector in a clock recovery loop configured to directly introduce different time delays to each of the plurality of ADC sampling clocks, wherein an output of the high-speed digital signal processor is input into the baud rate clock phase error detector.

[0015] The clock recovery loop may include a plurality of separate delay adjustable clock buffers following clock distribution, or a separate voltage controlled oscillator (VCO) for each ADC sampling clock, each VCO using information from the baud rate clock phase error detector.

[0016] The receiver may further include a low-speed DSP in parallel with the high-speed DSP, wherein the low-speed DSP is configured to perform block by block DSP, such as to find at least one of optical constellation

decision parameters, I/Q phase error compensation parameters, or optimal equalizer tap coefficients for input to the high-speed DSP.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017]

Fig. 1 is a pictorial diagram illustrating interconnection of nodes in a datacenter according to aspects of the disclosure.

Fig. 2 is a circuit diagram of a conventional receiver according to the prior art.

Fig. 3 is an example circuit diagram of a coherent receiver according to aspects of the disclosure.

Fig. 4 is an example circuit diagram of a low-speed DSP according to aspects of the disclosure.

Fig. 5 is another example circuit diagram of a coherent receiver according to aspects of the disclosure.

Figs. 6A-B provide other example circuit diagrams of a coherent receiver according to aspects of the disclosure.

Fig. 7 is a block diagram of an example node according to aspects of the disclosure.

Fig. 8 is a flow diagram illustrating an example method according to aspects of the disclosure.

DETAILED DESCRIPTION

[0018] According to implementations described herein, a low-power coherent receiver is provided which is enabled with enhanced performance for intra-datacenter reach optical interconnection applications using several techniques. The first is a coherent skew adjustment technique which enables lower-power baud-rate ADC sampling and baud-rate-spaced coherent equalization. The second is a real-valued or mixed-valued low-power coherent equalization technique, where a single-tap real-valued 4x4 MIMO equalizer plus four real-valued or two mixed-valued single-input single-out (SISO) equalizers are used for simultaneous polarization recovery, in-phase and quadrature (I/Q) phase error correction, and bandwidth equalization. The third is a power-efficient dual-DSP architecture to enhance coherent receiver performance, in which a complementary low-speed coherent DSP is introduced for optimal I/Q phase error correction and constellation decision parameters determination through more sophisticated algorithms that are too power hungry to be implemented in the primary high-speed DSP.

[0019] Fig. 1 illustrates a datacenter 100 including a plurality of racks 112, 114, 116, each rack shelving a plurality of nodes, such as servers, switches, routers, storage devices, etc. The nodes may be capable of optical communication, and therefore may include transmitters and receivers for communicating over optical links. The nodes within a rack may be interconnected by links, such as intra-rack links 140. A plurality of racks may be arranged in a plurality of rows 110, 120, 130. Some or all of the nodes within a row may also be interconnected, such as by intra-row links 150. Further, one or more of the nodes within a rack or row may be coupled to a core computing device 165, such as by core links 160. Any of the intra-rack links 140, intra-row links 150, and core links 160 may be considered intra-datacenter links. According to some examples, the datacenter 100 may also be coupled to another datacenter 101, which may be in a remote geographical location or on a same campus, by inter-datacenter link 170.

[0020] Some or all of the intra-datacenter links may be optical links, such as fiber ribbon links, bit-parallel wavelength division multiplexed (WDM) links, etc., over either multimode fiber (MMF) or single mode fiber (SMF). The optical links may be configured for transmission over relatively short distances, such as 2km or less.

[0021] While the nodes of the datacenter 100 of Fig. 1 are illustrated in a particular arrangement, it should be understood that the datacenter 100 may include nodes arranged in any of a variety of different architectures. For example, one possible architecture is a layered architecture, including core, aggregation, and access layers. In this example, the core layer may provide a high-speed packet switching backplane for all flows going in and out of the data center. Aggregation layer modules may provide for functions such as service module integration, Layer 2 domain definitions, spanning tree processing, default gateway redundancy, content switching, firewall, SSL offload, intrusion detection, network analysis, firewall and server load balancing, etc. In the access layer, the servers may physically attach to the network. Other possible architectures include, by way of example only, a multi-tier model, server cluster model, or any of a variety of other models.

[0022] Moreover, while the aspects of this disclosure are described primarily with respect to intra-datacenter links, it should be understood that the features described are also applicable to other types of link, such as from a central office to home, enterprise links, etc.

[0023] Fig. 2 illustrates a conventional receiver for short range optical communications. Conventionally, all pragmatic coherent receivers have used ADC oversampling and fractional-spaced equalization, where equalizer tap spacing is smaller than a symbol period. Lower-power baud-rate sampling and baud-rate spaced equalization techniques have been used in short reach IM/DD PAM4 systems, but baud-rate sampling and equalization (BRSE) techniques have not been achievable in coherent systems for two main reasons. First, the BRSE technique is sensitive to ADC sampling time, and optimal performance can only be achieved by sampling at the center of each signal pulse. Such a requirement can be challenging to meet for coherent systems that require joint processing of four received signals, the four signals including in-phase and quadrature components in two orthogonal polarizations. This is because there are unknown and variable time delays, or "skews," between the

four signals. Second, the BRSE technique has limited fiber CD and PMD tolerance, which is unacceptable for traditional coherent use cases with significant fiber CD and PMD. For intra-datacenter use cases, fiber CD and PMD is usually much smaller due to the use of O-band wavelength as well as shorter transmission reach, typically less than 2km.

[0024] As shown in Fig. 2, the coherent receiver has four inputs 202 - two for in-phase and two for quadrature, with each of the in-phase and quadrature having an x polarization and a y polarization. Each of the inputs 202 receives a separate signal, and the signals need to be synchronized. Accordingly, the conventional coherent receiver requires a skew compensation module 210 and an I/Q phase compensation module 220 between ADC sampling clocks 204 and chromatic dispersion (CD) equalization 230. The skew compensation module 210 and I/Q compensation module 220 may be digital signal processors. Because traditional skew compensation methods are used, the conventional coherent receiver also requires ADC oversampling, and therefore includes an oversampling clock phase error detector 240 between CD equalization 230 and clock recovery loop 250.

[0025] Conventional coherent receiver 200 further includes a multi-tap complex-valued 2x2 MIMO equalizer 260 for simultaneous bandwidth equalization and polarization recovery, and two additional (equivalent) 2x2 real-valued MIMO equalizer for I/Q phase error compensation (functional block 220), since the 2x2 complex-valued MIMO equalizer is not effective for I/Q phase error compensation.

[0026] Fig. 3 illustrates a novel dual-receiver design, enabling BRSE. As shown in this example, four ADC sampling clocks 304 receive signals from four input 302. The coherent receiver 300 does not require a skew compensation module or I/Q phase compensation module as shown in the conventional receiver. Rather, skew adjustment is performed by directly introducing different time delays to the four ADC sampling clocks. For example, a delay-adjustable clock buffer 380 follows clock distribution functional block 358 for each of the four ADC sampling clocks. In some examples, the delay adjustable clock buffer 380 could be integrated into the clock distribution unit.

[0027] The delay for each of the four clock buffers 380 can be individually or jointly optimized by monitoring phase errors detected by baud-rate clock phase error detector 352, which could be implemented by the classic Mueller-Mueller phase error detector using phase-recovered quadrature amplitude modulation (QAM) signals in both the X- and Y-polarizations. In some examples, one phase error detector 352 may be used to detect the averaged clock phase error over the four signal paths. A two-step optimization process could be used, wherein first the initial clock buffer delay is identical for all the four sampling clocks. Accordingly, the four clocks may be phase-synchronized. The common clock phase may be optimized by adjusting the phase of voltage controlled oscillator (VCO) 356. In the second step, once the common clock phase is optimized, individual clock phase may be fine-tuned, one at a time, by adjusting the corresponding clock buffer delay to minimize the average clock phase error. This skew compensation method may also be used for oversampled coherent systems, to remove the need for the additional skew compensation DSP required for the traditional coherent receiver.

[0028] The coherent receiver 300 of Fig. 3 also includes a power-efficient dual-DSP architecture. For example, a high-speed DSP 360 includes two different types of real-valued equalizers that achieve bandwidth equalization and polarization recovery. The operational speed of the high-speed DSP may be equal to the ADC sampling rate, which may be, for example, >50GHz. The first type may be a real-valued multi-tap single input single output (SISO) equalizer 362 for each of the four ADC sampling clocks 304. The SISO equalizers 362 may be linear or nonlinear, and may be used for bandwidth equalization of the four input signals. The signals output from the SISO equalizer 362 may be input to the second type of equalizer, such as single-tap 4x4 real-valued MIMO equalizer 364, which may be used for polarization recovery and for phase error compensation. This single-tap 4x4 MIMO equalizer 364 may further achieve simultaneous receiver in-phase (I) and quadrature (Q) phase error compensation. As compared to the conventional receiver illustrated in Fig. 2, the receiver of Fig. 3 not only removes the need for independent I/Q compensation DSP, it also greatly reduces the bandwidth equalizer complexity due to the use of real-valued SISO equalizer. For example, to achieve the same bandwidth equalization capability, the receiver 300 may reduce the implementation complexity by about 75%. Whereas a single-tap complex-valued 2x2 MIMO linear equalizer requires 16 real-valued multiplication operations, 4 single-tap real-valued SISO linear equalizers only require 4 real-valued multiplication operations.

[0029] The four real-valued outputs from the MIMO equalizer 364 are converted into two complex-valued signals and then are sent into carrier recovery unit 366, which is output to symbol and forward error correction (FEC) decoder 368. In parallel, complementary low-speed DSP 370 may perform block by block DSP. In this regard, more sophisticated DSP algorithms, such as certain machine learning based algorithms, may be executed in a parallel low-speed non-streaming block by block coherent DSP 370 to help find optimal constellation decision parameters as well as the I/Q phase correction parameters for the primary high-speed coherent DSP 360. This low-speed DSP 370 may also help find the optimal equalizer tap coefficients if the link state change is relatively slow. The low-speed DSP may operate at a speed several orders lower than the ADC sampling speed, for example from 100KHz to 100MHz.

[0030] Fig. 4 illustrates an example of the low-speed DSP 370 in more detail. The complementary low-speed DSP 370 may be in a separate functional block from the

receiver 300, but on a same or different integrated circuit.

[0031] As shown, the low-speed DSP 370 includes data buffer 371, and I/Q phase error compensation 372, which output I/Q phase error compensation parameters 377. The I/Q phase error compensation parameters can be expressed as a 2x2 real-valued matrix, consisting of four real-valued numbers.

[0032] The four signals output from the I/Q phase error compensation unit 372 are then input to advance adaptive equalizer unit 373, and then multiplexed into carrier recovery unit 374, both of which units interface with decision parameters discovery and equalizer (EQ) algorithm 376. The unit 376 employs certain adaptive equalization algorithms, for example, the common least mean square algorithm (LMS) to determine how to update the equalizer tap coefficients. This functional block also employs certain heuristic algorithms or the blind search algorithm to find the optimal constellation decision parameters. Metrics unit 375 may be used to find metrics such as signal to noise ratio (SNR), bit error ratio (BER), noise variance, etc. Output from the metrics unit 375 may also be output to the decision parameters discovery and EQ algorithm 376. In this regard, starting with an ideal case, parameters may be changed to look for SNR, and then find constellation decision boundary parameters and EQ parameters to optimize.

[0033] The constellation decision parameters may include an actual location of each constellation point as well as a decision boundary between neighboring constellation points. The location of each constellation point is used in symbol decision making in the equalizer and the carrier recovery circuits. For power-constrained short-reach coherent transmission systems employing low-cost components, a received signal constellation may be distorted/shifted due to insufficient modulator extinction ratio (ER) and non-negligible component nonlinearities, even without inter-symbol interference (ISI). For such a coherent system, the receiver performance strongly depends on the constellation decision parameters used for the equalizer. Non-optimal constellation decision parameters could result in significant performance penalty. But optimal constellation decision parameters can be hard to find using conventional least mean square (LMS) based algorithms. LMS based algorithms have been universally used for high-speed coherent equalizers due to their simplicity. However, implementing more sophisticated algorithms, such as certain machine learning based algorithms, directly into the high-speed DSP is impractical since power consumption and ASIC area cost could be too high for short-reach applications. By introducing the complementary low-speed non-streaming coherent DSP 370, more advanced DSP algorithms could be used to find optimal parameters required by the equalizer with negligible power and cost impact. Additionally, this low-speed DSP 370 may be used to find optimal I/Q phase error compensation parameter, which could be challenging to find with the conventional LMS based algorithms.

[0034] Fig. 5 illustrates another example implementation of the skew adjustment technique. This implementation includes four clock recovery loops 452, 455, 456, 458 with a shared baud-rate phase error detector 352. Since there are four VCOs, skew adjustment can be achieved by operating each VCO at slightly different clock phase. This can be achieved by jointly optimizing the four VCOs by using a single clock phase error signal from the baud-rate phase error detector using the classic gradient based algorithms.

[0035] Figs. 6A and 6B illustrate further example implementations. In Fig. 6A, single-tap 4x4 MIMO equalizer 564 may be implemented before SISO bandwidth equalizers 662. In Fig. 6B, the single-tap 4x4 MIMO equalizer 564 may be implemented between the four SISO bandwidth equalizers 662. In this example, the same number of SISO bandwidth equalizers may be used as in Fig. 6A, but the inputs may be split in half, thereby making it more powerful.

[0036] The four SISO equalizers 662 and the single-tap 4x4 MIMO equalizer 564 may be optimized independently, or they may also be optimized jointly as a single equalizer. For example, referring to the implementation shown in Fig. 6B, the tap of the 4x4 MIMO equalizer can be selected as the central tap, while the left SISO equalizer taps as the precursor taps and the right SISO equalizers as the post-cursor taps, or vice versa depending on the definition. Such a design could increase bandwidth equalization capability without increasing the actual equalizer tap length.

[0037] Additionally, the four real-valued SISO equalizers may be replaced by two mixed-value SISO equalizers (one mixed-value SISO equalizer per polarization), where the input signals to the mixed-value SISO equalizer are complex-valued numbers, which can be expressed by Ix+jQx for x -polarization and Iy+jQy for y-polarization, but the coefficient for each mixed-value SISO equalizer tap can be chosen to be either real-valued number or complex-valued number. If all the equalizer taps are designed to have real-valued coefficients, both the performance and implementation complexity for the two mixed-value SISO equalizer will be similar to the 4 real-valued SISO equalizer. If a portion of the mixed-value SISO equalizer taps (e.g. the middle three taps) are designed to have complex-valued tap coefficients, then the implementation complexity will increase, but fiber CD tolerance will also improve.

[0038] Fig. 7 is a block diagram illustrating an example node 700, such as datacenter switch. The node 700 includes various components, including one or more processors 720, memory 730, and other components typically present in switches, routers, servers, or other nodes. The one or more processors 720 may be in communication with other components of the node 700, such as transmitter 750, receiver 760, and other components that are not shown, such as fibers, amplifiers, circuitry, wiring, etc.

[0039] The memory 730 stores information accessible by processor 720, including instructions 732 and data

734 that may be executed or otherwise used by the processor 720. The memory 730 may be of any type capable of storing information accessible by the processor, including a computer-readable medium, or other medium that stores data that may be read with the aid of an electronic device, such as a hard-drive, memory card, ROM, RAM, DVD or other optical disks, as well as other write-capable and read-only memories. Systems and methods may include different combinations of the foregoing, whereby different portions of the instructions and data are stored on different types of media.

[0040] The instructions 732 may be any set of instructions to be executed directly (such as machine code) or indirectly (such as scripts) by the processor. For example, the instructions may be stored as computer code on the computer-readable medium. In that regard, the terms "instructions" and "programs" may be used interchangeably herein. The instructions may be stored in object code format for direct processing by the processor, or in any other computer language including scripts or collections of independent source code modules that are interpreted on demand or compiled in advance. Functions, methods and routines of the instructions are explained in more detail below.

[0041] The data 734 may be retrieved, stored or modified by processor 720 in accordance with the instructions 732. For instance, although the system and method is not limited by any particular data structure, the data may be stored in computer registers, in a relational database as a table having a plurality of different fields and records, XML documents or flat files. The data may also be formatted in any computer-readable format. The data may comprise any information, such as numbers, descriptive text, proprietary codes, references to data stored in other areas of the same memory or different memories (including other network locations) or information that is used by a function to calculate the relevant data.

[0042] The processor 720 may be any conventional processor, such as processors from Intel Corporation or Advanced Micro Devices. Alternatively, the processor may be a dedicated device such as an ASIC. Although Fig. 7 functionally illustrates the processor, memory, and other elements of the node 700 as being within the same block, it will be understood by those of ordinary skill in the art that the processor and memory may actually comprise multiple processors and memories that may or may not be stored within the same physical housing. For example, memory may be a hard drive or other storage media located in a server farm of a data center. Accordingly, references to a processor or computer will be understood to include references to a collection of processors or computers or memories that may or may not operate in parallel.

[0043] The transmitter 750 may include any commercially available components, or it may have specialized hardware. The receiver 760 may include the components described above in connection with Figs. 3-6. While the transmitter 750 and receiver 760 are shown as separate entities, it should be understood that they may be a single transceiver unit.

[0044] Fig. 8 illustrates a method 800 of receiving short range optical signals at a coherent receiver. The method 800 may be performed by, for example, a network node including the coherent receiver. While the operations associated with the method 800 are described in a particular order, it should be understood that they may be performed in a different order or simultaneously. Moreover, operations may be added or omitted.

[0045] In block 810, a plurality of optical signals are received at a plurality of ADC sampling clocks. The plurality of optical signals may include in-phase and quadrature signals, each having x and y polarizations. One signal may be received at each ADC sampling clock. Accordingly, for example, a system designed for receiving four individual signals will include four ADC sampling clocks.

[0046] In block 820, high-speed digital signal processing is performed in parallel with low-speed digital signal processing of block 830. The high-speed DSP may be executed without an independent I/Q compensation unit. Rather, the high-speed DSP may include performing SISO equalization at a plurality of real-valued or mixed-valued SISO equalizers, and MIMO equalization at a real-valued MIMO equalizer. While SISO equalization (block 822) is illustrated first, it should be understood, as discussed above, that MIMO equalization (block 824) may alternatively be performed first. In other examples, the MIMO equalizer may be between SISO equalizers.

[0047] In block 830, the low-speed DSP may be executed to identify or optimize one or more parameters for input to the high-speed DSP. For example, the low-speed DSP may find constellation decision parameters (block 832), equalizer tap coefficients (block 834), or any of a variety of other parameters. The low-speed DSP may perform, for example, block-by-block processing.

[0048] In block 840, skew adjustment is performed by directly introducing different time delays to the plurality of ADC sampling clocks. This may be performed without a dedicated skew compensation unit. Rather, introduction of the time delays may be performed as part of a clock recovery loop and may be based on baud rate clock phase error detection. The time delays are used in further receipt and processing of optical signals.

[0049] The skew-adjustment techniques described above enable lower-power baud-rate sampling and equalization technology for coherent systems. The real-valued coherent equalization technique reduces coherent equalizer implementation complexity by about 75%. About 30% overall coherent receiver power and area/cost reduction is achievable with combined use of both technologies. Furthermore, the proposed dual-DSP architecture enables the use of more advanced DSP algorithms to improve the coherent receiver performance with negligible power and cost impact.

[0050] The provision of the examples described herein, as well as clauses phrased as "such as," "including"

and the like, should not be interpreted as limiting the subject matter of the claims to the specific examples; rather, the examples are intended to illustrate only one of many possible embodiments. Further, the same reference numbers in different drawings can identify the same or similar elements.

Claims

1. A method of processing received optical signals at a coherent receiver (300), the method comprising:

   receiving (810), at a plurality of analog-to-digital converter ADC sampling clocks (304), a plurality of separate signals (Ix, Qx, Iy, Qy) based on the received optical signals;
   performing baud-rate ADC sampling at each of the plurality of ADC sampling clocks (304);
   providing the plurality of signals output by the plurality of ADC sampling clocks to a high-speed digital signal processor (360);
   performing (820), at the high-speed digital signal processor (360) high-speed processing of each of the plurality of signals, wherein the high-speed processing provides bandwidth equalization and polarization recovery by: processing the signals using two different types of real-valued or mixed-value equalizers, said processing comprises:

      inputting each of the plurality of signals to one of a plurality of real-valued or mixed-value multi-tap single input single output SISO equalizers (362, 562); and
      inputting the plurality of signals into a real-valued single tap multiple input multiple output MIMO equalizer (364, 564); and

   directly introducing (840) different time delays to each of the plurality of ADC sampling clocks (304), comprising: detecting, by a baud rate clock phase error detector (352) in a clock recovery loop (350, 450), phase errors,
   directly introducing different time delays to each of the plurality of ADC sampling clocks (304), and
   inputting an output of the high-speed digital signal processor (360) into the baud rate clock phase error detector (352).

2. The method of claim 1, wherein directly introducing (840) the different time delays to each of the plurality of ADC sampling clocks (304) comprises using a plurality of separate delay adjustable clock buffers (380) following clock distribution (358) in a clock recovery loop (350).

3. The method of claim 1, wherein directly introducing (840) the different time delays to each of the plurality of ADC sampling clocks (304) comprises using a separate voltage controlled oscillator VCO in a clock recovery loop (450) for each ADC sampling clock (304), each VCO using information from a common baud rate clock phase error detector (352).

4. The method of claim 1, wherein one signal is received (810) at each of the plurality of ADC sampling clocks (304), and wherein the plurality of separate optical signals include in-phase signals and quadrature signals, each having x and y polarizations.

5. The method of claim 1, wherein the output of each SISO equalizer (362, 562) is input into the MIMO equalizer (364, 564).

6. The method of claim 1, wherein the output of the MIMO equalizer (364, 564) is input into the plurality of SISO equalizers (362, 562).

7. The method of claim 1. further comprising executing a low-speed digital signal processor (370) in parallel with the high-speed digital signal processor (360), the low-speed digital signal processor (370) performing block by block digital signal processing.

8. The method of claim 7, wherein the low-speed digital signal processor (370) finds at least one of optical constellation decision parameters, I/Q phase error compensation parameters or optimal equalizer tap coefficients for input to the high-speed digital signal processor (360).

9. A low-power coherent optical receiver (300), comprising:

   a plurality of analog-to-digital converter ADC sampling clocks (304) adapted to receive (810) a plurality of separate signals (Ix, Qx, Iy, Qy) based on received optical signals;
   wherein each ADC sampling clock (304) is configured to perform baud-rate ADC sampling;
   a high-speed digital signal processor (360) configured to perform (820) high-speed processing of each of the plurality of signals output by the ADC sampling clocks (304), wherein the high-speed processor (360) is configured to provide bandwidth equalization and polarization recovery,
   wherein the high-speed digital signal processor (360) further comprises two different types of real-valued or mixed-value equalizers connected to each other, comprising:

      a plurality of multi-tap single input single output SISO equalizers (362, 562); and

a single-tap multiple input multiple output MIMO equalizer (364, 564); and
a baud rate clock phase error detector (352) in a clock recovery loop (350, 450) configured to directly introduce different time delays to each of the plurality of ADC sampling clocks (304),
wherein an output of the high-speed digital signal processor (360) is input into the baud rate clock phase error detector (352).

10. The receiver of claim 9, wherein the clock recovery loop (350) further comprises a plurality of separate delay adjustable clock buffers (380) following clock distribution (358), or
wherein the clock recovery loop (450) further comprises a separate voltage controlled oscillator VCO for each ADC sampling clock (304), each VCO using information from the baud rate clock phase error detector (352).

11. The receiver of claim 9, wherein each of the plurality of ADC sampling clocks (304) is configured to receive (810) one optical signal of the plurality of separate optical signals, the plurality of separate optical signals including in-phase signals and quadrature signals, each having x and y polarizations.

12. The receiver of claim 9, wherein the output of each SISO equalizer (362, 562) is input into the MIMO equalizer (364, 564).

13. The receiver of claim 9, wherein the output of the MIMO equalizer (364, 564) is input into the plurality of SISO equalizers (362, 562).

14. The receiver of claim 9, further comprising a low-speed digital signal processor (370) in parallel with the high-speed digital signal processor (360), wherein the low-speed digital signal processor (370) is configured to perform block by block digital signal processing.

15. The receiver of claim 14, wherein the low-speed digital signal processor (370) is configured to find at least one of optical constellation decision parameters, I/Q phase error compensation parameters, or optimal equalizer tap coefficients for input to the high-speed digital signal processor (306).

Patentansprüche

1. Verfahren zum Verarbeiten von empfangenen optischen Signalen an einem kohärenten Empfänger (300), wobei das Verfahren Folgendes umfasst:

Empfangen (810) einer Vielzahl von separaten Signalen (Ix, Qx, Iy, Qy) basierend auf den empfangenen optischen Signalen an einer Vielzahl von Analog-zu-Digital-Wandlern-Abtasttakten (analog-to-digital converter, ADC) (304);
Durchführen des Baudraten-ADC-Abtastens an jedem der Vielzahl von ADC-Abtasttakten (304);
Bereitstellen der Vielzahl von Signalen, die von der Vielzahl von ADC-Abtasttakten ausgegeben werden, an einen digitalen Hochgeschwindigkeitssignalprozessor (360);
Durchführen (820) eines Hochgeschwindigkeitsverarbeitens jedes der Vielzahl von Signalen an dem digitalen Hochgeschwindigkeitssignalprozessor (360), wobei das Hochgeschwindigkeitsverarbeiten eine Bandbreitenentzerrung und
eine Polarisationswiederherstellung bereitstellt, durch: Verarbeiten der Signale unter Verwendung von zwei unterschiedlichen Typen von realwertigen oder gemischtwertigen Entzerrern, wobei das Verarbeiten Folgendes umfasst:

Eingeben jedes der Vielzahl von Signalen in einen einer Vielzahl von realwertigen oder gemischtwertigen Multi-Tap-Single-Input-Single-Output-Entzerrern (single input single output, SISO) (362, 562); und
Eingeben der Vielzahl von Signalen in einen realwertigen Multiple-Input-Multiple-Output-Entzerrer (multiple input multiple output, MIMO) (364, 564); und
direktes Einführen (840) unterschiedlicher Zeitverzögerungen in jeden der Vielzahl von ADC-Abtasttakten (304), umfassend:
Detektieren von Phasenfehlern durch einen Baudraten-Taktphasenfehlerdetektor (352) in einer Taktwiederherstellungsschleife (350, 450),
direktes Einführen unterschiedlicher Zeitverzögerungen für jeden der Vielzahl von ADC-Abtasttakten (304), und
Eingeben einer Ausgabe des digitalen Hochgeschwindigkeitssignalprozessors (360) in den Baudraten-Taktphasenfehlerdetektor (352).

2. Verfahren nach Anspruch 1, wobei das direkte Einführen (840) der unterschiedlichen Zeitverzögerungen in jeden der Vielzahl von ADC-Abtasttakten (304) Verwenden einer Vielzahl von separaten verzögerungseinstellbaren Taktpuffern (380) nach der Taktverteilung (358) in einer Taktwiederherstellungsschleife (350) umfasst.

3. Verfahren nach Anspruch 1, wobei das direkte Einführen (840) der unterschiedlichen Zeitverzögerungen in jeden der Vielzahl von ADC-Abtasttakten (304) das Verwenden eines separaten spannungs-

gesteuerten Oszillators (voltage controlled oscillator, VCO) in einer Taktwiederherstellungsschleife (450) für jeden ADC-Abtasttakt (304) umfasst, wobei jeder VCO Informationen von einem gemeinsamen Baudraten-Taktphasenfehlerdetektor (352) verwendet.

4. Verfahren nach Anspruch 1, wobei ein Signal an jedem der Vielzahl von ADC-Abtasttakten (304) empfangen wird (810) und wobei die Vielzahl von separaten optischen Signalen phasengleiche Signale und Quadratursignale beinhaltet, die jeweils x- und y-Polarisierungen aufweisen.

5. Verfahren nach Anspruch 1, wobei die Ausgabe jedes SISO-Entzerrers (362, 562) in den MIMO- Entzerrer (364, 564) eingegeben wird.

6. Verfahren nach Anspruch 1, wobei die Ausgabe des MIMO-Entzerrers (364, 564) in die Vielzahl von SISO-Entzerrern (362, 562) eingegeben wird.

7. Verfahren nach Anspruch 1, ferner umfassend Ausführen eines digitalen Niedriggeschwindigkeitssignalprozessors (370) parallel zu dem digitalen Hochgeschwindigkeitssignalprozessor (360), wobei der digitale Niedriggeschwindigkeitssignalprozessor (370) ein blockweises digitales Signalverarbeiten durchführt.

8. Verfahren nach Anspruch 7, wobei der digitale Niedriggeschwindigkeitssignalprozessor (370) mindestens einen von optischen Konstellationsentscheidungsparametern, I/Q-Phasenfehlerkompensationsparametern oder optimalen Entzerrerabgriffskoeffizienten zur Eingabe in den digitalen Hochgeschwindigkeitssignalprozessor (360) findet.

9. Kohärenter optischer Empfänger (300) mit geringer Leistung, umfassend:

eine Vielzahl von Analog-zu-Digital-Wandlern-Abtasttakten (analog-to-digital converter, ADC) (304) die angepasst ist, um eine Vielzahl von separaten Signalen (Ix, Qx, Iy, Qy) basierend auf empfangenen optischen Signalen zu empfangen (810);
wobei jeder ADC-Abtasttakt (304) dazu konfiguriert ist, eine ADC-Abtastung mit Baudrate durchzuführen;
einen digitalen Hochgeschwindigkeitssignalprozessor (360), der dazu konfiguriert ist, das Hochgeschwindigkeitsverarbeiten jedes der Vielzahl von Signalen, die von den ADC-Abtasttakten (304) ausgegeben werden, durchzuführen (820), wobei der Hochgeschwindigkeitsprozessor (360) dazu konfiguriert ist, eine Bandbreitenentzerrung und Polarisierungswiederherstellung bereitzustellen,
wobei der digitale Hochgeschwindigkeitssignalprozessor (360) ferner zwei unterschiedliche Typen von miteinander verbundenen realwertigen oder gemischtwertigen Entzerrern umfasst, umfassend:

eine Vielzahl von Multi-Tap-Single-Input-Single-Output-Entzerrern (362, 562); und einen Multiple-Input-Multiple-Output-Entzerrer (364, 564); und einen Baudraten-Taktphasenfehlerdetektor (352) in einer Taktwiederherstellungsschleife (350, 450), der dazu konfiguriert ist, unterschiedliche Zeitverzögerungen in jeden der Vielzahl von ADC-Abtasttakten (304) direkt einzuführen,
wobei eine Ausgabe des digitalen Hochgeschwindigkeitssignalprozessors (360) eine Eingabe in den Baudraten-Taktphasenfehlerdetektor (352) ist.

10. Empfänger nach Anspruch 9, wobei die Taktwiederherstellungsschleife (350) ferner eine Vielzahl von separaten verzögerungseinstellbaren Taktpuffern (380) nach der Taktverteilung (358) umfasst oder wobei die Taktwiederherstellungsschleife (450) ferner einen separaten spannungsgesteuerten Oszillator VCO für jeden ADC-Abtasttakt (304) umfasst, wobei jeder VCO Informationen von dem Baudraten-Taktphasenfehlerdetektor (352) verwendet.

11. Empfänger nach Anspruch 9, wobei jeder der Vielzahl von ADC-Abtasttakten (304) dazu konfiguriert ist, ein optisches Signal aus der Vielzahl von separaten optischen Signalen zu empfangen (810), wobei die Vielzahl von separaten optischen Signalen phasengleiche Signale und Quadratursignale umfasst, die jeweils x- und y-Polarisierungen aufweisen.

12. Empfänger nach Anspruch 9, wobei die Ausgabe jedes SISO-Entzerrers (362, 562) in den MIMO-Entzerrer (364, 564) eingegeben wird.

13. Empfänger nach Anspruch 9, wobei die Ausgabe des MIMO-Entzerrers (364, 564) in die Vielzahl von SISO-Entzerrern (362, 562) eingegeben wird.

14. Empfänger nach Anspruch 9, ferner umfassend einen digitalen Niedriggeschwindigkeitssignalprozessor (370) parallel zu dem digitalen Hochgeschwindigkeitssignalprozessor (360), wobei der digitale Niedriggeschwindigkeitssignalprozessor (370) dazu konfiguriert ist, ein blockweises digitales Signalverarbeiten durchzuführen.

15. Empfänger nach Anspruch 14, wobei der digitale

Niedriggeschwindigkeitssignalprozessor (370) dazu konfiguriert ist, mindestens einen von optischen Konstellationsentscheidungsparametern, I/Q-Phasenfehlerkompensationsparametern oder optimalen Entzerrerabgriffskoeffizienten zur Eingabe in den digitalen Hochgeschwindigkeitssignalprozessor (306) zu finden.

Revendications

1. Procédé de traitement de signaux optiques reçus au niveau d'un récepteur cohérent (300), le procédé comprenant :

   la réception (810), au niveau d'une pluralité d'horloges d'échantillonnage ADC de convertisseur analogique-numérique (304), d'une pluralité de signaux séparés (Ix, Qx, Iy, Qy) basés sur les signaux optiques reçus ;
   la réalisation d'un échantillonnage ADC à débit en bauds à chacune de la pluralité d'horloges d'échantillonnage ADC (304) ;
   la fourniture de la pluralité de signaux délivrés en sortie par la pluralité d'horloges d'échantillonnage ADC à un processeur de signal numérique à grande vitesse (360) ;
   la réalisation (820), au niveau du processeur de signal numérique à grande vitesse (360), d'un traitement à haute vitesse de chacun de la pluralité de signaux, dans lequel le traitement à haute vitesse fournissant une égalisation de bande passante et une récupération de polarisation en : traitant les signaux à l'aide de deux types différents d'égaliseurs à valeur réelle ou à valeur mixte, ledit traitement comprend :

      l'entrée de chacun de la pluralité de signaux dans l'un d'une pluralité d'égaliseurs SISO (362, 562) multiprises à valeurs réelles ou mixtes, avec une seule entrée et une seule sortie ; et
      l'entrée de la pluralité de signaux dans un égaliseur MIMO à prise unique et à entrées et sorties multiples (364, 564) à valeur réelle ; et
      l'introduction directe (840) de retards temporels différents dans chacune de la pluralité d'horloges d'échantillonnage ADC (304), comprenant : la détection, par un détecteur d'erreur de phase d'horloge de débit en bauds (352) dans une boucle de récupération d'horloge (350, 450), d'erreurs de phase,
      l'introduction directe de différents retards temporels dans chacune des pluralités d'horloges d'échantillonnage ADC (304) ; et
      l'entrée d'une sortie du processeur de signal numérique à haute vitesse (360) dans le détecteur d'erreur de phase d'horloge de débit en bauds (352).

2. Procédé selon la revendication 1, dans lequel l'introduction directe (840) des différents retards temporels dans chacune de la pluralité d'horloges d'échantillonnage ADC (304) comprend l'utilisation d'une pluralité de tampons d'horloge réglables à retard distincts (380) suivant la distribution d'horloge (358) dans une boucle de récupération d'horloge (350).

3. Procédé selon la revendication 1, dans lequel l'introduction directe (840) des différents retards temporels dans chacune de la pluralité d'horloges d'échantillonnage ADC (304) comprend l'utilisation d'un oscillateur commandé en tension VCO séparé dans une boucle de récupération d'horloge (450) pour chaque horloge d'échantillonnage ADC (304), chaque VCO utilisant des informations provenant d'un détecteur d'erreur de phase d'horloge à débit en bauds commun (352).

4. Procédé selon la revendication 1, dans lequel un signal est reçu (810) par chacune de la pluralité d'horloges d'échantillonnage ADC (304), et dans lequel la pluralité de signaux optiques séparés comprend des signaux en phase et des signaux en quadrature, chacun ayant des polarisations x et y.

5. Procédé selon la revendication 1, dans lequel la sortie de chaque égaliseur SISO (362, 562) est entrée dans l'égaliseur MIMO (364, 564).

6. Procédé selon la revendication 1, dans lequel la sortie de l'égaliseur MIMO (364, 564) est entrée dans la pluralité d'égaliseurs SISO (362, 562).

7. Procédé selon la revendication 1, comprenant également l'exécution d'un processeur de signal numérique à faible vitesse (370) en parallèle avec le processeur de signal numérique à haute vitesse (360), le processeur de signal numérique à faible vitesse (370) effectuant un traitement de signal numérique bloc par bloc.

8. Procédé selon la revendication 7, dans lequel le processeur de signal numérique à faible vitesse (370) trouve au moins l'un des paramètres de décision de constellation optique, des paramètres de compensation d'erreur de phase I/Q ou des coefficients de prise d'égaliseur optimaux pour l'entrée dans le processeur de signal numérique à haute vitesse (360).

9. Récepteur optique cohérent à faible puissance (300), comprenant :

une pluralité d'horloges d'échantillonnage ADC du convertisseur analogique-numérique (304) adaptées pour recevoir (810) une pluralité de signaux distincts (Ix, Qx, Iy, Qy) basés sur les signaux optiques reçus ;
dans lequel chaque horloge d'échantillonnage ADC (304) est configurée pour effectuer un échantillonnage ADC à débit en bauds ;
un processeur de signal numérique à haute vitesse (360) configuré pour effectuer (820) un traitement à grande vitesse de chacun de la pluralité de signaux émis par les horloges d'échantillonnage ADC (304), dans lequel le processeur à haute vitesse (360) est configuré pour fournir une égalisation de bande passante et une récupération de polarisation,
dans lequel le processeur de signal numérique à grande vitesse (360) comprend également deux types différents d'égaliseurs à valeur réelle ou à valeur mixte connectés l'un à l'autre, comprenant :

une pluralité d'égaliseurs SISO multiprises à entrée unique et sortie unique (362, 562) ; et
un égaliseur MIMO simple prise à entrées multiples et sorties multiples (364, 564) ; et un détecteur d'erreur de phase d'horloge de débit en bauds (352) dans une boucle de récupération d'horloge (350, 450) configuré pour introduire directement différents retards temporels dans chacune de la pluralité d'horloges d'échantillonnage ADC (304), dans lequel une sortie du processeur de signal numérique à haute vitesse (360) est entrée dans le détecteur d'erreur de phase d'horloge de débit en bauds (352).

10. Récepteur selon la revendication 9, dans lequel la boucle de récupération d'horloge (350) comprend également une pluralité de tampons d'horloge réglables à retard distincts (380) suivant la distribution d'horloge (358), ou
dans lequel la boucle de récupération d'horloge (450) comprend également un oscillateur commandé en tension VCO séparé pour chaque horloge d'échantillonnage ADC (304), chaque VCO utilisant des informations provenant du détecteur d'erreur de phase d'horloge de débit en bauds (352).

11. Récepteur selon la revendication 9, dans lequel chacune de la pluralité d'horloges d'échantillonnage ADC (304) est configurée pour recevoir (810) un signal optique de la pluralité de signaux optiques séparés, la pluralité de signaux optiques séparés comportant des signaux en phase et des signaux en quadrature, chacun ayant des polarisations x et y.

12. Récepteur selon la revendication 9, dans lequel la sortie de chacun des égaliseurs SISO (362, 562) est entrée dans l'égaliseur MIMO (364, 564).

13. Récepteur selon la revendication 9, dans lequel la sortie de l'égaliseur MIMO (364, 564) est entrée dans la pluralité d'égaliseurs SISO (362, 562).

14. Récepteur selon la revendication 9, comprenant également un processeur de signal numérique à faible vitesse (370) en parallèle avec le processeur de signal numérique à haute vitesse (360), dans lequel le processeur de signal numérique à faible vitesse (370) est configuré pour effectuer un traitement de signal numérique bloc par bloc.

15. Récepteur selon la revendication 14, dans lequel le processeur de signal numérique à faible vitesse (370) est configuré pour trouver au moins l'un des paramètres de décision de constellation optique, des paramètres de compensation d'erreur de phase I/Q ou des coefficients de prise d'égaliseur optimaux pour l'entrée dans le processeur de signal numérique à haute vitesse (306).

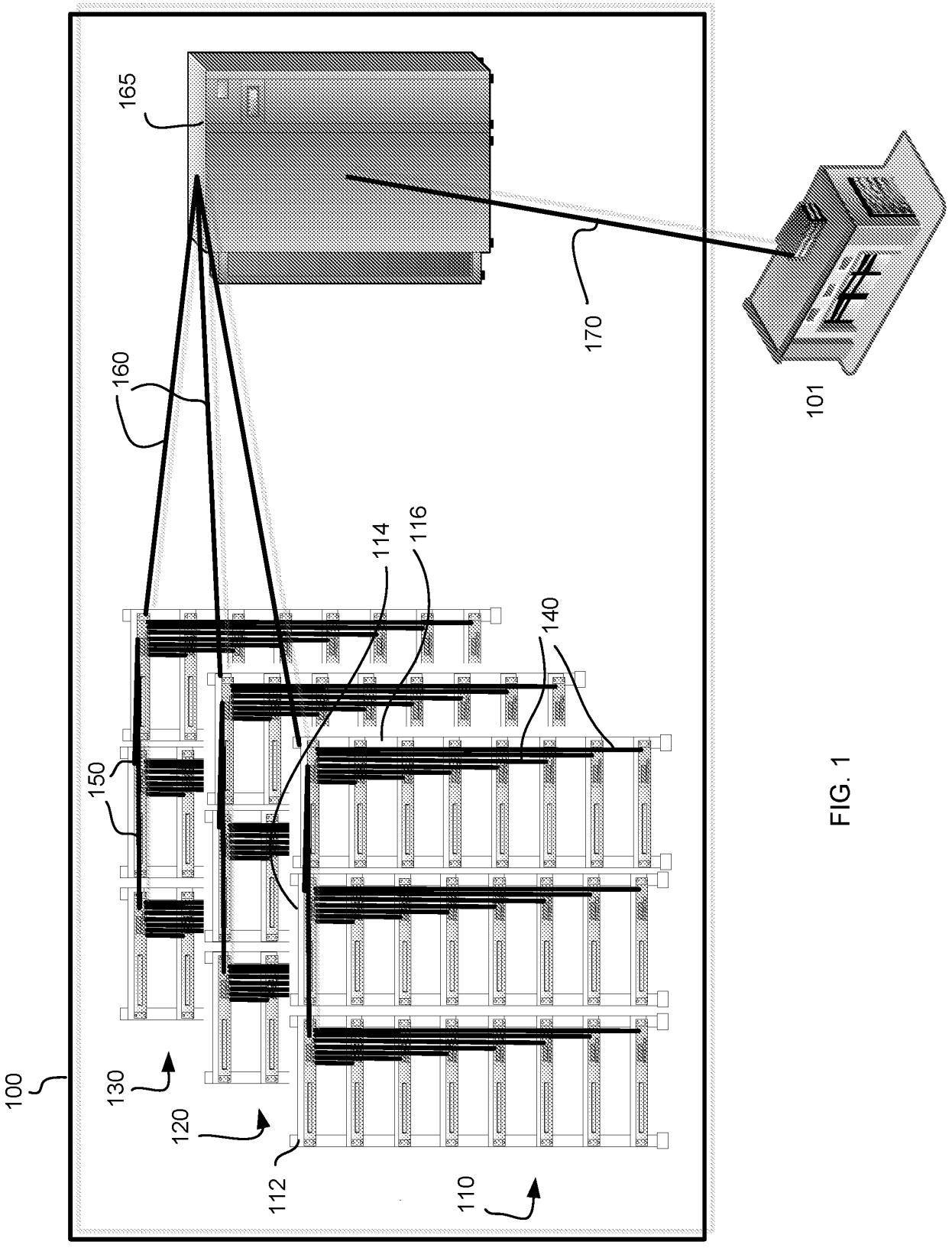

FIG. 1

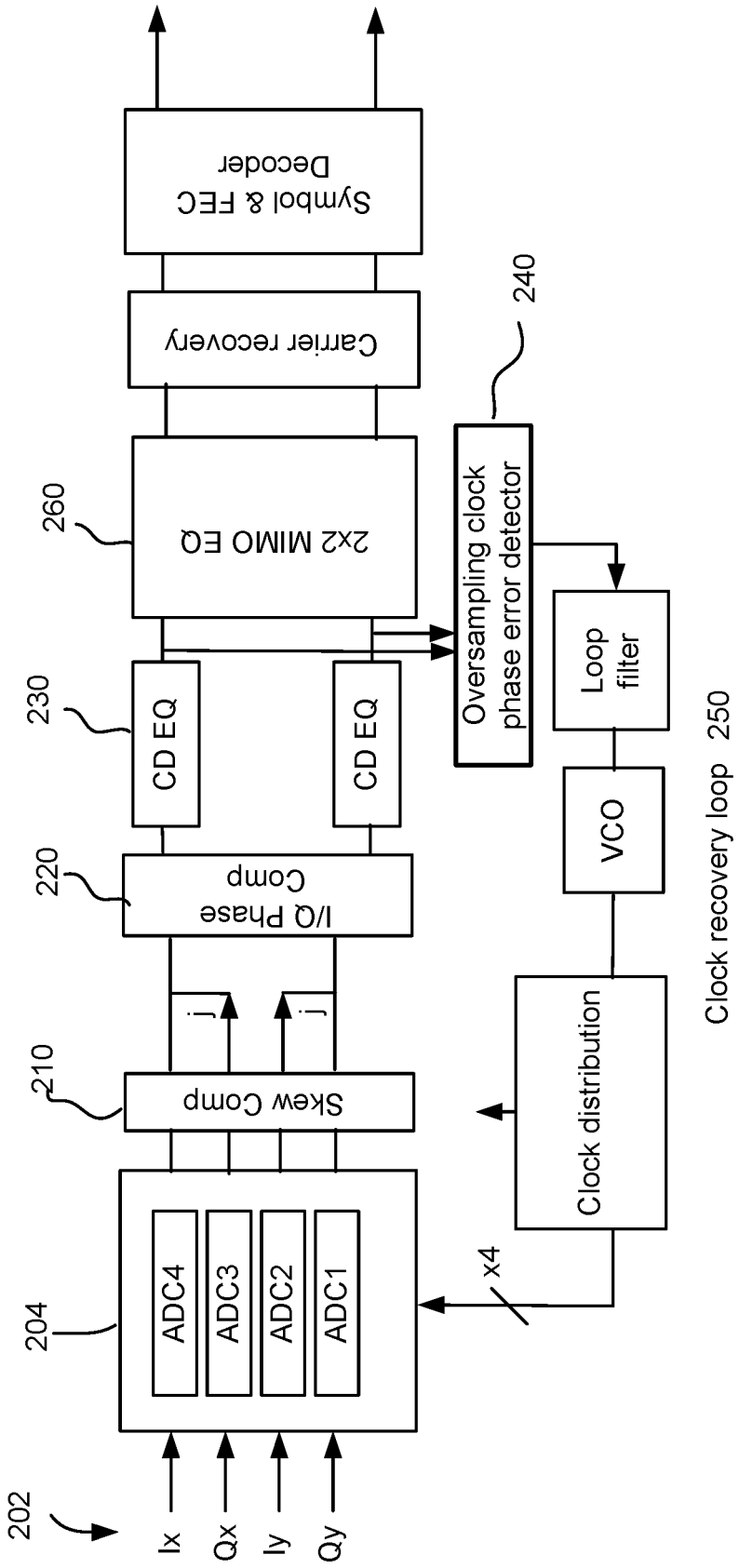

FIG. 2
(Prior Art)

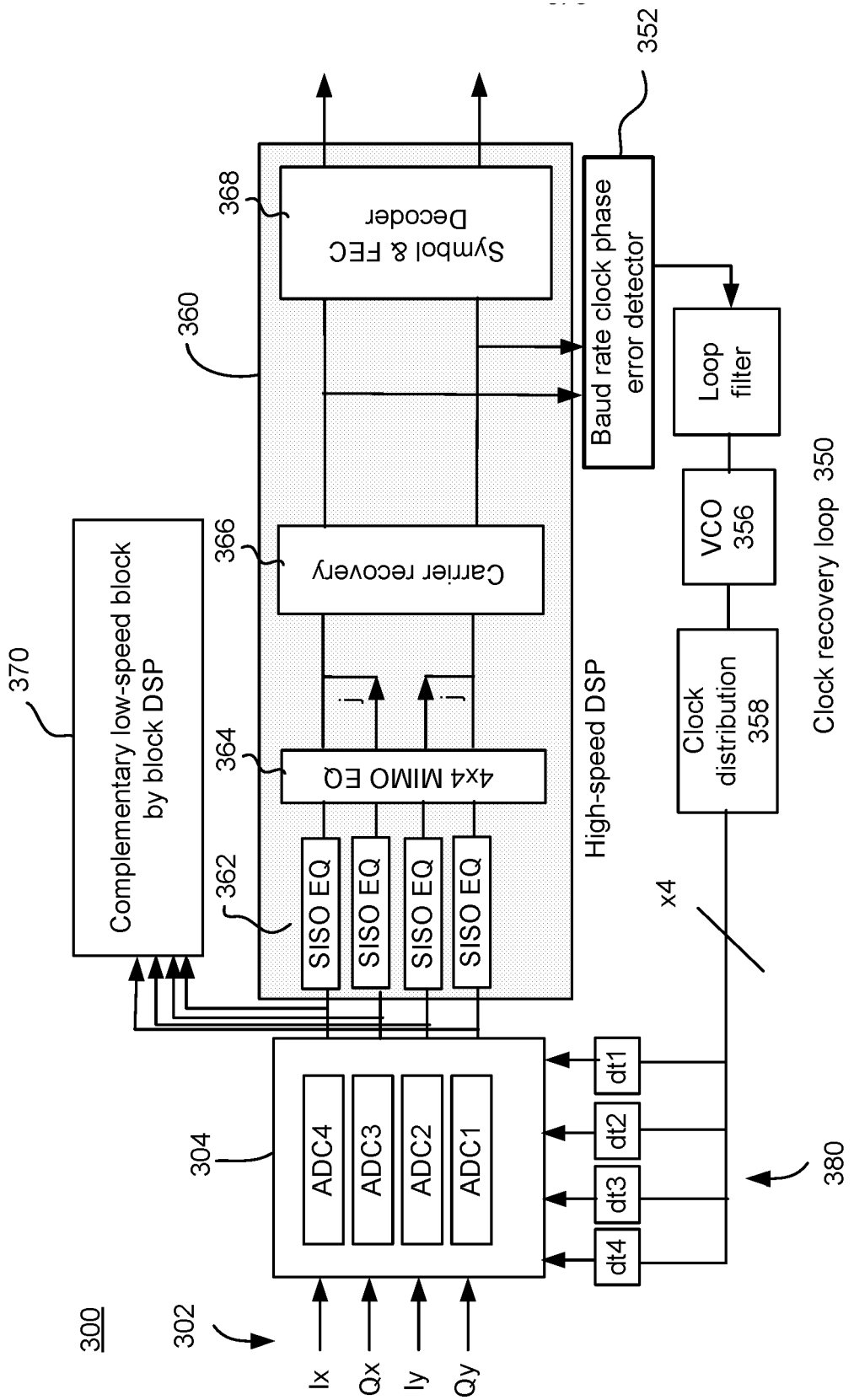
300
302
Ix
Qx
Iy
Qy
304
ADC4
ADC3
ADC2
ADC1
dt1
dt2
dt3
dt4
380
x4
Clock distribution 358
VCO 356
Loop filter
Clock recovery loop 350
352
Baud rate clock phase error detector
High-speed DSP
362
SISO EQ
SISO EQ
SISO EQ
SISO EQ
364
4x4 MIMO EQ
j
j
366
Carrier recovery
360
368
Symbol & FEC Decoder
370
Complementary low-speed block by block DSP

FIG. 3

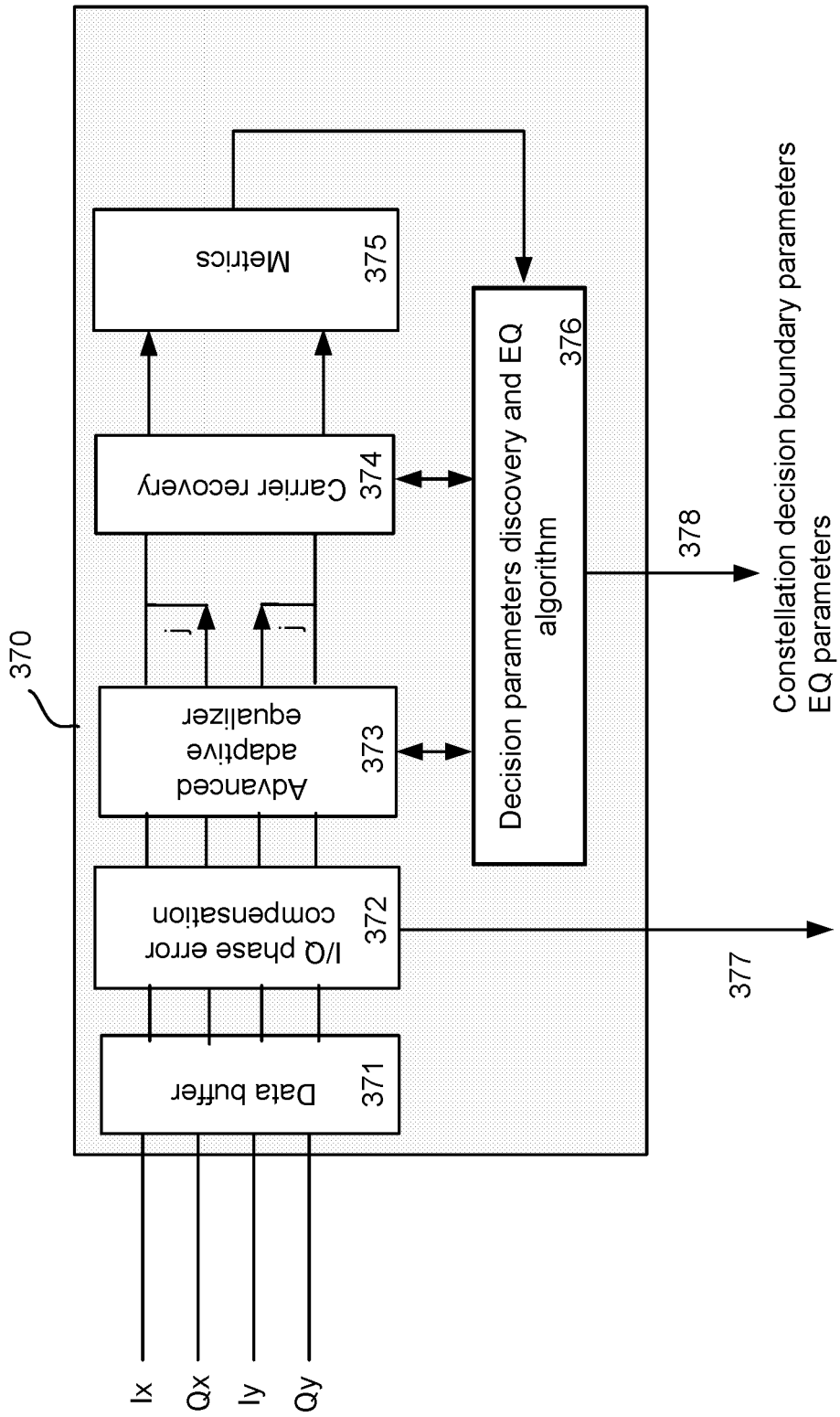
370
Data buffer
371
I/Q phase error compensation
372
Advanced adaptive equalizer
373
Carrier recovery
374
Metrics
375
Decision parameters discovery and EQ algorithm
376
j
j
Ix
Qx
Iy
Qy
377
378
I/Q phase error compensation parameters
Constellation decision boundary parameters
EQ parameters

FIG. 4

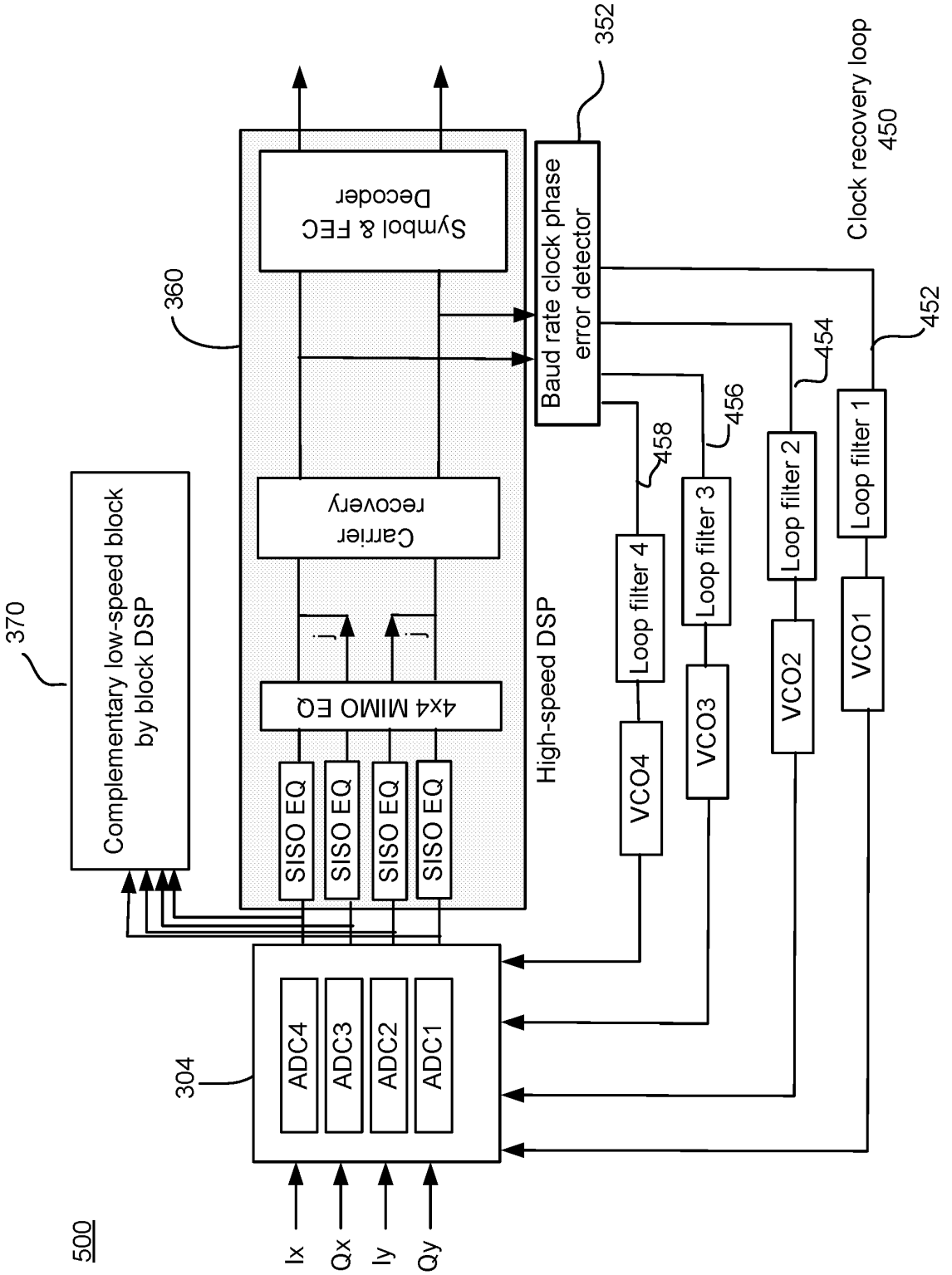
500
Ix
Qx
Iy
Qy
304
ADC4
ADC3
ADC2
ADC1
SISO EQ
SISO EQ
SISO EQ
SISO EQ
4x4 MIMO EQ
Carrier recovery
Symbol & FEC Decoder
360
High-speed DSP
Complementary low-speed block by block DSP
370
Baud rate clock phase error detector
352
Clock recovery loop
450
VCO4
VCO3
VCO2
VCO1
Loop filter 4
Loop filter 3
Loop filter 2
Loop filter 1
458
456
454
452

FIG. 5

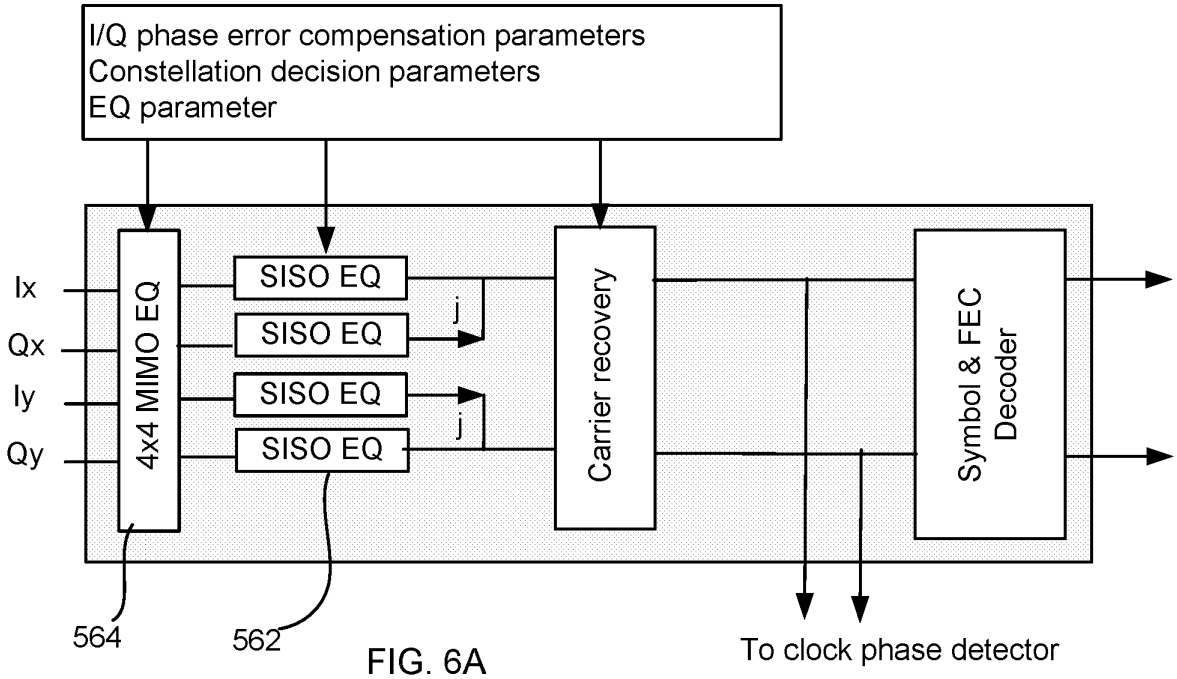
I/Q phase error compensation parameters
Constellation decision parameters
EQ parameter
Ix
Qx
Iy
Qy
4x4 MIMO EQ
SISO EQ
SISO EQ
SISO EQ
SISO EQ
j
j
Carrier recovery
Symbol & FEC Decoder
564
562
To clock phase detector

FIG. 6A

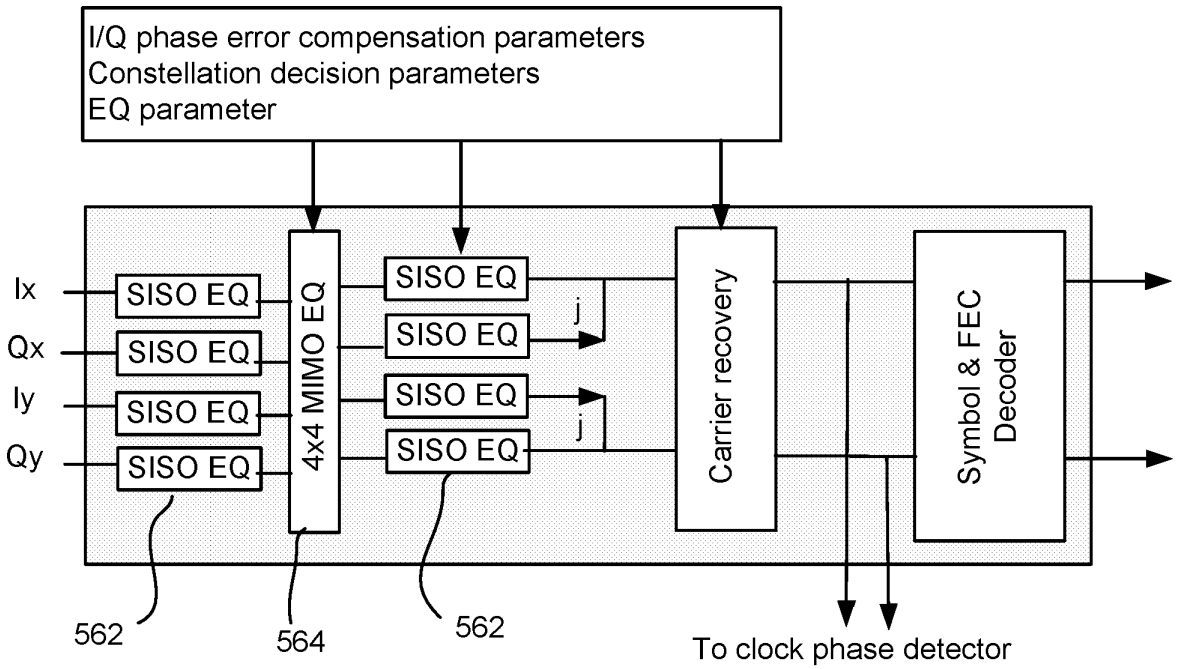
I/Q phase error compensation parameters
Constellation decision parameters
EQ parameter
Ix
Qx
Iy
Qy
SISO EQ
SISO EQ
SISO EQ
SISO EQ
4x4 MIMO EQ
SISO EQ
SISO EQ
SISO EQ
SISO EQ
j
j
Carrier recovery
Symbol & FEC Decoder
562
564
562
To clock phase detector

FIG. 6B

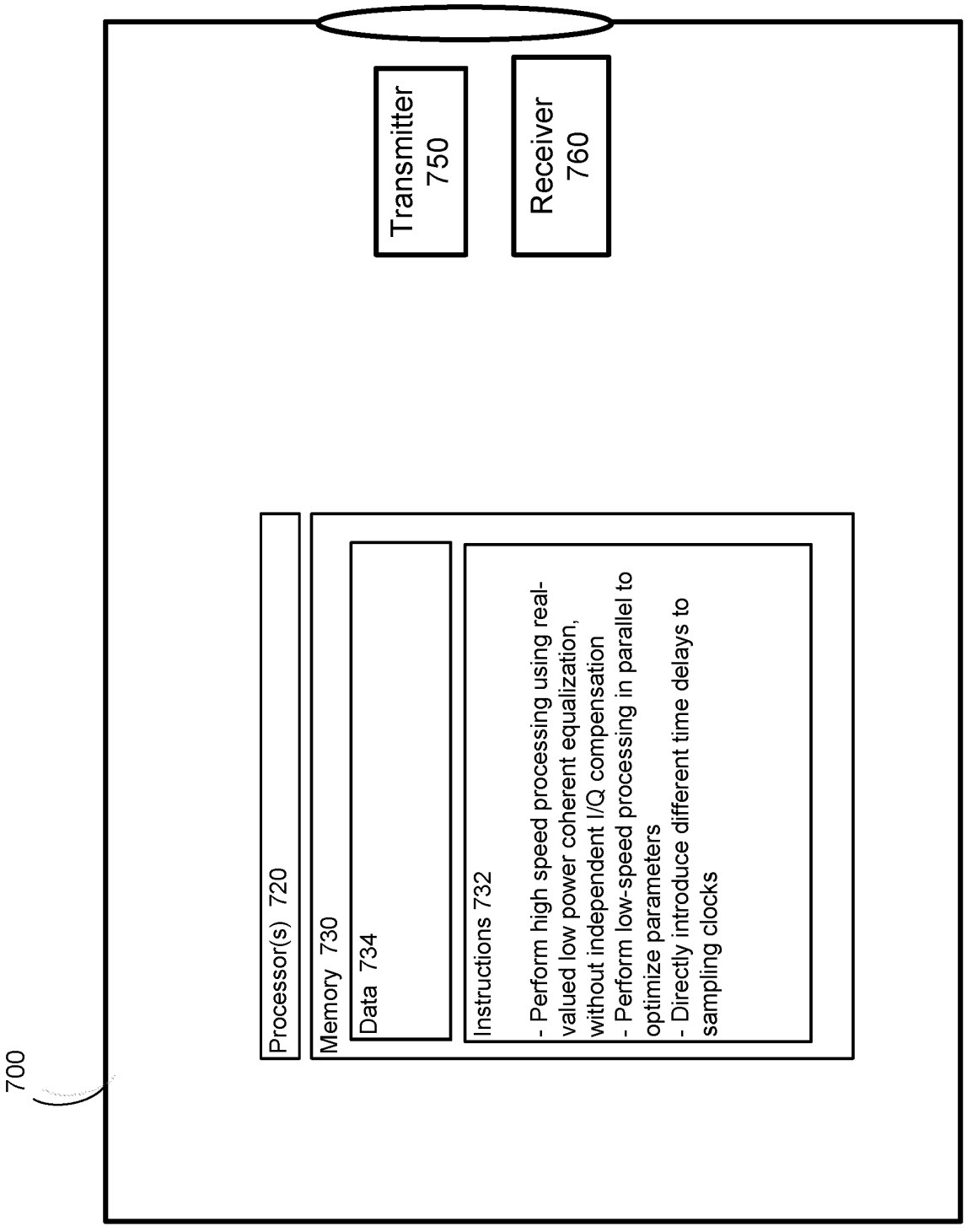
700
Processor(s) 720
Memory 730
Data 734
Instructions 732
- Perform high speed processing using real-valued low power coherent equalization, without independent I/Q compensation
- Perform low-speed processing in parallel to optimize parameters
- Directly introduce different time delays to sampling clocks
Transmitter 750
Receiver 760

FIG. 7

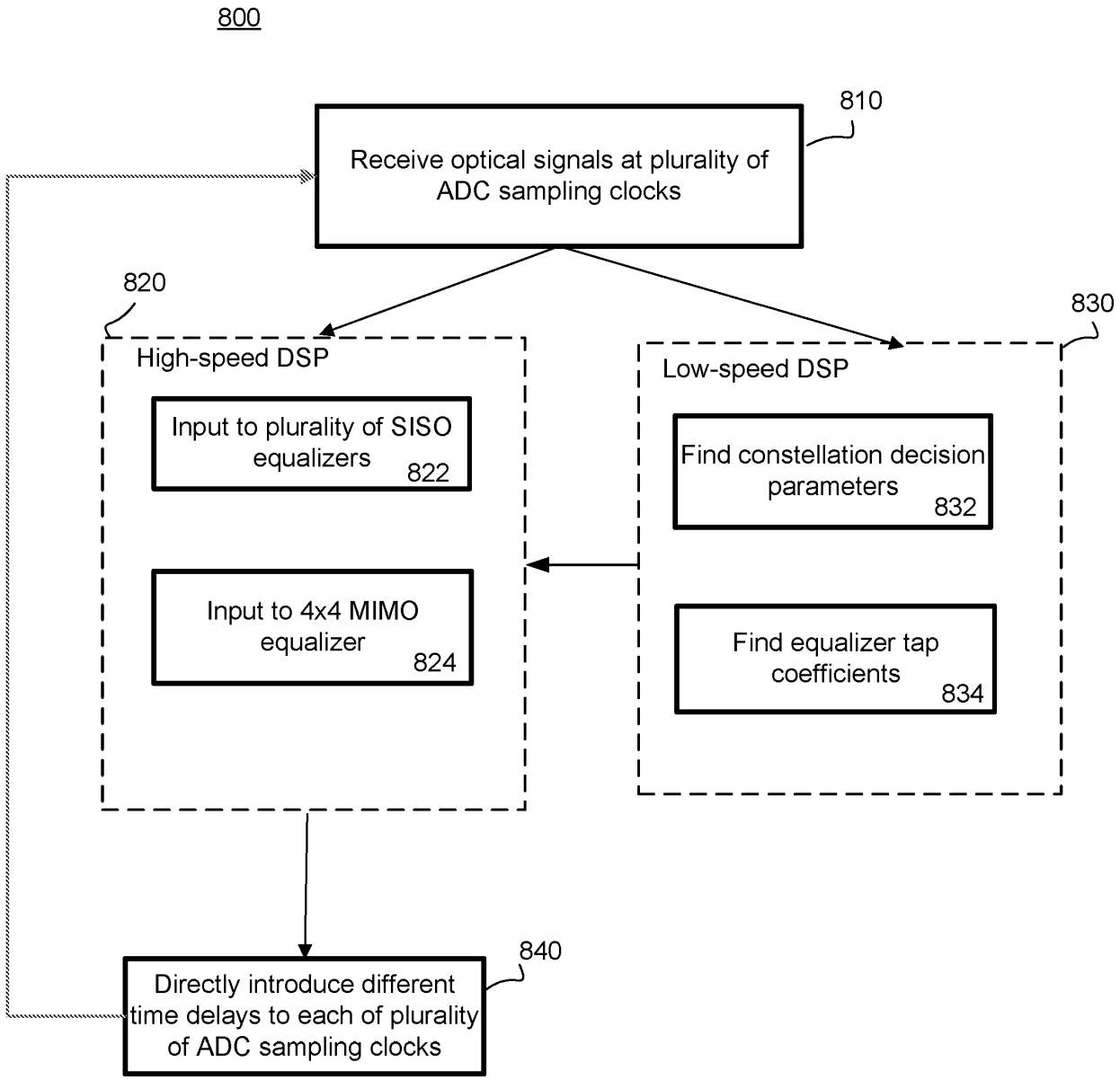
800
Receive optical signals at plurality of ADC sampling clocks
810
820
High-speed DSP
Input to plurality of SISO equalizers
822
Input to 4x4 MIMO equalizer
824
830
Low-speed DSP
Find constellation decision parameters
832
Find equalizer tap coefficients
834
840
Directly introduce different time delays to each of plurality of ADC sampling clocks

Fig. 8

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 42166619 **[0001]**
- US 9240843 B1 **[0005]**
- US 9036751 B1 **[0006]**
- WO 2014194940 A1 **[0007]**