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Chee et al.

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(54) **RADIO FREQUENCY FRONT END SYSTEM WITH AN INTEGRATED TRANSMIT/RECEIVE SWITCH**

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Related U.S. Application Data

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(51) **Int. Cl.**

H04B 1/44	(2006.01)
H04B 1/48	(2006.01)
H04B 1/525	(2015.01)

(52) **U.S. Cl.**

CPC ***H04B 1/48*** (2013.01); ***H04B 1/525*** (2013.01); *Y10T 29/49018* (2015.01)

(58) **Field of Classification Search**

CPC H04B 1/44; H04B 1/48; H04B 1/525
USPC 455/82, 83
See application file for complete search history.

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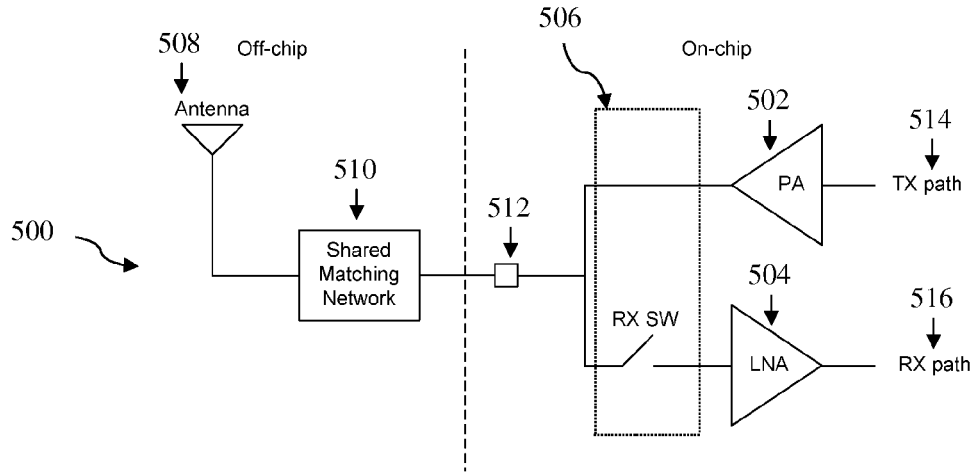
(57) **ABSTRACT**

A Radio Frequency (RF) front end system and method are disclosed. The RF front end system comprises an antenna, a matching network coupled to the antenna, a power amplifier (PA) coupled to the matching network via a port on a transmit path, a low noise amplifier (LNA) coupled to the matching network via the port on a receive path and at least one transmit/receive switch (T/R SW) coupled between the port and at least one of the PA and LNA.

18 Claims, 9 Drawing Sheets



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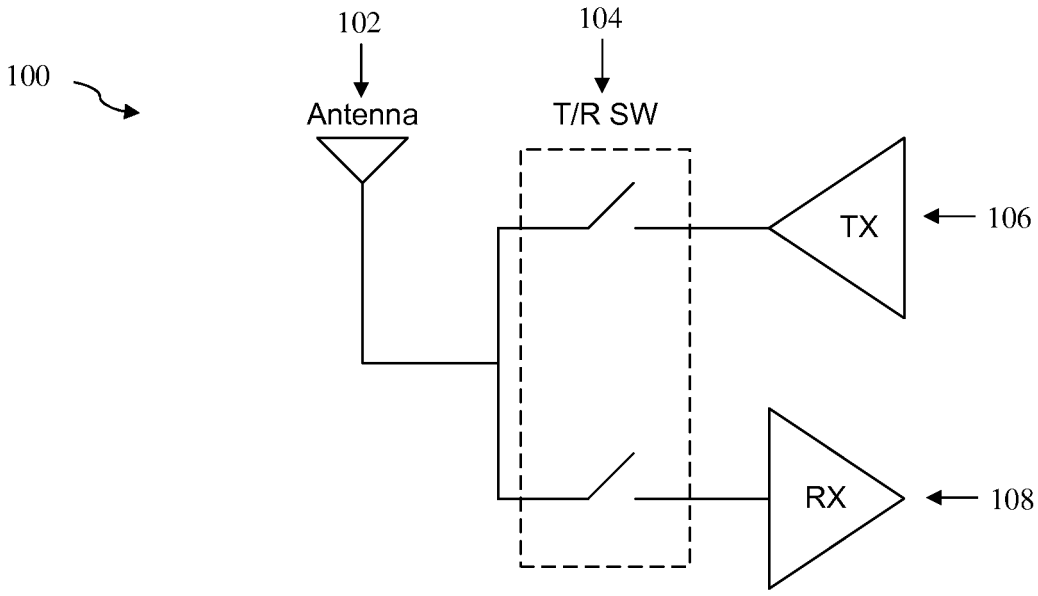


Figure 1
Prior Art

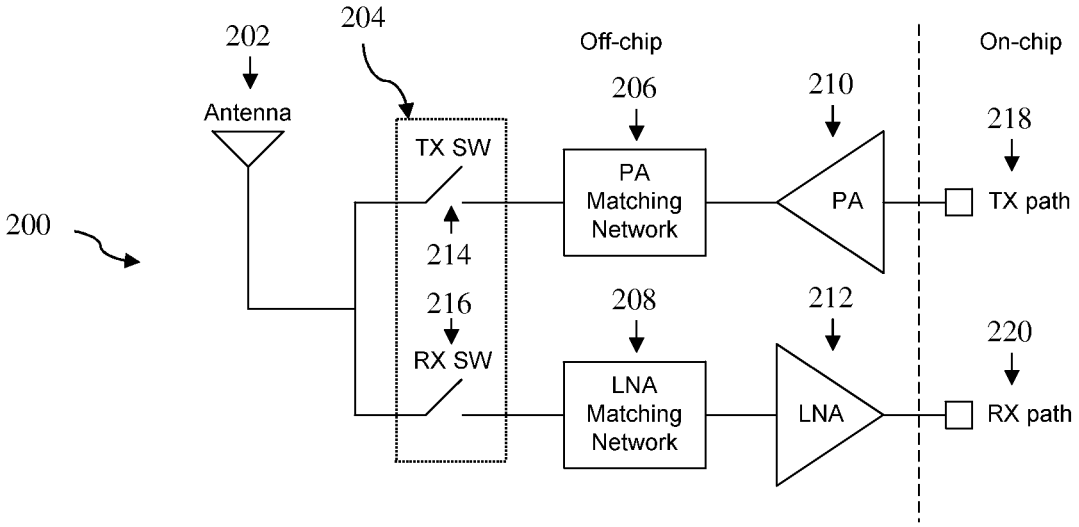


Figure 2

Prior Art

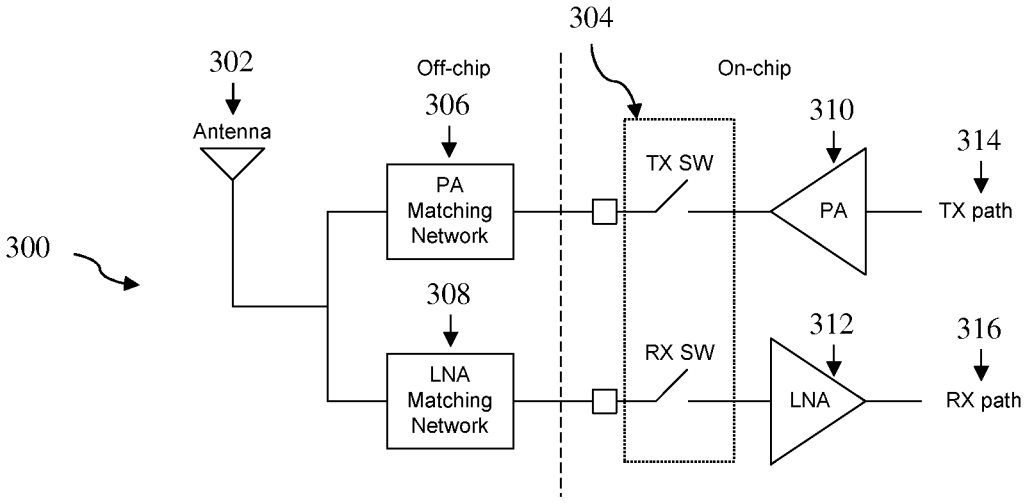


Figure 3

Prior Art

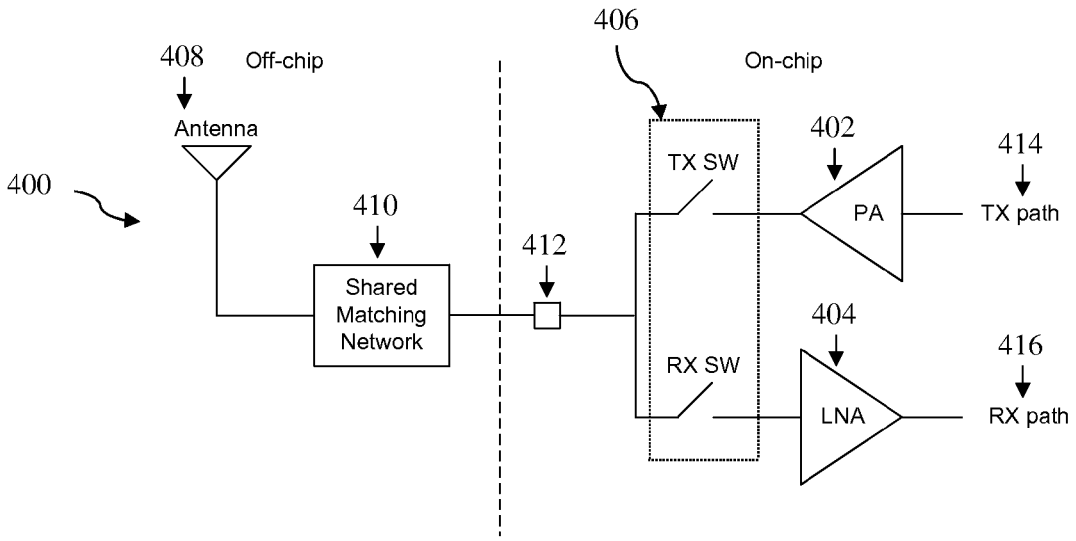

406
408
Off-chip
On-chip
Antenna
402
414
TX SW
400
PA
TX path
410
412
Shared
Matching
Network
404
416
RX SW
LNA
RX path

Figure 4

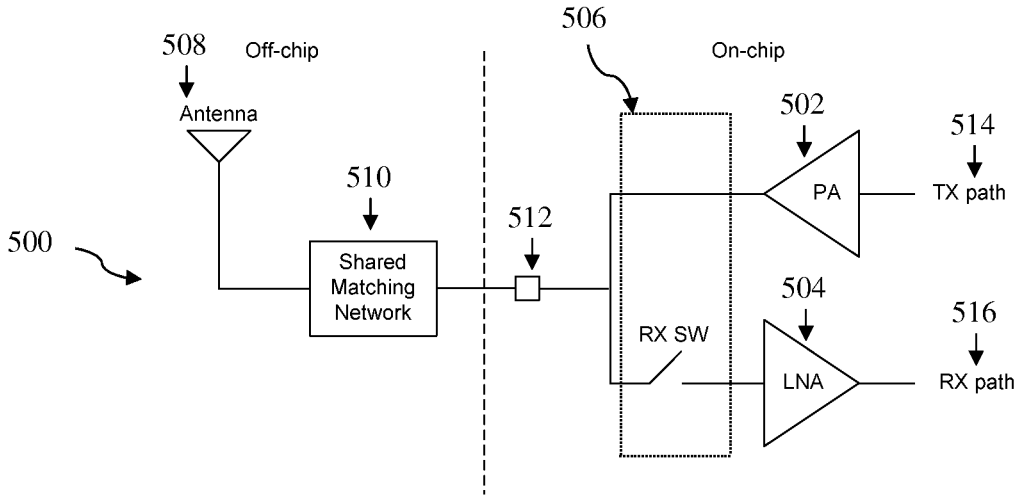

506
508
Off-chip
On-chip
Antenna
502
514
PA
TX path
510
500
512
Shared
Matching
Network
504
516
RX SW
LNA
RX path

Figure 5

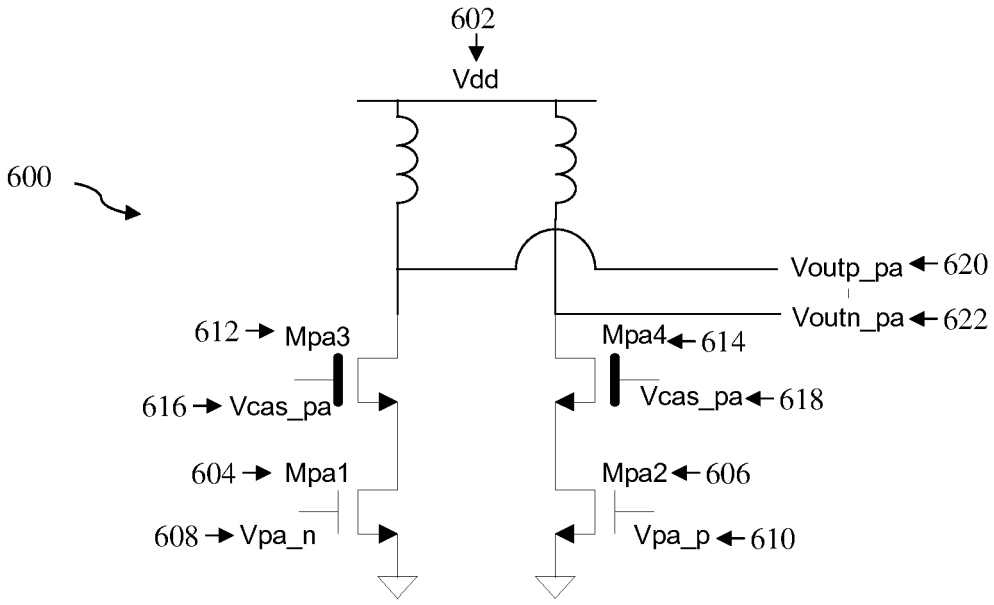

602
Vdd
600
Voutp_pa
620
Voutn_pa
622
612
Mpa3
Mpa4
614
616
Vcas_pa
Vcas_pa
618
604
Mpa1
Mpa2
606
608
Vpa_n
Vpa_p
610

Figure 6

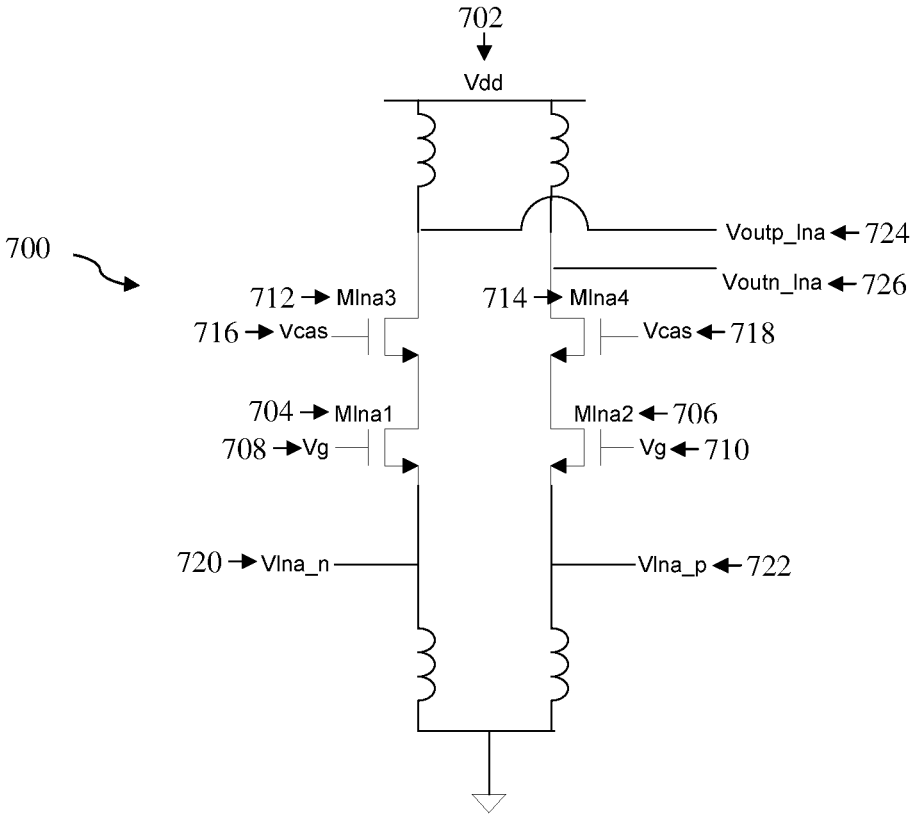

702
Vdd
700
Voutp_lna 724
Voutn_lna 726
712 Mlna3
714 Mlna4
716 Vcas
Vcas 718
704 Mlna1
Mlna2 706
708 Vg
Vg 710
720 Vlna_n
Vlna_p 722

Figure 7

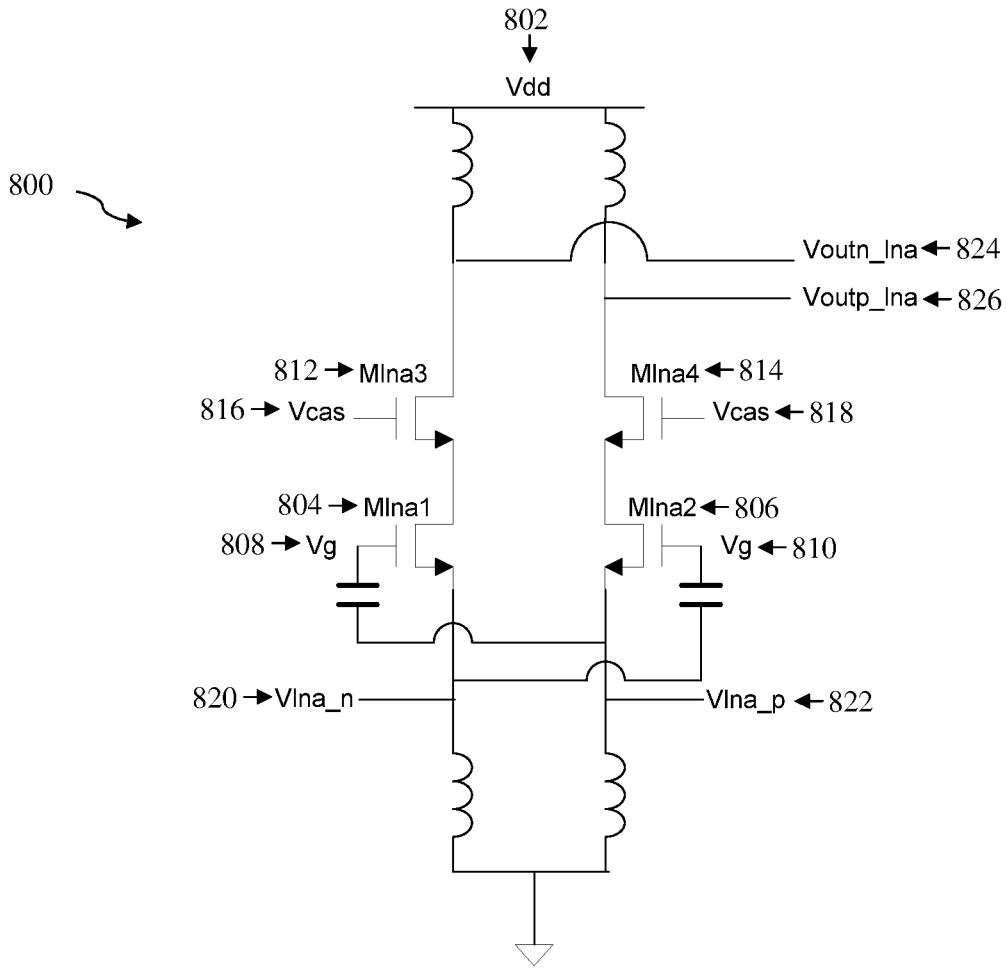
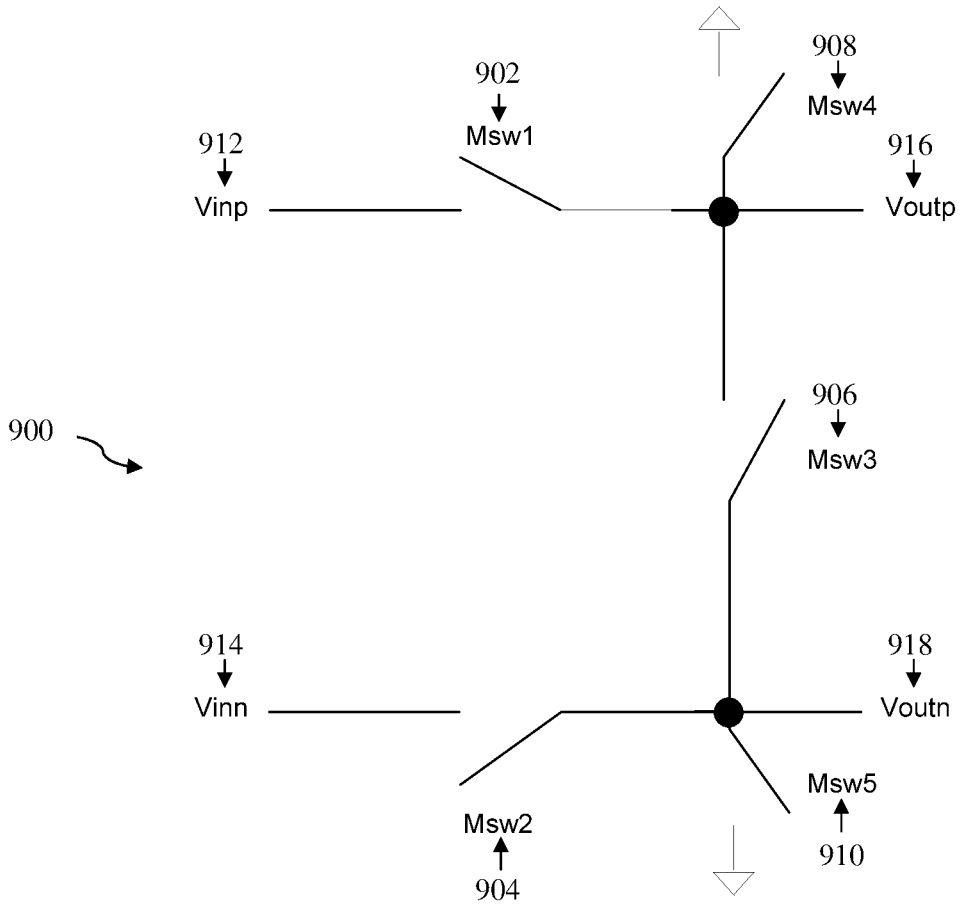

802
Vdd
800
Voutn_lna 824
Voutp_lna 826
812 Mlna3
Mlna4 814
816 Vcas
Vcas 818
804 Mlna1
Mlna2 806
808 Vg
Vg 810
820 Vlna_n
Vlna_p 822

Figure 8


900
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Msw1
904
Msw2
906
Msw3
908
Msw4
910
Msw5
912
Vinp
914
Vinn
916
Voutp
918
Voutn

Figure 9

RADIO FREQUENCY FRONT END SYSTEM WITH AN INTEGRATED TRANSMIT/RECEIVE SWITCH

CROSS-REFERENCE TO RELATED APPLICATION

Under 35 U.S.C. §120 the present application is a continuation of U.S. Pat. Ser. No. 13/204,544, filed Aug. 5, 2011, entitled "RADIO FREQUENCY FRONT END SYSTEM WITH AN INTEGRATED TRANSMIT/RECEIVE SWITCH" which is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates to a Radio Frequency (RF) front end system, and more particularly, to a RF front end system utilized in a transceiver system.

BACKGROUND

Some conventional transceivers do not isolate transmitters from receivers to allow for independent optimization of the transmitters and receivers. Other conventional transceivers integrate Radio Frequency (RF) front end components off-chip to isolate transmitters from receivers which increases the cost and size of the RF front end systems. Accordingly, what is desired is to provide a system and method that overcomes the above issues. The present invention addresses such a need.

SUMMARY OF THE INVENTION

A Radio Frequency (RF) front end system and method are disclosed. The RF front end system comprises an antenna, a matching network coupled to the antenna, a power amplifier (PA) coupled to the matching network via a port on a transmit path, a low noise amplifier (LNA) coupled to the matching network via the port on a receive path and at least one transmit/receive switch (T/R SW) coupled between the port and at least one of the PA and LNA.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings illustrate several embodiments of the invention and, together with the description, serve to explain the principles of the invention. One of ordinary skill in the art will recognize that the particular embodiments illustrated in the drawings are merely exemplary, and are not intended to limit the scope of the present invention.

FIG. **1** illustrates a conventional time division duplexing (TDD) transceiver front end system.

FIG. **2** illustrates an existing transmit/receive switch (T/R SW) implementation.

FIG. **3** illustrates another existing T/R SW implementation.

FIG. **4** illustrates a proposed T/R SW implementation in accordance with an embodiment.

FIG. **5** illustrates a proposed T/R SW implementation with a TX SW integrated with an output stage of the PA in accordance with an embodiment.

FIG. **6** illustrates an output stage of the PA in accordance with an embodiment.

FIG. **7** illustrates a common-gate LNA in accordance with an embodiment.

FIG. **8** illustrates a cross-coupled common-gate LNA in accordance with an embodiment.

FIG. **9** illustrates an integrated T/R SW in accordance with an embodiment.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention relates to a Radio Frequency (RF) front end system, and more particularly, to a RF front end system utilized in a transceiver system. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiments shown but is to be accorded the widest scope consistent with the principles and features described herein.

A Radio Frequency (RF) front end system and method are disclosed. The RF front end system comprises an antenna, a matching network coupled to the antenna, a power amplifier (PA) coupled to the matching network via a port on a transmit path, a low noise amplifier (LNA) coupled to the matching network via the port on a receive path and at least one transmit/receive switch (T/R SW) coupled between the port and at least one of the PA and LNA. In so doing, a more robust integrated T/R SW solution is achieved and the cost, size and package pin count of the RF front end is further reduced. To describe the features of the present invention in more detail, refer now to the following description in conjunction with the accompanying Figures.

In a conventional time division duplexing (TDD) transceiver front end system, a T/R SW is used to share the antenna between a transmitter and receiver. FIG. **1** illustrates a conventional TDD transceiver front end system **100** that includes an antenna **102**, a T/R SW **104**, a transmitter (TX) **106**, and a receiver (RX) **108**. However, in this conventional TDD transceiver front end system **100**, the transmitter **106** and the receiver **108** may not be optimized with the antenna impedance.

To address this problem, FIG. **2** illustrates an existing transceiver front end system **200** that includes an antenna **202**, a T/R SW **204**, a PA matching network **206**, a LNA matching network **208**, a power amplifier (PA) **210** and a low noise amplifier (LNA) **212** that are all integrated as off-chip components. During receive, the transmit switch (TX SW) **214** is open and the receive switch (RX SW) **216** is closed which connects the antenna **202** to the receive path (RX path) **220** and isolates the transmit path (TX path) **218** from the RX path **220**. During transmit, the TX SW **214** is closed and the RX SW **216** is open which connects the antenna **202** to the TX path **218** and isolates the RX **220** path from the TX path **218**.

Thus, in this transceiver front end system **200**, the T/R SW **204** allows the antenna **202** to be shared between the TX path **218** and RX path **220** while providing isolation between them. With the TX path **218** isolated from the RX path **220**, the PA matching network **206** and the LNA matching network **208** can each be optimized independently for the PA **210** and the LNA **212** respectively. However, in this transceiver front end system **200**, the RF front end components, including the T/R SW **204**, PA **210** and LNA **212**, are integrated off-chip which increases the cost and size of the RF front end.

To address this problem and reduce the cost and size of the RF front end, FIG. **3** illustrates another existing transceiver front end system **300** that includes an antenna **302**, a T/R SW **304**, a PA matching network **306**, a LNA matching network **308**, a PA **310**, a LNA **312**, a TX path **314** and a RX path **316**. In this transceiver front end system **300**, the RF front end components, including the T/R SW **304**, PA **310** and LNA **312**, are integrated on-chip. In this transceiver front end system **300**, the PA **310** and the LNA **312** have their own matching networks **306** and **308** that interact with each other. The PA **310** and its matching network **306** loads the RX path **316** during receive and the LNA **312** and its matching network **308** loads the TX path **314** during transmit. However, in this transceiver front end system **300**, it is difficult to achieve a robust matching network that is optimized for both the PA **310** and the LNA **312** without significant performance degradation.

The present invention addresses these drawbacks. FIG. **4** illustrates a transceiver front end system **400** that includes a PA **402**, LNA **404** and T/R SW **406** integrated on-chip and an antenna **408** and matching network **410** integrated off-chip. In the transceiver front end system **400**, the PA **402** and LNA **404** are combined together at a port **412** and share the same matching network **410**. In order to share the same matching network **410** and package pin, the PA **402** and LNA **404** are designed with similar optimal impedance. In another embodiment, the port **412** is a single RF port. In the transceiver front end system **400**, the T/R SW **406** isolates the TX path **414** from the RX path **416** to minimize the loading on each other.

It is understood that the transceiver front end system **400** may result in switch loss in the TX path **414**. FIG. **5** illustrates another transceiver front end system **500** that includes a PA **502**, LNA **504** and T/R SW **506** integrated on-chip and an antenna **508** and matching networking **510** integrated off-chip. In the transceiver front end system **500**, the PA **502** and LNA **504** are combined together at a port **512** and share the same matching network **510**. In order to share the same matching network **510** and package pin, the PA **502** and LNA **504** are designed with similar optimal impedance. In another embodiment, the port **512** is a single RF port. In the transceiver front end system **500**, the switch loss in the TX path **514** is eliminated by integrating the TX SW with the output stage of the PA **502**.

FIG. **6** illustrates one implementation of such output stage of the PA **600**. The output stage of the PA **600** includes an integrated circuit (IC) power supply pin Vdd **602**, input devices Mpa**1** **604** and Mpa**2** **606**, voltages Vpa_n **608** and Vpa_p **610** corresponding to the input devices Mpa**1** **604** and Mpa**2** **606**, cascode devices Mpa**3** **612** and Mpa**4** **614**, voltages Vcas_pa **616** and Vcas_pa **618** corresponding to the cascode devices Mpa**3** **612** and Mpa**4** **614**, and differential output signals Voutp_pa **620** and Voutn_pa **622**.

In the output stage of the PA **600**, the IC power supply pin Vdd **602** is differentially coupled to the input devices Mpa**1** **604** and Mpa**2** **606** and to the cascode devices Mpa**3** **612** and Mpa**4** **614**. In the output stage of the PA **600**, input device Mpa**1** **604** is in series with cascode device Mpa**3** **612** and input device Mpa**2** **606** is in series with cascode device Mpa**4** **614**. Furthermore, input device Mpal **604** and cascade device Mpa**3** **612** provide differential output signal Voutn_pa **622** and input device Mpa**2** **606** and cascade device Mpa**4** **614** provide differential output signal Voutp_pa **620**.

The input devices Mpa**1** **604** and Mpa**2** **606** can be made of a variety of materials including but not limited to thin oxide devices to provide a large transconductance. The cascode devices Mpa**3** **612** and Mpa**4** **614** can also be made of a variety of materials including but not limited to thick oxide devices to provide isolation between the input and output and prevent device breakdown due to the large output swing. The cascode devices Mpa**3** **612** and Mpa**4** **614** also function as the TX SW to isolate the TX path from the RX path when Vcas_pa is pulled low. The output stage of the PA **600** illustrates a differential version of the PA. In another embodiment, the output stage of the PA **600** can be applied to a single-ended version of the PA.

As previously mentioned, the PA and LNA in FIGS. **4** and **5** are designed with similar optimal impedance to allow the PA and LNA to share the same matching network. However, a common source inductive degenerated LNA typically has a much higher optimal impedance than the optimal impedance of a PA. Thus, in one embodiment, the present invention utilizes a common-gate LNA because the common-gate LNA has a similar optimal impedance as the PA.

FIG. **7** illustrates a common-gate LNA **700** that includes an IC power supply pin Vdd **702**, input devices Mlna**1** **704** and Mlna**2** **706**, voltages Vg **708** and Vg **710** corresponding to the input devices Mal **704** and Mlna**2** **706**, cascode devices Mlna**3** **712** and Mlna**4** **714**, voltages Vcas **716** and Vcas **718** corresponding to the cascode devices Mlna**3** **712** and Mina **714**, input signals Vlna_n **720** and Vlna_p **722**, and differential output signals Voutp_lna **724** and Voutn_lna **726**.

In the common-gate LNA **700**, the IC power supply pin Vdd **702** is differentially coupled to the input devices Mlna**1** **704** and Mlna**2** **706** and to the cascode devices Mlna**3** **712** and Mlan**4** **714**. In the common-gate LNA **700**, input device Mlna**1** **704** is in series with cascode device Mlna**3** **712** and input device Mlna**2** **706** is in series with cascode device Mlna**4** **714**. Furthermore, input device Mlna**1** **704** and cascade device Mlna**3** **712** provide differential output signal Voutn_lna **726** and input device Mlna**2** **706** and cascade device Mlna**4** **714** provide differential output signal Voutp_lna **724**.

In the common-gate LNA **700**, the input impedance is inversely proportional to the transconductance of the input devices Mlna**1** **704** and Mlna**2** **706**. The transconductance of the input devices Mlna**1** **704** and Mlna**2** **706** can be set to a variety of settings including but not limited to a common RF port impedance. Additionally, the cascode devices Mlna**3** **712** and Mlna**4** **714** are used to isolate the input from the output. The common-gate LNA **700** illustrates a differential version of the LNA. In another embodiment, the common-gate LNA **700** can be applied to a single-ended version of the LNA.

One of ordinary skill in the art readily recognizes that other implementations of a LNA that includes a similar optimal impedance to a PA may be utilized and that would be within the spirit and scope of the present invention. FIG. **8** illustrates another implementation of the LNA as a cross-coupled common-gate LNA **800** that includes an IC power supply pin Vdd **802**, input devices Mlna**1** **804** and Mlna**2** **806**, voltages Vg **808** and Vg **810** corresponding to the input devices Mlna**1** **804** and Mlna**2** **806**, cascode devices Mlna**3** **812** and Mlna**4** **814**, voltages Vcas **816** and Vcas **818** corresponding to the cascode devices Mlna**3** **812** and Mina **814**, input signals Vlna_n **820** and Vlna_p **822**, and differential output signals Voutn_lna **824** and Voutp_lna **826**.

In the cross-coupled gate LNA **800**, the IC power supply pin Vdd **802** is differentially coupled to the input devices Mlna**1** **804** and Mlna**2** **806** and to the cascode devices Mlna**3** **812** and Mlan**4** **814**. In the cross-coupled gate LNA **800**, input device Mlna**1** **804** is in series with cascode device Mlna**3** **812** and input device Mlna**2** **806** is in series with

cascode device Mlna4 **814**. Furthermore, input device Mlna1 **804** and cascode device Mlna3 **812** provide differential output signal Voutn_lna **824** and input device Mlna2 **806** and cascode device Mlna4 **814** provide differential output signal Voutp_lna **826**.

In the cross-coupled common-gate LNA **800**, the input signal Vlna_p **822** is fed to the gate of Mlna1 **804** and the source of Mlna2 **806** and the input signal Vlna_n **820** is fed to the gate of Mlna2 **806** and the source of Mlna1 **804**. The cross-coupled common-gate LNA **800** illustrates a differential version of the LNA. In another embodiment, the cross-coupled common-gate LNA **800** can be applied to a single-ended version of the LNA.

In another embodiment, a common source LNA with feedback implementation is utilized. The feedback reduces the optimal input impedance of a common source LNA to a level that is similar to the optimal impedance of the PA.

One of ordinary skill in the art readily recognizes that the present invention may utilize various implementations of an integrated transmit/receive switch (T/R SW) and that would be within the spirit and scope of the present invention. FIG. **9** illustrates an integrated transmit/receive switch (T/R SW) **900** that includes series transistors Msw1 **902** and Msw2 **904**, shunt transistors Msw3 **906**, Msw4 **908** and Msw5 **910**, input signals Vinp **912** and Vinn **914** and output signals Voutp **916** and Voutn **918**. Shunt transistor Msw3 **906** shunts the differential mode signal whereas shunt transistors Msw4 **908** and Msw5 **910** shunt both the common mode and differential mode signals.

When integrated T/R SW **900** is on, shunt transistors Msw3-5 **906-910** are off and series transistors Msw1-2 **902-904** are on to allow the input signals Vinp **912** and Vinn **914** to pass through the integrated T/R SW **900** to the output with minimal loss. When integrated T/R SW **900** is off, shunt transistors Msw 1-2 **902-904** are off and shunt transistors Msw 3-5 **906-910** are all on. The high series impedance and low shunt impedance attenuate the large signal of the PA and isolate the input of the LNA from the output of the PA. The integrated T/R SW **900** illustrates a differential version of the T/R SW. In another embodiment, a single-ended version of the T/R SW can be implemented.

One of ordinary skill in the art readily recognizes that the integrated T/R SW **900** can be implemented in a variety of other ways including but not limited to omitting the shunt transistor Msw3 **906**, omitting the shunt transistors Msw4 **908** and Msw5 **910**, using a field-effect transistor (FET) or using a transmission gate and that would be within the spirit and scope of the present invention.

As above described, by isolating the TX path from the RX path, integrating the RF front end components on-chip and creating a matching network that is optimized for both the PA and the LNA, the present invention achieves a more robust integrated T/R SW solution. Thus, the cost, size and package pin count of the RF front end system is reduced by the present invention.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

What is claimed is:

1. A Radio Frequency (RF) front end system comprising:

a power amplifier (PA) configured to couple to a matching network via a port on a transmit (TX) path;

a low noise amplifier (LNA) configured to couple to the matching network via the port on a receive (RX) path, wherein the PA and the LNA are combined together at the port; and

a transmit/receive switch (T/R SW) coupled in series between the port and the LNA, and a non-switchable direct connection formed between the PA and the port; and

wherein an output stage of the PA is configured to perform switching functionality.

2. The RF front end system of claim **1**, wherein the port is a single RF port.

3. The RF front end system of claim **1**, wherein the output stage of the PA includes a power supply pin Vdd differentially coupled to first and second input devices and to first and second cascade devices, wherein the first input device is in series with the first cascade device and the second input device is in series with the second cascade device, wherein the first input device and first cascade device provide a first differential output signal and the second input device and second cascade device provide a second differential output signal.

4. The RF front end system of claim **3**, wherein the first and second input devices are thin oxide devices and the first and second cascade devices are thick oxide devices.

5. The RF front end system of claim **1**, wherein the output stage of the PA is single-ended.

6. The RF front end system of claim **1**, wherein the LNA is a common-gate LNA.

7. The RF front end system of claim **6**, wherein the common-gate LNA includes a power supply pin Vdd differentially coupled to first and second input devices and first and second cascade devices, wherein the first input device is in series with the first cascade device and the second input device is in series with the second cascade device, wherein the first input device and first cascade device provide a first differential output signal and the second input device and second cascade device provide a second differential output signal.

8. The RF front end system of claim **7**, wherein an input impedance of the common-gate LNA is inversely proportional to a transconductance of the first and second input devices.

9. The RF front end system of claim **8**, wherein the input impedance is a common RF port impedance.

10. The RF front end system of claim **6**, wherein the common-gate LNA is single-ended.

11. The RF front end system of claim **1**, wherein the LNA is a cross-coupled common-gate LNA.

12. The RF front end system of claim **1**, wherein the LNA is a common source LNA with feedback implementation.

13. The RF front end system of claim **1**, wherein the at least one T/R SW includes first and second series transistors, first, second and third shunt transistors, first and second input signals, and first and second output signals.

14. The RF front end system of claim **1**, wherein the at least one T/R SW is single-ended.

15. The RF front end system of claim **1**, wherein the at least one T/R SW is implemented using a field-effect transistor (FET) or a transmission gate.

16. The RF front end system of claim **1**, wherein the at least one T/R SW is a plurality of transmit-receive switches.

17. A method for creating a Radio Frequency (RF) front end, the method comprising:

coupling a power amplifier (PA) to a matching network via a port on a transmit (TX) path;

coupling a low noise amplifier (LNA) to the matching network via the port on a receive (RX) path, wherein the PA and the LNA are combined together at the port;

coupling a transmit/receive switch (T/R SW) in series between the port and the LNA, and providing a non-switchable direct connection between the PA and the port;

and

combining the PA and the LNA together at the port, wherein an output stage of the PA is configured to perform switching functionality.

18. The method of claim **17**, further comprising integrating an antenna and the matching network off-chip.

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