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Huang et al.

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(54) **SEMICONDUCTOR ARRANGEMENT AND FORMATION THEREOF**

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B81C 1/00	(2006.01)
H01L 23/48	(2006.01)

(52) **U.S. Cl.**

CPC ***B81C 1/00301*** (2013.01); *B81B 2207/07* (2013.01); *B81C 1/00269* (2013.01); *H01L 23/48* (2013.01); *H01L 23/481* (2013.01); *H01L 2924/1461* (2013.01)

(58) **Field of Classification Search**

CPC H01L 2924/1461; H01L 23/481; H01L 23/52; H01L 23/522; H01L 23/5226; H01L 23/528; H01L 23/535; H01L 23/538; H01L 21/768; H01L 21/823475; H01L 21/823871

USPC 257/773

See application file for complete search history.

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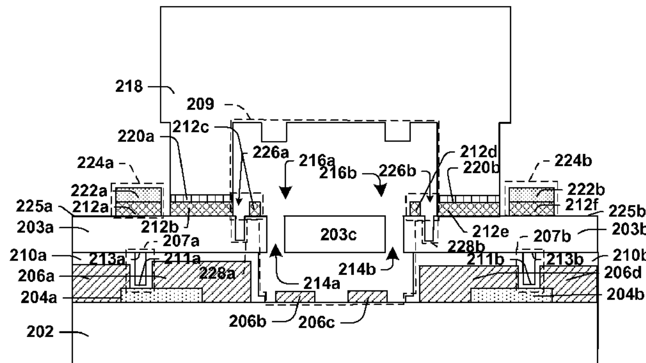
(57) **ABSTRACT**

A semiconductor arrangement and method of formation are provided. The semiconductor arrangement includes a MEMS device in a MEMS area, where a first metal layer is connected to a first metal connect adjacent the MEMS area and a cap is over the MEMS area to vacuum seal the MEMS area. A first wafer portion is over and bonded to the first metal layer which connects the first metal connect to a first I/O port using metal routing. The first metal layer and the first wafer portion bond requires 10% less bonding area than a bond not including the first metal layer. The semiconductor arrangement including the first metal layer has increased conductivity and requires less processing than an arrangement that requires a dopant implant to connect a first metal connect to a first I/O port and has a better vacuum seal due to a reduction in outgassing.

20 Claims, 5 Drawing Sheets



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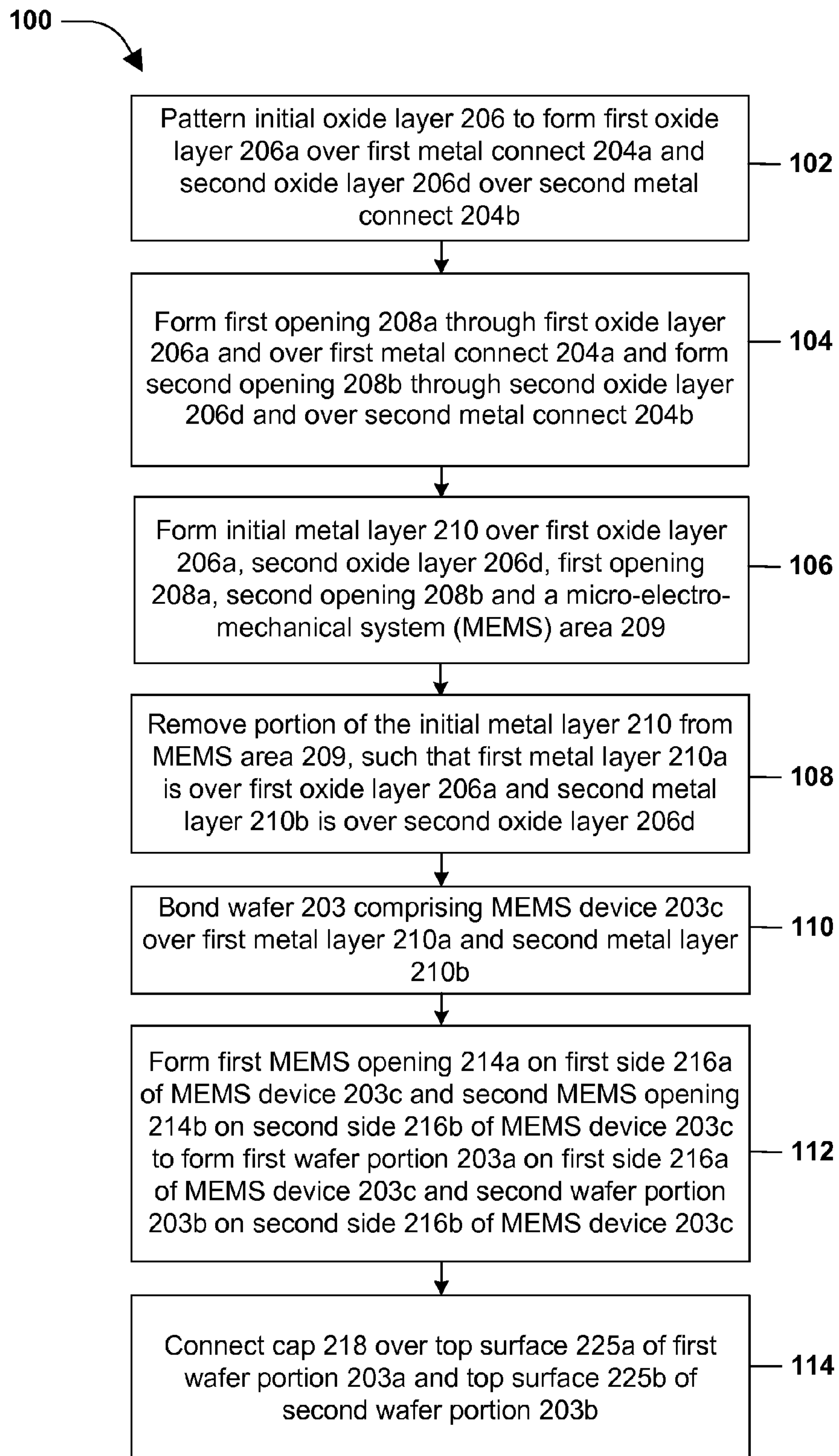

FIG. 1

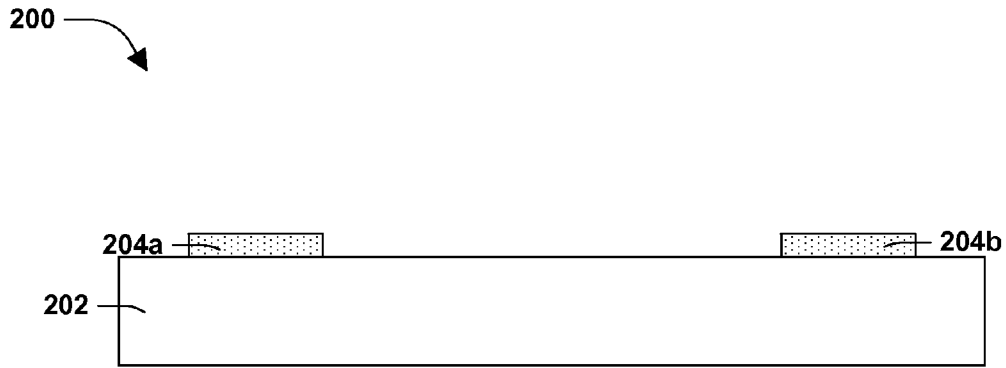

FIG. 2

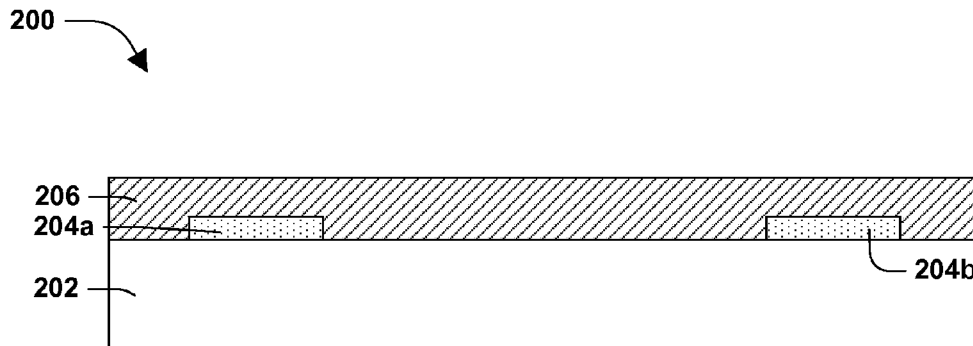

FIG. 3

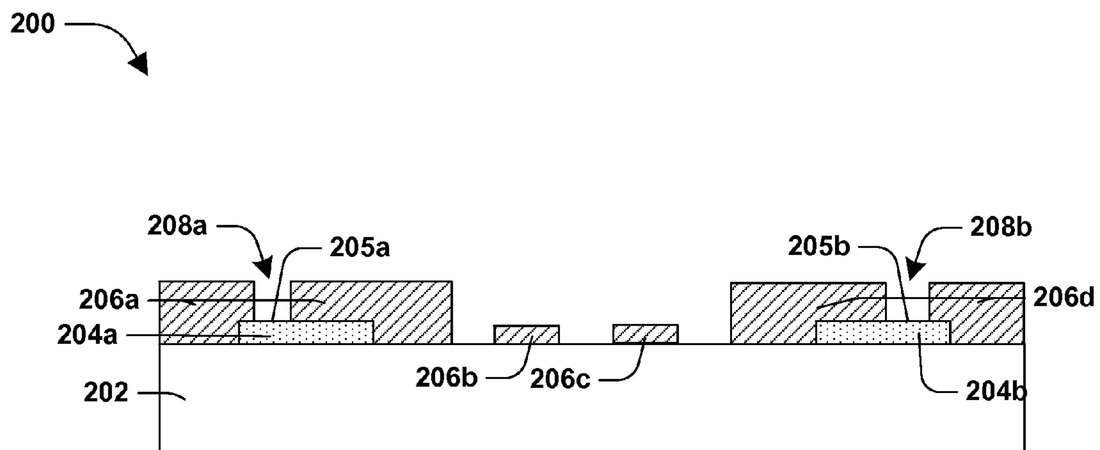

FIG. 4

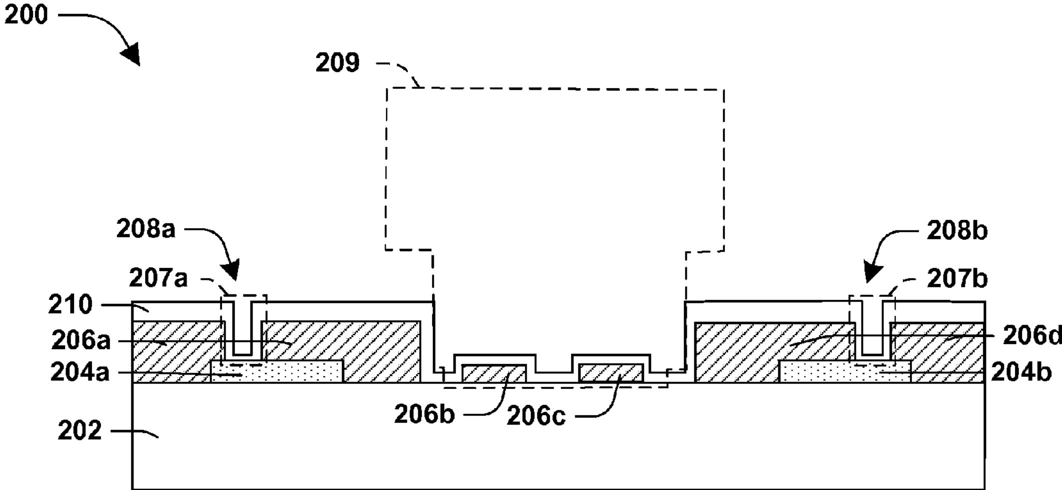

FIG. 5

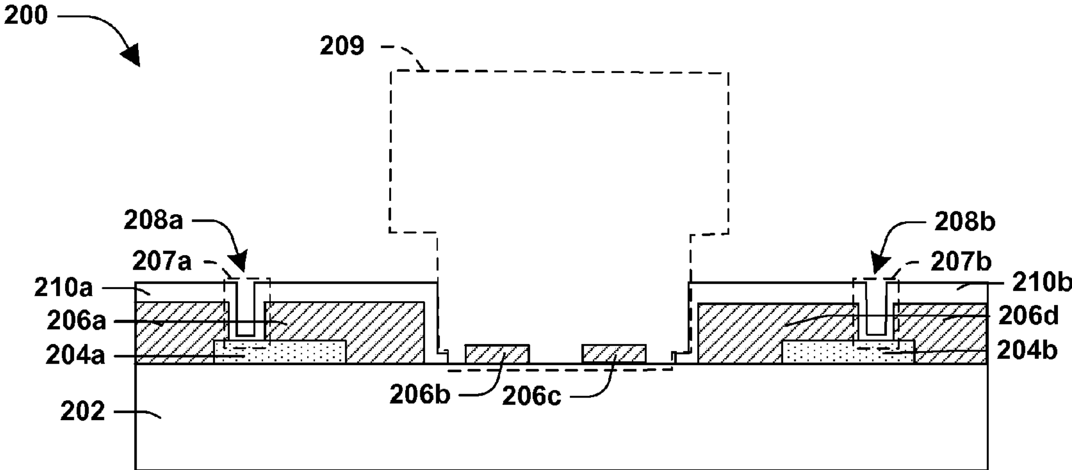

FIG. 6

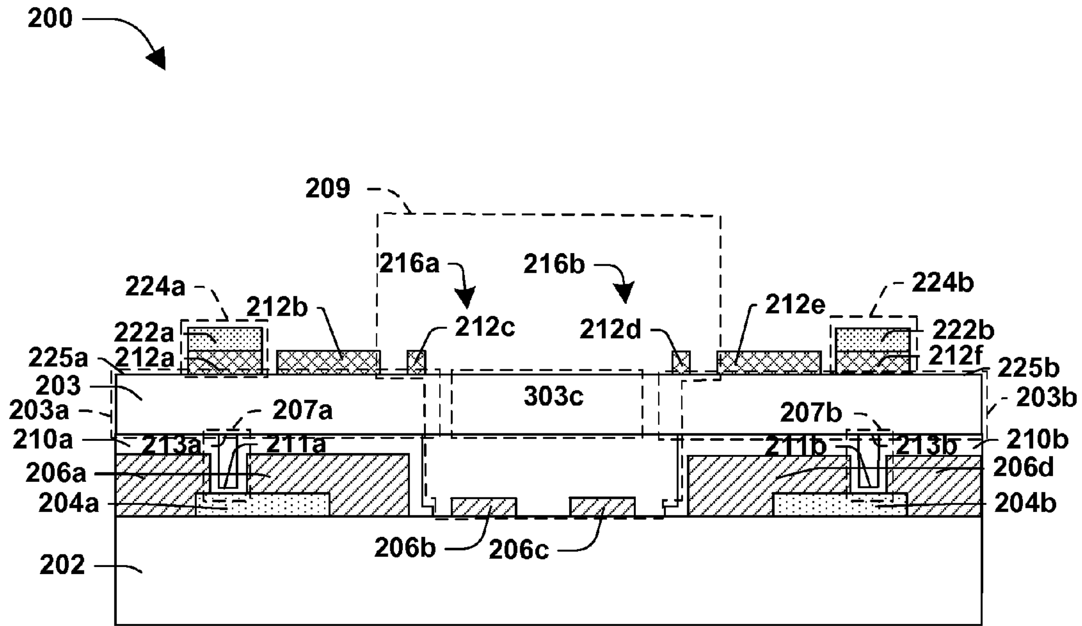

FIG. 7

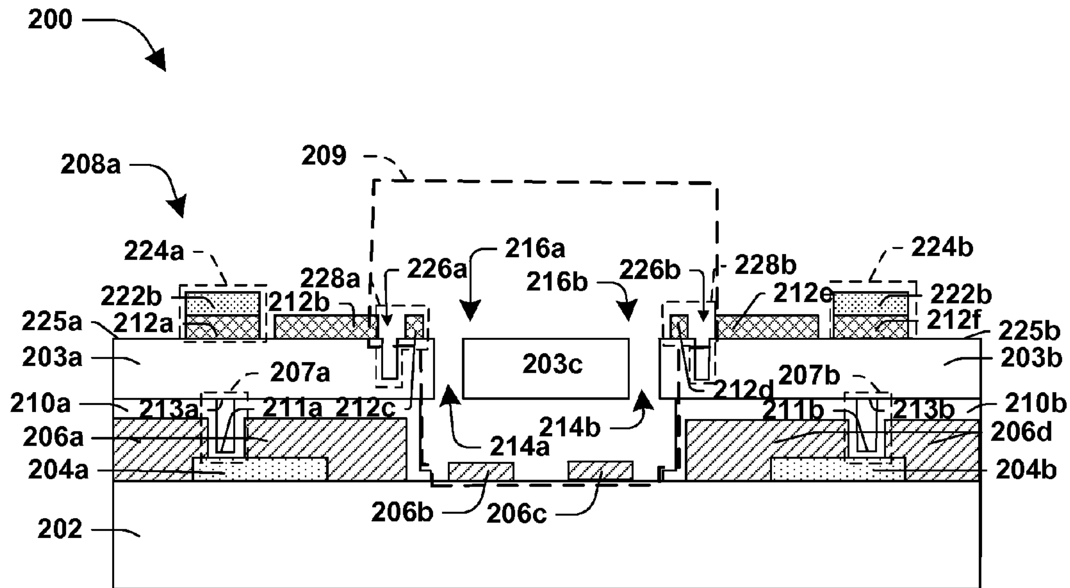

FIG. 8

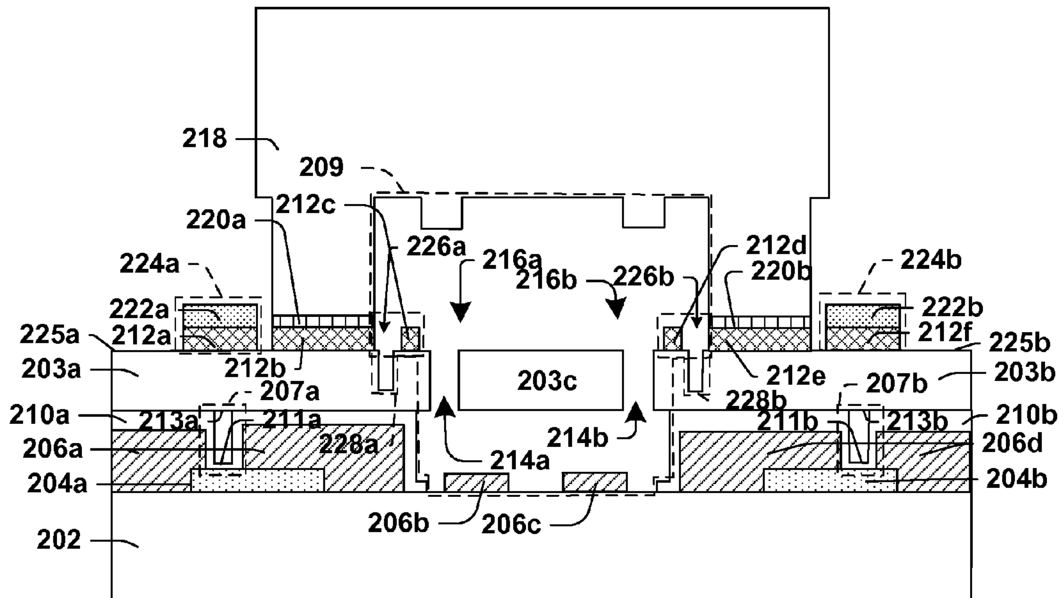

FIG. 9

SEMICONDUCTOR ARRANGEMENT AND FORMATION THEREOF

BACKGROUND

A semiconductor arrangement comprises one or more micro-electro-mechanical system (MEMS) devices. In a MEMS device, such as a pressure sensor, generally at least two of sensing, processing or actuating functions are combined on a single microchip.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** is a flow diagram illustrating a method of forming a semiconductor arrangement, in accordance with some embodiments.

FIG. **2** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **3** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **4** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **5** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **6** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **7** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **8** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **9** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated **90** degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

One or more techniques for forming a semiconductor arrangement and resulting structures formed thereby are provided herein.

A method **100** of forming a semiconductor arrangement **200** according to some embodiments is illustrated in FIG. **1** and one or more structures formed thereby at various stages of fabrication are illustrated in FIGS. **2-9**. According to some embodiments, such as illustrated in FIG. **9**, the semiconductor arrangement **200** comprises a first metal connect **204*a*** adjacent a second metal connect **204*b*** on a substrate **202**. In some embodiments, a first oxide layer **206*a*** is over the first metal connect **204*a*** and a second oxide layer **206*d*** is over the second metal connect **204*b***. In some embodiments, a first metal layer **210*a*** is over the first oxide layer **206*a***, such that a portion **207*a*** of the first metal layer **210*a*** is in contact with a top surface **205*a*** of the first metal connect **204*a***, as illustrated in FIG. **4**. In some embodiments, a second metal layer **210*b*** is over the second oxide layer **206*d***, such that a portion **207*b*** of the second metal layer **210*b*** is in contact with a top surface **205*b*** of the second metal connect **204*b***, as illustrated in FIG. **4**. In some embodiments, the first metal layer **210*a*** and the second metal layer **210*b*** comprise titanium. In some embodiments, a micro-electro-mechanical system (MEMS) area **209** is between the first metal layer **210*a*** and the second metal layer **210*b***, as illustrated in FIG. **9**. In some embodiments, the MEMS area **209** comprises a MEMS device **203*c***. In some embodiments, a first wafer portion **203*a*** comprising silicon is bonded to the first metal layer **210*a*** by a titanium silicon bond and a second wafer portion **203*b*** comprising silicon is bonded to the second metal layer **210*b*** by a titanium silicon bond. In some embodiments, a cap **218** is connected over a top surface **225*a*** of the first wafer portion **203*a*** by a first bond and connected over a top surface **225*b*** of the second wafer portion **203*b*** by a second bond. In some embodiments, the first bond comprises a first eutectic bond between a first bonding pad **212*b*** and a first cap bonding pad **220*a*** of the cap **218**. In some embodiments, the first bonding pad **212*b*** is on the top surface **225*a*** of the first wafer portion **203*a*** and comprises at least one of aluminum or copper. In some embodiments, the first cap bonding pad **220*a*** comprises germanium. In some embodiments, the second bond comprises a second eutectic bond between a second bonding pad **212*e*** and a second cap bonding pad **220*b*** of the cap **218**. In some embodiments, the second bonding pad **212*e*** is on the top surface **225*b*** of the second wafer portion **203*b*** and comprises at least one of aluminum or copper. In some embodiments, the second cap bonding pad **220*b*** comprises germanium. In some embodiments, connecting the cap **218** vacuum seals the MEMS area **209**, and thus the MEMS device **203*c*** therein. In some embodiments, a first I/O port **224*a*** comprises a first glue pad **222*a*** comprising at least one of titanium or nitride over a first metal pad **212*a*** comprising at least one of aluminum or copper, the first metal pad **212*a*** on the top surface **225*a*** of the first wafer portion **203*a*** adjacent the cap **218** outside of the MEMS area **209**. In some embodiments, a second I/O port **224*b*** comprises a second glue pad **222*b*** comprising at least one of titanium or nitride over a second metal pad **212*f*** comprising at least one of aluminum or copper, the second metal pad **212*f*** on the top surface **225*b*** of the second wafer portion **203*b*** adjacent the cap **218** outside of the MEMS area **209**. In some embodiments, at least one of a first metal routing (not shown) connects the first metal layer **210*a*** to the first I/O port **224*a***

or second metal routing (not shown) connects the second metal layer **210**_b_ to the second I/O port **224**_b_. In some embodiments, the bond between the first metal layer **210**_a_ and the first wafer portion **203**_a_ requires between about 5% to about 10% less bonding area than a bond that is not between a first metal layer and a first wafer portion. In some embodiments, the first metal layer **210**_a_ and the second metal layer **210**_b_ increase the conductivity of the semiconductor arrangement **200**, as compared to an arrangement that lacks at least one of a first metal layer or a second metal layer. In some embodiments, the semiconductor arrangement **200** comprising the first metal layer **210**_a_ connecting via a first metal routing the first metal connect **204**_a_ to the first I/O port **224**_a_ requires less processing than a device that requires a dopant implant to connect a first metal connect to a first I/O port. Further, a semiconductor device that does not require a dopant implant to connect a first metal connect to a first I/O port has at least one of an enhanced first bond or an enhanced second bond and thus a greater vacuum seal, due to a reduction in outgassing as compared to a semiconductor arrangement that requires the dopant implant.

At **102**, an initial oxide layer **206** is patterned to form the first oxide layer **206**_a_ over the first metal connect **204**_a_ and the second oxide layer **206**_d_ over the second metal connect **204**_b_, as illustrated in FIG. **4**. Turning to FIG. **2**, prior to FIG. **4**, the first metal connect **204**_a_ is adjacent the second metal connect **204**_b_ over the substrate **202**, according to some embodiments. In some embodiments, the substrate **202** comprises at least one of silicon or germanium. According to some embodiments, the substrate **202** comprises at least one of an epitaxial layer, a silicon-on-insulator (SOI) structure, a wafer, or a die formed from a wafer. In some embodiments, the substrate **202** comprises at least one CMOS device. In some embodiments, at least one of the first metal connect **204**_a_ or the second metal connect **204**_b_ comprises at least one of aluminum or copper. In some embodiments, at least one of the first metal connect **204**_a_ or the second metal connect **204**_b_ has a metal layer thickness between about 2 Å to about 16 Å. In some embodiments, an initial oxide layer **206** is formed over the first metal connect **204**_a_ and the second metal connect **204**_b_, as illustrated in FIG. **3**. In some embodiments, the initial oxide layer **206** comprises oxide. In some embodiments, the initial oxide layer **206** is formed by deposition. In some embodiments, the initial oxide layer **206** has an initial oxide thickness between about 1800 Å to about 2400 Å. In some embodiments, the initial oxide layer **206** is patterned to form the first oxide layer **206**_a_, the second oxide layer **206**_d_, a first bump layer **206**_b_ and a second bump layer **206**_c_, the first bump layer **206**_b_ between the first oxide layer **206**_a_ and the second bump layer **206**_c_ on the substrate **202** and the second bump layer **206**_c_ between the second oxide layer **206**_d_ and the first bump layer **206**_b_ on the substrate **202**. In some embodiments, at least one of the first oxide layer **206**_a_ or the second oxide layer **206**_d_ has an oxide layer thickness between about 1200 Å to about 1800 Å. In some embodiments, at least one of the first bump layer **206**_b_ or the second bump layer **206**_c_ has a bump layer thickness between about 5 Å to about 50 Å.

At **104**, a first opening **208**_a_ is formed through the first oxide layer **206**_a_ over the first metal connect **204**_a_ and a second opening **208**_b_ is formed through the second oxide layer **206**_d_ over the second metal connect **204**_b_, as illustrated in FIG. **4**, according to some embodiments. In some embodiments, the first opening **208**_a_ exposes the top surface **205**_a_ of the first metal connect **204**_a_ and the second opening **208**_b_ exposes the top surface **205**_b_ of the second metal connect **204**_b_. In some embodiments, at least one of the first opening **208**_a_ or the second opening **208**_b_ are formed by etching.

At **106**, an initial metal layer **210** is formed over the first oxide layer **206**_a_, the second oxide layer **206**_d_, the first opening **208**_a_, and the second opening **208**_b_, as illustrated in FIG. **5**, according to some embodiments. In some embodiments, the initial metal layer **210** is formed over the substrate **202**, the first bump layer **206**_b_ and the second bump layer **206**_c_ in the MEMS area **209**. In some embodiments, the initial metal layer **210** is formed by deposition. In some embodiments, the initial metal layer **210** is formed conformally to the first oxide layer **206**_a_, the second oxide layer **206**_d_, the first opening **208**_a_, the second opening **208**_b_, the substrate **202**, the first bump layer **206**_b_ and the second bump layer **206**_c_. In some embodiments, the initial metal layer **210** comprises titanium. In some embodiments, the initial metal layer **210** has a metal layer thickness between about 100 Å to about 7,000 Å.

At **108**, a portion of the initial metal layer **210** is removed from the MEMS area **209**, such that the first metal layer **210**_a_ is formed over the first oxide layer **206**_a_ and the second metal layer **210**_a_ is formed over the second oxide layer **206**_d_, as illustrated in FIG. **6**, according to some embodiments. In some embodiments, the portion of the initial metal layer **210** is removed by etching. In some embodiments, removing the portion of the initial metal layer **210** exposes the first bump layer **206**_b_ and the second bump layer **206** and the substrate **202** in the MEMS area **209**. In some embodiments, the first metal layer **210**_a_ has a first metal thickness between about 100 Å to about 7,000 Å. In some embodiments, the second metal layer **210**_b_ has a second metal thickness between about 100 Å to about 7,000 Å. In some embodiments, the portion **207**_a_ of the first metal layer is in contact with the top surface **205**_a_ of the first metal connect **204**_a_. In some embodiments, the portion **207**_b_ of the second metal layer is in contact with the top surface **205**_b_ of the second metal connect **204**_b_.

At **110**, a wafer **203** comprising a MEMS device **203**_c_ is bonded over the first metal layer **210**_a_ and the second metal layer **210**_b_, as illustrated in FIG. **7**, according to some embodiments. In some embodiments, the wafer **203** comprises at least one of an epitaxial layer, a silicon-on-insulator (SOI) structure, a wafer, or a die formed from a wafer. In some embodiments, the wafer **203** comprises silicon. In some embodiments, the wafer **203** is bonded to the first metal layer **210**_a_ and the second metal layer **210**_b_ by a titanium-silicon wafer bond. In some embodiments, a first vacancy is formed between a top surface **211**_a_ of the portion **207**_a_ of the first metal layer **210**_a_ and a first wafer portion bottom surface **213**_a_ of the first wafer portion **203**_a_. In some embodiments, a second vacancy is formed between a top surface **211**_b_ of the portion **207**_b_ of the second metal layer **210**_b_ and a second wafer portion bottom surface **213**_b_ of the second wafer portion **203**_b_. In some embodiments, an initial metal pad comprising at least one of aluminum or copper is formed over the wafer **203**. In some embodiments, the initial metal pad is patterned to form the first metal pad **212**_a_, the first bonding pad **212**_b_, a first squish prevention node **212**_c_, a second squish prevention node **212**_d_, the second bonding pad **212**_e_ and the second metal pad **212**_f_. In some embodiments, the first metal pad **212**_a_ and the first bonding pad **212**_b_ are on a first side **216**_a_ of the MEMS device **203**_c_ outside the MEMS area **209**, such that that the first bonding pad **212**_b_ is between the first squish prevention node **212**_c_ and the first metal pad **212**_a_. In some embodiments, the second metal pad **212**_f_ and the second bonding pad **212**_e_ are on a second side **216**_b_ of the MEMS device **203**_c_ outside the

MEMS area **209**, such that that the second bonding pad **212***e* is between the second squish prevention node **212***d* and the second metal pad **212***f*. In some embodiments, the first squish prevention node **212***c* and the second squish prevention node **212***d* are in the MEMS area **209**. In some embodiments, the first glue pad **222***a* comprising at least one of titanium or nitride is formed over the first metal pad **212***a* to form the first I/O port **224***a*. In some embodiments, the second glue pad **222***b* comprising at least one of titanium or nitride is formed over the second metal pad **212***f* to form the second I/O port **224***b*. In some embodiments, at least one of the first metal routing (not shown) connects the first metal connect **204***a* via the first metal layer **210***a* to the first I/O port **224***a* or the second metal routing (not shown) connects the second metal connect **204***b* via the second metal layer **210***b* to the second I/O port **224***b*. In some embodiments, at least one of the first I/O port **224***a* or the second I/O port **224***b* comprises an input port for the semiconductor arrangement **200**. In some embodiments, at least one of the first I/O port **224***a* or the second I/O port **224***b* comprises an output port for the semiconductor arrangement **200**.

At **112**, a first MEMS opening **214***a* is formed on the first side **216***a* of the MEMS device **203***c* to form the first wafer portion **203***a* on the first side **216***a* of the MEMS device **203***c* and a second MEMS opening **214***b* is formed on the second side **216***b* of the MEMS device **203***c* to form the second wafer portion **203***b* on the second side **216***b* of the MEMS device **203***c*, as illustrated in FIG. **8**, according to some embodiments. In some embodiments, a first squish prevention opening **226***a* is formed in the MEMS area **209** between the first squish prevention node **212***c* and the first bonding pad **212***b*, to form a first squish prevention region **228***a* comprising the first squish prevention node **212***c* and the first squish prevention opening **226***a*. In some embodiments, a second squish prevention opening **226***b* is formed in the MEMS area **209** between the second squish prevention node **212***d* and the second bonding pad **212***e*, to form a second squish prevention region **228***b* comprising the second squish prevention node **212***d* and the second squish prevention opening **226***b*. In some embodiments, at least one of the first MEMS opening **214***a*, the second MEMS opening **214***b*, the first squish prevention opening **226***a* or the second squish prevention opening **226***b* are formed by etching. In some embodiments, the MEMS device **203***a* is separated from the first wafer portion **203***a* and the second wafer portion **203***b* by the first MEMS opening **214***a* and the second MEMS opening **214***b*, such that the first MEMS opening **214***a* and the second MEMS opening **214***b* go through the wafer **203**. In some embodiments, the MEMS device **203***a* is attached to an anchor (not shown), such that the MEMS device **203***a* does not fall when the first MEMS opening **214***a* and the second MEMS opening **214***b* are formed.

At **114**, the cap **218** is connected over the top surface **225***a* of the first wafer portion **203***a* and over the top surface **225***b* of the second wafer portion **203***b*, as illustrated in FIG. **9**, according to some embodiments. In some embodiments, the cap **218** comprises silicon. In some embodiments, the cap **218** is connected to the top surface **225***a* of the first wafer portion **203***a* by the first bond and connected to the top surface **225***b* of the second wafer portion **203***b* by the second bond. In some embodiments, the first bond comprises the first eutectic bond between the first bonding pad **212***b* and the first cap bonding pad **220***a* of the cap **218**. In some embodiments, the first bonding pad **212***b* is on the top surface **225***a* of the first wafer portion **203***a* and comprises at least one of aluminum or copper. In some embodiments, the first cap bonding pad **220***a* comprises germanium. In some embodiments, the second bond comprises the second eutectic bond between the second bonding pad **212***e* and the second cap bonding pad **220***b* of the cap **218**. In some embodiments, the second bonding pad **212***e* is on the top surface **225***b* of the second wafer portion **203***b* and comprises at least one of aluminum or copper. In some embodiments, the second cap bonding pad **220***b* comprises germanium. In some embodiments, some of the first bonding pad **212***b* will squish toward the first squish prevention region **226***a* during the formation of the first eutectic bond. In some embodiments, the first squish prevention region **226***a* prevents the squished first bonding pad **212***b* material from migrating to the substrate **202**. In some embodiments, some of the second bonding pad **212***e* will squish toward the second squish prevention region **226***b* during the formation of the second eutectic bond. In some embodiments, the second squish prevention region **226***b* prevents the squished second bonding pad **212***e* material from migrating to the substrate **202**. In some embodiments, at least one of the first eutectic bond is between at least one of germanium, aluminum or copper or the second eutectic bond is between at least one of germanium, aluminum or copper. In some embodiments, the cap **218** is vacuum sealed, such that there is little to no air in the MEMS area **209**. In some embodiments, the semiconductor arrangement **200** comprises at least one of a motion sensor, a pressure sensor, a radio sensor, or an accelerometer. In some embodiments, the bond between the first metal layer **210***a* and the first wafer portion **203***a* requires between about 5% to about 10% less bonding area than a bond that is not between a first metal layer and a first wafer portion. In some embodiments, the first metal layer **210***a* and the second metal layer **210***b* increase the conductivity of the semiconductor arrangement **200**, as compared to an arrangement that lacks at least one of a first metal layer or a second metal layer. In some embodiments, the semiconductor arrangement **200** comprising the first metal layer **210***a* connecting via a first metal routing the first metal connect **204***a* to the first I/O port **224***a* requires less processing than a device that requires a dopant implant to connect a first metal connect to a first I/O port. Further, a semiconductor device that does not require a dopant implant to connect a first metal connect to a first I/O port has at least one of an enhanced first bond or an enhanced second bond and thus a greater vacuum seal, due to a reduction in outgassing as compared to a semiconductor arrangement that requires the dopant implant.

According to some embodiments, a semiconductor arrangement comprises a first metal connect adjacent a second metal connect, the first metal connect and the second metal connect over a substrate and a first metal layer is over the first metal connect such that a portion of the first metal layer is in contact with a top surface of the first metal connect. In some embodiments, a second metal layer is over the second metal connect such that a portion of the second metal layer is in contact with a top surface of the second metal connect. In some embodiments, a micro electromechanical system (MEMS) area is between the first metal layer and the second metal layer, the MEMS area comprising a MEMS device. In some embodiments, a first wafer portion is bonded to the first metal layer over the first metal connect and a second wafer portion is bonded to the second metal layer over the second metal connect. In some embodiments, a cap is connected to a top surface of the first wafer portion by a first bond and connected to a top surface of the second wafer portion by a second bond, such that the cap goes over the MEMS area.

According to some embodiments, a method of forming a semiconductor arrangement comprises patterning an initial oxide layer to form a first oxide layer over a first metal connect and a second oxide layer over a second metal connect, where the first metal connect is adjacent the second metal connect on a substrate. According to some embodiments, the method of forming a semiconductor arrangement further comprises forming a first opening through the first oxide layer over the first metal connect, such that a top surface of the first metal connect is exposed and forming a second opening through the second oxide layer over the second metal connect, such that a top surface of the second metal connect is exposed. According to some embodiments, the method of forming a semiconductor arrangement further comprises forming an initial metal layer conformally over the first oxide layer, the second oxide layer, the first opening, the second opening and a micro electro-mechanical system (MEMS) area between the first oxide layer and the second oxide layer, such that a portion of a first metal layer of the initial metal layer is in contact with the top surface of the first metal connect and a portion of a second metal layer of the initial metal layer is in contact with the top surface of the second metal connect. According to some embodiments, the method of forming a semiconductor arrangement further comprises removing a portion of the initial metal layer from the MEMS area such that the first metal layer of the initial metal layer is formed over the first oxide layer and the second metal layer of the initial metal layer is formed over the second oxide layer and bonding a wafer comprising a MEMS device of the MEMS area over the first metal layer and the second metal layer.

According to some embodiments, a semiconductor arrangement comprises a first metal connect adjacent a second metal connect, the first metal connect and the second metal connect over a substrate, a first metal layer over the first metal connect such that a portion of the first metal layer is in contact with a top surface of the first metal connect. In some embodiments, a first oxide layer is between the first metal connect and the first metal layer and a second metal layer is over the second metal connect such that a portion of the second metal layer is in contact with a top surface of the second metal connect. In some embodiments, a second oxide layer is between the second metal connect and the second metal layer. In some embodiments, a micro electro-mechanical system (MEMS) area is between the first metal layer and the second metal layer, the MEMS area comprising a MEMS device. In some embodiments, a first wafer portion is bonded to the first metal layer over the first metal connect and a second wafer portion is bonded to the second metal layer over the second metal connect. In some embodiments, a cap is connected to a top surface of the first wafer portion by a first bond and connected to a top surface of the second wafer portion by a second bond, such that the cap goes over the MEMS area.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Various operations of embodiments are provided herein. The order in which some or all of the operations are described should not be construed to imply that these operations are necessarily order dependent. Alternative ordering will be appreciated having the benefit of this description. Further, it will be understood that not all operations are necessarily present in each embodiment provided herein. Also, it will be understood that not all operations are necessary in some embodiments.

It will be appreciated that layers, features, elements, etc. depicted herein are illustrated with particular dimensions relative to one another, such as structural dimensions or orientations, for example, for purposes of simplicity and ease of understanding and that actual dimensions of the same differ substantially from that illustrated herein, in some embodiments. Additionally, a variety of techniques exist for forming the layers features, elements, etc. mentioned herein, such as etching techniques, implanting techniques, doping techniques, spin-on techniques, sputtering techniques such as magnetron or ion beam sputtering, growth techniques, such as thermal growth or deposition techniques such as chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma enhanced chemical vapor deposition (PECVD), or atomic layer deposition (ALD), for example.

Moreover, "exemplary" is used herein to mean serving as an example, instance, illustration, etc., and not necessarily as advantageous. As used in this application, "or" is intended to mean an inclusive "or" rather than an exclusive "or". In addition, "a" and "an" as used in this application and the appended claims are generally be construed to mean "one or more" unless specified otherwise or clear from context to be directed to a singular form. Also, at least one of A and B and/or the like generally means A or B or both A and B. Furthermore, to the extent that "includes", "having", "has", "with", or variants thereof are used, such terms are intended to be inclusive in a manner similar to the term "comprising". Also, unless specified otherwise, "first," "second," or the like are not intended to imply a temporal aspect, a spatial aspect, an ordering, etc. Rather, such terms are merely used as identifiers, names, etc. for features, elements, items, etc. For example, a first element and a second element generally correspond to element A and element B or two different or two identical elements or the same element.

Also, although the disclosure has been shown and described with respect to one or more implementations, equivalent alterations and modifications will occur to others skilled in the art based upon a reading and understanding of this specification and the annexed drawings. The disclosure comprises all such modifications and alterations and is limited only by the scope of the following claims. In particular regard to the various functions performed by the above described components (e.g., elements, resources, etc.), the terms used to describe such components are intended to correspond, unless otherwise indicated, to any component which performs the specified function of the described component (e.g., that is functionally equivalent), even though not structurally equivalent to the disclosed structure. In addition, while a particular feature of the disclosure may have been disclosed with respect to only one of several implementations, such feature may be combined with one or more other features of the other implementations as may be desired and advantageous for any given or particular application.

What is claimed is:

1. A semiconductor arrangement, comprising:

a first metal connect and a second metal connect, the first metal connect and the second metal connect over a substrate;

a first metal layer over the first metal connect, a portion of the first metal layer in contact with a top surface of the first metal connect;

a second metal layer over the second metal connect, a portion of the second metal layer in contact with a top surface of the second metal connect;

a micro electro-mechanical system (MEMS) area between the first metal layer and the second metal layer, the MEMS area comprising a MEMS device;

a first wafer portion bonded to the first metal layer over the first metal connect, the first metal layer comprising titanium, the first wafer portion comprising silicon, and the first wafer portion bonded to the first metal layer at an interface of the first wafer portion and the first metal layer via a titanium-silicon bond;

a second wafer portion bonded to the second metal layer over the second metal connect; and

a cap coupled to a top surface of the first wafer portion by a first bond and coupled to a top surface of the second wafer portion by a second bond, the cap extending over the MEMS area.

2. The semiconductor arrangement of claim **1**, at least one of:

the first metal layer having a first metal thickness between about 100 Å to about 7,000 Å; or

the second metal layer having a second metal thickness between about 100 Å to 7,000 Å.

3. The semiconductor arrangement of claim **1**, comprising at least one of:

a first oxide layer between the first metal connect and the first metal layer; or

a second oxide layer between the second metal connect and the second metal layer.

4. The semiconductor arrangement of claim **3**, comprising at least one of:

a first vacancy between a top surface of the portion of the first metal layer and a first wafer portion bottom surface of the first wafer portion; or

a second vacancy between a top surface of the portion of the second metal layer and a second wafer portion bottom surface of the second wafer portion.

5. The semiconductor arrangement of claim **1**, at least one of:

the first bond comprising a first eutectic bond between at least one of germanium, aluminum or copper; or

the second bond comprising a second eutectic bond between at least one of germanium, aluminum or copper.

6. The semiconductor arrangement of claim **1**, at least one of:

the first metal connect comprising at least one of aluminum or copper; or

the second metal connect comprising at least one of aluminum or copper.

7. The semiconductor arrangement of claim **1**, the cap comprising silicon.

8. The semiconductor arrangement of claim **1**, the substrate comprising a CMOS device.

9. The semiconductor arrangement of claim **1**, comprising at least one of a first metal routing coupling the first metal layer to a first I/O port or a second metal routing coupling the second metal layer to a second I/O port.

10. The semiconductor arrangement MEMS arrangement of claim **1**, the first metal layer in contact with the substrate.

11. A semiconductor arrangement, comprising:

a first metal connect and a second metal connect, the first metal connect and the second metal connect over a substrate;

a first metal layer over the first metal connect, a portion of the first metal layer in contact with a top surface of the first metal connect;

a first oxide layer between the first metal connect and the first metal layer, wherein:

the first metal layer is in contact with a top surface of the first oxide layer,

the first metal layer is in contact with a first sidewall of the first oxide layer overlying the first metal connect, and

the first metal layer is in contact with the substrate;

a second metal layer over the second metal connect, a portion of the second metal layer in contact with a top surface of the second metal connect;

a second oxide layer between the second metal connect and the second metal layer;

a micro electro-mechanical system (MEMS) area between the first metal layer and the second metal layer, the MEMS area comprising a MEMS device;

a first wafer portion bonded to the first metal layer over the first metal connect;

a second wafer portion bonded to the second metal layer over the second metal connect; and

a cap coupled to a top surface of the first wafer portion by a first bond and coupled to a top surface of the second wafer portion by a second bond, the cap extending over the MEMS area.

12. The semiconductor arrangement of claim **11**, the substrate comprising a CMOS device.

13. The semiconductor arrangement of claim **11**, comprising at least one of:

a first vacancy between a top surface of the portion of the first metal layer and a first wafer portion bottom surface of the first wafer portion; or

a second vacancy between a top surface of the portion of the second metal layer and a second wafer portion bottom surface of the second wafer portion.

14. The semiconductor arrangement of claim **11**, at least one of:

the first bond comprising a first eutectic bond between at least one of germanium, aluminum or copper; or

the second bond comprising a second eutectic bond between at least one of germanium, aluminum or copper.

15. A micro-electro-mechanical system (MEMS) arrangement, comprising:

a first metal connect over a substrate;

a first oxide layer over the first metal connect and in contact with a sidewall and a top surface of the first metal connect;

a first metal layer over the first oxide layer and in contact with the first oxide layer and the first metal connect;

a first wafer portion bonded to the first metal layer;

a cap coupled to a top surface of the first wafer portion at a bonding region, wherein the first wafer portion defines a squish prevention opening between the bonding region and a MEMS device; and

a squish prevention node overlying the first wafer portion and between the squish prevention opening and the MEMS device.

16. The MEMS arrangement of claim **15**, the first metal layer in contact with the substrate.

17. The MEMS arrangement of claim **15**, comprising:

a second metal connect over a substrate;

a second oxide layer over the second metal connect and in contact with the second metal connect;

a second metal layer over the second oxide layer and in contact with the second oxide layer and the second metal connect;

a second wafer portion bonded to the second metal layer; and

a second input/output port over the second wafer portion and electrically coupled to the second metal layer.

18. The MEMS arrangement of claim **17**, the MEMS device between the first wafer portion and the second wafer portion.

19. The MEMS arrangement of claim **15**, the cap enclosing the MEMS device.

20. The MEMS arrangement of claim **15**, the squish prevention node comprising at least one of aluminum or copper.

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