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Hu et al.

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(54) DISPLAY DEVICES WITH HIGH RESOLUTION AND SPATIAL DENSITY MODULATION ARCHITECTURE

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G09G 3/20	(2006.01)
G09G 3/36	(2006.01)

(52) **U.S. Cl.**
CPC ***G09G 3/2074*** (2013.01); ***G09G 3/3607*** (2013.01); ***G09G 3/3648*** (2013.01); *G09G 3/2014* (2013.01); *G09G 3/3614* (2013.01); *G09G 2300/0804* (2013.01); *G09G 2300/0842* (2013.01); *G09G 2300/0857* (2013.01); *G09G 2330/025* (2013.01)

(58) **Field of Classification Search**
CPC G06F 3/044; G06G 3/3611; G09G 3/003; G09G 3/007; G09G 3/2051; G09G 3/2085; G09G 3/364; G09G 2320/0626; G09G 2320/064; G09G 3/2033
USPC 345/173, 174, 205, 77, 426, 599, 614
See application file for complete search history.

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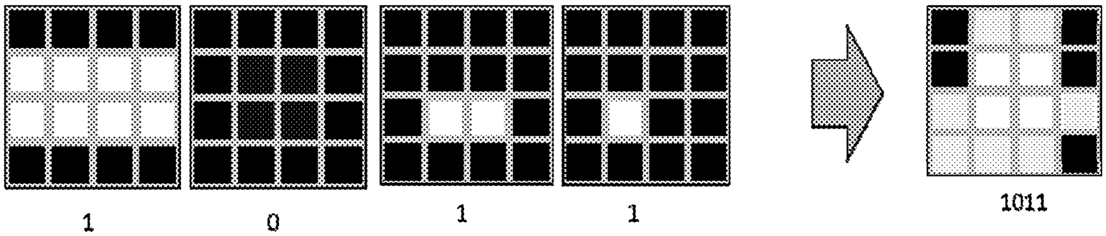
(57) ABSTRACT

Architecture and designs of display devices are described, where the display devices possesses high spatial resolution as well as high intensity resolution and may be readily used in various projection applications, storage and optical communications. According to one aspect of the present invention, a display device includes an array of image elements, each of the image elements further includes an array of sub-image elements. These sub-image elements are driven by PWM as in digital modulation. A portion of an image element area, namely some of the sub-image elements, is turned on, which has the same perceived effect of turning on an entire image element for a specific time. In addition, various designs of an image element or a sub-image element are described.

20 Claims, 16 Drawing Sheets



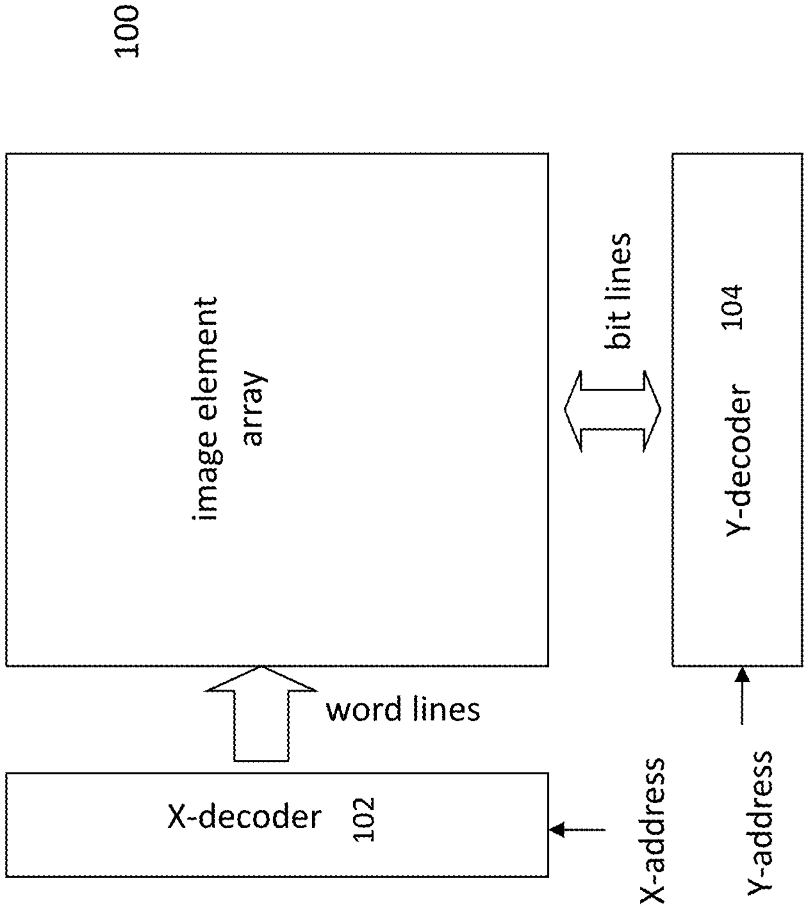

100
image element array
bit lines
Y-decoder 104
word lines
X-decoder 102
X-address
Y-address

FIG. 1

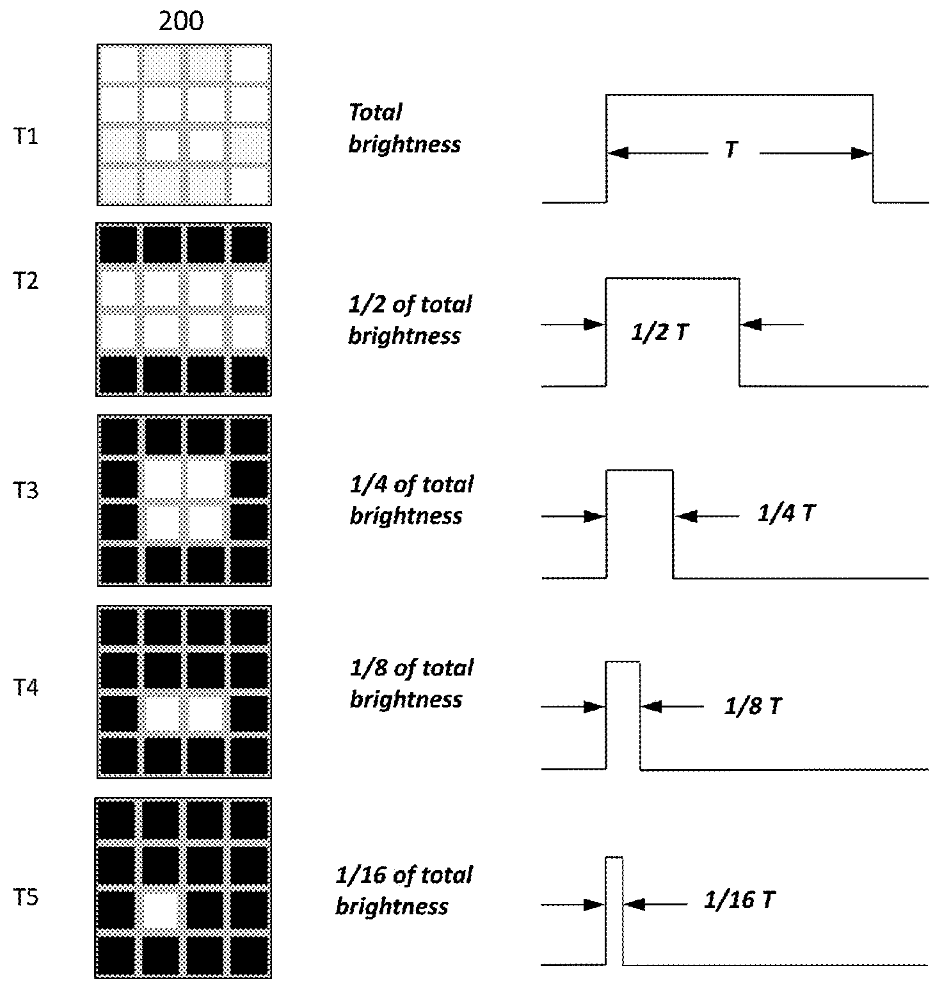

200
T1
Total brightness
T
T2
1/2 of total brightness
1/2 T
T3
1/4 of total brightness
1/4 T
T4
1/8 of total brightness
1/8 T
T5
1/16 of total brightness
1/16 T

FIG. 2A

Fig. 2

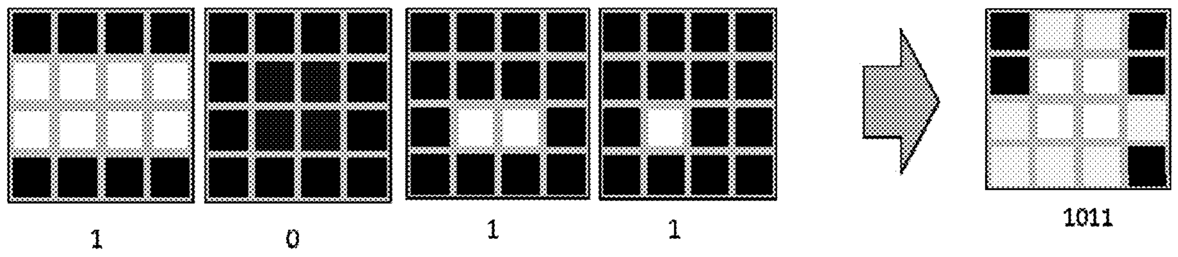


FIG. 2B

number of sub elements	binary code	Number of patterns
0	0000	1
1	0001	16
2	0010	120
3	0011	560
4	0100	1820
5	0101	4368
6	0110	8008
7	0111	11440
8	1000	12870
9	1001	11440
10	1010	8008
11	1011	4368
12	1100	1820
13	1101	560
14	1110	120
15	1111	16

FIG. 2C

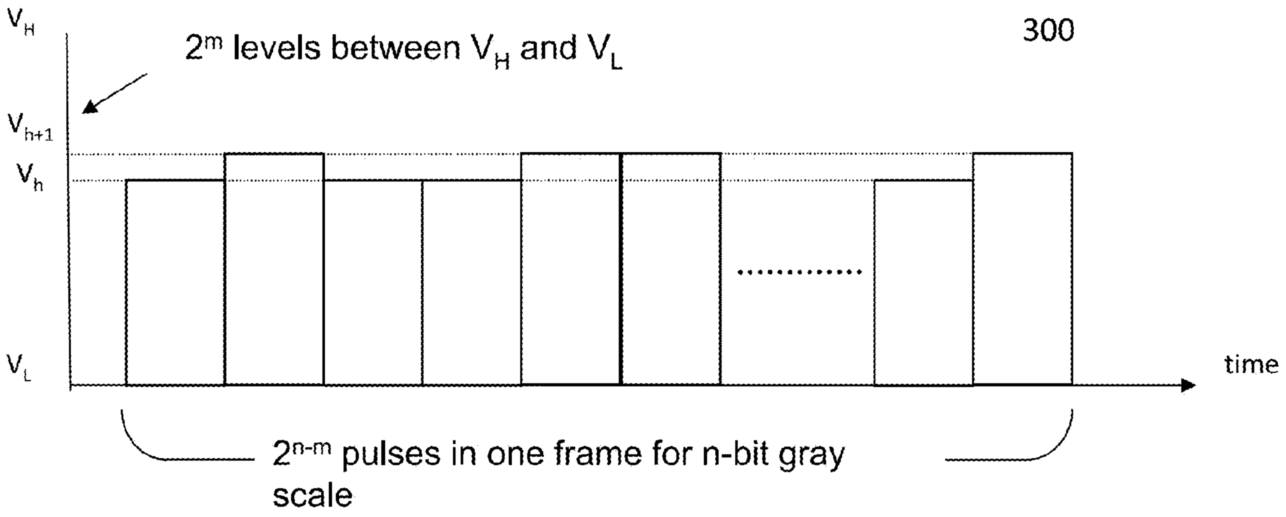

300
V_H
V_{h+1}
V_h
V_L
2^m levels between V_H and V_L
time
2^{n-m} pulses in one frame for n-bit gray scale

FIG. 3A

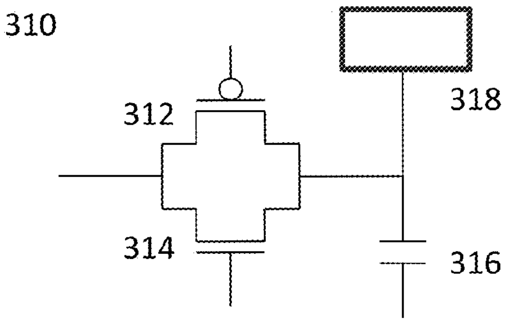

310
312
314
318
316

FIG. 3B

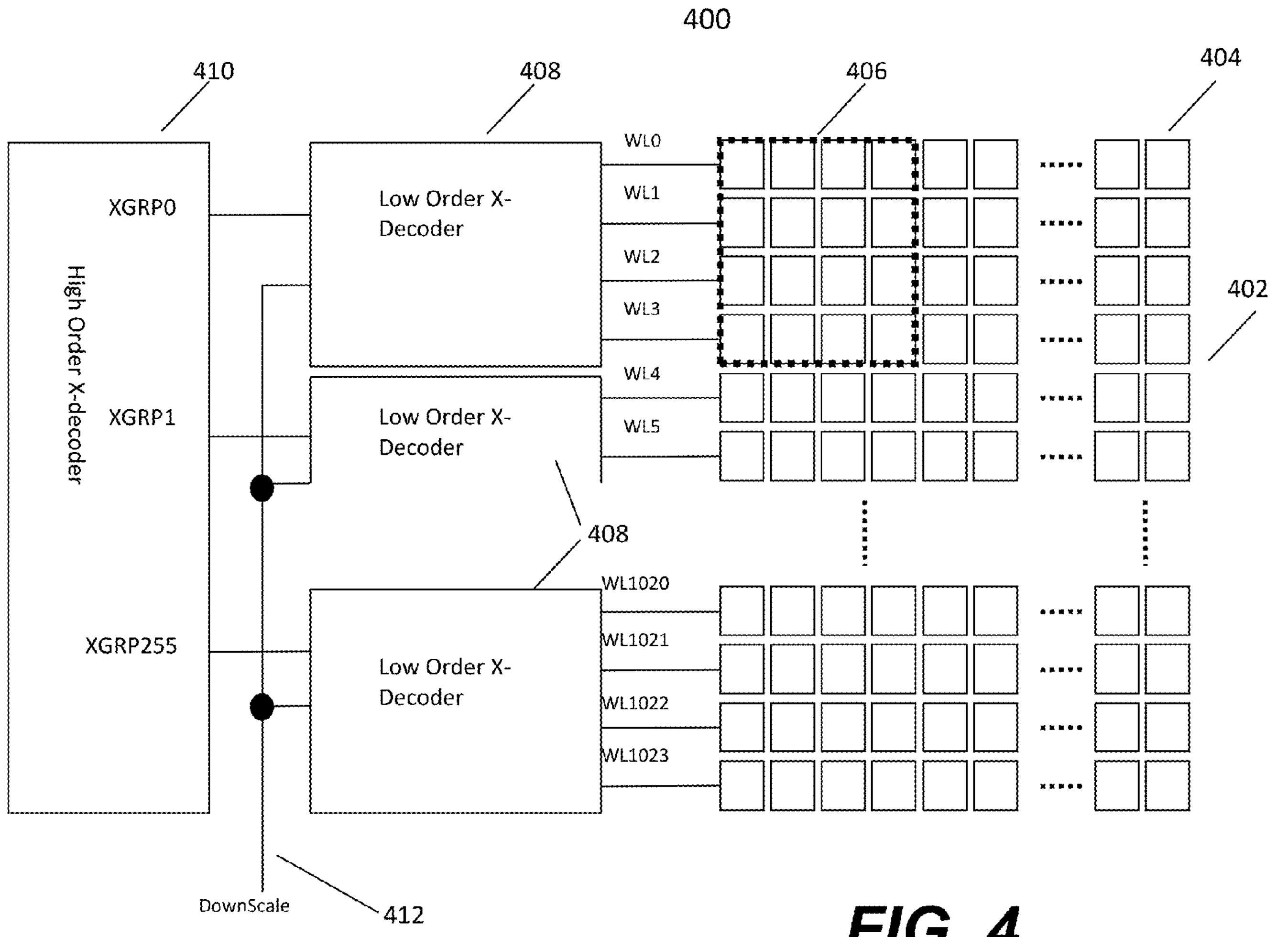

400
410
408
406
404
402
408
High Order X-decoder
XGRP0
XGRP1
XGRP255
Low Order X-Decoder
Low Order X-Decoder
Low Order X-Decoder
WL0
WL1
WL2
WL3
WL4
WL5
WL1020
WL1021
WL1022
WL1023
DownScale
412

FIG. 4

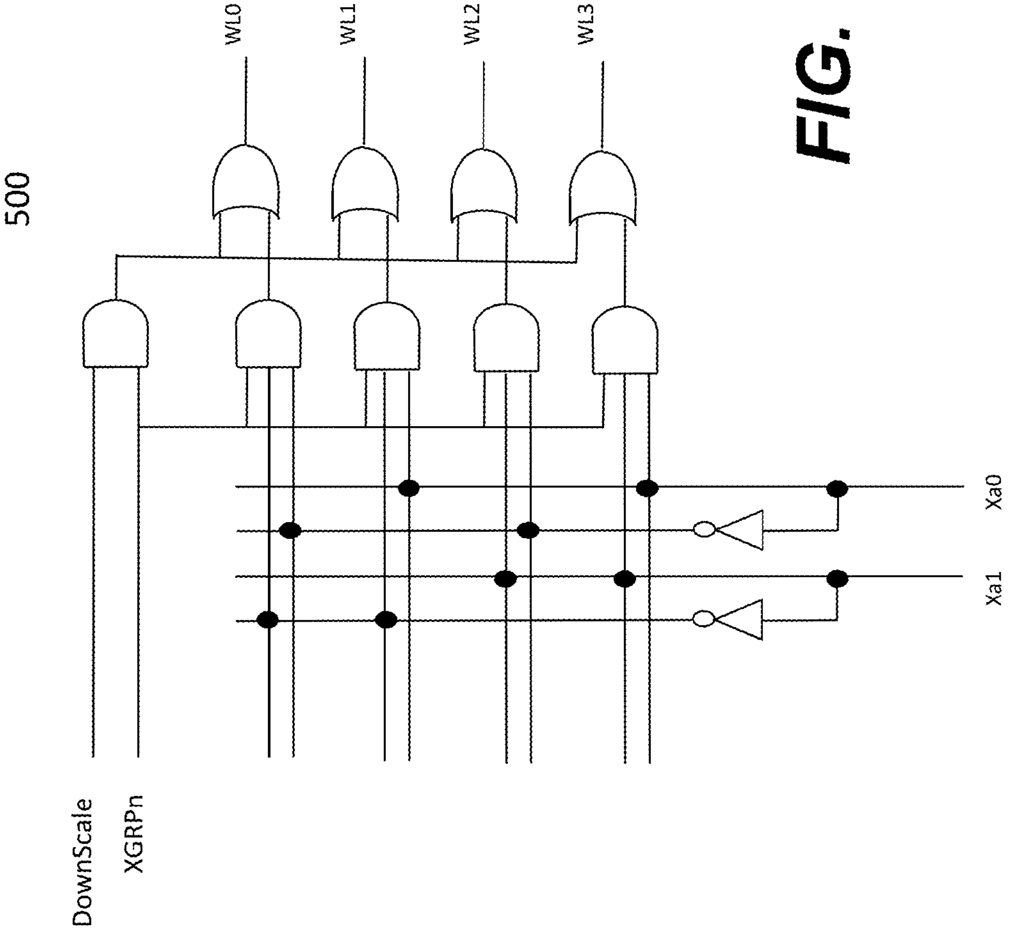


FIG. 5

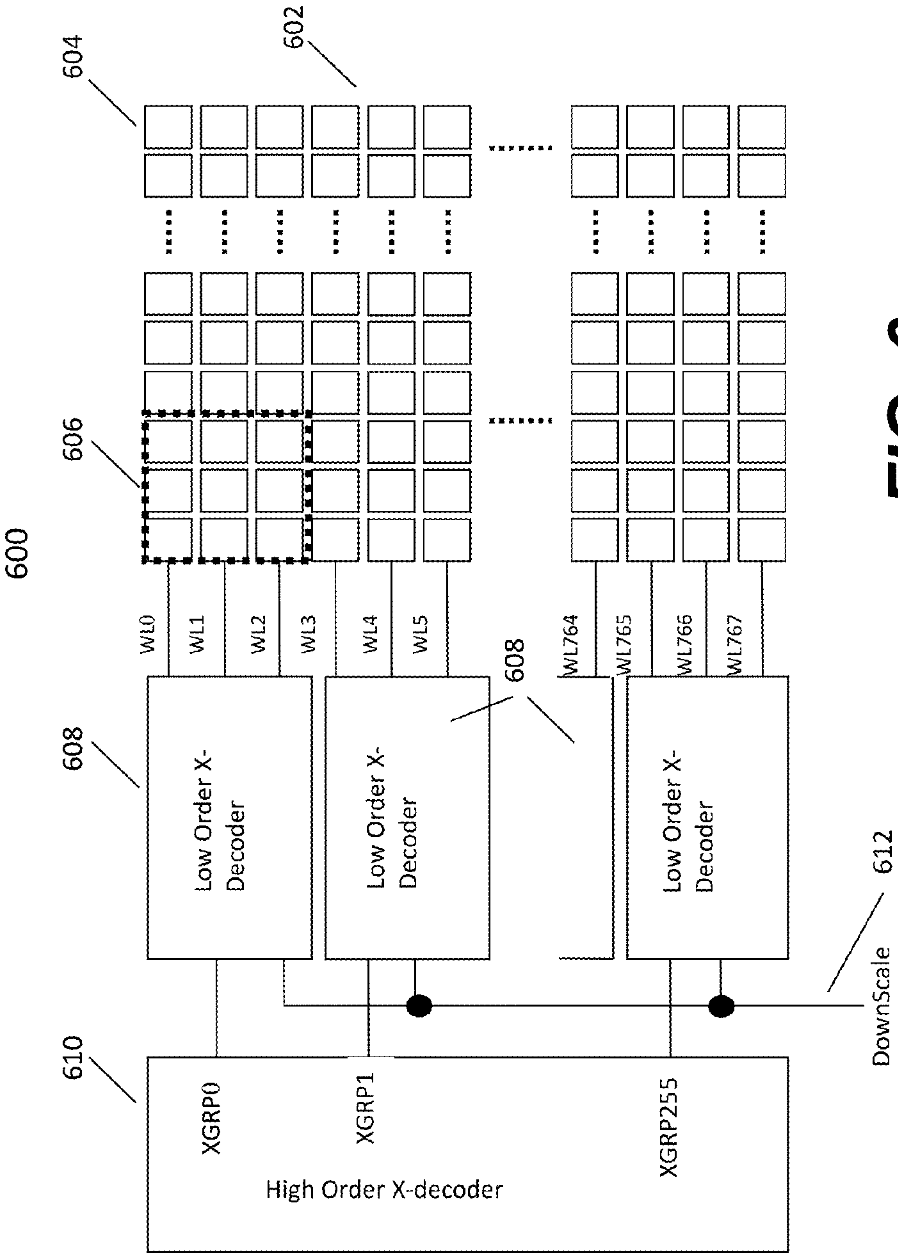

600
604
602
606
WL0
WL1
WL2
WL3
WL4
WL5
WL764
WL765
WL766
WL767
608
Low Order X-Decoder
Low Order X-Decoder
Low Order X-Decoder
612
DownScale
610
XGRP0
XGRP1
XGRP255
High Order X-decoder

FIG. 6

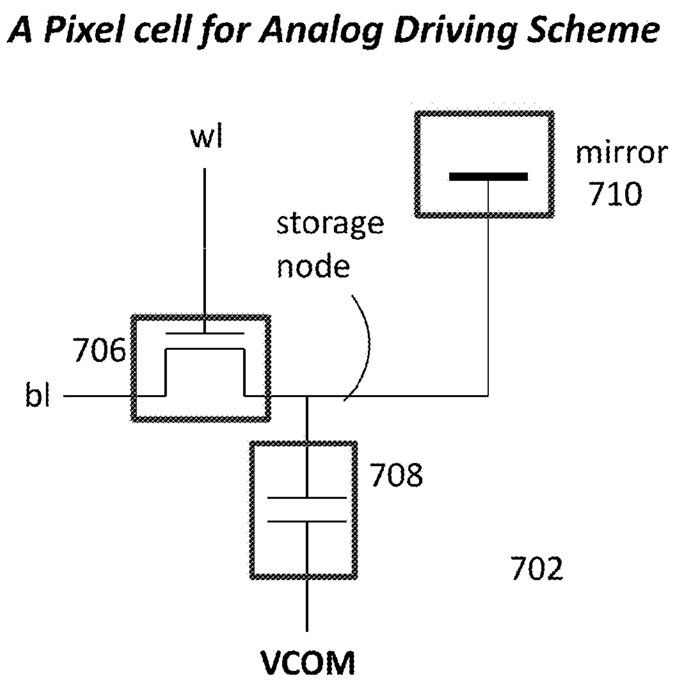

A Pixel cell for Analog Driving Scheme

FIG. 7A

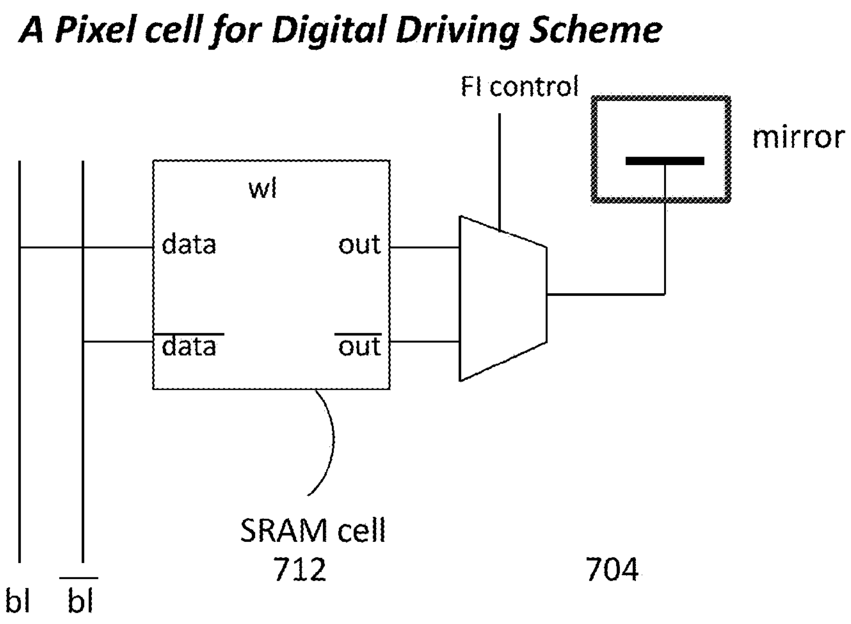

A Pixel cell for Digital Driving Scheme

FIG. 7B

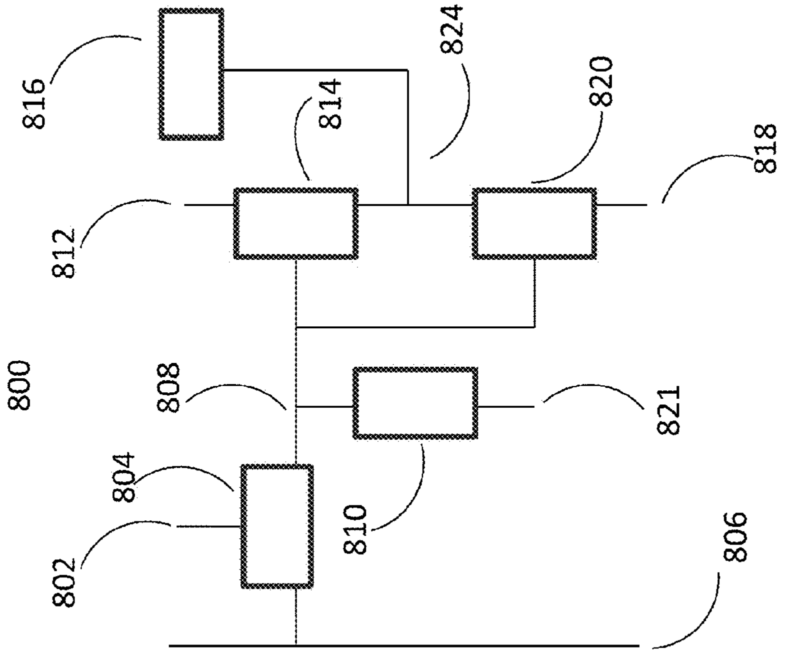

800
802
804
806
808
810
812
814
816
818
820
821
824

FIG. 8A

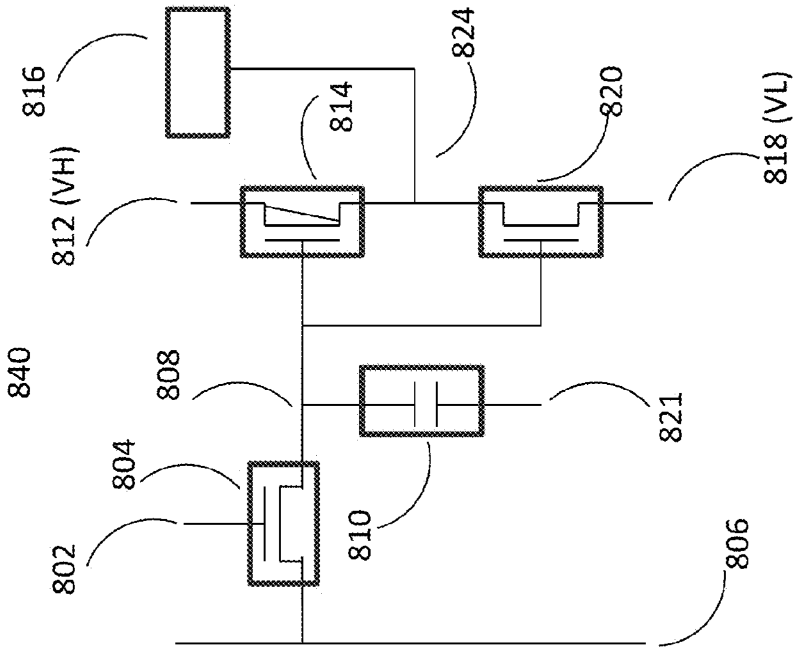

840
802
804
806
808
810
812 (VH)
814
816
818 (VL)
820
821
824

FIG. 8B

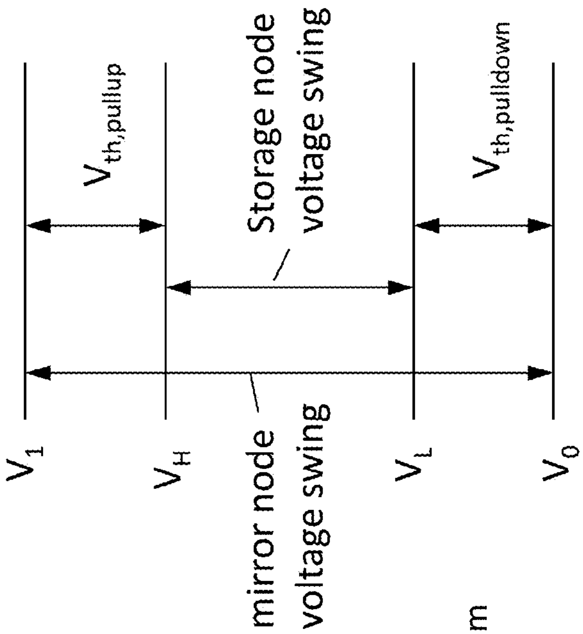

V1
VH
VL
V0
Vth,pullup
Storage node voltage swing
Vth,pulldown
mirror node voltage swing

FIG. 9B

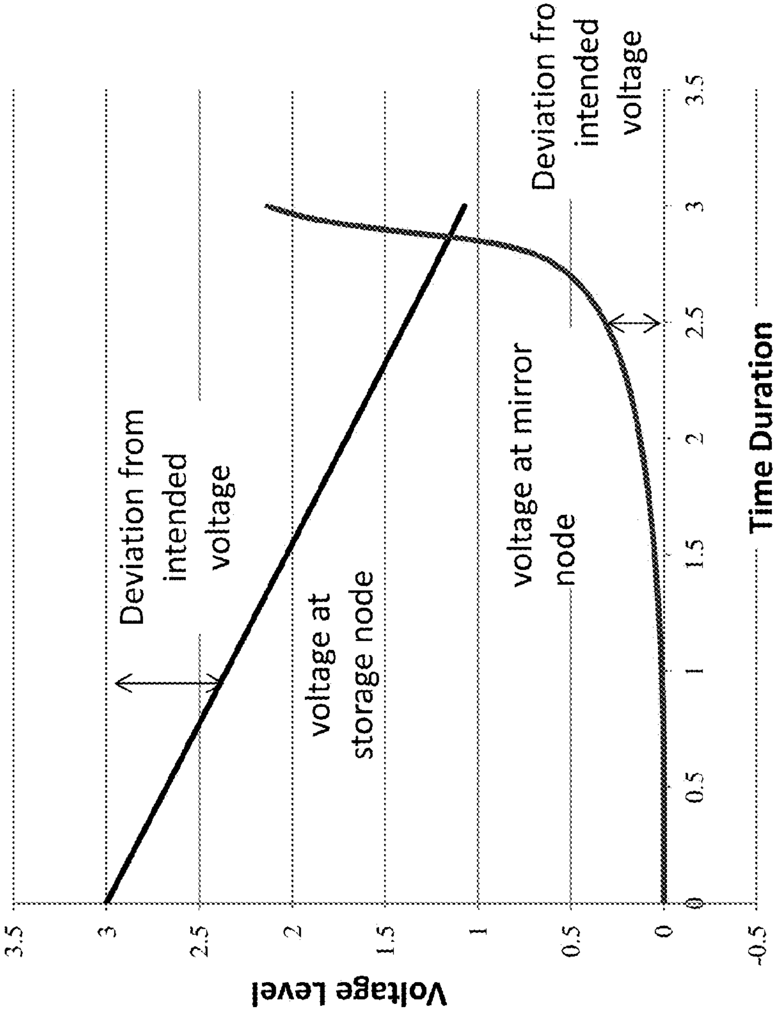

Voltage Level
3.5
3
2.5
2
1.5
1
0.5
0
-0.5
0
0.5
1
1.5
2
2.5
3
3.5
Time Duration
Deviation from intended voltage
voltage at storage node
voltage at mirror node
Deviation from intended voltage

FIG. 9A

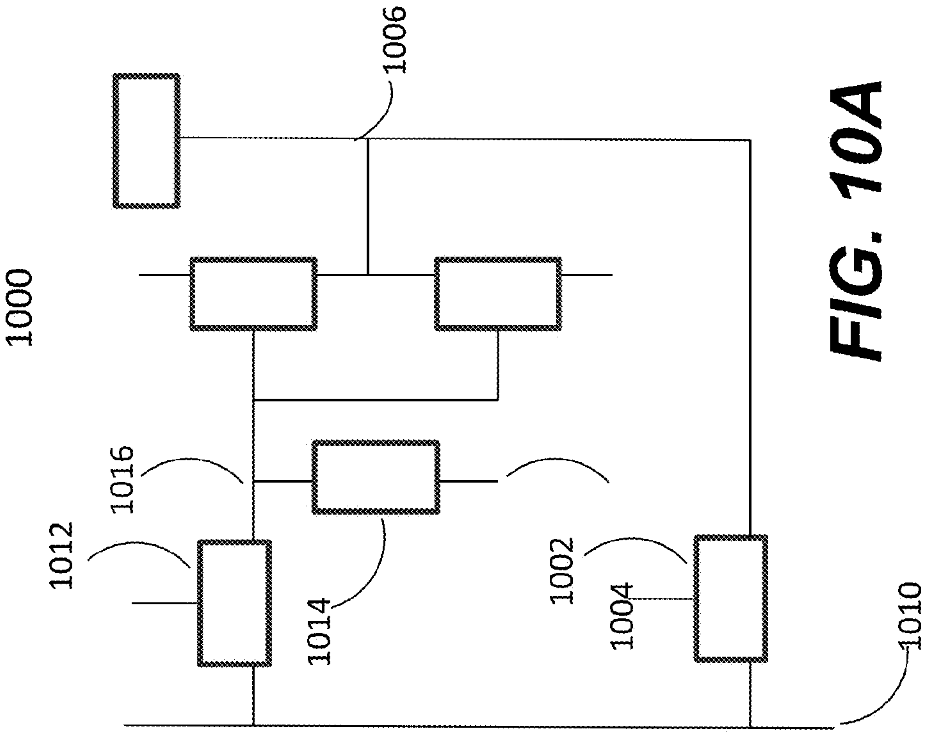


FIG. 10A

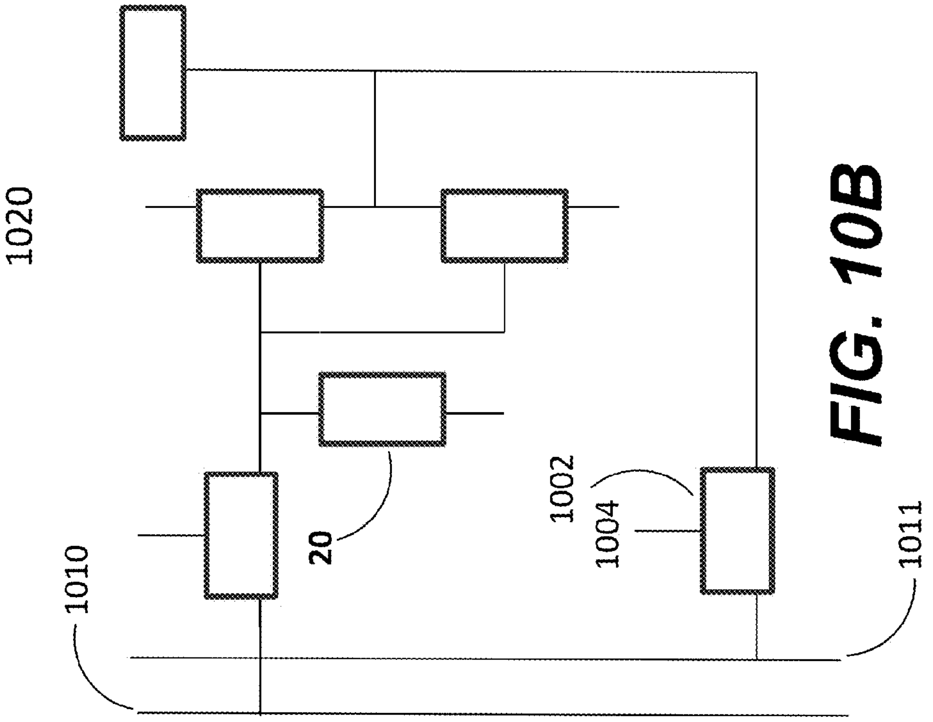


FIG. 10B

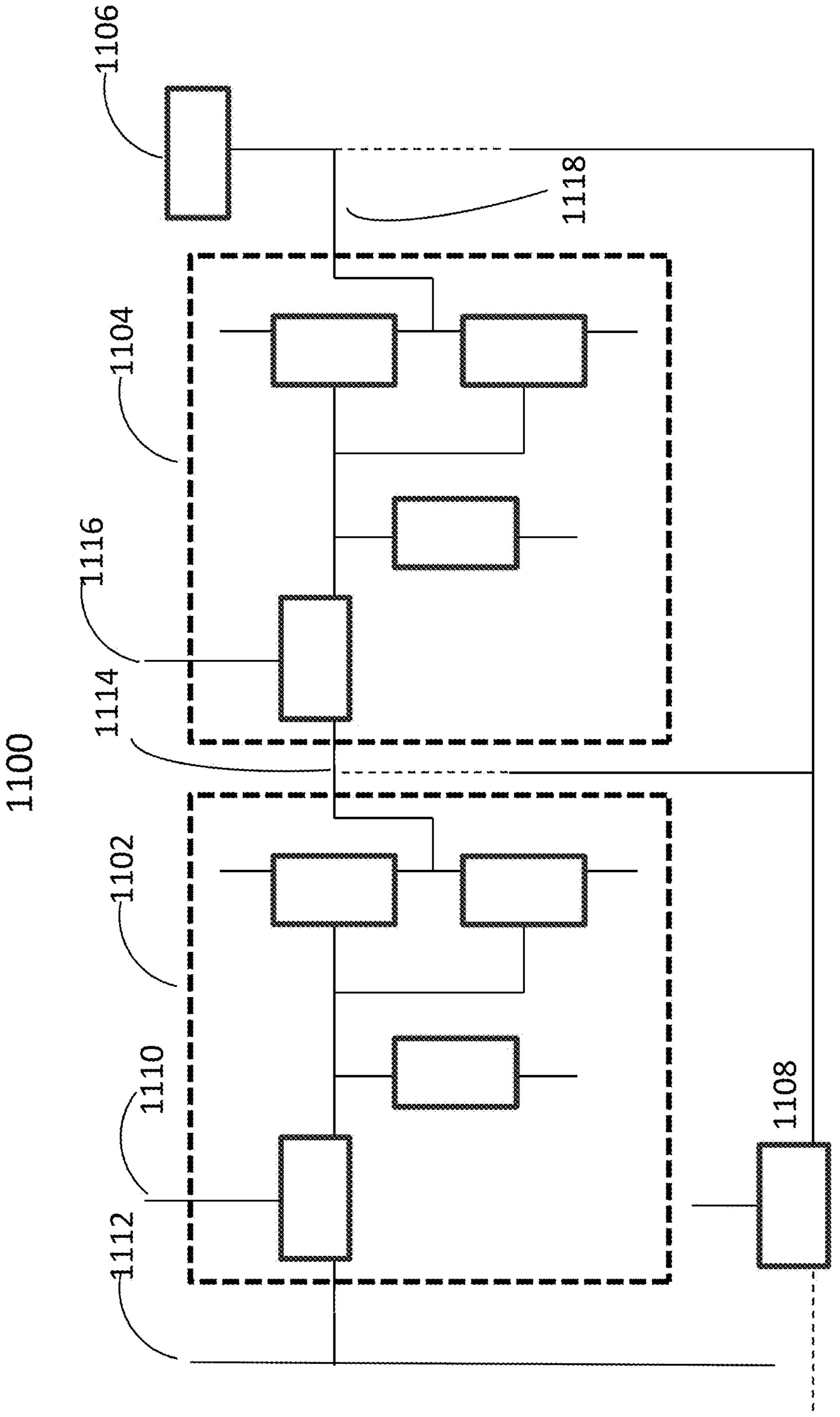


FIG. 11

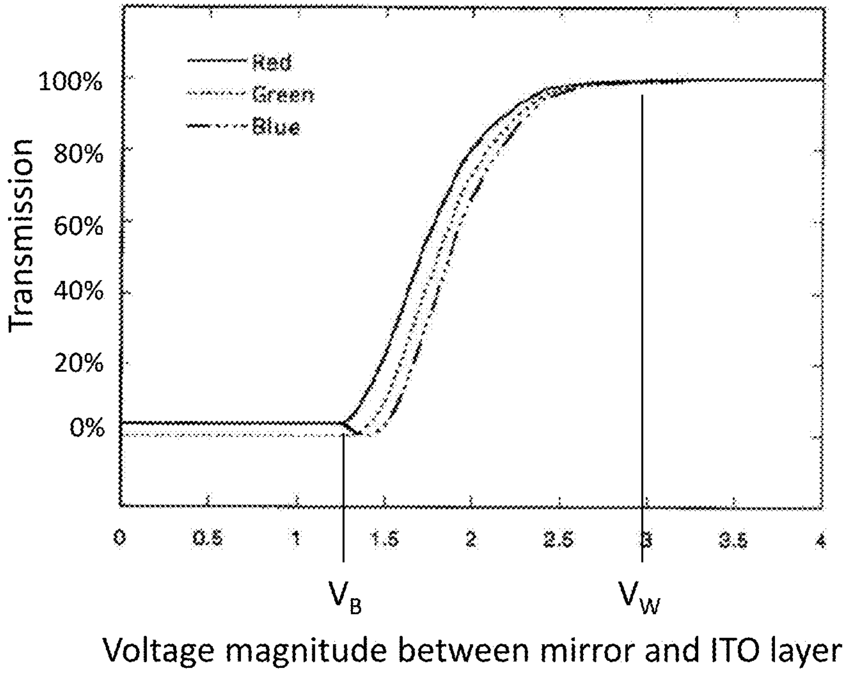
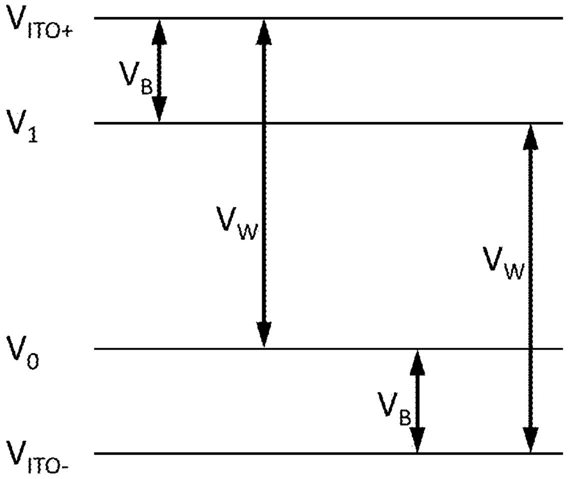


FIG. 12A



V_W: voltage when liquid crystal has maximum transmission

V_B: voltage when liquid crystal has minimum transmission

FIG. 12B

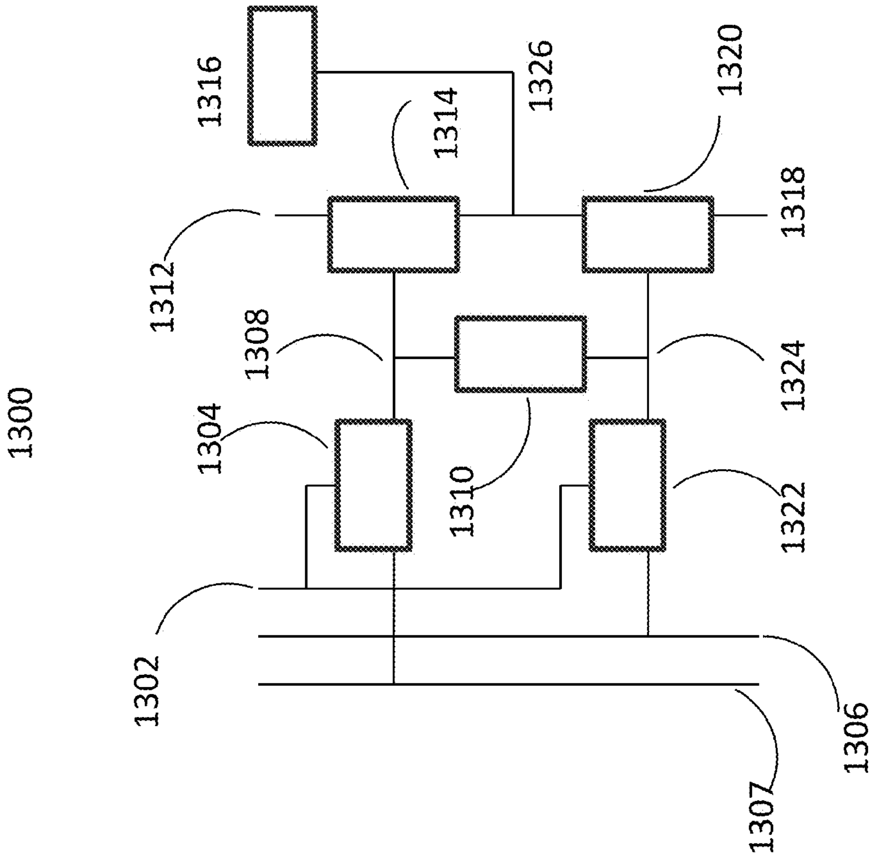


FIG. 13A

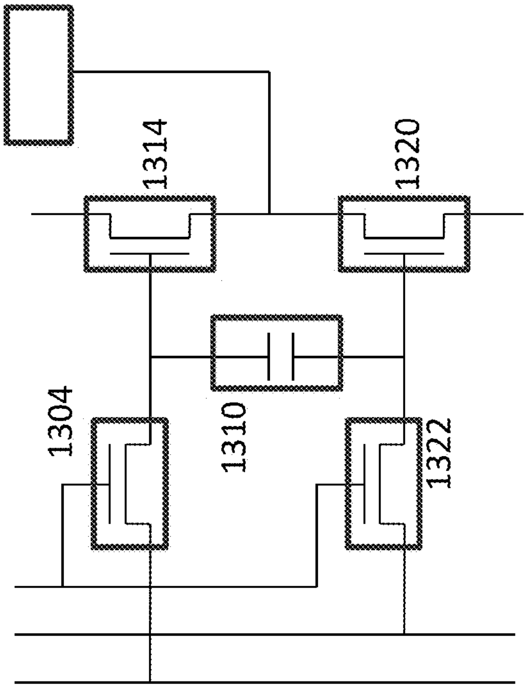


FIG. 13B

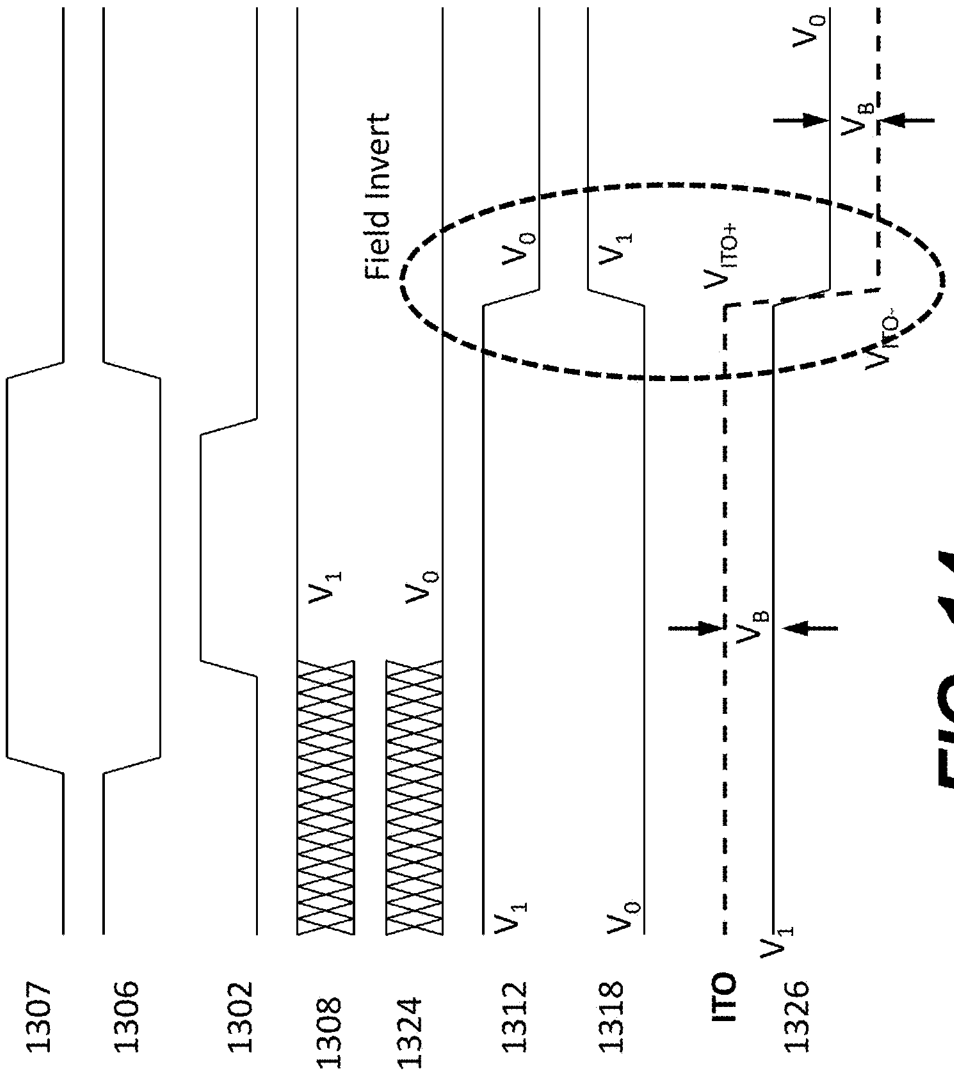

1307
1306
1302
1308
1324
1312
1318
ITO
1326
V_1
V_0
V_1
V_0
V_1
V_0
V_1
V_B
Field Invert
V_0
V_1
V_{ITO+}
V_{ITO-}
V_B
V_0

FIG. 14

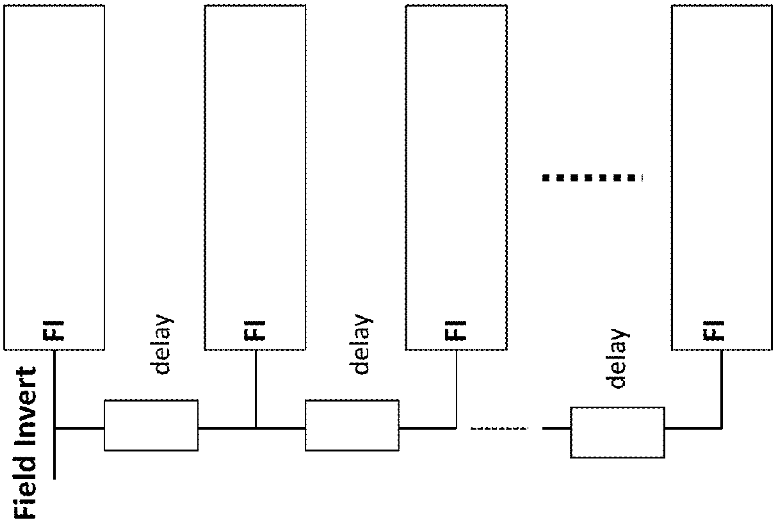


FIG. 15B

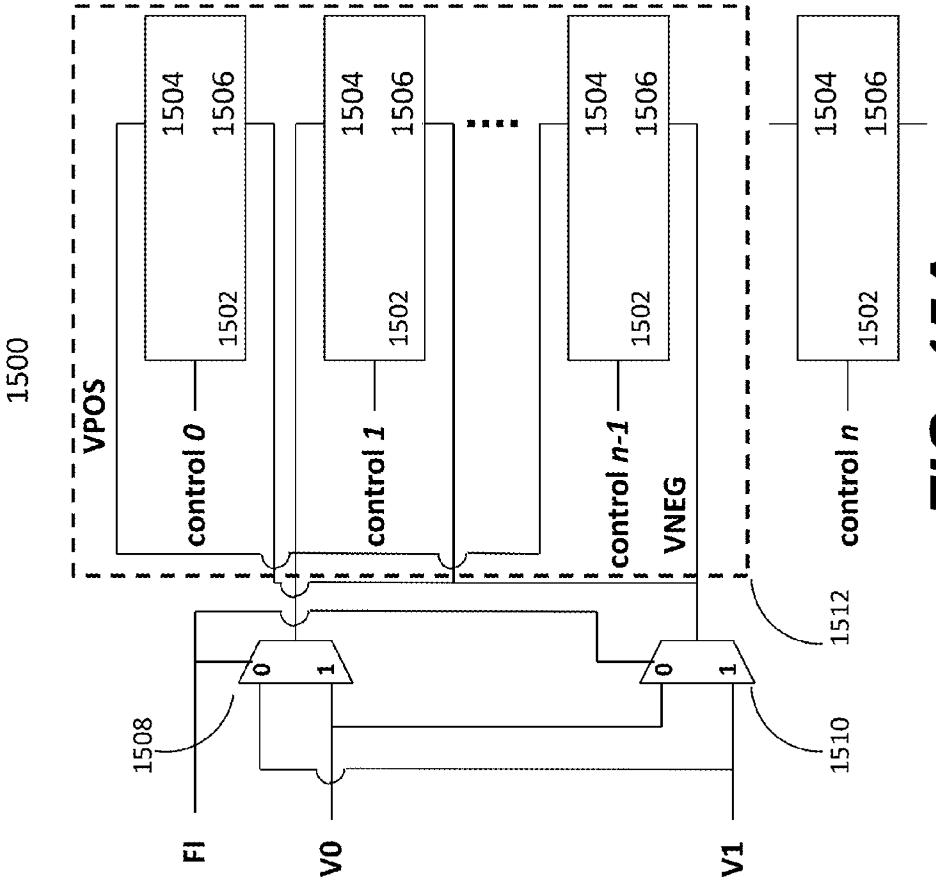


FIG. 15A

DISPLAY DEVICES WITH HIGH RESOLUTION AND SPATIAL DENSITY MODULATION ARCHITECTURE

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the priorities of the following provisional applications for all purpose: U.S. Prov. App. Ser. No. 61/858,669 entitled "Dynamic Pixel Cell with Field Invert", filed on Jul. 26, 2013, U.S. Prov. App. Ser. No. 61/859,289, entitled "Spatial Density Modulation and Programmable Resolution of Picture Element with Multiple Sub-image Elements on Image Array", filed on Jul. 28, 2013, and U.S. Prov. App. Ser. No. 61/859,968 entitled "Pixel Cell with Capacitor for Digital Modulation", filed on Jul. 30, 2013.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to the area of display devices and more particularly relates to architecture and designs of display devices, where the display devices are of high in both spatial and intensity resolutions, and may be used in various projection applications, storage and optical communications.

Description of the Related Art

In a computing world, a display usually means two different things, a showing device or a presentation. A showing device or a display device is an output mechanism that shows text and often graphic images to users while the outcome from such a display device is a display. The meaning of a display is well understood to those skilled in the art given a context. Depending on application, a display can be realized on a display device using a cathode ray tube (CRT), liquid crystal display (LCD), light-emitting diode, gas plasma, or other image projection technology (e.g., front or back projection, and holography).

A display is usually considered to include a screen or a projection medium (e.g., a surface or a 3D space) and supporting electronics that produce the information on the screen. One of the important components in a display is a device, sometime referred to as an imaging device, to form images to be displayed or projected on the display. An example of the device is a spatial light modulator (SLM). It is an object that imposes some form of spatially varying modulation on a beam of light. A simple example is an overhead projector transparency.

Usually, an SLM modulates the intensity of the light beam. However, it is also possible to produce devices that modulate the phase of the beam or both the intensity and the phase simultaneously. SLMs are used extensively in holographic data storage setups to encode information into a laser beam in exactly the same way as a transparency does for an overhead projector. They can also be used as part of a holographic display technology.

Depending on implementation, images can be created on an SLM electronically or optically, hence electrically addressed spatial light modulator (EASLM) and optically addressed spatial light modulator (OASLM). This current disclosure is directed to an EASLM. As its name implies, images on an electrically addressed spatial light modulator (EASLM) are created and changed electronically, as in most electronic displays. An example of an EASLM is the Digital Micromirror Device or DMD at the heart of DLP displays or Liquid crystal on silicon (LCoS or LCOS) using ferroelectric liquid crystals (FLCoS) or nematic liquid crystals (electrically controlled birefringence effect).

As the video technology advances, besides the spatial resolution, LCOS microdisplays look for means to increase the levels of gray shades, namely the intensity resolution, for better picture quality. One of the objectives in this patent is to disclose an architecture of display device suitable to be used in LCOS microdisplays, where the display device possesses high spatial resolution as well as high intensity resolution.

SUMMARY OF THE INVENTION

This section is for the purpose of summarizing some aspects of the present invention and to briefly introduce some preferred embodiments. Simplifications or omissions in this section as well as in the abstract and the title may be made to avoid obscuring the purpose of this section, the abstract and the title. Such simplifications or omissions are not intended to limit the scope of the present invention.

The present invention is generally related to architecture and designs of display devices, where the display devices possesses high spatial resolution as well as high intensity resolution and may be readily used in various projection applications, storage and optical communications. According to one aspect of the present invention, the display device includes an array of image elements, each of the image elements further includes an array of image sub-elements. These sub-image elements are driven by PWM as in digital modulation. Human eyes serve as a temporal filter as well as a spatial filter to an image or video. A portion of an image element area is turned on, namely, some of the sub-image elements are turned on, which has the same perceived effect of turning on an entire image element for a specific time. As the resolution of PWM is limited to the liquid crystal response time, modulating a portion of an image element area provides finer gray levels beyond what is currently available in digital modulation. In other words, image elements with sub-image elements increase the spatial resolution to break the limitation in the temporal intensity resolution due to the liquid crystal response time.

According to another aspect of the present invention, as referred to herein as gray level driving scheme, a hybrid approach is described to address the limitations in both digital drive scheme and analog drive scheme. An n-bit gray scale is first divided into two parts. The m most significant bits (MSB) of the n-bit gray scale form a group to generate 2^m of distinct voltage levels between two voltages, and remaining n−m bits of the gray scale are implemented with 2^{n-m} pulses of equal duration in one frame, similar to count-based Pulse Width Modulation (C-PWM) in digital drive scheme. Assigning more bits to the MSB group greatly reduces the total bit count needed to implement the n-bit gray scale, gradually approaching the bit count of analog drive scheme, resulting in a finer gray scale.

According to still another aspect of the present invention, designs of an image element or a sub-image element are described to achieve the high resolution display devices, both in spatial and intensity. In one embodiment, a display device is designed to include a plurality of image elements, each of the image elements including a set of sub-image elements arranged in rows and columns, each of the sub-image elements addressed by a control line and a data line, and a driving circuit provided to drive the image elements in accordance with a video signal to be displayed via the display device, the driving circuit designed to turn on a portion of each of the image elements to achieve similar perceived effect of having the each of the image elements turned on for a predefined time.

According to yet another aspect of the present invention, only some of the sub-image elements in an image element are tuned on in response to a brightness level assigned to the image element to achieve an intensity level in a much finer scale.

The present invention may be implemented as an apparatus, a method, a part of system. Different implementations may yield different benefits, objects and advantages. In one application, the display device is employed in a holographic projector to advantageously display an image or video on a medium (e.g., the 3D space).

There are many other objects, together with the foregoing attained in the exercise of the invention in the following description and resulting in the embodiment illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, aspects, and advantages of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings where:

FIG. **1** shows an example of a display device to show how image elements are addressed;

FIG. **2**A illustrates graphically the concept of brightness equivalence between PWM and SAM;

FIG. **2**B shows that, for the SAM modulation, gray levels of sub-image elements can be written with one plane update;

FIG. **2**C lists the number of patterns available for the same binary weighed gray level for a 4×4 sub-image element array;

FIG. **3**A illustrates an exemplary waveform of a storage node in a pixel element when this hybrid driving scheme is applied;

FIG. **3**B shows a new cell that is so designed to perform both digital and analog pixel driving scheme (a.k.a., hybrid driving method);

FIG. **4** shows a block diagram of an implementation when the number of rows and columns of the sub-image elements in an image element are in the power of 2;

FIG. **5** shows one exemplary implementation of a low order X-decoder that may be used in FIG. **4**;

FIG. **6** shows an example of block diagram of an implementation when the number of rows or columns of the sub-image elements in an image element is 3;

FIGS. **7**A and **7**B show respectively two functional diagrams for the analog driving method and digital driving method;

FIG. **8**A shows a functional block diagram of an image element according to one embodiment of the present invention;

FIG. **8**B shows an exemplary implementation of the block diagram of FIG. **8**A in CMOS;

FIG. **9**A shows an implementation greatly extending the duration of a valid signal and removing the need of refresh operation;

FIG. **9**B shows that a pull-up device remains non-conducting as long as $|V_{th,\ pullup}|>V_1-V_H\ V_H$ and a pull-down device remains non-conducting as long as $V_{th,\ pulldown}>V_L-V_0$;

FIG. **10**A shows one embodiment of a pixel with read back operations;

FIG. **10**B shows that a data node is removed from a read pass device and replaced with another data node;

FIG. **11** shows an embodiment of an image element with planar update where there two proposed pixel cells, a mirror plate and a pass device for read back;

FIG. **12**A and FIG. **12** B show, respectively, a voltage magnitude curve between the mirror and ITO layers and relationships among the voltages applied thereon;

FIG. **13**A shows one exemplary embodiment of a pixel cell with field invert;

FIG. **13**B shows an exemplary implementation of FIG. **13**A in CMOS;

FIG. **14** shows voltages at respective nodes; and

FIG. **15**A shows a functional block diagram of cascading several field inverters; and

FIG. **15**B shows a time delay element is inserted between two groups of field inverters.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The detailed description of the invention is presented largely in terms of procedures, steps, logic blocks, processing, and other symbolic representations that directly or indirectly resemble the operations of data processing devices coupled to networks. These process descriptions and representations are typically used by those skilled in the art to most effectively convey the substance of their work to others skilled in the art.

Reference herein to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment can be included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment, nor are separate or alternative embodiments mutually exclusive of other embodiments. Further, the order of blocks in process flowcharts or diagrams representing one or more embodiments of the invention do not inherently indicate any particular order nor imply any limitations in the invention.

Referring now to the drawings, in which like numerals refer to like parts throughout the several views. FIG. **1** shows an example of a display device **100** to show how image elements are addressed. As is the case in most memory cell architecture, image elements or pixels are best accessed via decoding a sequence of pre-determined address bits to specify the location of a target image element. These pre-determined address bits are further divided into X-address bits and Y-address bits. The X-address bits decode the location of control line (word line) of an image element while the Y-address bits decode the location of data line (bit line) of the image element. The set of circuits that decode the X-address bits into selected control lines (word lines) is called X-decoder **102**. The set of circuits that decode Y-address bits into selected data lines (bit lines) is called Y-decoder **104**.

In general, there are two driving methods, analog and digital, to provide a gray level to each of the image elements. As used herein, gray or a gray level implies a brightness or intensity level, not necessarily an achromatic gray level between black and white. For example, a red color is being displayed, in which case a gray level of the color means how much red (e.g., a brightness level in red) to be displayed. To facilitate the description of the present invention, the word gray will be used throughout the description herein. In the analog driving method, the gray level is determined by a voltage level stored in a storage node. In the digital driving method, the gray level is determined by a pulse width modulation (PWM), where the mixture of an ON state voltage duration and an OFF state voltage duration results in a gray level through the temporal filtering of human eyes. To increase the intensity resolution of the display device **100**, for better picture quality, both of the analog and digital methods have limitations in increasing the resolution in intensity.

With analog driving method, one gray level is often limited to a minute swing of voltage range, usually in mV range, which makes the gray level sensitive to any source that can cause a voltage level to change. Such exemplary sources include leakage currents of MOS transistors and switching noise. In order to overcome such issues and extend the voltage tolerance on a gray level, LCOS microdisplay manufacturers often resort to high voltage process technologies instead of taking advantage of the general logic process. The use of high voltage devices, in turn, limits the size of image element. In addition, the analog driving method is prone to manufacturing process parameter mismatch, both inside the chip and from chip to chip.

On the other hand, the digital driving method relies on pulse width modulation (PWM) to form an equivalent gray level accumulatively. This process needs to write data to the image elements several times. The gray level resolution is bounded by the minimal time duration that the liquid crystal can respond to. As a result, users of the digital driving scheme often look for liquid crystals with fast response time to overcome the limitation.

Most of digital pixel drive schemes control the width of a single pulse of a fixed amplitude output from each pixel during a frame period (Single Pulse Width Modulation, or S-PWM), a sequence of identical individual pulse from each pixel during a frame period (Count-based Pulse Width Modulation, C-PWM), or a sequence of binary-weighted-in-time individual light pulses from each pixel during a frame period (Binary-Coded Pulse Width Modulation, or B-PWM). The use of time domain digital modulation assumes that the electro-optical response of LC responds to the RMS drive signals, allowing an analog electro-optical response to be controlled by the duty cycle of a square wave as in B-PWM, or a sequence of binary-weighted square waves as in C-PWM.

According to one embodiment of the present invention, a sub-image element approach is used to achieve what is referred herein as a hybrid driving scheme, namely some are driven using the digital driving method and others are driven by the analog driving method. When dividing an image element (a.k.a., a pixel) into sub-pixels of equal size, for example, n subpixels, 2^n sub-pixels are sufficient to produce 2^n gray levels or n-bit grayscale. When an image element is divided into an array of smaller and, perhaps, identical image elements (i.e., sub-image elements), the array may have one or more rows of sub-image elements and one or more columns of sub-image elements. Each sub-image element can be independently programmed through their associated control lines and data lines.

These sub-image elements are driven by PWM as in digital modulation. Human eyes serve as a temporal filter as well as a spatial filter to an image or video. Turning on brightening a portion of an image element area has the same perceived effect of turning on or brightening an image element for a particular time. As the resolution of PWM is limited to the liquid crystal response time, modulating a portion of an image element area provides finer gray levels beyond what is currently available in digital modulation. In other words, image elements with sub-image elements increase the spatial resolution to break the limitation in the temporal intensity resolution due to the liquid crystal response time.

The process of modifying the ON state and OFF state of sub-image elements to generate additional gray levels is referred to herein as "spatial area modification" (SAM). FIG. **2**A illustrates graphically the concept of brightness equivalence between PWM and SAM. As fast responding liquid crystal material may not have all the characteristics suitable for applications, adopting the SAM modulation can widen the material selection to a broader range of liquid crystals. In addition, the SAM modulation can always achieve a fraction of minimal PWM modulation brightness. FIG. **2**A shows that an image element includes an array of smaller and identical image elements (sub-image elements). Each of the sub-image elements can be independently programmed through their associated control lines and data lines.

In the conventional PWM digital modulation, the complete array of image elements can only be programmed with data of the same gray level weighting. Data of different gray level weighting needs another update of entire plane (e.g., all elements in the array are refreshed). The cumulative effect of multiple plane updates with different gray levels produces the desired overall gray level.

In FIG. **2**A, an element **200** has 16 sub-image elements, all of which are driven to be ON entirely at T**1**, which is equivalent to a full brightness (white). On the other side, the element **200** is driven to be OFF entirely at another time (not shown), which is equivalent to a full darkness (black). When some of the sub-image elements in the element **200** are turned on (i.e., ON) or off (i.e., OFF) at different times (e.g., T**2**, T**3**, T**4** or T**5**), resulting in various gray levels. All of the perceived gray levels are corresponding to what a single image element could produce when controlled by the PWM digital modulation.

FIG. **2**B shows that, according to one embodiment, for the SAM modulation, gray levels of sub-image elements can be written with one plane update. As programming a gray level of 1011 to an image element with 4×4 sub-image elements would require turning on 11 sub-image elements as: 1×(8 sub element)+0×(4 sub element)+1×(2 sub elements)+1×(1 sub element)=11 sub-elements. Thus it can be concluded that any pattern with 11 sub-elements turned on can match the gray level. According to one embodiment, instead of writing sequentially with 4 plane updates, the gray level in the SAM modulation can be written with one plane update.

The examples in FIG. **2**A and FIG. **2**B both imply a linear relationship between the area of image element and the perceived brightness. It may not be the case in reality. As the pulse width of spatial density modulation is still limited to the response time of the liquid crystals, the responding rise and fall time of the liquid crystals may produce a brightness level not necessarily proportional to the percentage of the area being turned on. According to one embodiment, a lookup table is provided to cross-reference a target gray level versus the number of sub-image elements.

When the image element does not require full brightness or full darkness, there is more than one pattern of sub-image element array that can satisfy the required number of sub-image elements. FIG. **3** lists a table showing the number of patterns available for the same binary weighed gray level for a 4×4 sub-image element array. There are many ways of determining the corresponding location of sub-image elements to the binary weights and gray levels.

Fixed Location: the number and location of sub-elements corresponding to a specific gray level are fixed. This is the easiest way of implementing the spatial area modulation.

Rotation: for each binary weighed gray level, a certain number of patterns are selected. These patterns follow a pre-determined sequence to be the pattern of sub-element array for a specified gray level. In video or images, an area with no or little gray shade difference can result in contour artifact. Rotating the pattern of a sub-element array reduces the effect as the image never "sticks" while showing the same gray level. The number of patterns depends on their availability as well as the limitation in implementation. Implementation can be done through the use of a look-up table or a state machine to scramble through the patterns.

Random Selection: each binary weighed gray level has a certain number of patterns to display. However, the pattern of sub-element array for the gray level is randomly chosen. This scheme has the benefit of further reducing the contour issue as even neighboring image elements can display different patterns while showing the same gray level. The number of patterns depends on their availability as well as the limitation in implementation. An exemplary implementation is the use of a look-up table with a random pointer or a state machine to randomly choose the patterns.

Algorithms: with a determined number of sub-image elements for the gray level, the pattern of the array is generated through a pre-determined computational algorithm. The algorithm can take into account of multiple purposes: lateral liquid crystal fringing field, patterns of surrounding image elements, compensation of gray level digitization. It can be implemented with several image processing techniques, such as image enhancement, image sharpening, motion estimation motion compensation (MEMC). It can also utilize skills like digital halftoning or error diffusion commonly used in printing. The details of the algorithms are not to be further described to avoid obscuring aspects of the present invention.

According to one embodiment, when display with additional gray levels is not needed, the sub-image element array is treated as just one image element. All the sub-image elements receive the same data simultaneously. As the sub-image elements are uniform, it can be treated as down-scaling the resolution. For example, a display with 1920×1080 image elements with each element containing 2×2 sub-element array can also be viewed as a display with 3840×2160 image elements, i.e., all the sub-element are now promoted to an element.

As described above, a display device or microdisplay with an array of image elements can be scaled down in resolution as an array of a lower resolution microdisplay when a plural number of rows and columns of sub-image elements in each image element are merged, or turned on or off simultaneously. For example, a microdisplay can be treated as having m rows of image elements and n columns of image elements with each image element having a rows of sub image elements and b columns of sub-image elements, provided that the native image element array has m×a rows and n×b columns, where numbers, a, b, m, and n are positive integers.

When the display resolution is scaled down, video inputs to the display are scaled down accordingly. All sub-image elements of an image element are treated as part of the image element and therefore would be programmed to be read out as an identical (or averaged) gray value simultaneously. All the control lines associated to a rows of sub image elements need to be selected simultaneously and all the data lines associated to b columns of sub image elements need to be selected simultaneously as well.

Referring back to FIG. **1**, the X-decoders **102** provided to select the control lines of the rows and the Y-decoders **104** provided to select the data lines of the columns need to be modified accordingly. In this case, the X-address bits are divided into two parts: low order X-address bits and high order X-address bits. It is assumed that the number of X-address bits required to decode the control lines are u bits, and denoted u−1, u−2, . . . , 1, 0, with address 0 being the lowest order bit. The low order X-address bits are i−1, i−2, . . . , 1, 0, such that 2^i=a if a is a power of 2, or i is the minimum integer satisfying 2^i>a if otherwise. As a result, there are u−i bits of high order X-address bits and denoted u−1, u−2, . . . , u−i. The X-decoder is divided into two parts as well: the low order X-decoder that decodes with low order bits i−1, i−2, . . . , 1, 0, and the high order X-decoder that decodes with high order bits u−1, u−2, . . . , u−i.

Similar approaches can be done with the Y-address bits. It is assumed that the number of Y-address bits required to decode the data lines are v bits, and denoted v−1, v−2, . . . , 1, 0, with address 0 being the lowest order bit. The low order Y-address bits are j−1, j−2, . . . , 1, 0, such that 2^i=b if a is a power of 2, or j is the minimum integer satisfying 2^i>b if otherwise. As a result, there are v−j bits of high order Y-address bits and denoted v−1, v−2, . . . , v−j. The Y-decoder is divided into two parts as well: the low order Y-decoder that decodes with low order bits j−1, j−2, . . . , 1, 0, and the high order Y-decoder that decodes with high order bits v−1, v−2, . . . , v−j.

When the display resolution is down scaled to a lower resolution, decoding from the low order address bits is not needed. By applying a control signal, DownScale, to force the outputs of low order decoder to be logic "1", all the control lines of the target image element are selected.

Given a display device with the proposed sub-image elements, a corresponding driving method shall be used to take the advantage of the architecture. As described above, either one of the digital driving method and analog driving has its own limitations. According to one embodiment of the present invention, a mixed use of the digital driving method and analog driving method, referred to herein as a hybrid driving scheme, is proposed to address the limitations in both digital drive scheme and analog drive scheme. It is assumed that a display device is provided to display n-bit gray scale. The n-bit gray scale is first divided into two parts. The m most significant bits (MSB) of the n-bit gray scale form a group to generate 2^m of distinct voltage levels between two voltages, for example, a high voltage V_H and a low voltage V_L. These distinct voltage levels are denoted as V_0, V_1, V_2, . . . V_{2^m-1} respectively, with V_0=VL and V_{2^m-1}=VH. Similar to the analog drive scheme, these voltage levels can be generated from a digital-to-analog converter (DAC). The remaining n−m bits of gray scale are implemented with 2^{n-m} pulses of equal duration in one frame, similar to Count-based Pulse Width Modulation (C-PWM) in digital drive scheme. However, unlike the C-PWM modulation, these pulses do not produce V_H amplitude for logic "1" pulses, nor produce V_L amplitude for logic "0" pulses. Instead, these 2^{n-m} pulses have an amplitude of V_h for logic "0" pulses and an amplitude of V_{h+1} for logic "1" pulses, where V_h is a voltage level selected from V_0, V_1, V_2, . . . V_{2^m-1} voltage levels by the m-bit MSB group. V_h represents the lowest voltage possible for a targeted gray level, while V_{h+1}, the voltage one level higher than V_h, represents the upper bound of the targeted gray level.

According to one embodiment, FIG. **3**A illustrates an exemplary waveform of a storage node in a pixel element when this hybrid driving scheme is applied. It can be noted that it only takes m bit per pulse to generate the amplitude V_h for logic "0" pulse and V_{h+1} for logic "1" pulses. The logic "0" and logic "1" toggling is embedded in the m bits for a pulse. The total number of data bits required for one pixel per frame to complete the 2^n gray scale modulation is $m \times 2^{n-m}$. In comparison, a pure C-PWM scheme requires 2^n pulses with 1 bit per pulse to distinguish logic "0" pulses and logic "1" pulses. A total of 2^n bits per pixel per frame are needed. Assigning more bits to the MSB group greatly reduces the total bit count needed to implement the n-bit gray scale, gradually approaching the bit count of analog drive scheme.

Reducing the bit count per frame can either reduce the power consumption by slowing down the operating frequency, or increase the gray scale with the same power budget. As pulses are part of the modulation scheme, the refresh rate to the storage node is considerably higher than what is necessary in the analog driving scheme. A high refresh rate reduces the voltage variation to the storage node when in high impedance state.

Any pixel in an array only toggles between one voltage level and its adjacent voltage level. As to the digital modulation in C-PWM, the voltage on a storage node changes between V_H and V_L. The reduced voltage swing greatly minimizes the digital switching noise. The magnitude of switching noise reduces with the amplitude. Thus, a dark area has minimal noise.

According to one embodiment of the present invention, FIG. **3**B shows a new cell **310** that is so designed to perform both digital and analog pixel driving scheme (a.k.a., hybrid driving method). It includes two MOS transistors **312** and **314**, one being p-typed MOS transistor (PMOS) and the other being n-typed MOS transistor (NMOS). One of the NMOS diffusion terminals (source or drain) is tied to one of the PMOS diffusion terminals (source or drain). This common diffusion terminal is then coupled or connected to a line that is common to all pixels in a column of an image element array. This common line to all elements in a column is usually referred as a bit line. The other NMOS diffusion terminal is also tied to the other diffusion terminal of PMOS and coupled to the internal storage node of the element, where a storage element **316** (e.g., a capacitor) resides. The storage node **318** is coupled to or connected to a metal (e.g., aluminum) electrode that biases the liquid crystal in the cell. The gate of the NMOS transistor is connected to a bus line that is common to the gate of NMOS transistors of all pixels in a given row of a pixel array. The gate of the PMOS transistor is connected to another bus line that is common to the gate of PMOS transistors of all pixels in a given row of a pixel array. We referred the bus line connecting the gate of NMOS transistors of all pixels in a given row of a pixel array as NMOS word line, the bus line connecting the gate of NMOS transistors of all pixels in a given row of a pixel array as PMOS word line.

The formation of one NMOS transistor and one PMOS transistor with both ends of terminals tied together forms a transmission gate that can selectively block or pass a signal level from one terminal to the other terminal. When the gate of NMOS transistor is applied a high voltage level (usually denoted as logic "1"), the complementary low voltage level (denoted as logic "0") is applied to the gate of PMOS transistor, allowing both transistors to conduct and pass the signal from one terminal to another. When a low voltage level (logic "0") is applied to the gate of NMOS transistor and a high voltage level (logic "1") is applied to the gate of PMOS transistor, both transistors turn off and there is no conduction path between the two terminals of the transmission gate. The internal storage node is said to be in high impedance state. The voltage level of the internal storage node remains the same as the storage element retains the electrical charge.

One of the benefits, objects and advantages of the cell architecture of FIG. **3**B is Cancelling Coupling Effect, Balanced ON Resistance for different Voltage Level, Compact Design and Full Voltage Swing.

Cancelling Coupling Effect: the gate polarity of an NMOS transistor is opposite to the gate polarity of a PMOS transistor. Changing the gate of the NMOS transistor from a low voltage level to a high voltage level forms a conduction path between two diffusion terminals of the NMOS transistor. Changing the gate of a PMOS transistor from a high voltage level to a low voltage level forms a conduction path between two diffusion terminals of the PMOS transistor. Likewise, changing the gate of an NMOS transistor from a high voltage level to a low voltage level turns off the conduction path between two diffusion terminals of the NMOS transistor. Changing the gate of a PMOS transistor from a low voltage level to a high voltage level turns off the conduction path between two diffusion terminals of the PMOS transistor. When turning off the MOS transistors, signals switching at the gate of a MOS transistor can alter the amount of electric charge stored at the diffusion terminal through the parasitic capacitance between the gate and the diffusion terminal. Changing stored electric charge changes the voltage level on the internal storage node. The proposed pixel cell has an NMOS transistor and a PMOS transistor to form a transmission gate. The opposite gate polarity can cancel out the coupling effect as the coupling from the NMOS transistor offsets the coupling from the PMOS transistor.

Balanced ON Resistance for Different Voltage level: a line that is common to all pixels in a column of the pixel array. The gate of the MOS transistor is connected to a bus line that is common to all pixels in a given row of a pixel array. One of its two diffusion terminals (source or drain) is connected to a line that is common to all pixels in a column of the pixel array. The other diffusion terminal connects to the internal storage node of the pixel.

Compact Design: the proposed pixel cell contains only three components, one NMOS transistor, one PMOS transistor, and one capacitor. As will be seen in the proposed hybrid drive method, high voltage and high voltage transistors are not needed to counter the noise issue in analog drive scheme, transistors from general logic process technology can meet the design requirement. We can utilize advanced process technologies to create a pixel cell taking up minimal area. A compact pixel cell creates the possibility of spatial drive scheme. An important factor for sub-pixelation is that the sub-pixel areas should be too small to be visually resolved by the observer.

Full Voltage Swing: the advantage of the CMOS transmission gate compared to the NMOS transmission gate used in an analog pixel cell is to allow the input signal to be transmitted fully to the internal storage node without the threshold voltage attenuation.

Referring now to FIG. **4**, it shows a block diagram **400** of an exemplary implementation of an image element being divided into a plurality of sub-image elements, where the number of rows a is to the power of 2. In this case, a=4 and thus I=2. An array **402** of image elements has 1024 control lines as denoted from WL**0** to WL**1023**. Reference **404** indicates each of the image elements has one control line and one data line. Reference **406** is an image element when the display is scaled down to a lower resolution. In this case, each of the image elements has a 4×4 sub-image elements.

Accordingly, each of the image elements has four control lines and four data lines. A low order X-address decoder **408** is designed to generate 4 distinct control lines, WL**3**, WL**2**, WL**1**, and WL**0**. A high order X-address decoder **410** is designed to determine which one of the low order X-address decoders is selected. In embodiment, a scale down control signal **412** is provided to disable the low order X-decoder if the control signal **412** is logic "1", or enable the low order X-decoder if the control signal **412** is logic "0".

When a low order X-decoder is disabled, the output control lines are logic "1" if the low order X-decoder is selected by high order X-decoder; the output control lines are logic "0" if the low order X-decoder is not selected by high order X-decoder. FIG. **5** shows one exemplary implementation **500** for the low order X-decoder that may be used in FIG. **4**.

Similar implementation can be done when a is not to the power of 2. FIG. **6** shows an example of block diagram **600** of such an implementation when the number of rows a is 3. In this case, I=2. an array **602** of image elements has 768 control lines as denoted from WL**0** to WL**767**. Each of the image elements **604** has one control line and one data line. Reference **606** shows an image element when the display is scaled down to a lower resolution. In this case, the image element has 3×3 sub-image elements. Accordingly, one image element has three control lines and three data lines. Reference **608** indicates a low order X-address decoder that generates 3 distinct control lines, WL**2**, WL**1**, and WL**0**. Reference **610** indicates a high order X-address decoder that determines which one of the low order X-address decoder is selected. In embodiment, a scale down control signal **612** is provided to disable the low order X-decoder if the scale down control signal **612** is logic "1", or enable the low order X-decoder if the scale down control signal **612** is logic "0". When a low order X-decoder is disabled, the output control lines are logic "1" if the low order X-decoder is selected by high order X-decoder; the output control lines are logic "0" if the low order X-decoder is not selected by high order X-decoder. One implementation for the low order X-decoder may be done substantially similar to FIG. **5**.

In general, there are two ways to feed video signals to the image elements: analog driving method and digital driving method. Referring now to FIGS. **7**A and **7**B, two functional diagrams **702** and **704** for the analog driving method and digital driving method are shown. For the analog driving scheme, one pixel includes a pass device **706** and one capacitor **708**, with a storage node connected to a mirror circuit **710** to control a corresponding liquid crystal. For the digital driving method, pulse width modulation (PWM) is used to control the gray level of an image element. A static memory cell **712** (e.g., SRAM cell) is provided to store the logic "1" or logic "0" signal periodically. The logic "1" or logic "0" signal determines that the associated element to transmit the light fully or absorb the light completely, resulting in white and black. A various mixture of the logic "1" duration and the logic "0" duration decides a perceived gray level of the element.

The advancement of display technology requires packing ever more image elements into a microdisplay (e.g., LCoS) for higher resolution image quality. The size of a digital pixel cell is limited by the SRAM cell and associated circuits therefor. FIG. **8**A shows a functional block diagram **800** of an image element according to one embodiment of the present invention. A node **802** controls the state of a pass device **804**. When the device **804** is at ON state, a signal at node **806** is propagated to a node **808**. When the device **804** is at OFF state, there is no relationship between the nodes **806** and **808**. Data stored at the node **808** is held up by a storage device **810**. The node **812** is a source node for a pull-up device **814** while the node **818** is a source node for a pull-down device **820**. In one embodiment, the node **812** is connected to the highest voltage level appropriate to a mirror metal plate **816**, and the node **818** is connected to the lowest voltage level appropriate to the mirror metal plate **816**. The pull-up and pull-down devices **814** and **820** form a buffer stage, both are controlled by the state of the node **808** with opposite polarity. Namely, when the device **814** is at ON state, the device **820** is at OFF state, an output node **824** is sourced from the node **812**. When the device **820** is at ON state, the device **814** is at OFF state, the output node **824** is sourced from the node **818**.

FIG. **8**B shows an exemplary implementation of the block diagram **800** of FIG. **8**A in CMOS. According to one embodiment, NMOS is assigned to the pass device **804**. PMOS is assigned to the pull-up device **814**. NMOS is assigned to the pull-down device **820**. The storage device **810** can be a capacitor, including MOS gate capacitor, MIM capacitor, or deep trench capacitor. V**1** is assigned to the node **812**, where V**1** is the highest voltage suitable to the mirror plate **816**. V**0** is assigned to the node **818**, where V**0** is the lowest voltage suitable to the mirror plate **816**. The nodes **806** and **802** are the data node and control node for the pass device **804**, respectively, and toggle between VH and VL. In one embodiment, VH is the voltage level for logic "1" state and VL is the voltage level for logic "0" state.

The implementation of FIG. **8**B constructs an inverting image element pixel cell. The devices **814** and **820** form an inverter as well as an output buffer. A VH (logic "1") state at a data node being programmed to the storage node **808** results in a display of low voltage V**0** at the mirror plate **816**. A VL (logic "0") state at a data node being programmed to the storage node **808** results in a display of low voltage V**1** at the mirror plate **818**. The inverting output buffer digitizes the signal stored at the node **808**. As a result, the gradual voltage variation due to leakage current through diffusion and channel of the pass device **804** are filtered out. The mirror plate **816** sees a solid V**1** or V**0** even with deteriorating internal storage voltage level. This implementation greatly extends the duration of a valid signal and removes the need of refresh operation as shown in FIG. **9**A.

According to one embodiment, the voltage on the control node of MOS devices needs to exceed the minimal voltage, a threshold voltage, in order to switch the device from OFF state to ON state. Likewise, the voltage on control node of MOS devices needs to be less than the threshold voltage in order to switch the device from ON state to OFF state. The threshold voltage of the pull-up and pull-down devices (e.g., **814** and **820** of FIG. **8**A or **8**B) allows the maximal voltage swing on the mirror plate (the difference between V**1** and V**0**) to be different from the voltage swing on the storage node **808** (the difference between VH and VL).

The pull-up device **814** remains non-conducting as long as $|V_{th,\ pullup}|>V_1-V_{storage(max)}$. The pull-down device **820** remains non-conducting as long as $V_{th,\ pulldown}>V_{storage(min)}-V_0$. As shown in FIG. **9**B, the pull-up device remains non-conducting as long as $|V_{th,\ pullup}|>V_1-V_H$, the pull-down device remains non-conducting as long as $V_{th,\ pulldown}>V_L-V_0$. According to one embodiment, selecting high threshold voltage devices as devices **814** and **820** can increase the voltage swing of mirror plate and the higher voltage swing reduces the liquid crystal response time in LCOS, as shown in FIG. **9**B.

The threshold voltage of the device can limit the maximal or minimal voltage level to the storage node **808** due to the body effect of MOS devices. For NMOS type pass device, the maximal voltage level can pass from data node to storage node and is limited to $V_{control}-V_{th,pass}$, where $V_{th,pass}$ is the threshold voltage of NMOS device. For PMOS type pass device, the minimal voltage level can pass from data node to storage node and is limited to $V_{th,pass}$, where $V_{th,pass}$ is the magnitude of threshold voltage of PMOS device. For NMOS type pass device, increasing the control node voltage level to $V_{control}>V_H+V_{th,pass}$ assures to full passage of V_H voltage. For PMOS type pass device, reducing the control node voltage level to $V_{control}<V_L-V_{th,pass}$ assures to the full passage of V_L voltage.

Referring now to FIG. **10**A, it shows one embodiment **1000** of a pixel with read back operations. A pass device **1002** (read pass device) is coupled to a control node **1004**, with a source node **1004** thereof connected to a buffer output node **1006**, and the other end **1008** thereof to a data node **1010**. For the read back operation, with a device **1012** at OFF state and the switching device **1002** to ON state, the signal at the node **1006** is propagated to the data node **1010**. A sensing circuit (not shown) is designed to detect the state of the storage node **1014** by reading the state of the signal at the data node **1010**. The read back operation is non-destructive to the charge stored in the storage node **1016**, while providing a strong voltage level for logic “1” and a logic “0”.

According to one embodiment as shown in FIG. **10**B, the data node **1010** is removed from the device **1002** (read pass device) and replaced with a data node **1011**. Hence the data node **1010** is now a dedicated node for write operation while the data node **1011** is a dedicated node for read operation. Accordingly, the write and read operations can take place concurrently and independently. This embodiment provides an efficient way to characterize the timing of write operation by concurrently validating the read back data, where read back data is complement of write data.

FIG. **11** shows an embodiment of an image element with planar update. FIG. **11** shows two proposed pixel cells **1102** and **1104**, a mirror plate **1106** and a pass device **1108** for read back. When the planar update happens, all the data of the pixel cells in a pixel array are updated simultaneously, removing artifacts resulted from, for example, transitional image displays. The two pixel cells **1102** and **1104** are cascaded to form one pixel cell with the planar update capability. The cell **1102** stores the updated data while the cell **1104** stores the data in display. The control node **1110** of the cell **1102** writes the signal at the data node **1112** to the cell **1102**. The write data is inverted at the node **1114**. The control node **1116** of the cell **1104** writes the signal at the node **1114** to the cell **1104**. The data at the node **1112** is thus updated at the node **1118**. The control node **1116** can be connected together with the control node of other pixel cells. Data in these pixel cells connected to the same control node is updated simultaneously.

In LCoS, the liquid crystal layer is sandwiched between a mirror plate controlled by a pixel underneath it, and a common Indium-Tin-Oxide (ITO) layer above a liquid crystal layer. The birefringence mechanism used in steering the light polarity in LCoS responds to the magnitude of an electric field applied to the liquid crystal. The direction of the electric field does not matter. The electric field applied to the liquid crystal layer has to reach electrically neutral in the long term, avoiding impurities in liquid crystal to cause permanent damage.

A common practice to reach the electric field neutral is to apply “field invert” (FI) periodically. “Field invert” applies the equal amount of voltage difference across the liquid crystal but with inverted polarity, i.e., a voltage difference DV from ITO layer to mirror plate is inverted to −DV. So the common practice is to change the ITO voltage from VITO+ to VITO− while changing mirror plate voltage from V**1** to V**0**, and V**0** to V**1**, the magnitude of DV is retained while the electric field polarity changes. FIG. **12**A and FIG. **12** B show, respectively, a voltage magnitude curve between the mirror and ITO layers and relationships among the voltages applied thereon.

FIG. **13**A shows one exemplary embodiment **1300** of a pixel cell with field invert. Similar to FIG. **8**A, a node **1302** controls the state of a pass device **1304**. When the device **1304** is at ON state, a signal at node **1306** is propagated to a node **1308**. When the device **1304** is at OFF state, there is no relationship between the nodes **1306** and **1308**. When the device **1322** is at ON state, the signal at the node **1306** is propagated to the node **1324**. When the device **1322** is at OFF state, there is no relation between the nodes **1306** and **1324**.

A storage device **1310** is provided to hold up the state at the node **1308** and **1324**. The data nodes **1306** and **1307** contain complementary data. For example, if the data node **1306** is “logic 1”, then the data node **1307** is “logic 0”, or vice versa. As a result, the data at nodes **1308** and **1324** are complementary as well.

The node **1312** is a source node for a pull-up device **1314** while the node **1318** is a source node for a pull-down device **1320**. In one embodiment, the node **1312** is connected to the highest voltage level appropriate to a mirror metal plate **1316**, and the node **1318** is connected to the lowest voltage level appropriate to the mirror metal plate **1316**. The pull-up and pull-down devices **1314** and **1320** form a buffer stage, both are controlled by the state of the node **1308** with opposite polarity. Namely, when the device **1314** is at ON state, the device **1320** is at OFF state, an output node **1324** is sourced from the node **1312**. When the device **1320** is at ON state, the device **1314** is at OFF state, the output node **1324** is sourced from the node **1318**.

The state of device **1314** is controlled by the node **1308** while the state of device **1320** is controlled by the node **1324**. Since the nodes **1308** and **1324** have complementary data, only one of the devices **1314** and **1320** can be at ON state. The state of a destination node **1326** is determined by the state of devices **1314** and **1320**. If the device **1314** is at ON state and the device **1320** is at OFF state, the signal at the node **1312** propagates to the node **1326** via the device **1314**. If the device **1320** is at ON state and the device **1314** is at OFF state, the signal at the node **1318** propagates to the node **1326** via the device **1320**.

FIG. **13**B shows an exemplary implementation of the block diagram **1300** of FIG. **13**A in CMOS. According to one embodiment, NMOS is assigned to the pass devices **1304** and **1322**. PMOS is assigned to the pull-up device **1314**. NMOS is assigned to the pull-down device **1320**. The storage device **1310** can be a capacitor, including MOS gate capacitor, MIM capacitor, or deep trench capacitor. V**1** or V**0** is assigned to the node **1312**, where V**1** is the highest voltage suitable to the mirror plate **1316** and V**0** is the lowest voltage suitable to the mirror plate **1316**. Similarly, V**0** or V**1** is assigned to the node **1318**. The nodes **1306** and **1302** are the data node and control node for the pass device **1304**, respectively, and toggle between VH and VL. In one embodiment, VH is the voltage level for logic “1” state and VL is the voltage level for logic “0” state. FIG. **14** shows the voltages at respective nodes.

Referring now to FIG. **15**A, it shows a functional block diagram **1500** of cascading several field inverters. There are one row of pixel cells **1502**, each having a source node **1504** and another source node **1506**. The source nodes **1504** of the pixel cells **1502** are tied together or coupled together to form a VPOS node and the source nodes **1506** of the pixel cells **1502** are tied together to form a VNEG node. A switch **1508** is provided for the VPOS node while a switch **1510** is provided for the VNEG node. The switcher **1508** and **1510** are respectively driven with V**1** and V**0** as inputs thereto.

Reference **1512** indicates a group of n rows of the pixel cells **1502**, denoted row **0** to row n−1, all of the VPOS nodes are tied or coupled together and their VNEG nodes are also tied or coupled together. Subsequent rows of the total display pixel array are also grouped as multiple groups of n rows.

The switches **1508** and **1510** are controlled by a signal FI (field invert). When FI is logic "0", VPOS is driven to V**1** by the switch **1508** and VNEG is driven to V**0** by **1510**. When FI is logic "1", VPOS is driven to V**0** by the switch **1508** and VNEG is driven to V**1** by **1510**. A time delay element is inserted between FI signals of the group **1512** and its adjacent groups as shown in FIG. **15**B. Each group **1512** of n rows starts the field invert operation at different time step, delayed by a certain time step (predefined) than its preceding group of n rows. As a result, operating field invert by the cascading order reduces the overall power surge and switching noise.

The present invention has been described in sufficient detail with a certain degree of particularity. It is understood to those skilled in the art that the present disclosure of embodiments has been made by way of examples only and that numerous changes in the arrangement and combination of parts may be resorted without departing from the spirit and scope of the invention as claimed. Accordingly, the scope of the present invention is defined by the appended claims rather than the forgoing description of embodiments.

We claim:

1. A display device comprising:

a plurality of image elements, each of the image elements including a set of sub-image elements arranged in rows and columns, each of the sub-image elements addressed by a control line and a data line, wherein some or all of the sub-image elements in an image element are modulated to provide fine brightness levels in accordance with a predefined approach based on a number of patterns of the some or all of the sub-image elements in the image element, each of the patterns for a gray level is randomly chosen for a specified brightness level; and

a driving circuit provided to drive the image elements in accordance with a video signal to be displayed via the display device, the driving circuit designed to turn on a portion of each of the image elements to achieve similar perceived effect of having the each of the image elements turned on for a predefined time.

2. The display device as recited in claim **1**, wherein the some or all of the sub-image elements in an image element are tuned on in response to a brightness level assigned to the image element.

3. The display device as recited in claim **2**, wherein each of the image elements is designed to produce brightness levels in an n-bit scale, wherein the driving circuit generate 2^m of distinct voltage levels between two voltages, a high voltage V_H and a low voltage V_L, wherein m is the most significant bits (MSB) of the n-bit scale, remaining n-m bits of the n-bit scale are implemented with 2^{n-m} pulses of equal duration in one frame.

4. The display device as recited in claim **3**, wherein a perceived brightness level is an accumulative effect of turning on sequentially some or all of the sub-image elements in different patterns.

5. The display device as recited in claim **4**, wherein the different patterns are determined according to a look-up-table.

6. The display device as recited in claim **1**, wherein the predefined approach is further based on a fixed number and location of the sub-elements in the image element corresponding to a specific brightness level.

7. The display device as recited in claim **1**, wherein the patterns follow a pre-determined sequence for a specified brightness level.

8. The display device as recited in claim **1**, wherein the predefined approach is based on a pre-determined algorithm taking into account of some or all of: a lateral liquid crystal fringing field, patterns of surrounding image elements, and compensation of brightness level digitization.

9. The display device as recited in claim **1**, wherein the sub-image elements in each of the image elements are addressed simultaneously to reduce a spatial resolution of the display device.

10. The display device as recited in claim **1**, wherein each of the sub-image elements includes a pass device, a storage device, a pull-up device and a pull-down device, wherein the pull-up and pull-down devices form a buffer stage, an output of the buffer stage is used to control a metal plate next to a liquid crystal layer.

11. The display device as recited in claim **10**, wherein each of the sub-image elements is an inverting pixel cell as the pull-up device and the pull-down device form an inverter as well as an output buffer.

12. The display device as recited in claim **1**, wherein each of the sub-image elements includes a first cell and a second cell, each of the first and second cells includes a pass device, a storage device, a pull-up device and a pull-down device, wherein the pull-up and pull-down devices form a buffer stage, an output of the buffer stage in the first cell is coupled to the second cell, wherein an output of the second cell is used to control a metal plate next to a liquid crystal layer.

13. The display device as recited in claim **12**, wherein the each of the sub-image elements achieves planar update by cascading the first and second cells to form one sub-image element, wherein the first cell stores an updated datum while the second cell stores an datum to control the metal plate.

14. The display device as recited in claim **12**, wherein the each of the sub-image elements is structured to cause an electric field applied between a metal plate and an Indium-Tin-Oxide (ITO) coating polarity neutral.

15. The display device as recited in claim **12**, wherein the each of the sub-image elements is structured to apply an equal amount of voltage difference across a metal plate and an Indium-Tin-Oxide (ITO) coating with inverting polarity.

16. The display device as recited in claim **1**, wherein the display device is used on a holographic projector to project the video signal onto a medium.

17. The display device as recited in claim **1**, wherein the display device is used on a projector to project the video signal onto a medium.

18. A display device comprising:

a plurality of image elements, each of the image elements including a set of sub-image elements arranged in rows and columns, each of the sub-image elements addressed by a control line and a data line, wherein each of the image elements is designed to produce brightness levels in an n-bit scale, a driving circuit generates 2^m of distinct voltage levels between two voltages, a high voltage V_H and a low voltage V_L, wherein m is the most significant bits (MSB) of the n-bit scale, remaining n-m bits of the n-bit scale are implemented with 2^{n-m} pulses of equal duration in one frame; and

the driving circuit provided to drive the image elements in accordance with a video signal to be displayed via the display device, the driving circuit designed to turn on a portion of each of the image elements to achieve similar perceived effect of having the each of the image elements turned on for a predefined time.

19. The display device as recited in claim **18**, wherein a perceived brightness level is an accumulative effect of turning on sequentially some or all of the sub-image elements in different patterns.

20. The display device as recited in claim **19**, wherein the different patterns are determined according to a look-up-table.

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