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(54) **SEMICONDUCTOR DEVICE, DISPLAY DEVICE INCLUDING THE SEMICONDUCTOR DEVICE, DISPLAY MODULE INCLUDING THE DISPLAY DEVICE, AND ELECTRONIC APPLIANCE INCLUDING THE SEMICONDUCTOR DEVICE, THE DISPLAY DEVICE, AND THE DISPLAY MODULE**

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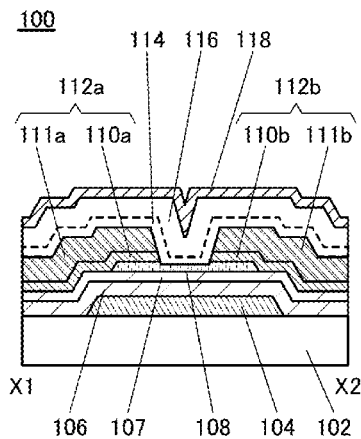
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(57) **ABSTRACT**

A change in electrical characteristics is inhibited and reliability is improved in a semiconductor device using a transistor including an oxide semiconductor. One embodiment of a semiconductor device including a transistor includes a gate electrode, first and second insulating films over the gate electrode, an oxide semiconductor film over the second insulating film, and source and drain electrodes electrically connected to the oxide semiconductor film. A third insulating film is provided over the transistor and a fourth insulating film is provided over the third insulating

(Continued)

100

114 116 118

112a

111a 110a

112b

110b 111b

X1 X2

106 107 108 104 102

film. The third insulating film includes oxygen. The fourth insulating film includes nitrogen. The amount of oxygen released from the third insulating film is $1\times10^{19}/cm^3$ or more by thermal desorption spectroscopy, which is estimated as oxygen molecules. The amount of oxygen molecules released from the fourth insulating film is less than $1\times10^{19}/cm^3$.

20 Claims, 51 Drawing Sheets

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(58) **Field of Classification Search**

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See application file for complete search history.

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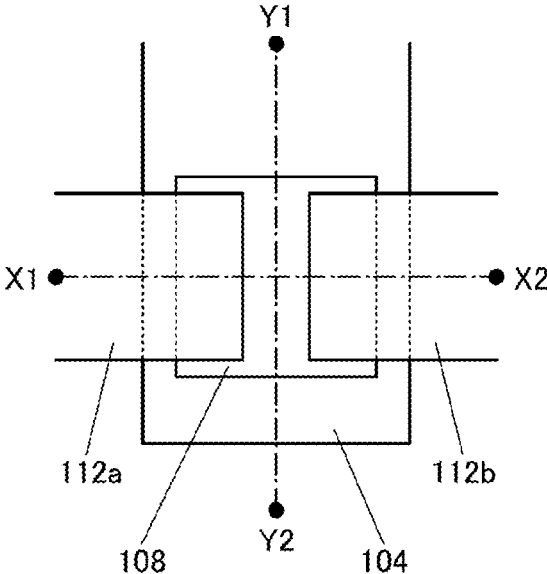
* cited by examiner
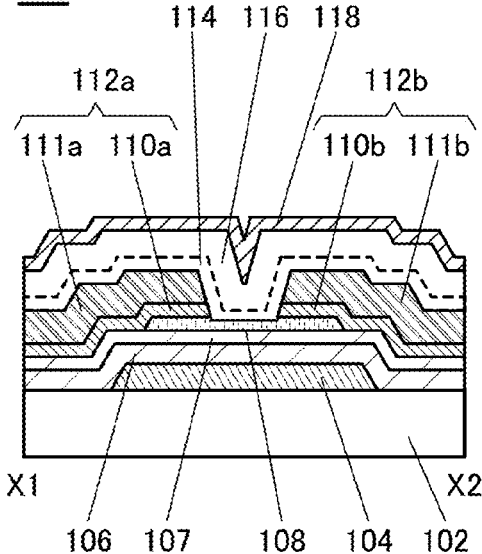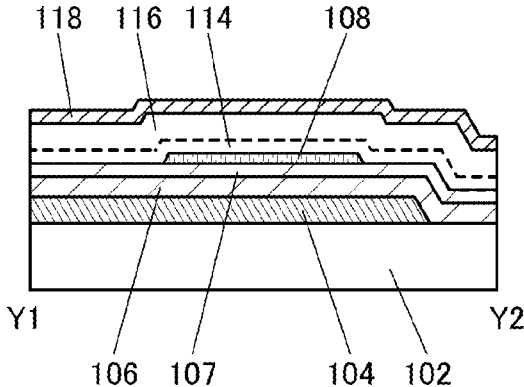
FIG. 1A
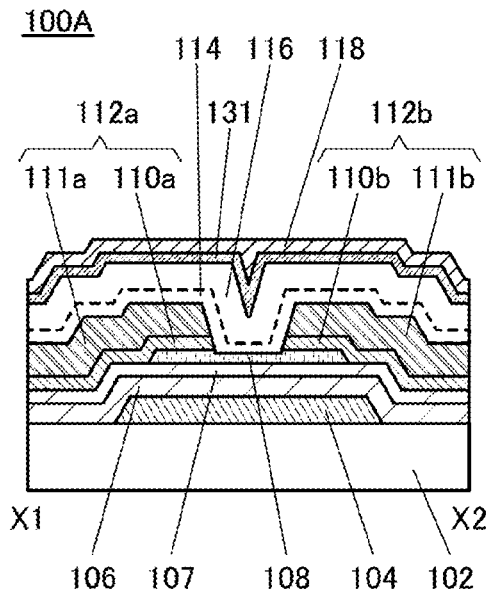
100

FIG. 1B

100

FIG. 1C

100

FIG. 2A

100A

114 116 118

112a   131   112b

111a 110a   110b 111b

X1   X2

106   107   108   104   102

FIG. 2B

100A

118   116   114   108   131

Y1   Y2

106   107   104   102

FIG. 2C

100B

114 116 118

112a   131   112b

111a 110a   110b 111b

X1   X2

106   107   108   104   102

FIG. 2D

100B

118   116   114   108   131

Y1   Y2

106   107   104   102

FIG. 3A

150

Y1

141a   141b

X1   X2

112a   112b

Y2

108   104

FIG. 3B

150

114 116 118

112a   112b

111a 110a   110b 111b

X1   X2

106 / 107   108 \ 104 102

141a   141b

FIG. 3C

150

118 116 114   108

Y1   Y2

106   107   104 102

FIG. 4A

150A

114 116 118

112a   131   112b

111a 110a   110b 111b

X1   X2

106 / 107   108 / 104 102

141a   141b

FIG. 4B

150A

118 116 114   108   131

Y1   Y2

106   107   104   102

FIG. 4C

150B

114 116 118

112a   131   112b

111a 110a   110b 111b

X1   X2

106 / 107   108 / 104 102

141a   141b

FIG. 4D

150B

118 116 114   108   131

Y1   Y2

106   107   104   102

FIG. 5A

160

114

Y1

Y2

X1

X2

112a

108

104

112b

FIG. 5B

160

112a

111a 110a

114 116 118

112b

110b 111b

X1

X2

106 107 108 104 102

FIG. 5C

160

118 116 114 108

Y1

Y2

106 107 104 102

FIG. 6A

160A

FIG. 6B

160A

FIG. 6C

160B

FIG. 6D

160B

FIG. 7A

<u>170</u>

Y1

142a

X1   ●   ● X2

112a   112b   142c

108   104   142b 120b 120a

Y2

FIG. 7B

<u>170</u>

114 116 118

112a   120b   112b

111a 110a   110b 111b

X1   120a   X2

102 106 107 108 104 142c

FIG. 7C

<u>170</u>

120b   116   114   108   118

Y1   Y2

106   107   104   102

142a   142b

FIG. 8A

100C

114

X1   X2

107   108a 108b 108c

108

FIG. 8B

100C

114

Y1   Y2

107   108a 108b 108c

108

FIG. 8C

100D

114

X1   X2

107   108a   108b

108

FIG. 8D

100D

114

Y1   Y2

107   108a   108b

108

FIG. 9A

FIG. 9B

FIG. 10A

X1   X2

106   107   104   102

FIG. 10B

108

X1   X2

FIG. 10C

112a   112b

111a   110a   110b   111b

X1   X2

FIG. 10D

114   116

X1   X2

FIG. 11A

130

X1   X2

FIG. 11B

141

X1   X2

FIG. 11C

131

X1   X2

FIG. 11D

118

X1   X2

FIG. 12A

130   108   114   116

X1   X2

FIG. 12B

141

X1   X2

FIG. 12C

131

X1   X2

FIG. 12D

141a   141b

X1   X2

FIG. 13A

FIG. 13B

FIG. 14A

118

X1   X2

FIG. 14B

118

Y1   Y2

FIG. 14C

142c

X1   X2

FIG. 14D

142a   142b

Y1   Y2

FIG. 15A

FIG. 15B

120

X1   X2

120

Y1   Y2

FIG. 15C

FIG. 15D

120b   120a

X1   X2

120b

Y1   Y2

FIG. 16A

114   130

X1   X2

FIG. 16B

141

X1   X2

FIG. 16C

131

X1   X2
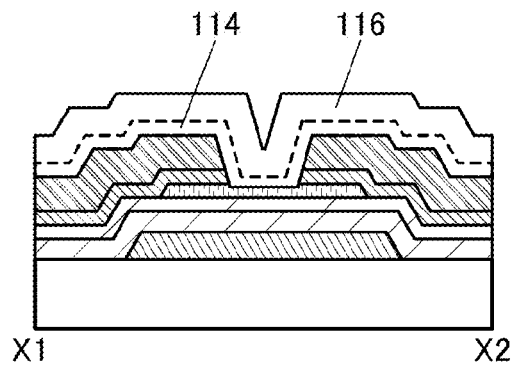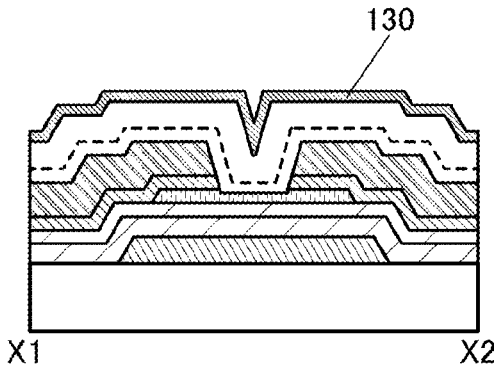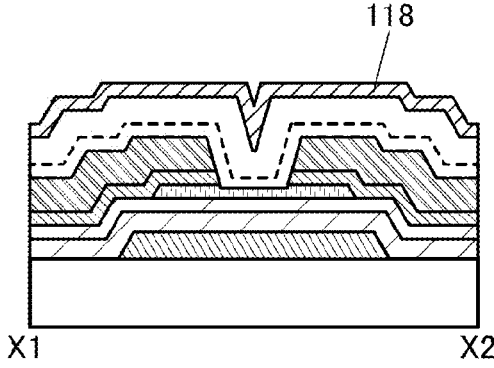
FIG. 16D

116   118

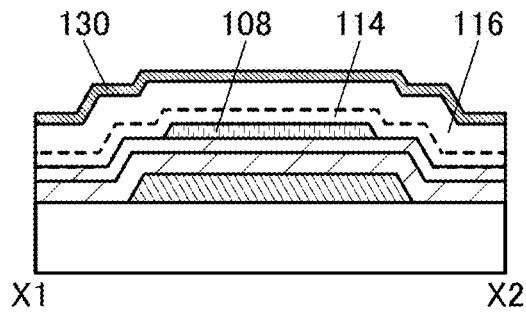X1   X2

FIG. 17A

FIG. 17B

FIG. 17C

FIG. 17D
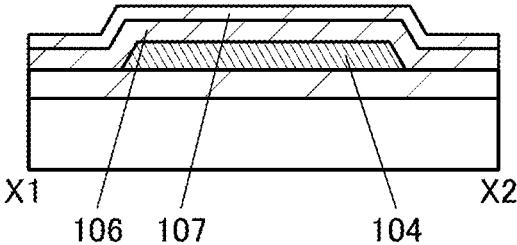
FIG. 18A

130

X1   X2

106   107   104   102

FIG. 18B

141

X1   X2

FIG. 18C

131

X1   X2

FIG. 19A

50 nm

FIG. 19B

3 nm

FIG. 19C

0.8 nm

3 nm

FIG. 19D

5161
5100
5120

FIG. 20A

10 nm

FIG. 20B

1 nm

FIG. 20C

1 nm

FIG. 20D

1 nm
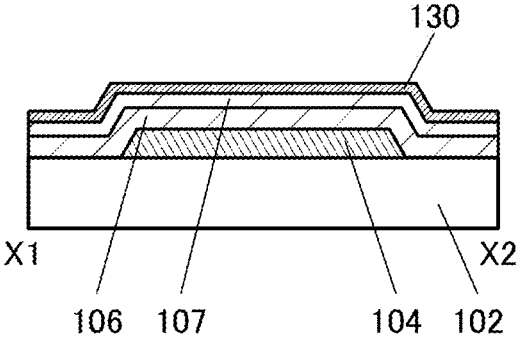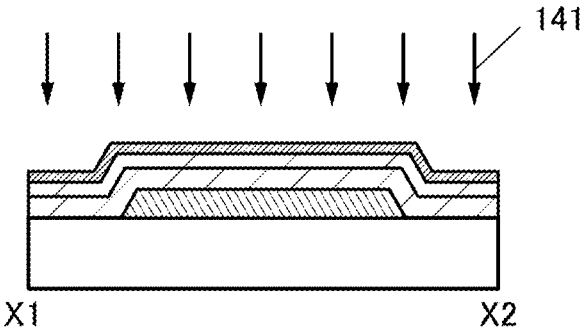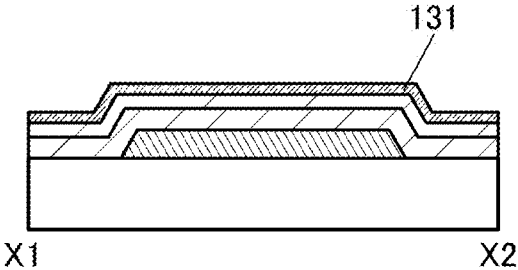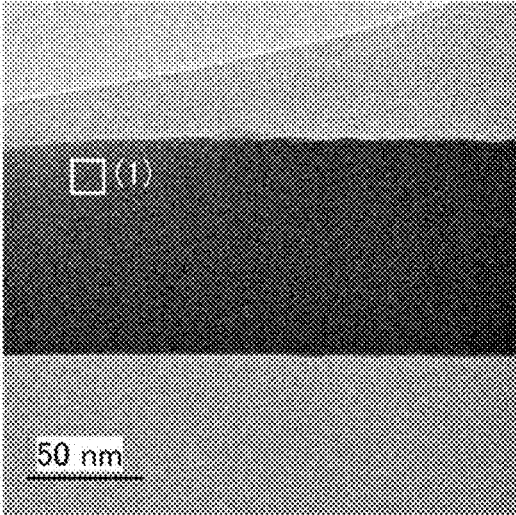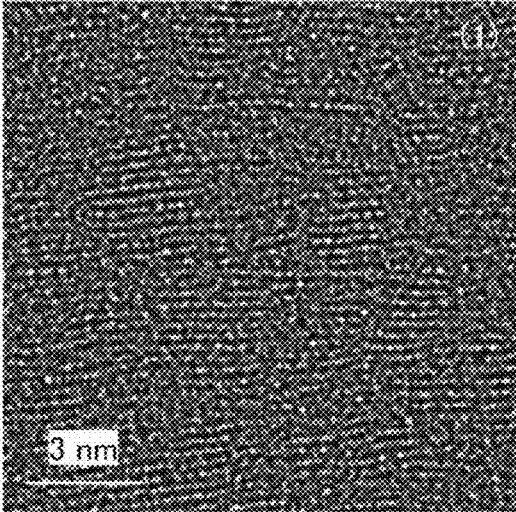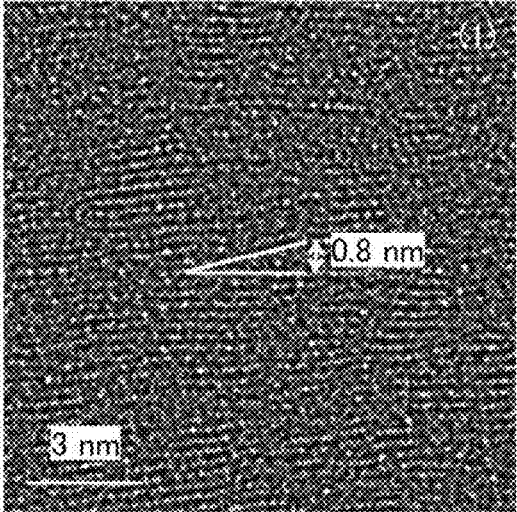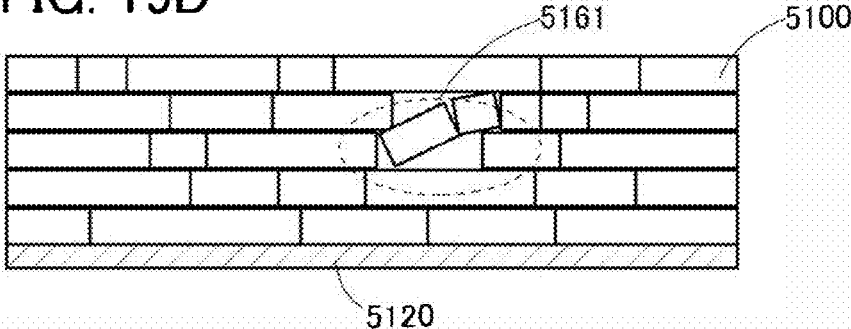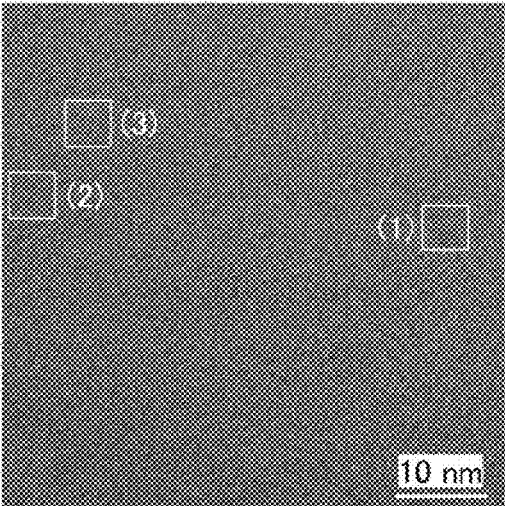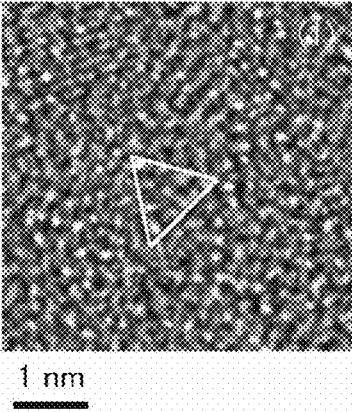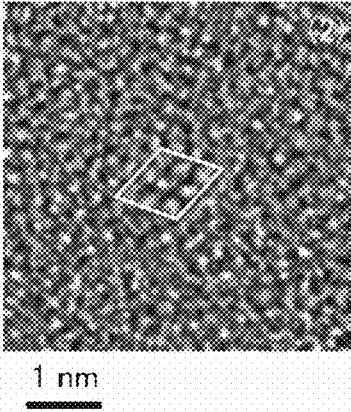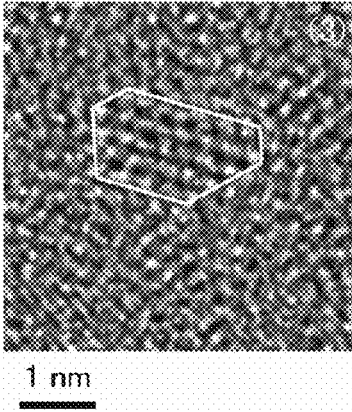
FIG. 21A

out-of-plane method
CAAC-OS
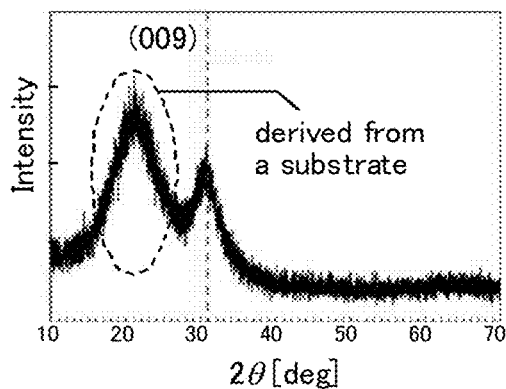
FIG. 21B

in-plane method ϕ scan
CAAC-OS
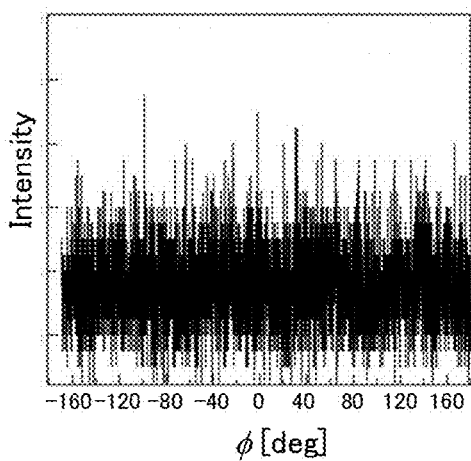
FIG. 21C

in-plane method ϕ scan
single crystal OS

FIG. 22

FIG. 23

●:In   ●:Ga   ●:Zn   ●:O
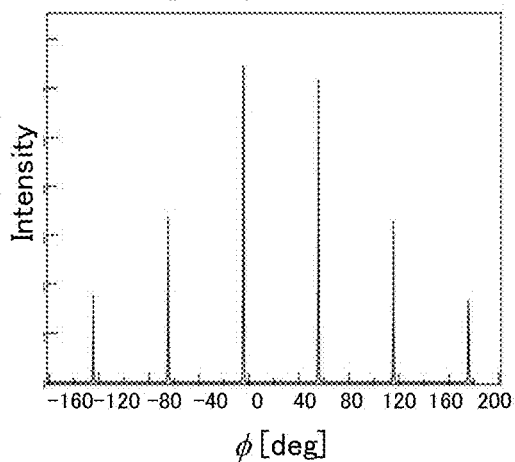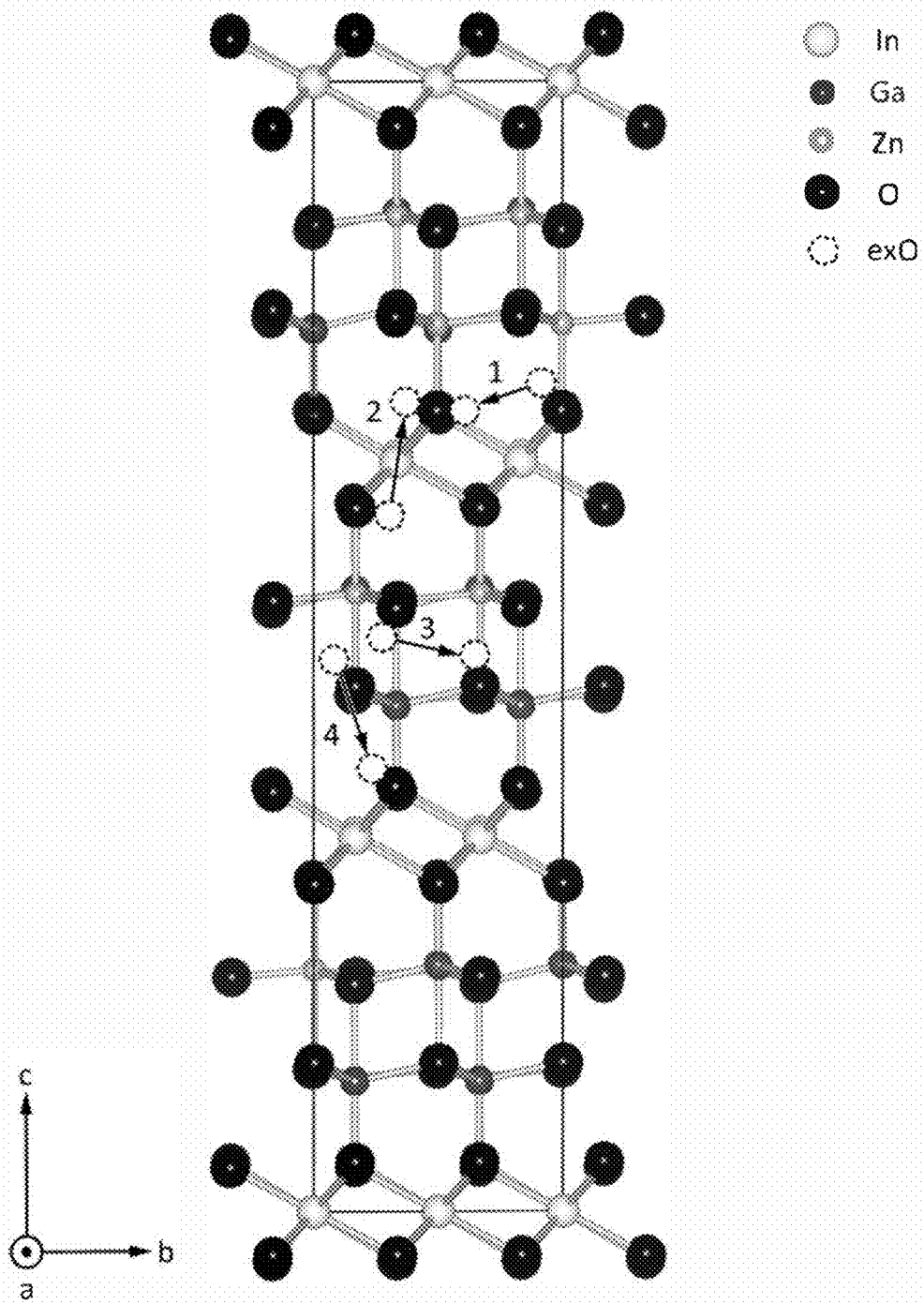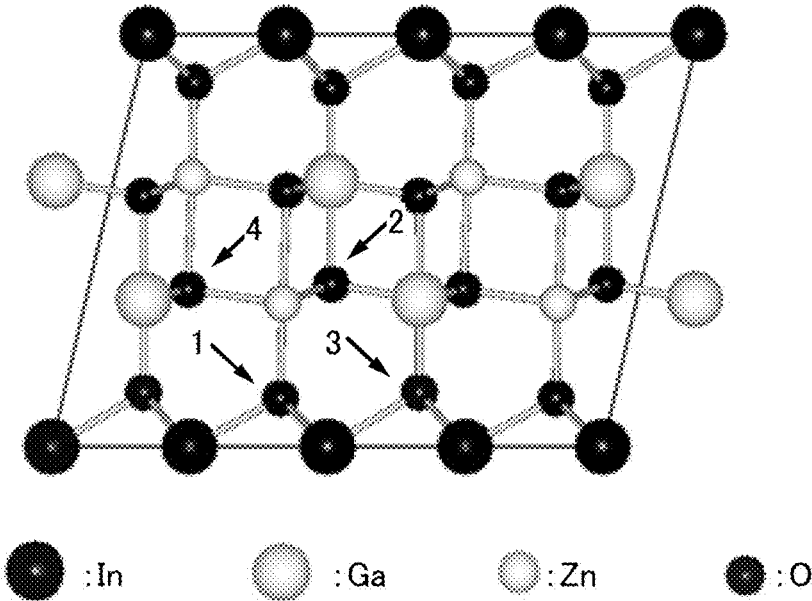
FIG. 24A   Initial (V_OH)

V_OH

FIG. 24B   Final (V_O, H–O)

V_O
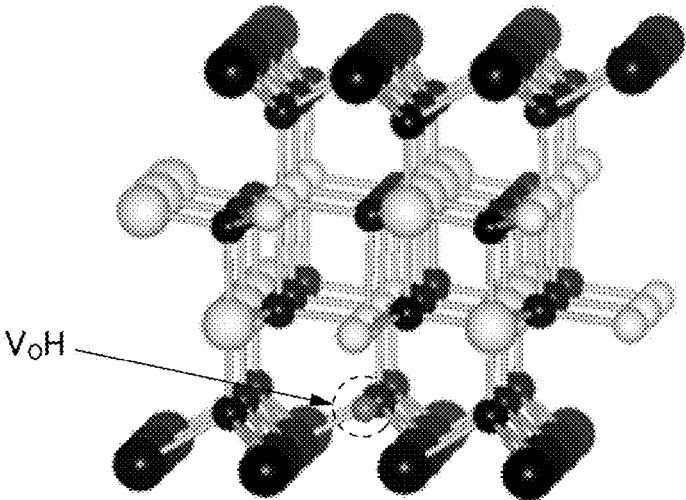
bonded to O
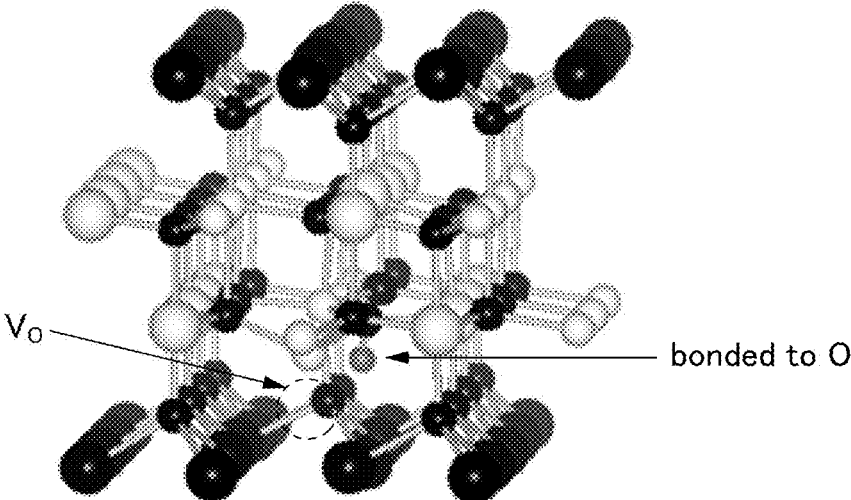
FIG. 25
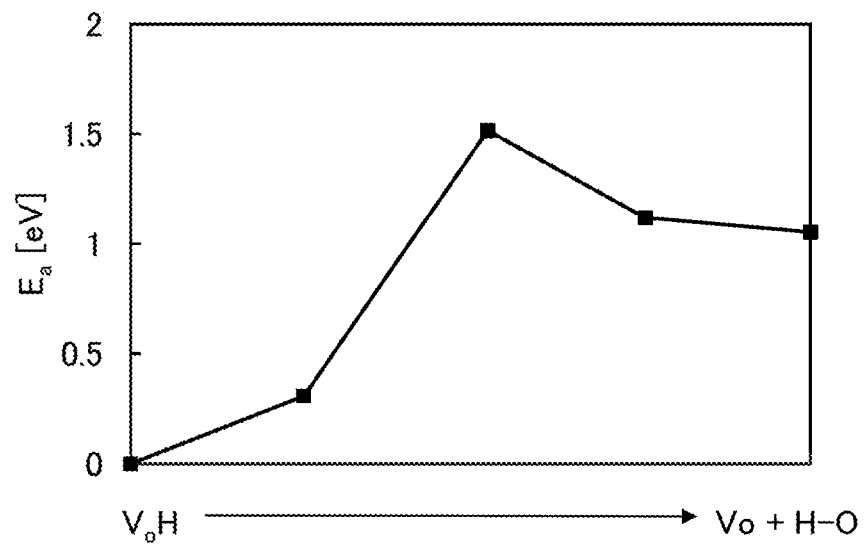
FIG. 26A   Initial (V_OH)

V₀H —

FIG. 26B   Final (V_O, H–O)

V_O
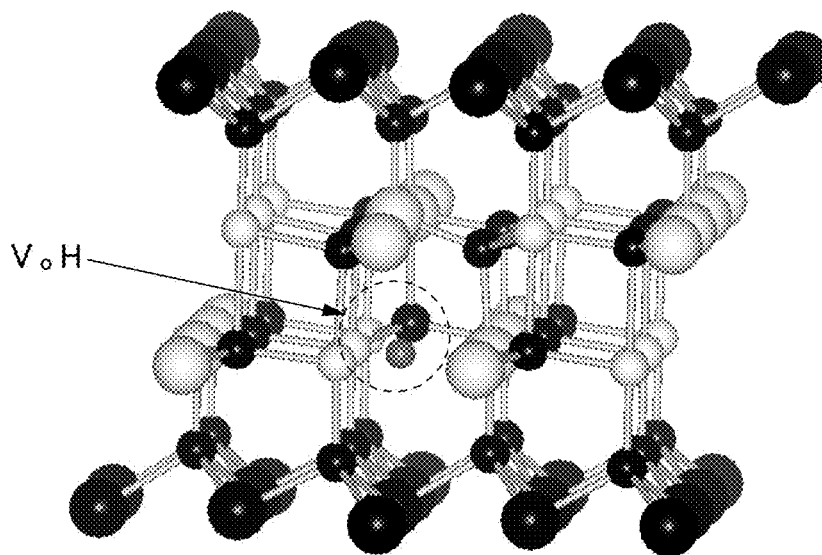
bonded to O
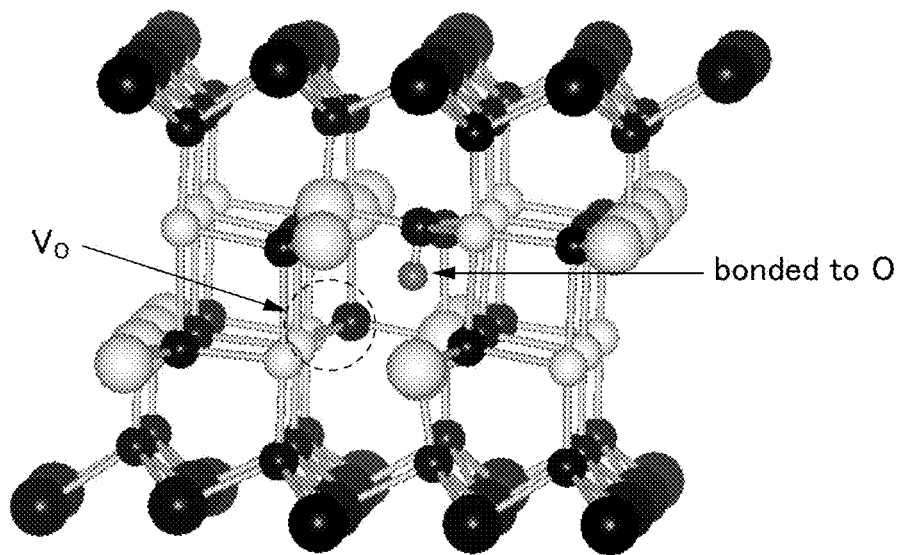
FIG. 27
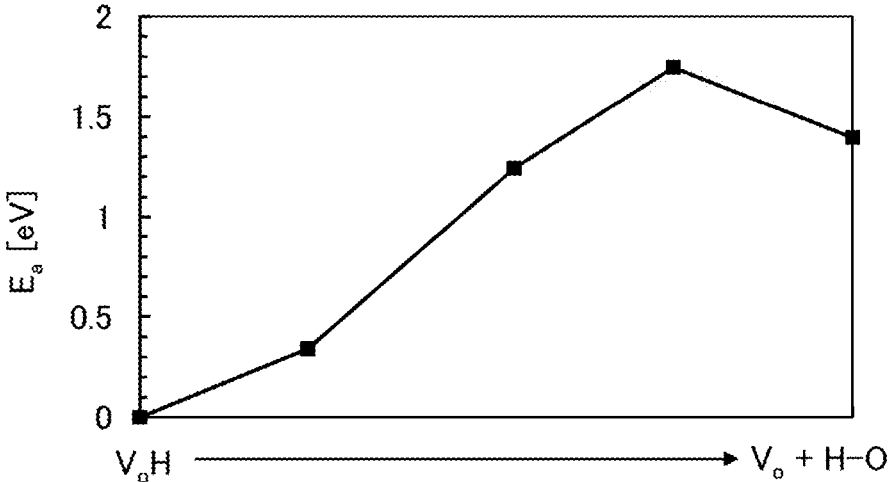
FIG. 28
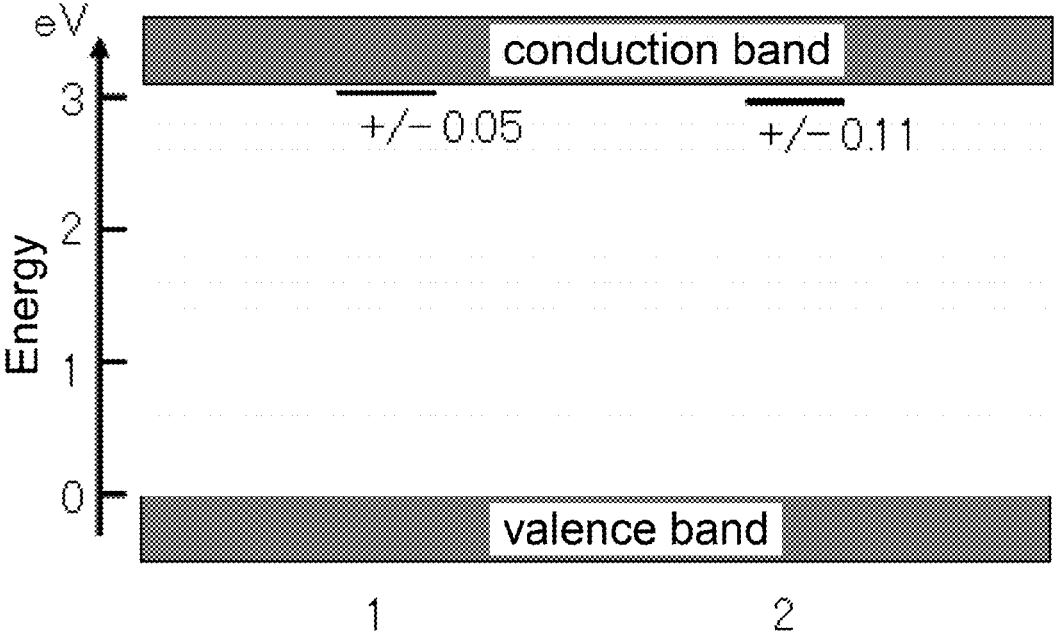
FIG. 29
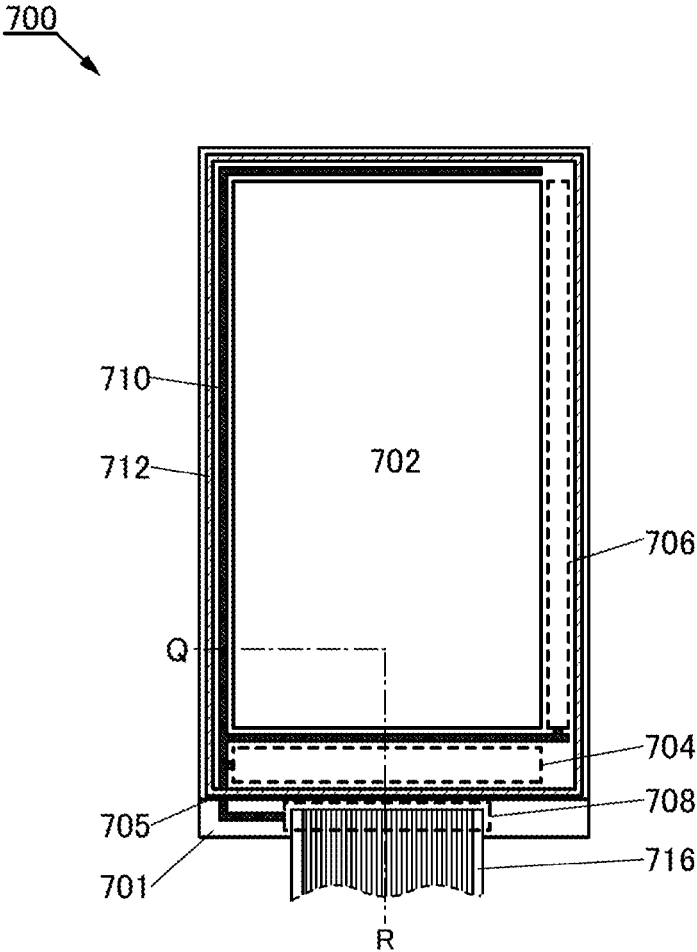
FIG. 30

700
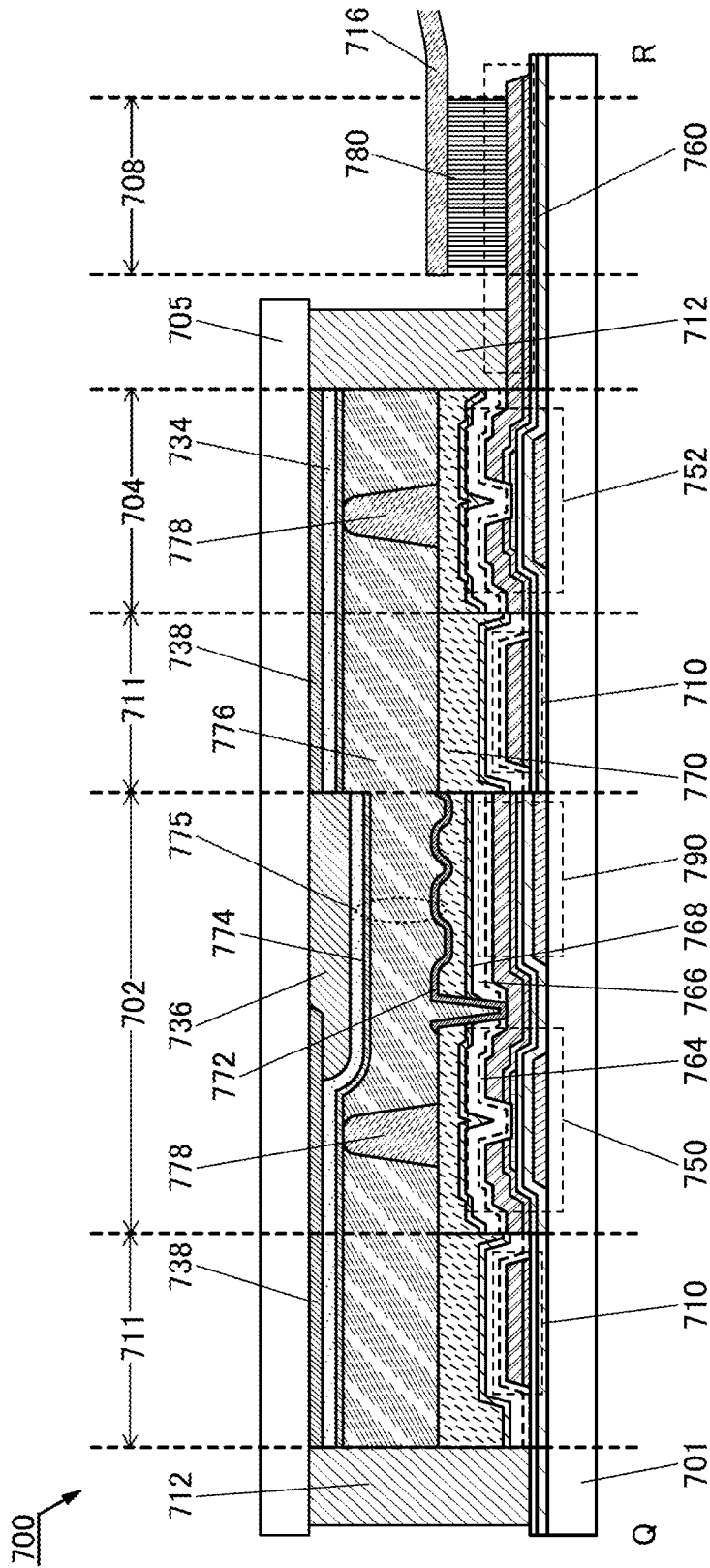
FIG. 31
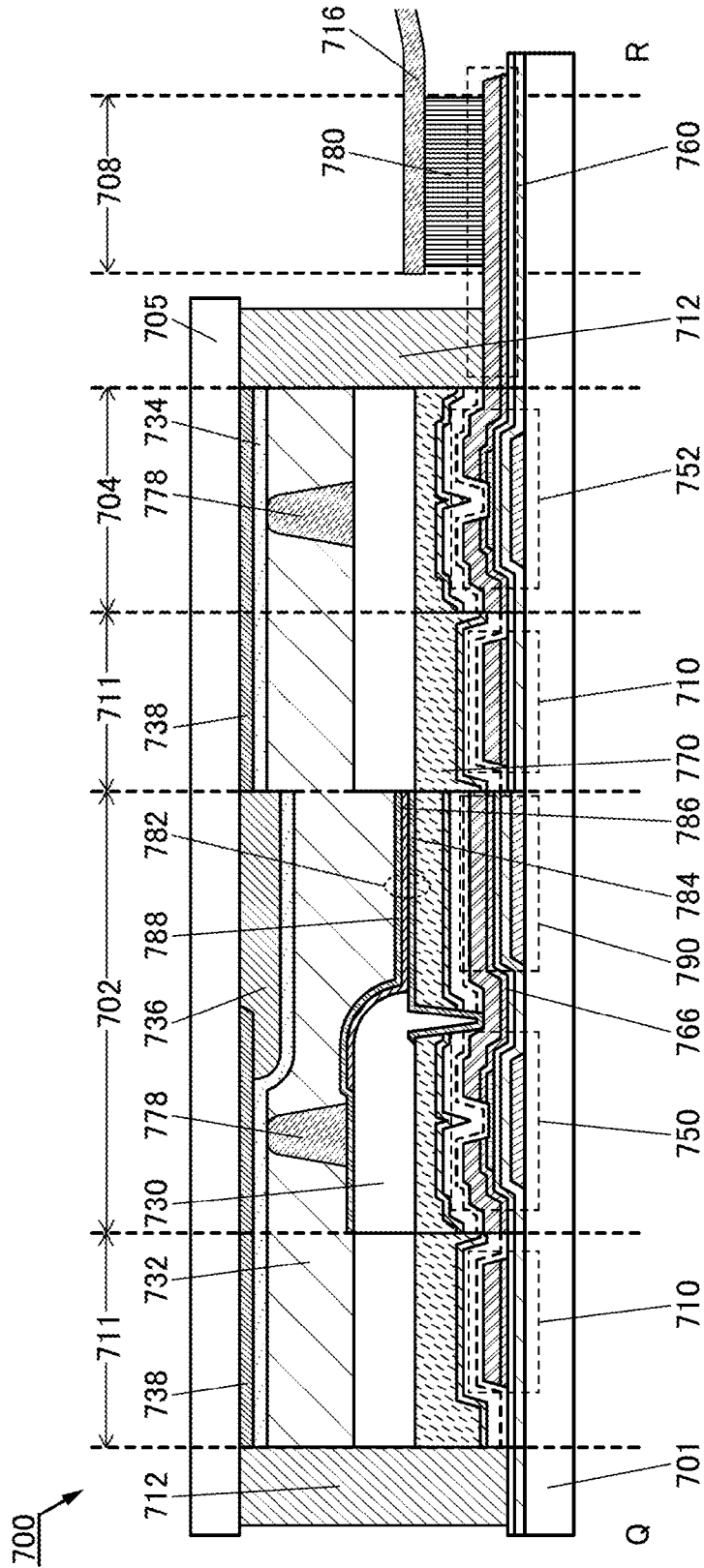
FIG. 32A

FIG. 32B

FIG. 32C

FIG. 33

8001
8003
8004
8005
8006
8007
8008
8009
8010
8011
8002
8000

FIG. 34A

9007
9004
9009
9000
9001
9010
9006
9005
9008
9003

FIG. 34B

9001
9000
9007
9003
9011
9004
9008
9005
9006
9002

FIG. 34C

9012
9004
9003
9008
9000
9007
9013 9006
9002
9001

FIG. 34D

9001
9000
9003
9006
9007
9004
9005
9008
9011

FIG. 34E

9014
9006
9015
9007
9000
9016
9003
9008
9001
9005
9004

FIG. 34F

9001
9000
9002
9003
9006
9007
9005
9004
9008
9011

FIG. 34G

9003
9007
9000
9003
9001
9005
9008
9006

FIG. 34H

9006
9000
9001
9007
9005
9008
9003
9017

FIG. 35
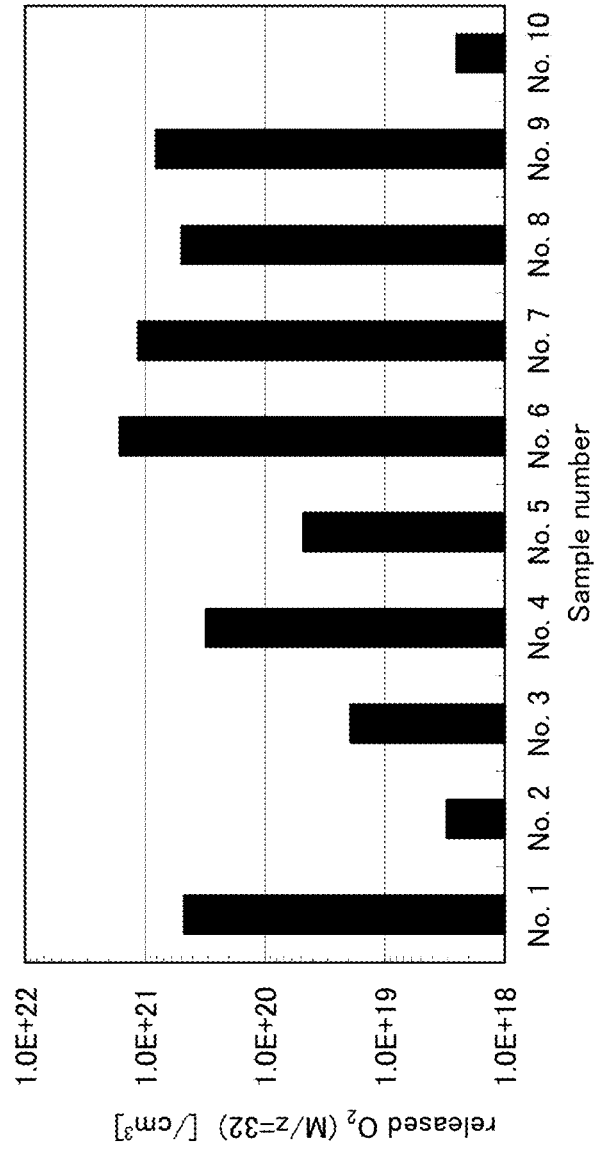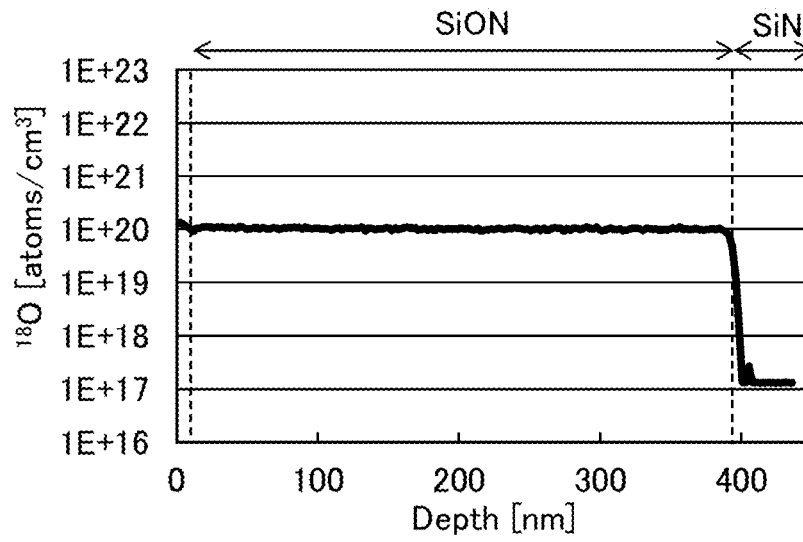
FIG. 36A

FIG. 36B
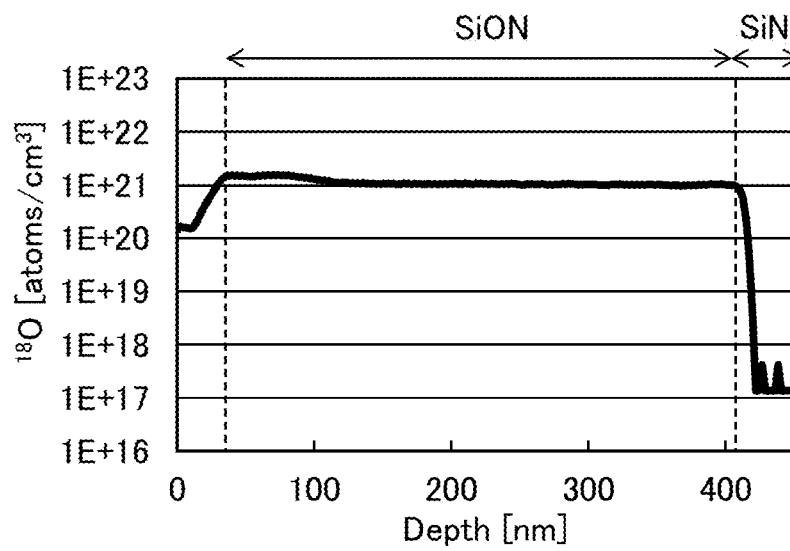
FIG. 37A
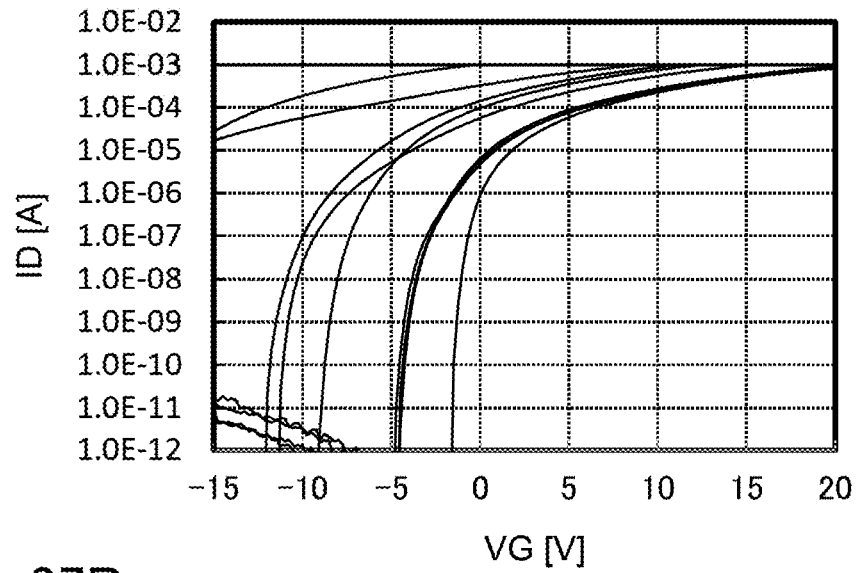
FIG. 37B
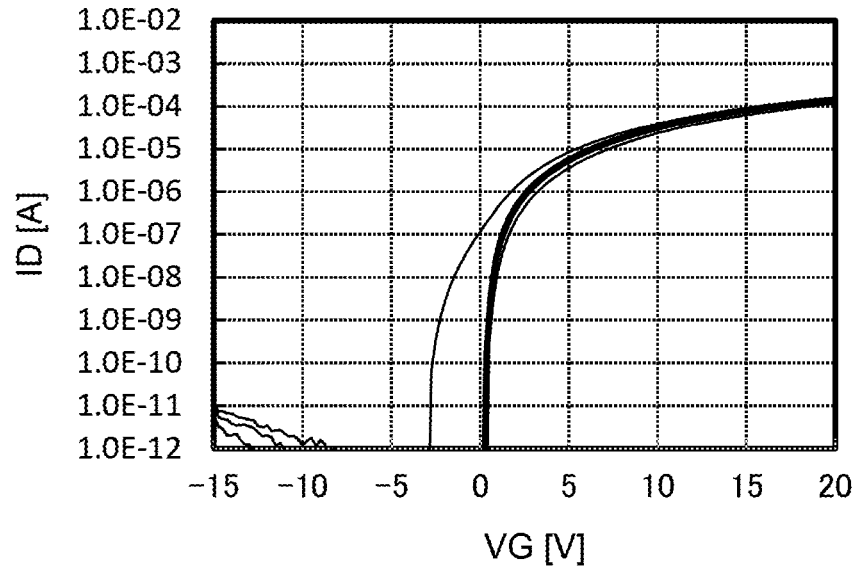
FIG. 38A

FIG. 38B

FIG. 39

FIG. 40A

Heated Substrate

1120

plasma

1100b

1100a

c-axis

1101

1107

1100a

1130

Target

FIG. 40B

1100

C

1120
(flat surface)

FIG. 40C

1100

C

C

1120
(uneven surface)

FIG. 41

Room-temperature Substrate

1120

1100b

plasma

1100a

c-axis

1100a

1101

1107

1130

Target

FIG. 42

FIG. 43

Fleming's left hand rule

Heated Substrate

FIG. 44A

$\cdots -In-O- \quad -O-In- \cdots$

1100a

1120

A   B

1100a

1120

Heated Substrate

FIG. 44B

$\cdots -In-O-In- \cdots \ +O\uparrow$

1100a

fixed

1120

A   B

1100a

1120

Heated Substrate

FIG. 45A

In

Ga

O

1st plane

Zn

2nd plane

c

b

InGaZnO₄

FIG. 45B

3rd plane   4th plane

b

c

a

FIG. 46A

FIG. 46B

normal incidence
of Ar or O
with energy
of 300 eV

Ga-Zn-O
In-O
Ga-Zn-O
Ga-Zn-O
In-O
Ga-Zn-O
Ga-Zn-O
In-O
Ga-Zn-O

temperature
control layer
(300K)

fixed layer

InGaZnO₄

incident point

In : ○   Ga : ○   Zn : ●   O : ●

FIG. 47A

at 100 ps after collision of Ar

crack
(small)

C

crack
(large)
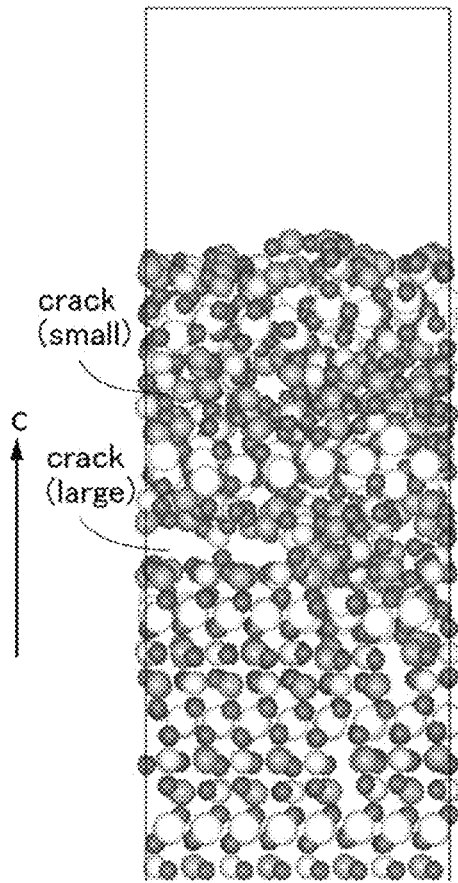
FIG. 47B

at 100 ps after collision of O

crack
(large)

crack
(small)

C

temperature
control layer
(300K)
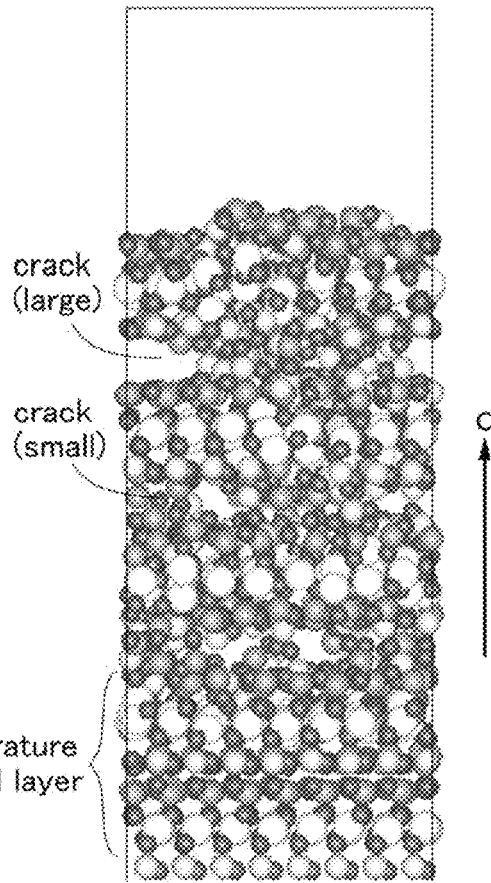
In : ◯   Ga : ◎   Zn : ◉   O : ●

FIG. 48A

trajectories of atoms
from 0 to 0.3 ps
after the incidence of Ar

Ar collides
with Ga

Ga collides
with Zn

Ga-Zn-O
In-O
Ga-Zn-O
Ga-Zn-O
In-O
Ga-Zn-O
Ga-Zn-O
In-O
Ga-Zn-O
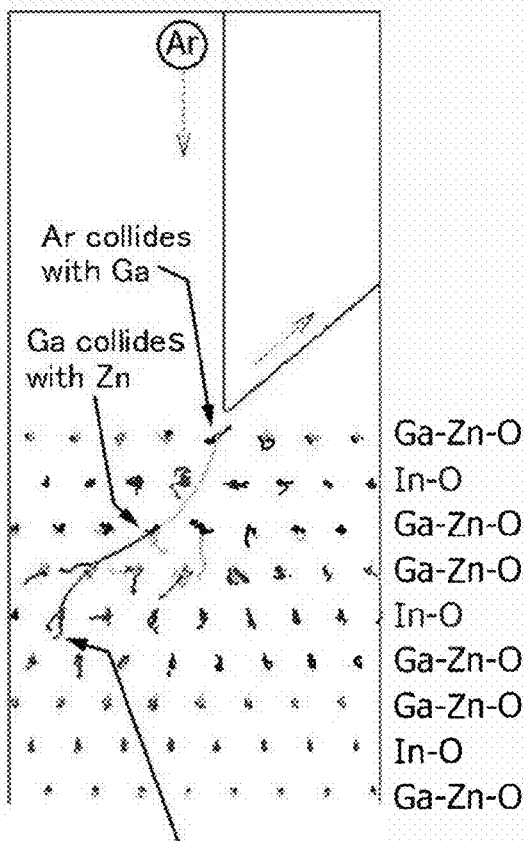
Zn, originally in the 3rd layer
(Ga-Zn-O layer), reaches the
vcinity of the 6th layer
Ga-Zn-O layer)

FIG. 48B

trajectories of atoms
from 0 to 0.3 ps
after the incidence of O

O collides
with Ga

Ga collides
with Zn
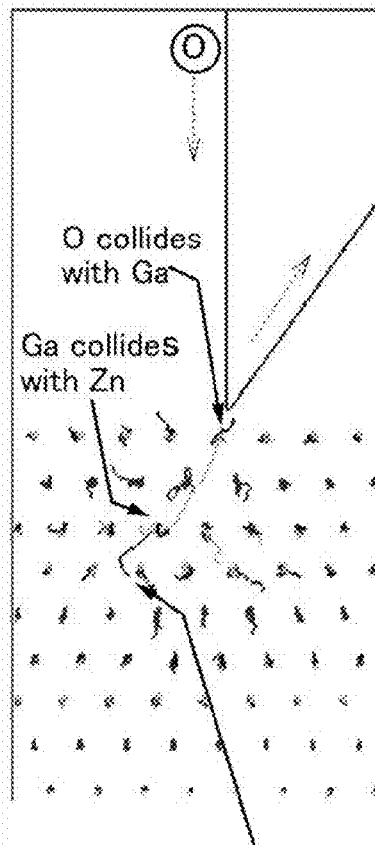
Zn, originally in the 3rd layer
(Ga-Zn-O layer), does not
reach the 5th layer (In-O layer)

FIG. 49A

In

Ga or Zn
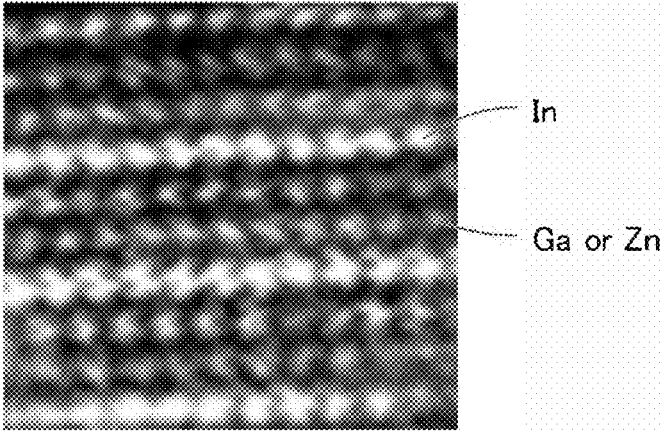
CAAC-OS film   1 nm

FIG. 49B

In

Ga or Zn
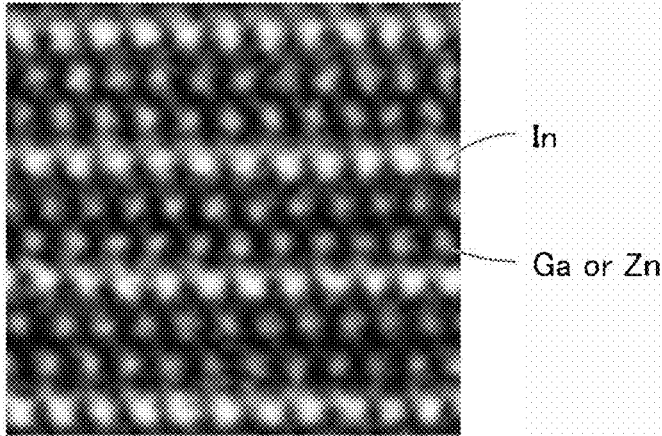
Target   1 nm
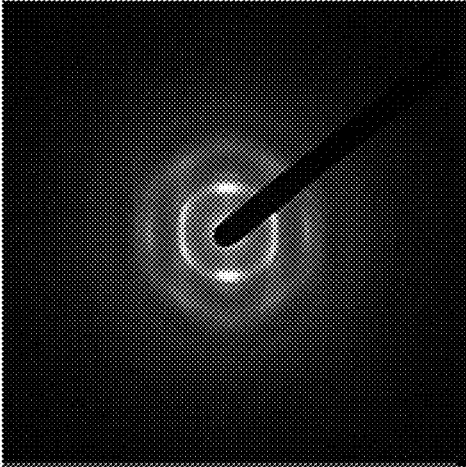
FIG. 50A

FIG. 50B
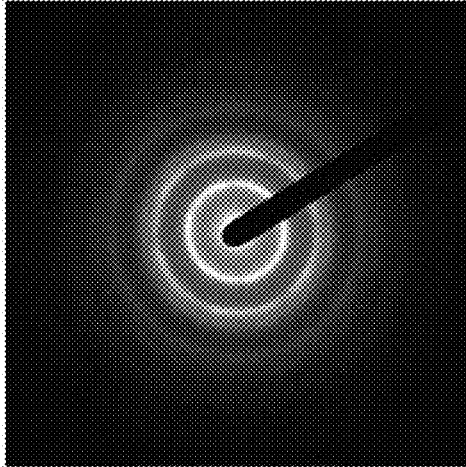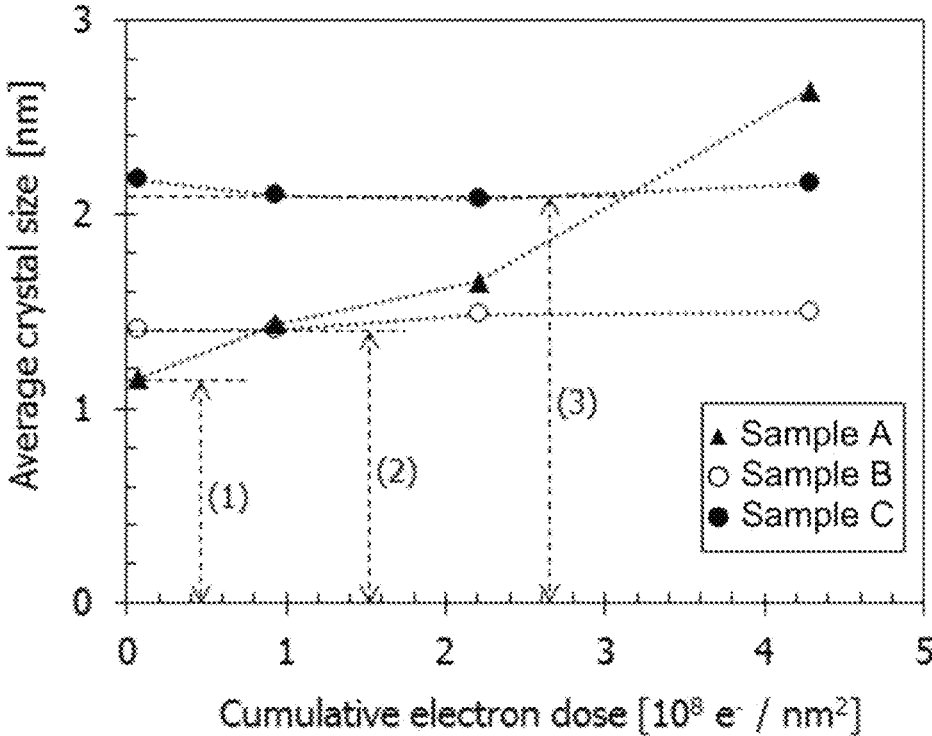
FIG. 51

SEMICONDUCTOR DEVICE, DISPLAY DEVICE INCLUDING THE SEMICONDUCTOR DEVICE, DISPLAY MODULE INCLUDING THE DISPLAY DEVICE, AND ELECTRONIC APPLIANCE INCLUDING THE SEMICONDUCTOR DEVICE, THE DISPLAY DEVICE, AND THE DISPLAY MODULE

BACKGROUND OF THE INVENTION

1. Field of the Invention

One embodiment of the present invention relates to a semiconductor device including an oxide semiconductor and a display device including the semiconductor device.

Note that one embodiment of the present invention is not limited to the above technical field. The technical field of one embodiment of the invention disclosed in this specification and the like relates to an object, a method, and a manufacturing method. In addition, the present invention relates to a process, a machine, manufacture, and a composition of matter. In particular, the present invention relates to a semiconductor device, a display device, a light-emitting device, a power storage device, a storage device, a driving method thereof, and a manufacturing method thereof.

In this specification and the like, a semiconductor device generally means a device that can function by utilizing semiconductor characteristics. A semiconductor element such as a transistor, a semiconductor circuit, an arithmetic device, and a memory device are each an embodiment of a semiconductor device. An imaging device, a display device, a liquid crystal display device, a light-emitting device, an electro-optical device, a power generation device (including a thin film solar cell, an organic thin film solar cell, and the like), and an electronic device may each include a semiconductor device.

2. Description of the Related Art

Attention has been focused on a technique for forming a transistor using a semiconductor thin film formed over a substrate having an insulating surface (also referred to as a field-effect transistor (FET) or a thin film transistor (TFT)). Such transistors are applied to a wide range of electronic devices such as an integrated circuit (IC) and an image display device (display device). A semiconductor material typified by silicon is widely known as a material for a semiconductor thin film that can be used for a transistor. As another material, an oxide semiconductor has been attracting attention (e.g., Patent Document 1).

Furthermore, for example, Patent document 2 discloses a semiconductor device in which, to reduce oxygen vacancy in an oxide semiconductor layer, an insulating film which releases oxygen by heating is used as a base insulating layer of the oxide semiconductor layer where a channel is formed.

REFERENCE

Patent Document

[Patent Document 1] Japanese Published Patent Application No. 2006-165529

[Patent Document 2] Japanese Published Patent Application No. 2012-009836

SUMMARY OF THE INVENTION

In the case where a transistor is manufactured using an oxide semiconductor film for a channel region, oxygen

vacancy formed in the oxide semiconductor film adversely affects the transistor characteristics; therefore, the oxygen vacancy causes a problem. For example, oxygen vacancy formed in the oxide semiconductor film is bonded with hydrogen to serve as a carrier supply source. The carrier supply source generated in the oxide semiconductor film causes a change in the electrical characteristics, typically, shift in the threshold voltage, of the transistor including the oxide semiconductor film. Furthermore, there is a problem in that electrical characteristics fluctuate among the transistors. Therefore, it is preferable that the amount of oxygen vacancy in the channel region of the oxide semiconductor film be as small as possible.

In view of the above problem, an object of one embodiment of the present invention is to inhibit a change in electrical characteristics and to improve reliability in a semiconductor device using a transistor including an oxide semiconductor. Another object of one embodiment of the present invention is to provide a semiconductor device with low power consumption. Another object of one embodiment of the present invention is to provide a novel semiconductor device. Another object of one embodiment of the present invention is to provide a novel display device.

Note that the description of the above object does not disturb the existence of other objects. In one embodiment of the present invention, there is no need to achieve all the objects. Objects other than the above objects will be apparent from and can be derived from the description of the specification and the like.

One embodiment of the present invention is a semiconductor device including a transistor which includes a gate electrode, a first insulating film over the gate electrode, a second insulating film over the first insulating film, an oxide semiconductor film over the second insulating film, a source electrode electrically connected to the oxide semiconductor film, and a drain electrode electrically connected to the oxide semiconductor film. A third insulating film is provided over the transistor, and a fourth insulating film is provided over the third insulating film. The third insulating film includes oxygen. The fourth insulating film includes nitrogen. The amount of oxygen molecules released from the third insulating film is greater than or equal to $1 \times 10^{19}/cm^3$ when measured by thermal desorption spectroscopy. The amount of oxygen molecules released from the fourth insulating film is less than $1 \times 10^{19}/cm^3$ when measured by the thermal desorption spectroscopy.

Another embodiment of the present invention is a semiconductor device including a transistor which includes a gate electrode, a first insulating film over the gate electrode, a second insulating film over the first insulating film, an oxide semiconductor film over the second insulating film, a source electrode electrically connected to the oxide semiconductor film, and a drain electrode electrically connected to the oxide semiconductor film. A third insulating film is provided over the transistor, a fifth insulating film is provided over the third insulating film, and a fourth insulating film is provided over the fifth insulating film. The third insulating film includes oxygen. The fourth insulating film includes nitrogen. The fifth insulating film includes metal. The fifth insulating film includes at least one of oxygen and nitrogen. The amount of oxygen molecules released from the third insulating film is greater than or equal to $1 \times 10^{19}/cm^3$ when measured by thermal desorption spectroscopy. The amount of oxygen molecules released from the fourth insulating film is less than $1 \times 10^{19}/cm^3$ when measured by the thermal desorption spectroscopy.

Another embodiment of the present invention is a semiconductor device including a transistor which includes a gate electrode, a first insulating film over the gate electrode, a second insulating film over the first insulating film, an oxide semiconductor film over the second insulating film, a third insulating film over the oxide semiconductor film, a source electrode electrically connected to the oxide semiconductor film, and a drain electrode electrically connected to the oxide semiconductor film. A fourth insulating film is provided over the transistor. The third insulating film includes oxygen. The fourth insulating film includes nitrogen. The amount of oxygen molecules released from the third insulating film is greater than or equal to $1\times10^{19}/cm^3$ when measured by thermal desorption spectroscopy. The amount of oxygen molecules released from the fourth insulating film is less than $1\times10^{19}/cm^3$ when measured by the thermal desorption spectroscopy.

Another embodiment of the present invention is a semiconductor device including a transistor which includes a gate electrode, a first insulating film over the gate electrode, a second insulating film over the first insulating film, an oxide semiconductor film over the second insulating film, a third insulating film over the oxide semiconductor film, a fifth insulating film over the third insulating film, a source electrode electrically connected to the oxide semiconductor film, and a drain electrode electrically connected to the oxide semiconductor film. A fourth insulating film is provided over the transistor. The third insulating film includes oxygen. The fourth insulating film includes nitrogen. The fifth insulating film includes a metal element. The fifth insulating film includes at least one of oxygen and nitrogen. The amount of oxygen molecules released from the third insulating film is greater than or equal to $1\times10^{19}/cm^3$ when measured by thermal desorption spectroscopy. The amount of oxygen molecules released from the fourth insulating film is less than $1\times10^{19}/cm^3$ when measured by the thermal desorption spectroscopy.

In any of the above structures, the third insulating film preferably includes oxygen, nitrogen, and silicon. In any of the above structures, the fourth insulating film preferably includes nitrogen and silicon.

In any of the above structures, the metal element included in the fifth insulating film preferably includes at least one of indium, zinc, titanium, aluminum, tungsten, tantalum, and molybdenum.

In any of the above structures, the first insulating film preferably includes nitrogen and silicon.

In any of the above structures, the oxide semiconductor film preferably includes O, In, Zn, and M (M is Ti, Ga, Y, Zr, La, Ce, Nd, or Hf). In any of the above structures, it is preferable that the oxide semiconductor film include a crystal part, the crystal part include a portion, and a c-axis of the portion be a parallel to a normal vector of a surface where the oxide semiconductor film is formed.

Another embodiment of the present invention is a display device including the semiconductor device according to any one of the above structures, and a display element. Another embodiment of the present invention is a display module including the display device and a touch sensor. Another embodiment of the present invention is an electronic appliance including the semiconductor device according to any one of the above structures, the display device, or the display module; and an operation key or a battery.

According to one object of one embodiment of the present invention, a change in electrical characteristics can be inhibited and reliability can be improved in a semiconductor device using a transistor including an oxide semiconductor.

Alternatively, according to one embodiment of the present invention, a semiconductor device with low power consumption can be provided. According to one embodiment of the present invention, a novel semiconductor device can be provided. According to one embodiment of the present invention, a novel display device can be provided.

Note that the description of these effects does not disturb the existence of other effects. One embodiment of the present invention does not necessarily achieve all the effects listed above. Other effects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A to 1C are a top view and cross-sectional views illustrating one embodiment of a semiconductor device.

FIGS. 2A to 2D are cross-sectional views each illustrating one embodiment of a semiconductor device.

FIGS. 3A to 3C are a top view and cross-sectional views illustrating one embodiment of a semiconductor device.

FIGS. 4A to 4D are cross-sectional views each illustrating one embodiment of a semiconductor device.

FIGS. 5A to 5C are a top view and cross-sectional views illustrating one embodiment of a semiconductor device.

FIGS. 6A to 6D are cross-sectional views each illustrating one embodiment of a semiconductor device.

FIGS. 7A to 7C are a top view and cross-sectional views illustrating one embodiment of a semiconductor device.

FIGS. 8A to 8D are cross-sectional views each illustrating one embodiment of a semiconductor device.

FIGS. 9A and 9B are band diagrams.

FIGS. 10A to 10D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 11A to 11D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 12A to 12D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 13A and 13B are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 14A to 14D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 15A to 15D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 16A to 16D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 17A to 17D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 18A to 18C are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 19A to 19D are Cs-corrected high-resolution TEM images of a cross section of a CAAC-OS and a cross-sectional schematic view of a CAAC-OS.

FIGS. 20A to 20D are Cs-corrected high-resolution TEM images of a plane of a CAAC-OS.

FIGS. 21A to 21C show structural analysis of a CAAC-OS and a single crystal oxide semiconductor by XRD.

FIG. 22 shows a movement path of oxygen in an In—Ga—Zn oxide.

FIG. 23 illustrates a calculation model.

FIGS. 24A and 24B illustrate an initial state and a final state, respectively.

FIG. 25 shows an activation barrier.

FIGS. 26A and 26B illustrate an initial state and a final state, respectively.

FIG. 27 shows an activation barrier.

FIG. 28 shows the transition levels of V_OH.

FIG. 29 is a top view illustrating one embodiment of a display device.

FIG. 30 is a cross-sectional view illustrating one embodiment of a display device.

FIG. 31 is a cross-sectional view illustrating one embodiment of a display device.

FIGS. 32A to 32C are a block diagram and circuit diagrams illustrating a display device.

FIG. 33 illustrates a display module.

FIGS. 34A to 34H illustrate electronic appliances.

FIG. 35 shows TDS measurement results.

FIGS. 36A and 36B show SIMS measurement results.

FIGS. 37A and 37B each show the electric characteristics of transistors in an example.

FIGS. 38A and 38B each show the electric characteristics of transistors in an example.

FIG. 39 shows results of reliability tests performed on transistors in an example.

FIG. 40A schematically illustrates a CAAC-OS deposition model, and FIGS. 40B and 40C are cross-sectional views of pellets and a CAAC-OS.

FIG. 41 schematically illustrates a deposition model of an nc-OS and a pellet.

FIG. 42 illustrates a pellet.

FIG. 43 illustrates force applied to a pellet on a formation surface.

FIGS. 44A and 44B illustrate transfer of pellets on formation surfaces.

FIGS. 45A and 45B illustrate an $InGaZnO_4$ crystal.

FIGS. 46A and 46B show a structure and the like of $InGaZnO_4$ before collision of an atom.

FIGS. 47A and 47B show a structure and the like of $InGaZnO_4$ after collision of an atom.

FIGS. 48A and 48B show trajectories of atoms after collision of atoms.

FIGS. 49A and 49B are cross-sectional HAADF-STEM images of a CAAC-OS and a target.

FIGS. 50A and 50B show electron diffraction patterns of a CAAC-OS.

FIG. 51 shows a change in crystal part of an In—Ga—Zn oxide induced by electron irradiation.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, embodiments will be described with reference to drawings. However, the embodiments can be implemented with various modes. It will be readily appreciated by those skilled in the art that modes and details can be changed in various ways without departing from the spirit and scope of the present invention. Thus, the present invention should not be interpreted as being limited to the following description of the embodiments.

In the drawings, the size, the layer thickness, and the region is exaggerated for clarity in some cases. Therefore, embodiments of the present invention are not limited to such a scale. Note that the drawings are schematic views showing

ideal examples, and embodiments of the present invention are not limited to shapes or values shown in the drawings.

Note that in this specification, ordinal numbers such as "first", "second", and "third" are used in order to avoid confusion among components, and the terms do not limit the components numerically.

Note that in this specification, terms for describing arrangement, such as "over" "above", "under", and "below", are used for convenience in describing a positional relation between components with reference to drawings. Furthermore, the positional relation between components is changed as appropriate in accordance with a direction in which each component is described. Thus, there is no limitation on terms used in this specification, and description can be made appropriately depending on the situation.

In this specification and the like, a transistor is an element having at least three terminals of a gate, a drain, and a source. In addition, the transistor has a channel region between a drain (a drain terminal, a drain region, or a drain electrode) and a source (a source terminal, a source region, or a source electrode), and current can flow through the drain region, the channel region, and the source region. Note that in this specification and the like, a channel region refers to a region through which current mainly flows.

Further, functions of a source and a drain might be switched when transistors having different polarities are employed or a direction of current flow is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be switched in this specification and the like.

Note that in this specification and the like, the expression "electrically connected" includes the case where components are connected through an "object having any electric function". There is no particular limitation on an "object having any electric function" as long as electric signals can be transmitted and received between components that are connected through the object. Examples of an "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and elements with a variety of functions as well as an electrode and a wiring.

Note that in this specification and the like, a "silicon oxynitride film" refers to a film that includes oxygen at a higher proportion than nitrogen, and a "silicon nitride oxide film" refers to a film that includes nitrogen at a higher proportion than oxygen.

In this specification and the like, the term "parallel" indicates that the angle formed between two straight lines is greater than or equal to $-10°$ and less than or equal to $10°$, and accordingly also includes the case where the angle is greater than or equal to $-5°$ and less than or equal to $5°$. A term "substantially parallel" indicates that the angle formed between two straight lines is greater than or equal to $-30°$ and less than or equal to $30°$. In addition, a term "perpendicular" indicates that the angle formed between two straight lines is greater than or equal to $80°$ and less than or equal to $100°$, and accordingly includes the case where the angle is greater than or equal to $85°$ and less than or equal to $95°$. A term "substantially perpendicular" indicates that the angle formed between two straight lines is greater than or equal to $60°$ and less than or equal to $120°$.

Embodiment 1

In this embodiment, a semiconductor device of one embodiment of the present invention is described with reference to FIGS. 1A to 1C, FIGS. 2A to 2D, FIGS. 3A to 3C, FIGS. 4A to 4D, FIGS. 5A to 5C, FIGS. 6A to 6D, FIGS.

7A to 7C, FIGS. 8A to 8D, FIGS. 9A and 9B, FIGS. 10A to 10D, FIGS. 11A to 11D, FIGS. 12A to 12D, FIGS. 13A and 13B, FIGS. 14A to 14D, FIGS. 15A to 15D, FIGS. 16A to 16D, FIGS. 17A to 17D, and FIGS. 18A to 18C.

Structural Example 1 of Semiconductor Device

FIG. 1A is a top view of a transistor 100 that is a semiconductor device of one embodiment of the present invention. FIG. 1B is a cross-sectional view taken along a dashed dotted line X1-X2 in FIG. 1A, and FIG. 1C is a cross-sectional view taken along a dashed dotted line Y1-Y2 in FIG. 1A. Note that in FIG. 1A, some components of the transistor 100 (e.g., an insulating film serving as a gate insulating film) are not illustrated to avoid complexity. Furthermore, the direction of the dashed dotted line X1-X1 may be called a channel length direction, and the direction of the dashed dotted line Y1-Y2 may be called a channel width direction. As in FIG. 1A, some components are not illustrated in some cases in top views of transistors described below.

The transistor 100 includes a conductive film 104 functioning as a gate electrode over a substrate 102, an insulating film 106 (also referred to as a first insulating film) over the substrate 102 and the conductive film 104, an insulating film 107 (also referred to as a second insulating film) over the insulating film 106, an oxide semiconductor film 108 over the insulating film 107, and conductive films 112a and 112b functioning as source and drain electrodes electrically connected to the oxide semiconductor film 108. Over the transistor 100, specifically, over the conductive films 112a and 112b and the oxide semiconductor film 108, insulating films 114 and 116 (also referred to as third insulating films) and an insulating film 118 (also referred to as a fourth insulating film) are provided. The insulating films 114, 116, and 118 function as protective insulating films for the transistor 100.

Note that in the transistor 100, the conductive film 112a has a two-layer structure formed of a conductive film 110a and a conductive film 111a. In addition, the conductive film 112b has a two-layer structure formed of a conductive film 110b and a conductive film 111b. Note that the structures of the conductive films 112a and 112b are not limited thereto, and the conductive films 112a and 112b each may have a single-layer structure or a stacked-layer structure including three or more layers.

The insulating film 106 and the insulating film 107 each serve as a gate insulating film of the transistor 100.

When oxygen vacancy is formed in the oxide semiconductor film 108 included in the transistor 100, electrons serving as carriers are generated; as a result, the transistor 100 tends to be normally-on. Therefore, for stable transistor characteristics, it is important to reduce oxygen vacancy in the oxide semiconductor film 108. In the structure of the transistor of one embodiment of the present invention, excess oxygen is introduced into an insulating film over the oxide semiconductor film 108, here, the insulating film 114 over the oxide semiconductor film 108, whereby oxygen is moved from the insulating film 114 to the oxide semiconductor film 108 to fill oxygen vacancy in the oxide semiconductor film 108. Alternatively, excess oxygen is introduced into the insulating film 116 over the oxide semiconductor film 108, whereby oxygen is moved from the insulating film 116 to the oxide semiconductor film 108 through the insulating film 114 to fill oxygen vacancy in the oxide semiconductor film 108. Alternatively, excess oxygen is introduced into the insulating films 114 and 116 over the oxide semiconductor film 108, whereby oxygen is moved from both the insulating films 114 and 116 to the oxide semiconductor film 108 to fill oxygen vacancy in the oxide semiconductor film 108.

Therefore, the insulating films 114 and 116 include oxygen. Specifically, the insulating films 114 and 116 include oxygen that is easily moved to the oxide semiconductor film 108 in the insulating films 114 and 116. Examples of the oxygen include O and O_2. It is preferable that the insulating films 114 and 116 each include a region (oxygen excess region) including oxygen in excess of that in the stoichiometric composition. In other words, the insulating films 114 and 116 are each an insulating film capable of releasing oxygen. Note that the oxygen excess region is formed in each of the insulating films 114 and 116 in such a manner that oxygen is introduced into the insulating films 114 and 116 after the deposition, for example. As a method for introducing oxygen, an ion implantation method, an ion doping method, a plasma immersion ion implantation method, plasma treatment, or the like may be employed.

The amount of oxygen molecules released from each of the insulating films 114 and 116 is greater than or equal to $1 \times 10^{19}/cm^3$ when measured by thermal desorption spectroscopy (TDS). Oxygen can exist between lattices uniformly or substantially uniformly in the insulating films 114 and 116. Oxygen in the insulating films 114 and 116 is released to the oxide semiconductor film 108 by heat treatment.

The amount of oxygen molecules released from the insulating film 118 is less than $1 \times 10^{19}/cm^3$ when measured by TDS.

Providing the insulating films 114 and 116 over the oxide semiconductor film 108 makes it possible to move oxygen in the insulating films 114 and 116 to the oxide semiconductor film 108, so that oxygen vacancy formed in the oxide semiconductor film 108 can be filled. Furthermore, the insulating film 118, which releases a small amount of oxygen, provided over the insulating films 114 and 116 can inhibit oxygen in the insulating films 114 and 116 from diffusing to the outside. The oxygen vacancy in the oxide semiconductor film 108 is filled, whereby a highly reliable semiconductor device can be provided.

Note that the insulating film 114 can be formed using an oxide insulating film having a low density of states due to nitrogen oxide between the energy of the valence band maximum (E_{v_os}) and the energy of the conduction band minimum (E_{c_os}) of the oxide semiconductor film. A silicon oxynitride film that releases less nitrogen oxide, an aluminum oxynitride film that releases less nitrogen oxide, and the like can be used as the oxide insulating film in which the density of states due to nitrogen oxide is low between E_{v_os} and E_{c_os}.

Note that a silicon oxynitride film that releases less nitrogen oxide is a film of which the amount of released ammonia is larger than the amount of released nitrogen oxide in thermal desorption spectroscopy analysis; the amount of released ammonia is typically greater than or equal to $1 \times 10^{18}/cm^3$ and less than or equal to $5 \times 10^{19}/cm^3$. Note that the amount of released ammonia is the amount of ammonia released by heat treatment with which the surface temperature of a film becomes higher than or equal to 50° C. and lower than or equal to 650° C., preferably higher than or equal to 50° C. and lower than or equal to 550° C.

Nitrogen oxide (NO_x; x is greater than or equal to 0 and less than or equal to 2, preferably greater than or equal to 1 and less than or equal to 2), typically NO_2 or NO, forms levels in the insulating film 114, for example. The level is positioned in the energy gap of the oxide semiconductor film

108. Therefore, when nitrogen oxide is diffused to the interface between the insulating film 114 and the oxide semiconductor film 108, an electron is trapped by the level on the insulating film 114 side. As a result, the trapped electron remains in the vicinity of the interface between the insulating film 114 and the oxide semiconductor film 108; thus, the threshold voltage of the transistor is shifted in the positive direction.

Nitrogen oxide reacts with ammonia and oxygen in heat treatment. Since nitrogen oxide included in the insulating film 114 reacts with ammonia included in the insulating film 116 in heat treatment, nitrogen oxide included in the insulating film 114 is reduced. Therefore, an electron is hardly trapped at the interface between the insulating film 114 and the oxide semiconductor film 108.

By using, for the insulating film 114, the oxide insulating film having a low density of states due to nitrogen oxide between E_{v_os} and E_{c_os}, the shift in the threshold voltage of the transistor can be reduced, which leads to a smaller change in the electrical characteristics of the transistor.

Note that in an ESR spectrum at 100 K or lower of the insulating film 114, by heat treatment of a manufacturing process of the transistor, typically heat treatment at a temperature higher than or equal to 300° C. and lower than the strain point of the substrate, a first signal that appears at a g-factor of greater than or equal to 2.037 and less than or equal to 2.039, a second signal that appears at a g-factor of greater than or equal to 2.001 and less than or equal to 2.003, and a third signal that appears at a g-factor of greater than or equal to 1.964 and less than or equal to 1.966 are observed. The split width of the first and second signals and the split width of the second and third signals that are obtained by ESR measurement using an X-band are each approximately 5 mT. The sum of the spin densities of the first signal that appears at a g-factor of greater than or equal to 2.037 and less than or equal to 2.039, the second signal that appears at a g-factor of greater than or equal to 2.001 and less than or equal to 2.003, and the third signal that appears at a g-factor of greater than or equal to 1.964 and less than or equal to 1.966 is lower than 1×10^{18} spins/cm^3, typically higher than or equal to 1×10^{17} spins/cm^3 and lower than 1×10^{18} spins/cm^3.

In the ESR spectrum at 100 K or lower, the first signal that appears at a g-factor of greater than or equal to 2.037 and less than or equal to 2.039, the second signal that appears at a g-factor of greater than or equal to 2.001 and less than or equal to 2.003, and the third signal that appears at a g-factor of greater than or equal to 1.964 and less than or equal to 1.966 correspond to signals attributed to nitrogen oxide (NO$_x$; x is greater than or equal to 0 and smaller than or equal to 2, preferably greater than or equal to 1 and less than or equal to 2). Typical examples of nitrogen oxide include nitrogen monoxide and nitrogen dioxide. In other words, the lower the total spin density of the first signal that appears at a g-factor of greater than or equal to 2.037 and less than or equal to 2.039, the second signal that appears at a g-factor of greater than or equal to 2.001 and less than or equal to 2.003, and the third signal that appears at a g-factor of greater than or equal to 1.964 and less than or equal to 1.966 is, the lower the content of nitrogen oxide in the oxide insulating film is.

The nitrogen concentration of the oxide insulating film having a low density of states due to nitrogen oxide between E_{v_os} and E_{c_os} measured by secondary mass spectrometry (SIMS) is lower than or equal to 6×10^{20} atoms/cm^3.

The oxide insulating film in which the density of states due to nitrogen oxide is low between E_{v_os} and E_{c_os} is

formed by a PECVD method at a substrate temperature of higher than or equal to 220° C., higher than or equal to 280° C., or higher than or equal to 350° C. using silane and nitrogen oxide, whereby a dense and hard film can be formed.

Other constituent elements of the semiconductor device of this embodiment are described below in detail.

<Substrate>

There is no particular limitation on the property of a material and the like of the substrate 102 as long as the material has heat resistance enough to withstand at least heat treatment to be performed later. For example, a glass substrate, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like may be used as the substrate 102. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, a compound semiconductor substrate made of silicon germanium or the like, an SOI substrate, or the like may be used as the substrate 102. Still alternatively, any of these substrates provided with a semiconductor element may be used as the substrate 102. In the case where a glass substrate is used as the substrate 102, a glass substrate having any of the following sizes can be used: the 6th generation (1500 mm×1850 mm), the 7th generation (1870 mm×2200 mm), the 8th generation (2200 mm×2400 mm), the 9th generation (2400 mm×2800 mm), and the 10th generation (2950 mm×3400 mm). Thus, a large-sized display device can be manufactured.

Alternatively, a flexible substrate may be used as the substrate 102, and the transistor 100 may be provided directly on the flexible substrate. Alternatively, a separation layer may be provided between the substrate 102 and the transistor 100. The separation layer can be used when part or the whole of a semiconductor device formed over the separation layer is separated from the substrate 102 and transferred onto another substrate. In such a case, the transistor 100 can be transferred to a substrate having low heat resistance or a flexible substrate as well.

<Conductive Film>

The conductive film 104 functioning as a gate electrode and the conductive films 112a and 112b functioning as a source electrode and a drain electrode can each be formed using a metal element selected from chromium (Cr), copper (Cu), aluminum (Al), gold (Au), silver (Ag), zinc (Zn), molybdenum (Mo), tantalum (Ta), titanium (Ti), tungsten (W), manganese (Mn), nickel (Ni), iron (Fe), and cobalt (Co); an alloy including any of these metal element as its component; an alloy including a combination of any of these elements; or the like.

Furthermore, the conductive films 104, 112a, and 112b may have a single-layer structure or a stacked-layer structure of two or more layers. For example, a single-layer structure of an aluminum film including silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a two-layer structure in which a titanium film is stacked over a titanium nitride film, a two-layer structure in which a tungsten film is stacked over a titanium nitride film, a two-layer structure in which a tungsten film is stacked over a tantalum nitride film or a tungsten nitride film, a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order, and the like can be given. Alternatively, an alloy film or a nitride film in which aluminum and one or more elements selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium are combined may be used.

The conductive films 104, 112a, and 112b can be formed using a light-transmitting conductive material such as

indium tin oxide, indium oxide including tungsten oxide, indium zinc oxide including tungsten oxide, indium oxide including titanium oxide, indium tin oxide including titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added.

A Cu—X alloy film (X is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) may be used for the conductive films **104**, **112**_a_, and **112**_b_. Use of a Cu—X alloy film enables the manufacturing cost to be reduced because wet etching process can be used in the processing.

<Gate Insulating Film>

As each of the insulating films **106** and **107** functioning as a gate insulating film of the transistor **100**, an insulating layer including at least one of the following films formed by a plasma enhanced chemical vapor deposition (PECVD) method, a sputtering method, or the like can be used: a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, an aluminum oxide film, a hafnium oxide film, an yttrium oxide film, a zirconium oxide film, a gallium oxide film, a tantalum oxide film, a magnesium oxide film, a lanthanum oxide film, a cerium oxide film, and a neodymium oxide film. Note that instead of a stacked structure of the insulating films **106** and **107**, an insulating film of a single layer formed using a material selected from the above or an insulating film of three or more layers may be used.

The insulating film **106** functions as a blocking film which keeps out oxygen. For example, in the case where excess oxygen is supplied to the insulating film **107**, the insulating film **114**, the insulating film **116**, and/or the oxide semiconductor film **108**, the insulating film **106** can keep out oxygen.

Note that the insulating film **107** that is in contact with the oxide semiconductor film **108** functioning as a channel region of the transistor **100** is preferably an oxide insulating film and preferably includes a region including oxygen in excess of the stoichiometric composition (oxygen-excess region). In other words, the insulating film **107** is an insulating film which is capable of releasing oxygen. In order to provide the oxygen excess region in the insulating film **107**, the insulating film **107** is formed in an oxygen atmosphere, for example. Alternatively, the oxygen excess region may be formed by introduction of oxygen into the insulating film **107** after the deposition. As a method for introducing oxygen, an ion implantation method, an ion doping method, a plasma immersion ion implantation method, plasma treatment, or the like may be employed.

In the case where hafnium oxide is used for the insulating film **107**, the following effect is attained. Hafnium oxide has a higher dielectric constant than silicon oxide and silicon oxynitride. Therefore, by using hafnium oxide or aluminum oxide, a physical thickness can be made larger than an equivalent oxide thickness; thus, even in the case where the equivalent oxide thickness is less than or equal to 10 nm or less than or equal to 5 nm, leakage current due to tunnel current can be low. That is, it is possible to provide a transistor with a low off-state current. Moreover, hafnium oxide with a crystalline structure has higher dielectric constant than hafnium oxide with an amorphous structure. Therefore, it is preferable to use hafnium oxide with a crystalline structure in order to provide a transistor with a low off-state current. Examples of the crystalline structure include a monoclinic crystal structure and a cubic crystal structure. Note that one embodiment of the present invention is not limited thereto.

In this embodiment, a silicon nitride film is formed as the insulating film **106**, and a silicon oxide film is formed as the insulating film **107**. The silicon nitride film has a higher

dielectric constant than a silicon oxide film and needs a larger thickness for capacitance equivalent to that of the silicon oxide film. Thus, when the silicon nitride film is included in the gate insulating film of the transistor **150**, the physical thickness of the insulating film can be increased. This makes it possible to reduce a decrease in withstand voltage of the transistor **100** and furthermore to increase the withstand voltage, thereby reducing electrostatic discharge damage to the transistor **100**.

<Oxide Semiconductor Film>

The oxide semiconductor film **108** contains O, In, Zn, and M (M is Ti, Ga, Y, Zr, La, Ce, Nd, or Hf). Typically, In—Ga oxide, In—Zn oxide, or In-M-Zn oxide can be used for the oxide semiconductor film **108**. It is particularly preferable to use In-M-Zn oxide for the semiconductor film **108**.

In the case where the oxide semiconductor film **108** is formed of In-M-Zn oxide, it is preferable that the atomic ratio of metal elements of a sputtering target used for forming the In-M-Zn oxide satisfy In$\geq$M and Zn$\geq$M. As the atomic ratio of metal elements of such a sputtering target, In:M:Zn=1:1:1, In:M:Zn=1:1:1.2, and In:M:Zn=3:1:2 are preferable. Note that the atomic ratios of metal elements in the formed oxide semiconductor film **108** vary from the above atomic ratio of metal elements of the sputtering target within a range of ±40% as an error.

Note that in the case where the oxide semiconductor film **108** is an In-M-Zn oxide film, the proportion of In and the proportion of M, not taking Zn and O into consideration, are preferably greater than or equal to 25 atomic % and less than 75 atomic %, respectively, further preferably greater than or equal to 34 atomic % and less than 66 atomic %, respectively.

The energy gap of the oxide semiconductor film **108** is 2 eV or more, preferably 2.5 eV or more, further preferably 3 eV or more. With the use of an oxide semiconductor having such a wide energy gap, the off-state current of the transistor **150** can be reduced.

The thickness of the oxide semiconductor film **108** is greater than or equal to 3 nm and less than or equal to 200 nm, preferably greater than or equal to 3 nm and less than or equal to 100 nm, further preferably greater than or equal to 3 nm and less than or equal to 50 nm.

An oxide semiconductor film with low carrier density is used as the oxide semiconductor film **108**. For example, an oxide semiconductor film whose carrier density is lower than or equal to 1×10^{17}/cm^3, preferably lower than or equal to 1×10^{15}/cm^3, further preferably lower than or equal to 1×10^{13}/cm^3, still further preferably lower than or equal to 1×10^{11}/cm^3 is used as the oxide semiconductor film **108**.

Note that, without limitation to the compositions and materials described above, a material with an appropriate composition may be used depending on required semiconductor characteristics and electrical characteristics (e.g., field-effect mobility and threshold voltage) of a transistor. Further, in order to obtain required semiconductor characteristics of a transistor, it is preferable that the carrier density, the impurity concentration, the defect density, the atomic ratio of a metal element to oxygen, the interatomic distance, the density, and the like of the oxide semiconductor film **108** be set to be appropriate.

Note that it is preferable to use, as the oxide semiconductor film **108**, an oxide semiconductor film in which the impurity concentration is low and density of defect states is low, in which case the transistor can have more excellent electrical characteristics. Here, the state in which impurity concentration is low and density of defect states is low (the amount of oxygen vacancy is small) is referred to as "highly

purified intrinsic" or "substantially highly purified intrinsic". A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has few carrier generation sources, and thus can have a low carrier density. Thus, a transistor in which a channel region is formed in the oxide semiconductor film rarely has a negative threshold voltage (is rarely normally on). A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has a low density of defect states and accordingly has few carrier traps in some cases. Further, the highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has an extremely low off-state current; even when an element has a channel width of 1×10^6 μm and a channel length L of 10 μm, the off-state current can be less than or equal to the measurement limit of a semiconductor parameter analyzer, i.e., less than or equal to 1×10^{-13} A, at a voltage (drain voltage) between a source electrode and a drain electrode of from 1 V to 10 V.

Accordingly, the transistor in which the channel region is formed in the highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film can have a small variation in electrical characteristics and high reliability. Charges trapped by the trap states in the oxide semiconductor film take a long time to be released and may behave like fixed charges. Thus, the transistor whose channel region is formed in the oxide semiconductor film having a high density of trap states has unstable electrical characteristics in some cases. As examples of the impurities, hydrogen, nitrogen, alkali metal, alkaline earth metal, and the like are given.

Hydrogen included in the oxide semiconductor film reacts with oxygen bonded to a metal atom to be water, and also causes oxygen vacancy in a lattice from which oxygen is released (or a portion from which oxygen is released). Due to entry of hydrogen into the oxygen vacancy, an electron serving as a carrier is generated in some cases. Furthermore, in some cases, bonding of part of hydrogen to oxygen bonded to a metal element causes generation of an electron serving as a carrier. Thus, a transistor including an oxide semiconductor film which contains hydrogen is likely to be normally on. Accordingly, it is preferable that hydrogen be reduced as much as possible in the oxide semiconductor film 108. Specifically, in the oxide semiconductor film 108, the concentration of hydrogen which is measured by SIMS is lower than or equal to 2×10^{20} atoms/cm³, preferably lower than or equal to 5×10^{19} atoms/cm³, further preferably lower than or equal to 1×10^{19} atoms/cm³, further preferably lower than or equal to 5×10^{18} atoms/cm³, further preferably lower than or equal to 1×10^{18} atoms/cm³, further preferably lower than or equal to 5×10^{17} atoms/cm³, further preferably lower than or equal to 1×10^{16} atoms/cm³.

When silicon or carbon that is one of elements belonging to Group 14 is included in the oxide semiconductor film 108, oxygen vacancy is increased in the oxide semiconductor film 108, and the oxide semiconductor film 108 becomes an n-type film. Thus, the concentration of silicon or carbon (the concentration is measured by SIMS) in the oxide semiconductor film 108 or the concentration of silicon or carbon (the concentration is measured by SIMS) in the vicinity of an interface with the oxide semiconductor film 108 is set to be lower than or equal to 2×10^{18} atoms/cm³, preferably lower than or equal to 2×10^{17} atoms/cm³.

In addition, the concentration of alkali metal or alkaline earth metal of the oxide semiconductor film 108, which is measured by SIMS, is lower than or equal to 1×10^{18} atoms/cm³, preferably lower than or equal to 2×10^{16} atoms/cm³. Alkali metal and alkaline earth metal might generate carriers when bonded to an oxide semiconductor, in which

case the off-state current of the transistor might be increased. Therefore, it is preferable to reduce the concentration of alkali metal or alkaline earth metal of the oxide semiconductor film 108.

Furthermore, when including nitrogen, the oxide semiconductor film 108 easily becomes n-type by generation of electrons serving as carriers and an increase of carrier density. Thus, a transistor including an oxide semiconductor film which contains nitrogen is likely to have normally-on characteristics. For this reason, nitrogen in the oxide semiconductor film is preferably reduced as much as possible; the concentration of nitrogen which is measured by SIMS is preferably set, for example, lower than or equal to 5×10^{18} atoms/cm³.

The oxide semiconductor film 108 may have a non-single-crystal structure, for example. The non-single crystal structure includes a c-axis aligned crystalline oxide semiconductor (CAAC-OS) which is described later, a polycrystalline structure, a microcrystalline structure described later, or an amorphous structure, for example. Among the non-single crystal structure, the amorphous structure has the highest density of defect states, whereas CAAC-OS has the lowest density of defect states.

The oxide semiconductor film 108 may have an amorphous structure, for example. The oxide semiconductor films having the amorphous structure each have disordered atomic arrangement and no crystalline component, for example. Alternatively, the oxide films having an amorphous structure have, for example, an absolutely amorphous structure and no crystal part.

Note that the oxide semiconductor film 108 may be a mixed film including two or more of the following: a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline structure, a region of CAAC-OS, and a region having a single-crystal structure. The mixed film has a single-layer structure including, for example, two or more of a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline structure, a CAAC-OS region, and a region having a single-crystal structure in some cases. Furthermore, in some cases, the mixed film has a stacked-layer structure of two or more of a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline structure, a CAAC-OS region, and a region having a single-crystal structure.

<Protective Insulating Film>

The insulating films 114, 116, and 118 function as protective insulating films. The insulating films 114 and 116 contains oxygen. Furthermore, the insulating film 114 is an insulating film which is permeable to oxygen. Note that the insulating film 114 also functions as a film which relieves damage to the oxide semiconductor film 108 at the time of forming the insulating film 116 in a later step.

A silicon oxide film, a silicon oxynitride film, or the like with a thickness greater than or equal to 5 nm and less than or equal to 150 nm, preferably greater than or equal to 5 nm and less than or equal to 50 nm can be used as the insulating film 114.

In addition, it is preferable that the number of defects in the insulating film 114 be small and typically, the spin density corresponding to a signal that appears at g=2.001 due to a dangling bond of silicon be lower than or equal to 3×10^{17} spins/cm³ by electron spin resonance (ESR) measurement. This is because if the density of defects in the

insulating film 114 is high, oxygen is bonded to the defects and the amount of oxygen that penetrates the insulating film 114 is decreased.

Note that all oxygen entering the insulating film 114 from the outside does not move to the outside of the insulating film 114 and some oxygen remains in the insulating film 114. Furthermore, movement of oxygen occurs in the insulating film 114 in some cases in such a manner that oxygen enters the insulating film 114 and oxygen included in the insulating film 114 moves to the outside of the insulating film 114. When an oxide insulating film which is permeable to oxygen is formed as the insulating film 114, oxygen released from the insulating film 116 provided over the insulating film 114 can be moved to the oxide semiconductor film 108 through the insulating film 114.

The insulating film 116 is formed using an oxide insulating film that contains oxygen in excess of that in the stoichiometric composition. Part of oxygen is released by heating from the oxide insulating film including oxygen in excess of that in the stoichiometric composition. The oxide insulating film including oxygen in excess of that in the stoichiometric composition is an oxide insulating film of which the amount of released oxygen converted into oxygen molecules is greater than or equal to $1.0 \times 10^{19}/\text{cm}^3$, preferably greater than or equal to $3.0 \times 10^{20}/\text{cm}^3$ in TDS analysis. Note that the temperature of the film surface in the TDS analysis is preferably higher than or equal to 100° C. and lower than or equal to 700° C., or higher than or equal to 100° C. and lower than or equal to 500° C.

A silicon oxide film, a silicon oxynitride film, or the like with a thickness greater than or equal to 30 nm and less than or equal to 500 nm, preferably greater than or equal to 50 nm and less than or equal to 400 nm can be used as the insulating film 116.

It is preferable that the number of defects in the insulating film 116 be small, and typically the spin density corresponding to a signal which appears at g=2.001 due to a dangling bond of silicon, be lower than 1.5×10^{18} spins/cm³, more preferably lower than or equal to 1×10^{18} spins/cm³ by ESR measurement. Note that the insulating film 116 is provided more apart from the oxide semiconductor film 108 than the insulating film 114 is; thus, the insulating film 116 may have higher density of defects than the insulating film 114.

Furthermore, the insulating films 114 and 116 can be formed using insulating films formed of the same kinds of materials; thus, a boundary between the insulating films 114 and 116 cannot be clearly observed in some cases. Thus, in this embodiment, the boundary between the insulating films 114 and 116 is shown by a dashed line. Although a two-layer structure of the insulating films 114 and 116 is described in this embodiment, the present invention is not limited to this. For example, a single-layer structure of the insulating film 114 may be used.

The insulating film 118 contains nitrogen. Alternatively, the insulating film 118 contains nitrogen and silicon. The insulating film 118 has a function of blocking oxygen, hydrogen, water, an alkali metal, an alkaline earth metal, or the like. It is possible to prevent outward diffusion of oxygen from the oxide semiconductor film 108, outward diffusion of oxygen included in the insulating films 114 and 116, and entry of hydrogen, water, or the like into the oxide semiconductor film 108 from the outside by providing the insulating film 118. A nitride insulating film, for example, can be used as the insulating film 118. The nitride insulating film is formed using silicon nitride, silicon nitride oxide, aluminum nitride, aluminum nitride oxide, or the like. Note that instead of the nitride insulating film having a blocking

effect against oxygen, hydrogen, water, alkali metal, alkaline earth metal, and the like, an oxide insulating film having a blocking effect against oxygen, hydrogen, water, and the like, may be provided. As the oxide insulating film having a blocking effect against oxygen, hydrogen, water, and the like, an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, a gallium oxynitride film, an yttrium oxide film, an yttrium oxynitride film, a hafnium oxide film, and a hafnium oxynitride film can be given.

Although the variety of films such as the conductive films, the insulating films, and the oxide semiconductor films which are described above can be formed by a sputtering method or a PECVD method, such films may be formed by another method, e.g., an atomic layer deposition (ALD) method or a thermal CVD method. As an example of a thermal CVD method, a metal organic chemical vapor deposition (MOCVD) method can be given.

A thermal CVD method has an advantage that no defect due to plasma damage is generated since it does not utilize plasma for forming a film.

Deposition by a thermal CVD method may be performed in such a manner that a source gas and an oxidizer are supplied to the chamber at a time so that the pressure in a chamber is set to an atmospheric pressure or a reduced pressure, and react with each other in the vicinity of the substrate or over the substrate.

Deposition by an ALD method may be performed in such a manner that the pressure in a chamber is set to an atmospheric pressure or a reduced pressure, source gases for reaction are sequentially introduced into the chamber, and then the sequence of the gas introduction is repeated. For example, two or more kinds of source gases are sequentially supplied to the chamber by switching respective switching valves (also referred to as high-speed valves). For example, a first source gas is introduced, an inert gas (e.g., argon or nitrogen) or the like is introduced at the same time as or after the introduction of the first gas so that the source gases are not mixed, and then a second source gas is introduced. Note that in the case where the first source gas and the inert gas are introduced at a time, the inert gas serves as a carrier gas, and the inert gas may also be introduced at the same time as the introduction of the second source gas. Alternatively, the first source gas may be exhausted by vacuum evacuation instead of the introduction of the inert gas, and then the second source gas may be introduced. The first source gas is adsorbed on the surface of the substrate to form a first layer; then the second source gas is introduced to react with the first layer; as a result, a second layer is stacked over the first layer, so that a thin film is formed. The sequence of the gas introduction is repeated plural times until a desired thickness is obtained, whereby a thin film with excellent step coverage can be formed. The thickness of the thin film can be adjusted by the number of repetition times of the sequence of the gas introduction; therefore, an ALD method makes it possible to accurately adjust a thickness and thus is suitable for manufacturing a minute FET.

The variety of films such as the conductive films, the insulating films, the oxide semiconductor films, and the metal oxide films in this embodiment can be formed by a thermal CVD method such as an MOCVD method. For example, in the case where an In—Ga—Zn—O film is formed, trimethylindium, trimethylgallium, and dimethylzinc are used. Note that the chemical formula of trimethylindium is $\text{In}(\text{CH}_3)_3$. The chemical formula of trimethylgallium is $\text{Ga}(\text{CH}_3)_3$. The chemical formula of dimethylzinc is $\text{Zn}(\text{CH}_3)_2$. Without limitation to the above combination, triethylgallium (chemical formula: $\text{Ga}(\text{C}_2\text{H}_5)_3$) can be used

instead of trimethylgallium and diethylzinc (chemical formula: $Zn(C_2H_5)_2$) can be used instead of dimethylzinc.

For example, in the case where a hafnium oxide film is formed by a deposition apparatus using an ALD method, two kinds of gases, i.e., ozone (O_3) as an oxidizer and a source gas which is obtained by vaporizing liquid containing a solvent and a hafnium precursor compound (a hafnium alkoxide solution, typically tetrakis(dimethylamide)hafnium (TDMAH)) are used. Note that the chemical formula of tetrakis(dimethylamide)hafnium is $Hf[N(CH_3)_2]_4$. Examples of another material liquid include tetrakis(ethylmethylamide)hafnium.

For example, in the case where an aluminum oxide film is formed by a deposition apparatus using an ALD method, two kinds of gases, e.g., H_2O as an oxidizer and a source gas which is obtained by vaporizing liquid containing a solvent and an aluminum precursor compound (e.g., trimethylaluminum (TMA)) are used. Note that the chemical formula of trimethylaluminum is $Al(CH_3)_3$. Examples of another material liquid include tris(dimethylamide)aluminum, triisobutylaluminum, and aluminum tris(2,2,6,6-tetramethyl-3,5-heptanedionate).

For example, in the case where a silicon oxide film is formed by a deposition apparatus using an ALD method, hexachlorodisilane is adsorbed on a surface where a film is to be formed, chlorine included in the adsorbate is removed, and radicals of an oxidizing gas (e.g., O_2 or dinitrogen monoxide) are supplied to react with the adsorbate.

For example, in the case where a tungsten film is formed using a deposition apparatus employing ALD, a WF_6 gas and a B_2H_6 gas are sequentially introduced plural times to form an initial tungsten film, and then a WF_6 gas and an H_2 gas are introduced at a time, so that a tungsten film is formed. Note that an SiH_4 gas may be used instead of a B_2H_6 gas.

For example, in the case where an oxide semiconductor film, e.g., an In—Ga—Zn—O film is formed using a deposition apparatus employing ALD, an $In(CH_3)_3$ gas and an O_3 gas are sequentially introduced plural times to form an InO_2 layer, a $Ga(CH_3)_3$ gas and an O_3 gas are introduced at a time to form a GaO layer, and then a $Zn(CH_3)_2$ gas and an O_3 gas are introduced at a time to form a ZnO layer. Note that the order of these layers is not limited to this example. A mixed compound layer such as an In—Ga—O layer, an In—Zn—O layer, or a Ga—Zn—O layer may be formed by mixing of these gases. Note that although an H_2O gas which is obtained by bubbling with an inert gas such as Ar may be used instead of an O_3 gas, it is preferable to use an O_3 gas, which does not contain H. Further, instead of an $In(CH_3)_3$ gas, an $In(C_2H_5)_3$ gas may be used. Instead of a $Ga(CH_3)_3$ gas, a $Ga(C_2H_5)_3$ gas may be used. Furthermore, a $Zn(CH_3)_2$ gas may be used.

Structure examples different from that of the transistor 100 in FIGS. 1A to 1C are described with reference to FIGS. 2A to 2D. Note that in the case where a portion has a function similar to that described above, the same hatch pattern is applied to the portion, and the portion is not especially denoted by a reference numeral in some cases.

Structure Example 2 of Semiconductor Device

FIG. 2A is a cross-sectional view in the channel length direction of a transistor 100A and FIG. 2B is a cross-sectional view in the channel width direction of the transistor 100A. FIG. 2C is a cross-sectional view in the channel length direction of a transistor 100B and FIG. 2D is a cross-sectional view in the channel width direction of the transistor 100B. Note that top views of the transistor 100A

and the transistor 100B are omitted here because they are similar to the top view of FIG. 1A.

The transistor 100A illustrated in FIGS. 2A and 2B includes the conductive film 104 functioning as a gate electrode over the substrate 102, the insulating film 106 over the substrate 102 and the conductive film 104, the insulating film 107 over the insulating film 106, the oxide semiconductor film 108 over the insulating film 107, and the conductive films 112a and 112b functioning as source and drain electrodes electrically connected to the oxide semiconductor film 108. Over the transistor 100A, specifically, over the conductive films 112a and 112b and the oxide semiconductor film 108, the insulating films 114, 116, and 118 and an insulating film 131 (also referred to as a fifth insulating film) are provided. The insulating films 114, 116, 118, and 131 function as protective insulating films for the transistor 100A.

The transistor 100A is different from the transistor 100 in FIGS. 1B and 1C in that the insulating film 131 is provided. Specifically, the insulating film 131 is provided between the insulating film 116 and the insulating film 118.

The transistor 100B illustrated in FIGS. 2C and 2D includes the conductive film 104 functioning as a gate electrode over the substrate 102, the insulating film 106 over the substrate 102 and the conductive film 104, the insulating film 107 over the insulating film 106, the oxide semiconductor film 108 over the insulating film 107, and the conductive films 112a and 112b functioning as source and drain electrodes electrically connected to the oxide semiconductor film 108. Over the transistor 100B, specifically, over the conductive films 112a and 112b and the oxide semiconductor film 108, the insulating films 114, 116, 118, and 131 are provided. The insulating films 114, 116, 118, and 131 function as protective insulating films for the transistor 100B.

The transistor 100B is different from the transistor 100 in FIGS. 1B and 1C in that the insulating film 131 is provided. Specifically, the insulating film 131 is provided between the insulating film 114 and the insulating film 116.

The insulating film 131 has a function of inhibiting release of oxygen included in the insulating film 114 and/or the insulating film 116. Furthermore, the insulating film 131 is formed of oxide or nitride of metal, and the metal includes at least one selected from indium, zinc, titanium, aluminum, tungsten, tantalum, and molybdenum.

The insulating film 131 can inhibit oxygen included in the insulating film 114 and/or the insulating film 116 from diffusing to the outside. In other words, the insulating film 131 is provided, whereby oxygen included in the insulating film 114 and/or the insulating film 116 can be favorably moved to the oxide semiconductor film 108 side. Thus, oxygen vacancy in the oxide semiconductor film 108 is filled, whereby a highly reliable semiconductor device can be provided.

A structure example different from that of the transistor 100 in FIGS. 1A to 1C is described with reference to FIGS. 3A to 3C. Note that in the case where a portion has a function similar to that described above, the same hatch pattern is applied to the portion, and the portion is not especially denoted by a reference numeral in some cases.

Structure Example 3 of Semiconductor Device

FIG. 3A is a top view of a transistor 150 that is a semiconductor device of one embodiment of the present invention. FIG. 3B is a cross-sectional view taken along dashed-dotted line X1-X2 illustrated in FIG. 3A, and FIG.

3C is a cross-sectional view taken along dashed-dotted line Y1-Y2 illustrated in FIG. 3A.

The transistor **150** includes the conductive film **104** functioning as a gate electrode over the substrate **102**, the insulating film **106** over the substrate **102** and the conductive film **104**, the insulating film **107** over the insulating film **106**, the oxide semiconductor film **108** over the insulating film **107**, the insulating film **114** over the oxide semiconductor film **108**, the insulating film **116** over the insulating film **114**, and the conductive films **112***a* and **112***b* functioning as source and drain electrodes electrically connected to the oxide semiconductor film **108** though openings **141***a* and **141***b* provided in the insulating film **114** and the insulating film **116**. Over the transistor **150**, specifically, over the conductive films **112***a* and **112***b* and the insulating film **116**, the insulating film **118** is provided. The insulating film **114** and the insulating film **116** function as protective insulating films for the oxide semiconductor film **108**. The insulating film **118** functions as a protective insulating film for the transistor **150**.

Although the transistors **100**, **100A**, and **100B** each have a channel-etched structure, the transistor **150** in FIGS. **3A** to **3C** has a channel-protective structure. Thus, either the channel-etched structure or the channel-protective structure can be applied to the semiconductor device of one embodiment of the present invention.

Like the transistor **100**, the transistor **150** is provided with the insulating film **114** over the oxide semiconductor film **108**; therefore, oxygen included in the insulating film **114** can fill oxygen vacancy in the oxide semiconductor film **108**.

A structure example different from that of the transistor **150** in FIGS. **3A** to **3C** is described with reference to FIGS. **4A** to **4D**. Note that in the case where a portion has a function similar to that described above, the same hatch pattern is applied to the portion, and the portion is not especially denoted by a reference numeral in some cases.

Structure Example 4 of Semiconductor Device

FIG. **4A** is a cross-sectional view in the channel length direction of a transistor **150A** and FIG. **4B** is a cross-sectional view in the channel width direction of the transistor **150A**. FIG. **4C** is a cross-sectional view in the channel length direction of a transistor **150B** and FIG. **4D** is a cross-sectional view in the channel width direction of the transistor **150B**. Note that top views of the transistor **150A** and the transistor **150B** are omitted here because they are similar to the top view of FIG. **3A**.

The transistor **150A** illustrated in FIGS. **4A** and **4B** includes the conductive film **104** functioning as a gate electrode over the substrate **102**, the insulating film **106** over the substrate **102** and the conductive film **104**, the insulating film **107** over the insulating film **106**, the oxide semiconductor film **108** over the insulating film **107**, the insulating film **114** over the oxide semiconductor film **108**, the insulating film **116** over the insulating film **114**, the insulating film **131** over the insulating film **116**, and the conductive films **112***a* and **112***b* functioning as source and drain electrodes electrically connected to the oxide semiconductor film **108** though the openings **141***a* and **141***b* provided in the insulating films **114**, **116**, and **131**. Over the transistor **150A**, specifically, over the conductive films **112***a* and **112***b* and the insulating film **131**, the insulating film **118** is provided. The insulating films **114**, **116**, and **131** function as protective insulating films for the oxide semiconductor film **108**. The insulating film **118** functions as a protective insulating film for the transistor **150A**.

The transistor **150A** is different from the transistor **150** in FIGS. **3B** and **3C** in that the insulating film **131** is provided. Specifically, the insulating film **131** is provided between the insulating film **116** and the insulating film **118**. The other components are the same as those of the transistor **150**, and the effect similar to that in the case of the transistor **150** is obtained.

The transistor **150B** illustrated in FIGS. **4C** and **4D** includes the conductive film **104** functioning as a gate electrode over the substrate **102**, the insulating film **106** over the substrate **102** and the conductive film **104**, the insulating film **107** over the insulating film **106**, the oxide semiconductor film **108** over the insulating film **107**, the insulating film **114** over the oxide semiconductor film **108**, the insulating film **131** over the insulating film **114**, the insulating film **116** over the insulating film **131**, and the conductive films **112***a* and **112***b* functioning as source and drain electrodes electrically connected to the oxide semiconductor film **108** though the openings **141***a* and **141***b* provided in the insulating films **114**, **116**, and **131**. Over the transistor **150B**, specifically, over the conductive films **112***a* and **112***b* and the insulating film **116**, the insulating film **118** is provided. The insulating films **114**, **116**, and **131** function as protective insulating films for the oxide semiconductor film **108**. The insulating film **118** functions as a protective insulating film for the transistor **150B**.

The transistor **150B** is different from the transistor **150** in FIGS. **3B** and **3C** in that the insulating film **131** is provided. Specifically, the insulating film **131** is provided between the insulating film **114** and the insulating film **116**. The other components are the same as those of the transistor **150**, and the effect similar to that in the case of the transistor **150** is obtained.

A structure example different from that of the transistor **150** in FIGS. **3A** to **3C** is described with reference to FIGS. **5A** to **5C**. Note that in the case where a portion has a function similar to that described above, the same hatch pattern is applied to the portion, and the portion is not especially denoted by a reference numeral in some cases.

Structural Example 5 of Semiconductor Device

FIG. **5A** is a top view of a transistor **160** that is a semiconductor device of one embodiment of the present invention. FIG. **5B** is a cross-sectional view taken along a dashed dotted line X1-X2 in FIG. **5A**, and FIG. **5C** is a cross-sectional view taken along a dashed dotted line Y1-Y2 in FIG. **5A**.

The transistor **160** includes the conductive film **104** functioning as a gate electrode over the substrate **102**, the insulating film **106** over the substrate **102** and the conductive film **104**, the insulating film **107** over the insulating film **106**, the oxide semiconductor film **108** over the insulating film **107**, the insulating film **114** over the oxide semiconductor film **108**, the insulating film **116** over the insulating film **114**, and the conductive films **112***a* and **112***b* functioning as source and drain electrodes electrically connected to the oxide semiconductor film **108**. Over the transistor **160**, specifically, over the conductive films **112***a* and **112***b* and the insulating film **116**, the insulating film **118** is provided. The insulating films **114** and **116** function as protective insulating films for the oxide semiconductor film **108**. The insulating film **118** functions as a protective insulating film for the transistor **160**.

The transistor **160** is different from the transistor **150** in FIGS. **3A** to **3C** in the shapes of the insulating films **114** and **116**. Specifically, the insulating films **114** and **116** of the

transistor **160** have island shapes and are provided over a channel region of the oxide semiconductor film **108**. The other components are the same as those of the transistor **150**, and the effect similar to that in the case of the transistor **150** is obtained.

A structure example different from that of the transistor **160** in FIGS. **5**A to **5**C is described with reference to FIGS. **6**A to **6**D. Note that in the case where a portion has a function similar to that described above, the same hatch pattern is applied to the portion, and the portion is not especially denoted by a reference numeral in some cases.

Structure Example 6 of Semiconductor Device

FIG. **6**A is a cross-sectional view in the channel length direction of a transistor **160**A and FIG. **6**B is a cross-sectional view in the channel width direction of the transistor **160**A. FIG. **6**C is a cross-sectional view in the channel length direction of a transistor **160**B and FIG. **6**D is a cross-sectional view in the channel width direction of the transistor **160**B. Note that top views of the transistor **160**A and the transistor **160**B are omitted here because they are similar to the top view of FIG. **5**A.

The transistor **160**A includes the conductive film **104** functioning as a gate electrode over the substrate **102**, the insulating film **106** over the substrate **102** and the conductive film **104**, the insulating film **107** over the insulating film **106**, the oxide semiconductor film **108** over the insulating film **107**, the insulating film **114** over the oxide semiconductor film **108**, the insulating film **116** over the insulating film **114**, the insulating film **131** over the insulating film **116**, and the conductive films **112**a and **112**b functioning as source and drain electrodes electrically connected to the oxide semiconductor film **108**. Over the transistor **160**A, specifically, over the conductive films **112**a and **112**b and the insulating film **131**, the insulating film **118** is provided. The insulating films **114**, **116**, and **131** function as protective insulating films for the oxide semiconductor film **108**. The insulating film **118** functions as a protective insulating film for the transistor **160**A.

The transistor **160**A is different from the transistor **160** in FIGS. **5**B and **5**C in that the insulating film **131** is provided. Specifically, the insulating film **131** of the transistor **160**A is provided between the insulating film **116** and the insulating film **118**. The other components are the same as those of the transistor **160**, and the effect similar to that in the case of the transistor **160** is obtained.

The transistor **160**B includes the conductive film **104** functioning as a gate electrode over the substrate **102**, the insulating film **106** over the substrate **102** and the conductive film **104**, the insulating film **107** over the insulating film **106**, the oxide semiconductor film **108** over the insulating film **107**, the insulating film **114** over the oxide semiconductor film **108**, the insulating film **131** over the insulating film **114**, the insulating film **116** over the insulating film **131**, and the conductive films **112**a and **112**b functioning as source and drain electrodes electrically connected to the oxide semiconductor film **108**. Over the transistor **160**B, specifically, over the conductive films **112**a and **112**b and the insulating film **116**, the insulating film **118** is provided. The insulating films **114**, **116**, and **131** function as protective insulating films for the oxide semiconductor film **108**. The insulating film **118** functions as a protective insulating film for the transistor **160**B.

The transistor **160**B is different from the transistor **160** in FIGS. **5**B and **5**C in that the insulating film **131** is provided. Specifically, the insulating film **131** of the transistor **160**B is

provided between the insulating film **114** and the insulating film **116**. The other components are the same as those of the transistor **160**, and the effect similar to that in the case of the transistor **160** is obtained.

A structure example different from that of the transistor **100** in FIGS. **1**A to **1**C is described with reference to FIGS. **7**A to **7**C. Note that in the case where a portion has a function similar to that described above, the same hatch pattern is applied to the portion, and the portion is not especially denoted by a reference numeral in some cases.

Structural Example 7 of Semiconductor Device

FIG. **7**A is a top view of a transistor **170** that is a semiconductor device of one embodiment of the present invention. FIG. **7**B is a cross-sectional view taken along a dashed dotted line X1-X2 in FIG. **7**A, and FIG. **7**C is a cross-sectional view taken along a dashed dotted line Y1-Y2 in FIG. **7**A.

The transistor **170** includes the conductive film **104** functioning as a gate electrode over the substrate **102**, the insulating film **106** over the substrate **102** and the conductive film **104**, the insulating film **107** over the insulating film **106**, the oxide semiconductor film **108** over the insulating film **107**, the insulating film **114** over the oxide semiconductor film **108**, the insulating film **116** over the insulating film **114**, and the conductive films **112**a and **112**b functioning as source and drain electrodes electrically connected to the oxide semiconductor film **108**. Over the transistor **170**, specifically, over the conductive films **112**a and **112**b and the insulating film **116**, the insulating film **118** and conductive films **120**a and **120**b are provided. The insulating films **114** and **116** function as protective insulating films for the oxide semiconductor film **108**. The insulating film **118** functions as a protective insulating film for the transistor **170**. The conductive film **120**a is connected to the conductive film **112**b through an opening **142**c provided in the insulating films **114**, **116**, and **118**. The conductive film **120**b is formed over the insulating film **118** to overlap the oxide semiconductor film **108**.

The insulating films **114**, **116**, and **118** in the transistor **170** function as second gate insulating films of the transistor **170**. The conductive film **120**a in the transistor **170** functions as, for example, a pixel electrode used for a display device. The conductive film **120**b in the transistor **170** functions as a second gate electrode (also referred to as a back gate electrode).

As illustrated in FIG. **7**C, the conductive film **120**b is connected to the conductive film **104** functioning as a gate electrode through openings **142**a and **142**b provided in the insulating films **106**, **107**, **114**, **116**, and **118**. Accordingly, the conductive film **120**b and the conductive film **104** are supplied with the same potential.

Note that although the structure in which the openings **142**a and **142**b are provided so that the conductive film **120**b and the conductive film **104** are connected to each other is described in this embodiment, one embodiment of the present invention is not limited thereto. For example, a structure in which only one of the openings **142**a and **142**b is provided so that the conductive film **120**b and the conductive film **104** are connected to each other, or a structure in which the openings **142**a and **142**b are not provided and the conductive film **120**b and the conductive film **104** are not connected to each other may be employed. Note that in the case where the conductive film **120**b and the conductive film **104** are not

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connected to each other, it is possible to apply different potentials to the conductive film **120***b* and the conductive film **104**.

As illustrated in FIG. 7B, the oxide semiconductor film **108** is positioned to face each of the conductive film **104** functioning as a gate electrode and the conductive film **120***b* functioning as a second gate electrode, and is sandwiched between the two conductive films functioning as gate electrodes. The lengths in the channel length direction and the channel width direction of the conductive film **120***b* functioning as a second gate electrode are longer than those in the channel length direction and the channel width direction of the oxide semiconductor film **108**. The whole oxide semiconductor film **108** is covered with the conductive film **120***b* with the insulating films **114**, **116**, and **118** positioned therebetween. Since the conductive film **120***b* functioning as a second gate electrode is connected to the conductive film **104** functioning as a gate electrode through the opening **142***a* and **142***b* provided in the insulating films **106**, **107**, **114**, **116**, and **118**, a side surface of the oxide semiconductor film **108** in the channel width direction faces the conductive film **120***b* functioning as a second gate electrode with the insulating films **114**, **116**, and **118** positioned therebetween.

In other words, in the channel width direction of the transistor **170**, the conductive film **104** functioning as a gate electrode and the conductive film **120***b* functioning as a second gate electrode are connected to each other through the openings provided in the insulating films **106** and **107** functioning as gate insulating films, and the insulating films **114**, **116**, and **118** functioning as second gate insulating films; and the conductive film **104** and the conductive film **120***b* surround the oxide semiconductor film **108** with the insulating films **106** and **107** functioning as gate insulating films, and the insulating films **114**, **116**, and **118** functioning as second gate insulating films positioned therebetween.

Such a structure makes it possible that the oxide semiconductor film **108** included in the transistor **170** is electrically surrounded by electric fields of the conductive film **104** functioning as a gate electrode and the conductive film **120***b* functioning as a second gate electrode. A device structure of a transistor, like that of the transistor **170**, in which electric fields of a gate electrode and a second gate electrode electrically surround an oxide semiconductor film where a channel region is formed can be referred to as a surrounded channel (s-channel) structure.

Since the transistor **170** has the s-channel structure, an electric field for inducing a channel can be effectively applied to the oxide semiconductor film **108** by the conductive film **104** functioning as a gate electrode; therefore, the current drive capability of the transistor **170** can be improved and high on-state current characteristics can be obtained. Since the on-state current can be increased, it is possible to reduce the size of the transistor **170**. In addition, since the transistor **170** is surrounded by the conductive film **104** functioning as a gate electrode and the conductive film **120***b* functioning as a second gate electrode, the mechanical strength of the transistor **170** can be increased.

Structure examples different from that of the transistor **100** in FIGS. 1A to 1C are described with reference to FIGS. 8A to 8D. Note that in the case where a portion has a function similar to that described above, the same hatch pattern is applied to the portion, and the portion is not especially denoted by a reference numeral in some cases.

Structure Example 8 of Semiconductor Device

FIGS. **8A** and **8B** each illustrate a cross-sectional view of a modification example of the transistor **100** in FIGS. 1B and

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1C. FIGS. **8C** and **8D** each illustrate a cross-sectional view of another modification example of the transistor **100** in FIGS. 1B and 1C.

A transistor **100C** in FIGS. **8A** and **8B** has the same structure as the transistor **100** in FIGS. 1B and 1C except that the oxide semiconductor film **108** has a three-layer structure. Specifically, the oxide semiconductor film **108** of the transistor **100C** includes an oxide semiconductor film **108***a*, an oxide semiconductor film **108***b*, and an oxide semiconductor film **108***c*.

A transistor **100D** in FIGS. **8C** and **8D** has the same structure as the transistor **100** in FIGS. 1B and 1C except that the oxide semiconductor film **108** has a two-layer structure. Specifically, the oxide semiconductor film **108** of the transistor **100D** includes the oxide semiconductor film **108***a* and the oxide semiconductor film **108***b*.

Here, a band structure including the oxide semiconductor films **108***a*, **108***b*, and **108***c* and insulating films in contact with the oxide semiconductor film **108** is described with reference to FIGS. **9A** and **9B**.

FIG. **9A** shows an example of a band structure in the thickness direction of a stack including the insulating film **107**, the oxide semiconductor films **108***a*, **108***b*, and **108***c*, and the insulating film **114**. FIG. **9B** shows an example of a band structure in the thickness direction of a stack including the insulating film **107**, the oxide semiconductor films **108***a* and **108***b*, and the insulating film **114**. For easy understanding, the conduction band minimum (Ec) of each of the insulating film **107**, the oxide semiconductor films **108***a*, **108***b*, and **108***c*, and the insulating film **114** is shown in the band structures.

In FIG. **9A**, a silicon oxide film is used as each of the insulating films **107** and **114**, an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements of In:Ga:Zn=1:1:1 is used as the oxide semiconductor film **108***a*, an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements of In:Ga:Zn=1:4:5 is used as the oxide semiconductor film **108***b*, and an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements of In:Ga:Zn=1:3:6 is used as the oxide semiconductor film **108***c*.

In the band structure of FIG. **9B**, a silicon oxide film is used as each of the insulating films **107** and **114**, an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements of In:Ga:Zn=1:1:1 is used as the oxide semiconductor film **108***a*, and a metal oxide film formed using a metal oxide target having an atomic ratio of metal elements of In:Ga:Zn=1:3:6 is used as the oxide semiconductor film **108***b*.

As illustrated in FIGS. **9A** and **9B**, the conduction band minimum smoothly varies between the oxide semiconductor film **108***a* and the oxide semiconductor film **108***b*. In other words, the conduction band minimum is continuously varied or continuously connected. To obtain such a band structure, it is preferable that there exist no impurity, which forms a defect state such as a trap center or a recombination center for the oxide semiconductor, at the interface between the oxide semiconductor film **108***a* and the oxide semiconductor film **108***b*.

To form a continuous junction between the oxide semiconductor film **108***a* and the oxide semiconductor film **108***b*, it is necessary to form the films successively without exposure to the air by using a multi-chamber deposition apparatus (sputtering apparatus) provided with a load lock chamber.

With the band structure of FIG. 9A or FIG. 9B, the oxide semiconductor film 108a serves as a well, and a channel region is formed in the oxide semiconductor film 108a in the transistor with the stacked-layer structure.

By providing the oxide semiconductor film 108b and/or the oxide semiconductor film 108c, the oxide semiconductor film 108a can be distanced away from trap states.

In addition, the trap states might be more distant from the vacuum level than the conduction band minimum (Ec) of the oxide semiconductor film 108a functioning as a channel region, so that electrons are likely to be accumulated in the trap states. When the electrons are accumulated in the trap states, the electrons become negative fixed electric charge, so that the threshold voltage of the transistor is shifted in the positive direction. Therefore, it is preferable that the trap states be closer to the vacuum level than the conduction band minimum (Ec) of the oxide semiconductor film 108a. Such a structure inhibits accumulation of electrons in the trap states. As a result, the on-state current and the field-effect mobility of the transistor can be increased.

In FIGS. 9A and 9B, the conduction band minimum of each of the oxide semiconductor films 108b and 108c is closer to the vacuum level than that of the oxide semiconductor film 108a. Typically, an energy difference between the conduction band minimum of the oxide semiconductor film 108a and the conduction band minimum of each of the oxide semiconductor films 108b and 108c is greater than or equal to 0.15 eV or greater than or equal to 0.5 eV, and less than or equal to 2 eV or less than or equal to 1 eV. That is, the difference between the electron affinity of each of the oxide semiconductor films 108b and 108c and the electron affinity of the oxide semiconductor film 108a is greater than or equal to 0.15 eV or greater than or equal to 0.5 eV, and less than or equal to 2 eV or less than or equal to 1 eV.

In such a structure, the oxide semiconductor film 108a serves as a main path of current and functions as a channel region. In addition, since the oxide semiconductor films 108b and 108c each include one or more metal elements included in the oxide semiconductor film 108a in which a channel region is formed, interface scattering is less likely to occur at the interface between the oxide semiconductor film 108a and the oxide semiconductor film 108b. Thus, the transistor can have high field-effect mobility because the movement of carriers is not hindered at the interface.

To prevent each of the oxide semiconductor films 108b and 108c from functioning as part of a channel region, a material having sufficiently low conductivity is used for the oxide semiconductor films 108b and 108c. Alternatively, a material which has a smaller electron affinity (a difference in energy level between the vacuum level and the conduction band minimum) than the oxide semiconductor film 108a and has a difference in the conduction band minimum from the oxide semiconductor film 108a (band offset) is used for the oxide semiconductor films 108b and 108c. Furthermore, to inhibit generation of a difference between threshold voltages due to the value of the drain voltage, it is preferable to form the oxide semiconductor films 108b and 108c using a material whose conduction band minimum is closer to the vacuum level than that of the oxide semiconductor film 108a is by more than 0.2 eV, preferably 0.5 eV or more.

It is preferable that the oxide semiconductor films 108b and 108c not have a spinel crystal structure. This is because if the oxide semiconductor films 108b and 108c have a spinel crystal structure, a constituent element of the conductive films 112a and 112b might be diffused into the oxide semiconductor film 108a at the interface between the spinel crystal structure and another region. Note that each of the

oxide semiconductor film 108b and 108c is preferably a CAAC-OS, which is described later, in which case a higher blocking property against constituent elements of the conductive films 112a and 112b, e.g., copper elements, is obtained.

The thickness of each of the oxide semiconductor films 108b and 108c is greater than or equal to a thickness that is capable of inhibiting diffusion of the constituent element of the conductive films 112a and 112b into the oxide semiconductor film 108a, and less than a thickness that inhibits supply of oxygen from the insulating film 114 to the oxide semiconductor film 108a. For example, when the thickness of each of the oxide semiconductor films 108b and 108c is greater than or equal to 10 nm, the constituent elements of the conductive films 112a and 112b can be prevented from diffusing into the oxide semiconductor film 108a. When the thickness of each of the oxide semiconductor films 108b and 108c is less than or equal to 100 nm, oxygen can be effectively supplied from the insulating films 114 and 116 to the oxide semiconductor film 108a.

When the oxide semiconductor films 108b and 108c are each an In-M-Zn oxide in which the atomic ratio of the element M (M is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf) is higher than that of In, the energy gap of each of the oxide semiconductor films 108b and 108c can be large and the electron affinity thereof can be small. Therefore, a difference in electron affinity between the oxide semiconductor film 108a and each of the oxide semiconductor films 108b and 108c may be controlled by the proportion of the element M. Furthermore, oxygen vacancy is less likely to be generated in the oxide semiconductor film in which the atomic ratio of Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf is higher than that of In because Ti, Ga, Y, Zr, La, Ce, Nd, Sn, and Hf each are a metal element that is strongly bonded to oxygen.

When an In-M-Zn oxide is used for the oxide semiconductor films 108b and 108c, the proportions of In and M, not taking Zn and O into consideration, is preferably as follows: the atomic percentage of In is less than 50 atomic % and the atomic percentage of M is greater than or equal to 50 atomic %; further preferably, the atomic percentage of In is less than 25 atomic % and the atomic percentage of M is greater than or equal to 75 atomic %. Alternatively, a gallium oxide film may be used as each of the oxide semiconductor films 108b and 108c.

Furthermore, in the case where each of the oxide semiconductor films 108a, 108b, and 108c is an In-M-Zn oxide, the proportion of M in each of the oxide semiconductor films 108b and 108c is higher than that in the oxide semiconductor film 108a. Typically, the proportion of M in each of the oxide semiconductor films 108b and 108c is 1.5 or more times, preferably twice or more, more preferably three or more times that in the oxide semiconductor film 108a.

Furthermore, in the case where the oxide semiconductor films 108a, 108b, and 108c are each an In-M-Zn oxide, when the oxide semiconductor film 108a has an atomic ratio of In:M:Zn=x_1:y_1:z_1 and the oxide semiconductor films 108b and 108c each have an atomic ratio of In:M:Zn=x_2:y_2:z_2, y_2/x_2 is larger than y_1/x_1, preferably y_2/x_2 is 1.5 or more times as large as y_1/x_1, further preferably, y_2/x_2 is two or more times as large as y_1/x_1, still further preferably y_2/x_2 is three or more times or four or more times as large as y_1/x_1. At this time, y_1 is preferably greater than or equal to x_1 in the oxide semiconductor film 108a, because stable electrical characteristics of a transistor can be achieved. However, when y_1 is three or more times as large as x_1, the field-effect

mobility of the transistor including the oxide semiconductor film $108a$ is reduced. Accordingly, y_1 is preferably smaller than three times x_1.

In the case where the oxide semiconductor film $108a$ is an In-M-Zn oxide and a target having the atomic ratio of metal elements of In:M:Zn=x_1:y_1:z_1 is used for depositing the oxide semiconductor film $108a$, x_1/y_1 is preferably greater than or equal to $\frac{1}{3}$ and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6, and z_1/y_1 is preferably greater than or equal to $\frac{1}{3}$ and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6. Note that when z_1/y_1 is greater than or equal to 1 and less than or equal to 6, a CAAC-OS to be described later is easily formed as the oxide semiconductor film $108a$. Typical examples of the atomic ratio of the metal elements of the target are In:M:Zn=1:1:1 and In:M:Zn=3:1:2.

In the case where the oxide semiconductor films $108b$ and $108c$ are each an In-M-Zn oxide and a target having an atomic ratio of metal elements of In:M:Zn=x_2:y_2:z_2 is used for depositing the oxide semiconductor films $108b$ and $108c$, x_2/y_2 is preferably less than x_1/y_1, and z_2/y_2 is preferably greater than or equal to $\frac{1}{3}$ and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6. When the atomic ratio of M with respect to indium is high, the energy gap of the oxide semiconductor films $108b$ and $108c$ can be large and the electron affinity thereof can be small; therefore, y_2/x_2 is preferably higher than or equal to 3 or higher than or equal to 4. Typical examples of the atomic ratio of the metal elements of the target include In:M:Zn=1:3:2, In:M:Zn=1:3:4, In:M:Zn=1:3:5, In:M:Zn=1:3:6, In:M:Zn=1:4:2, In:M:Zn=1:4:4, In:M:Zn=1:4:5, and In:M:Zn=1:5:5.

Furthermore, in the case where the oxide semiconductor films $108b$ and $108c$ are each an In-M oxide, when a divalent metal element (e.g., zinc) is not included as M, the oxide semiconductor films $108b$ and $108c$ which do not include a spinel crystal structure can be formed. As the oxide semiconductor films $108b$ and $108c$, for example, an In—Ga oxide film can be used. The In—Ga oxide can be formed by a sputtering method using an In—Ga metal oxide target (In:Ga=7:93), for example. To deposit the oxide semiconductor films $108b$ and $108c$ by a sputtering method using DC discharge, on the assumption that an atomic ratio of In:M is x:y, it is preferable that $y/(x+y)$ be less than or equal to 0.96, further preferably less than or equal to 0.95, for example, 0.93.

In each of the oxide semiconductor films $108a$, $108b$, and $108c$, the proportions of the atoms in the above atomic ratio vary within a range of ±40% as an error.

The structures of the transistors of this embodiment can be freely combined with each other.

<Method 1 for Manufacturing Semiconductor Device>

Next, a method for manufacturing the transistor **100** that is a semiconductor device of one embodiment of the present invention is described below in detail with reference to FIGS. **10**A to **10**D and FIGS. **11**A to **11**D.

Note that the films included in the transistor **100** (i.e., the insulating film, the oxide semiconductor film, the conductive film, and the like) can be formed by any of a sputtering method, a chemical vapor deposition (CVD) method, a vacuum evaporation method, and a pulsed laser deposition (PLD) method. Alternatively, a coating method or a printing method can be used. Although the sputtering method and a PECVD method are typical examples of the film formation

method, a thermal CVD method may be used. As the thermal CVD method, an MOCVD method or an ALD method may be used, for example.

Deposition by the thermal CVD method may be performed in such a manner that the pressure in a chamber is set to an atmospheric pressure or a reduced pressure, and a source gas and an oxidizer are supplied to the chamber at a time and react with each other in the vicinity of the substrate or over the substrate. Thus, no plasma is generated in the deposition; therefore, the thermal CVD method has an advantage that no defect due to plasma damage is caused.

Deposition by the ALD method may be performed in such a manner that the pressure in a chamber is set to an atmospheric pressure or a reduced pressure, source gases for reaction are sequentially introduced into the chamber, and then the sequence of the gas introduction is repeated. For example, two or more kinds of source gases are sequentially supplied to the chamber by switching switching valves (also referred to as high-speed valves). In such a case, a first source gas is introduced, an inert gas (e.g., argon or nitrogen) or the like is introduced at the same time as or after introduction of the first gas so that the source gases are not mixed, and then a second source gas is introduced. Note that in the case where the first source gas and the inert gas are introduced at a time, the inert gas serves as a carrier gas, and the inert gas may also be introduced at the same time as the introduction of the second source gas. Alternatively, the first source gas may be exhausted by vacuum evacuation instead of the introduction of the inert gas, and then the second source gas may be introduced. The first source gas is adsorbed on the surface of the substrate to form a first single-atomic layer; then the second source gas is introduced to react with the first single-atomic layer; as a result, a second single-atomic layer is stacked over the first single-atomic layer, so that a thin film is formed.

The sequence of the gas introduction is repeated plural times until a desired thickness is obtained, whereby a thin film with excellent step coverage can be formed. The thickness of the thin film can be adjusted by the number of repetition times of the sequence of the gas introduction; therefore, an ALD method makes it possible to accurately adjust a thickness and thus is suitable for manufacturing a minute transistor.

First, a conductive film is formed over the substrate **102** and processed through a lithography process and an etching process, whereby the conductive film **104** functioning as a gate electrode is formed. Then, the insulating films **106** and **107** functioning as gate insulating films are formed over the conductive film **104** (see FIG. **10**A).

The conductive film **104** functioning as a gate electrode can be formed by a sputtering method, a CVD method, a vacuum evaporation method, or a PLD method. Alternatively, a coating method or a printing method can be used. Although typical deposition methods are a sputtering method and PECVD method, a thermal CVD method, such as an MOCVD method, or an ALD method described above may be used.

In this embodiment, a glass substrate is used as the substrate **102**, and as the conductive film **104** functioning as a gate electrode, a 100-nm-thick tungsten film is formed by a sputtering method.

The insulating films **106** and **107** functioning as gate insulating films can be formed by a sputtering method, a PECVD method, a thermal CVD method, a vacuum evaporation method, a PLD method, or the like. In this embodiment, a 400-nm-thick silicon nitride film as the insulating

film **106** and a 50-nm-thick silicon oxynitride film as the insulating film **107** are formed by a PECVD method.

Note that the insulating film **106** can have a stacked-layer structure of silicon nitride films. Specifically, the insulating film **106** can have a three-layer stacked-layer structure of a first silicon nitride film, a second silicon nitride film, and a third silicon nitride film. An example of the three-layer stacked-layer structure is as follows.

For example, the first silicon nitride film can be formed to have a thickness of 50 nm under the condition where silane at a flow rate of 200 sccm, nitrogen at a flow rate of 2000 sccm, and an ammonia gas at a flow rate of 100 sccm are supplied as a source gas to a reaction chamber of a PECVD apparatus; the pressure in the reaction chamber is controlled to 100 Pa, and a power of 2000 W is supplied using a 27.12 MHz high-frequency power source.

The second silicon nitride film can be formed to have a thickness of 300 nm under the condition where silane at a flow rate of 200 sccm, nitrogen at a flow rate of 2000 sccm, and an ammonia gas at a flow rate of 2000 sccm are supplied as a source gas to the reaction chamber of the PECVD apparatus; the pressure in the reaction chamber is controlled to 100 Pa, and a power of 2000 W is supplied using a 27.12 MHz high-frequency power source.

The third silicon nitride film can be formed to have a thickness of 50 nm under the condition where silane at a flow rate of 200 sccm and nitrogen at a flow rate of 5000 sccm are supplied as a source gas to the reaction chamber of the PECVD apparatus; the pressure in the reaction chamber is controlled to 100 Pa, and a power of 2000 W is supplied using a 27.12 MHz high-frequency power source.

Note that the first silicon nitride film, the second silicon nitride film, and the third silicon nitride film can be each formed at a substrate temperature of 350° C.

When the insulating film **106** has the three-layer stacked-layer structure of silicon nitride films, for example, in the case where a conductive film including Cu is used as the conductive film **104**, the following effect can be obtained.

The first silicon nitride film can inhibit diffusion of a copper (Cu) element from the conductive film **104**. The second silicon nitride film has a function of releasing hydrogen and can improve withstand voltage of the insulating film functioning as a gate insulating film. The third silicon nitride film releases a small amount of hydrogen and can inhibit diffusion of hydrogen released from the second silicon nitride film.

The insulating film **107** is preferably an insulating film including oxygen to improve characteristics of an interface with the oxide semiconductor film **108** formed later.

Next, the oxide semiconductor film **108** is formed over the insulating film **107** (see FIG. 10B).

In this embodiment, an oxide semiconductor film is formed by a sputtering method using an In—Ga—Zn metal oxide target (having an atomic ratio of In:Ga:Zn=1:1:1.2), a mask is formed over the oxide semiconductor film through a lithography process, and the oxide semiconductor film is processed into a desired region, whereby the oxide semiconductor film **108** having an island shape is formed.

After the oxide semiconductor film **108** is formed, heat treatment may be performed at a temperature higher than or equal to 150° C. and lower than the strain point of the substrate, preferably higher than or equal to 200° C. and lower than or equal to 450° C., further preferably higher than or equal to 300° C. and lower than or equal to 450° C. The heat treatment performed here serves as one kind of treatment for increasing the purity of the oxide semiconductor film and can reduce hydrogen, water, and the like included

in the oxide semiconductor film **108**. Note that the heat treatment for the purpose of reducing hydrogen, water, and the like may be performed before the oxide semiconductor film **108** is processed into an island shape.

An electric furnace, an RTA apparatus, or the like can be used for the heat treatment performed on the oxide semiconductor film **108**. With the use of an RTA apparatus, the heat treatment can be performed at a temperature higher than or equal to the strain point of the substrate if the heating time is short. Therefore, the heat treatment time can be shortened.

Note that the heat treatment performed on the oxide semiconductor film **108** may be performed under an atmosphere of nitrogen, oxygen, ultra-dry air (air in which a water content is 20 ppm or less, preferably 1 ppm or less, further preferably 10 ppb or less), or a rare gas (argon, helium, or the like). The atmosphere of nitrogen, oxygen, ultra-dry air, or a rare gas preferably does not contain hydrogen, water, and the like. Furthermore, after heat treatment performed in a nitrogen atmosphere or a rare gas atmosphere, heat treatment may be additionally performed in an oxygen atmosphere or an ultra-dry air atmosphere. As a result, hydrogen, water, and the like can be released from the oxide semiconductor film and oxygen can be supplied to the oxide semiconductor film at the same time. Consequently, the amount of oxygen vacancies in the oxide semiconductor film can be reduced.

In the case where the oxide semiconductor film **108** is formed by a sputtering method, as a sputtering gas, a rare gas (typically argon), oxygen, or a mixed gas of a rare gas and oxygen is used as appropriate. In the case of using the mixed gas of a rare gas and oxygen, the proportion of oxygen to a rare gas is preferably increased. In addition, increasing the purity of a sputtering gas is necessary. For example, as an oxygen gas or an argon gas used for a sputtering gas, a gas which is highly purified to have a dew point of −40° C. or lower, preferably −80° C. or lower, further preferably −100° C. or lower, still further preferably −120° C. or lower is used, whereby entry of moisture and the like into the oxide semiconductor film **108** can be minimized.

In the case where the oxide semiconductor film **108** is formed by a sputtering method, a chamber in a sputtering apparatus is preferably evacuated to be a high vacuum state (to the degree of about 5×10^{-7} Pa to 1×10^{-4} Pa) with an adsorption vacuum evacuation pump such as a cryopump in order to remove water or the like, which serves as an impurity for the oxide semiconductor film **108**, as much as possible. Alternatively, a turbo molecular pump and a cold trap are preferably combined so as to prevent a backflow of a gas, especially a gas including carbon or hydrogen from an exhaust system to the inside of the chamber.

Next, the conductive films **112a** and **112b** functioning as a source electrode and a drain electrode are formed over the insulating film **107** and the oxide semiconductor film **108** (see FIG. 10C).

In this embodiment, the conductive films **112a** and **112b** are formed in the following manner: a stack formed of a 50-nm-thick tungsten film and a 400-nm-thick aluminum film is formed by a sputtering method, a mask is formed over the stack through a lithography process, and the stack is processed into desired regions. Although the conductive films **112a** and **112b** each have a two-layer stacked structure in this embodiment, one embodiment of the present invention is not limited thereto. For example, the conductive films **112a** and **112b** each may have a three-layer stacked-layer structure formed of a 50-nm-thick tungsten film, a 400-nm-thick aluminum film, and a 100-nm-thick titanium film.

After the conductive films 112a and 112b are formed, a surface of the oxide semiconductor film 108 (on a back channel side) may be cleaned. The cleaning may be performed, for example, using a chemical solution such as phosphoric acid. The cleaning using a chemical solution such as a phosphoric acid can remove impurities (e.g., an element included in the conductive films 112a and 112b and the like) attached to the surface of the oxide semiconductor film 108.

Note that a recessed portion might be formed in part of the oxide semiconductor film 108 at the step of forming the conductive films 112a and 112b and/or the cleaning step.

Through the steps, the transistor 100 is formed.

Next, over the transistor 100, specifically, over the oxide semiconductor film 108 and the conductive films 112a and 112b of the transistor 100, the insulating films 114 and 116 functioning as protective insulating films of the transistor 100 are formed (see FIG. 10D).

Note that after the insulating film 114 is formed, the insulating film 116 is preferably formed in succession without exposure to the air. After the insulating film 114 is formed, the insulating film 116 is formed in succession by adjusting at least one of the flow rate of a source gas, pressure, a high-frequency power, and a substrate temperature without exposure to the air, whereby the concentration of impurities attributed to the atmospheric component at the interface between the insulating film 114 and the insulating film 116 can be reduced and oxygen in the insulating films 114 and 116 can be moved to the oxide semiconductor film 108; accordingly, the amount of oxygen vacancy in the oxide semiconductor film 108 can be reduced.

For example, as the insulating film 114, a silicon oxynitride film can be formed by a PECVD method. In this case, a deposition gas including silicon and an oxidizing gas are preferably used as a source gas. Typical examples of the deposition gas including silicon include silane, disilane, trisilane, and silane fluoride. Examples of the oxidizing gas include dinitrogen monoxide and nitrogen dioxide. An insulating film including nitrogen and having a small number of defects can be formed as the insulating film 114 by a PECVD method under the conditions where the ratio of the oxidizing gas to the deposition gas is higher than 20 times and lower than 100 times, preferably higher than or equal to 40 times and lower than or equal to 80 times and the pressure in a treatment chamber is lower than 100 Pa, preferably lower than or equal to 50 Pa.

In this embodiment, a silicon oxynitride film is formed as the insulating film 114 by a PECVD method under the conditions where the substrate 102 is held at a temperature of 220° C., silane at a flow rate of 50 sccm and dinitrogen monoxide at a flow rate of 2000 sccm are used as a source gas, the pressure in the treatment chamber is 20 Pa, and a high-frequency power of 100 W at 13.56 MHz (1.6×10^{-2} W/cm^2 as the power density) is supplied to parallel-plate electrodes.

As the insulating film 116, a silicon oxide film or a silicon oxynitride film is formed under the conditions where the substrate placed in a treatment chamber of the PECVD apparatus that is vacuum-evacuated is held at a temperature higher than or equal to 180° C. and lower than or equal to 280° C., preferably higher than or equal to 200° C. and lower than or equal to 240° C., the pressure is greater than or equal to 100 Pa and less than or equal to 250 Pa, preferably greater than or equal to 100 Pa and less than or equal to 200 Pa with introduction of a source gas into the treatment chamber, and a high-frequency power of greater than or equal to 0.17 W/cm^2 and less than or equal to 0.5 W/cm^2, preferably

greater than or equal to 0.25 W/cm^2 and less than or equal to 0.35 W/cm^2 is supplied to an electrode provided in the treatment chamber.

As the deposition conditions of the insulating film 116, the high-frequency power having the above power density is supplied to a reaction chamber having the above pressure, whereby the degradation efficiency of the source gas in plasma is increased, oxygen radicals are increased, and oxidation of the source gas is promoted; thus, the oxygen content in the insulating film 116 becomes higher than that in the stoichiometric composition. On the other hand, in the film formed at a substrate temperature within the above temperature range, the bond between silicon and oxygen is weak, and accordingly, part of oxygen in the film is released by heat treatment in a later step. Thus, it is possible to form an oxide insulating film which includes oxygen in excess of that in the stoichiometric composition and from which part of oxygen is released by heating.

Note that the insulating film 114 functions as a protective film for the oxide semiconductor film 108 in the step of forming the insulating film 116. Therefore, the insulating film 116 can be formed using the high-frequency power having a high power density while damage to the oxide semiconductor film 108 is reduced.

Note that in the deposition conditions of the insulating film 116, when the flow rate of the deposition gas including silicon with respect to the oxidizing gas is increased, the number of defects in the insulating film 116 can be reduced. Typically, it is possible to form an oxide insulating layer in which the number of defects is small, i.e., the spin density of a signal which appears at g=2.001 originating from a dangling bond of silicon is lower than 6×10^{17} spins/cm^3, preferably lower than or equal to 3×10^{17} spins/cm^3, further preferably lower than or equal to 1.5×10^{17} spins/cm^3 by ESR measurement. As a result, the reliability of the transistor can be improved.

Heat treatment may be performed after the insulating films 114 and 116 are formed. The heat treatment can reduce nitrogen oxide included in the insulating films 114 and 116. By the heat treatment, part of oxygen included in the insulating films 114 and 116 can be moved to the oxide semiconductor film 108, so that the amount of oxygen vacancy included in the oxide semiconductor film 108 can be reduced.

The temperature of the heat treatment performed on the insulating films 114 and 116 is typically higher than or equal to 150° C. and lower than or equal to 400° C., preferably higher than or equal to 300° C. and lower than or equal to 400° C., further preferably higher than or equal to 320° C. and lower than or equal to 370° C. The heat treatment may be performed under an atmosphere of nitrogen, oxygen, ultra-dry air (air in which a water content is 20 ppm or less, preferably 1 ppm or less, further preferably 10 ppb or less), or a rare gas (argon, helium, and the like). Note that an electric furnace, an RTA apparatus, and the like can be used for the heat treatment, in which it is preferable that hydrogen, water, and the like not be included in the nitrogen, oxygen, ultra-dry air, or rare gas.

In this embodiment, the heat treatment is performed at 350° C. for 1 hour in an atmosphere of nitrogen and oxygen.

Next, a film 130 that inhibits release of oxygen is formed over the insulating film 116 (see FIG. 11A).

The film 130 that inhibits release of oxygen includes at least one of indium, zinc, titanium, aluminum, tungsten, tantalum, and molybdenum. For example, a conductive material such as an alloy including any of the metal elements, an alloy including any of the metal elements in

combination, a metal oxide including any of the metal elements, a metal nitride including any of the metal elements, or a metal nitride oxide including any of the metal elements is used.

The film 130 that inhibits release of oxygen can be formed using, for example, a tantalum nitride film, a titanium film, an indium tin oxide (ITO) film, an aluminum film, or an oxide semiconductor film (e.g., an IGZO film having an atomic ratio of In:Ga:Zn=1:4:5).

Next, oxygen 141 is added to the insulating films 114 and 116 and the oxide semiconductor film 108 through the film 130 (see FIG. 11B).

The thickness of the film 130 that inhibits release of oxygen can be greater than or equal to 1 nm and less than or equal to 20 nm, or greater than or equal to 2 nm and less than or equal to 10 nm. In this embodiment, a 5-nm-thick tantalum nitride film is used as the film 130.

As a method for adding the oxygen 141 to the insulating films 114 and 116 and the oxide semiconductor film 108 through the film 130, an ion doping method, an ion implantation method, plasma treatment, or the like is given. When the film 130 is provided over the insulating film 116 and then oxygen is added, the film 130 serves as a protective film for preventing oxygen from being released from the insulating film 116. Thus, a larger amount of oxygen can be added to the insulating films 114 and 116 and the oxide semiconductor film 108.

In the case where oxygen is introduced by plasma treatment, by making oxygen excited by a microwave to generate high density oxygen plasma, the amount of oxygen introduced into the insulating film 116 can be increased.

Note that by the addition of the oxygen 141, the film 130 becomes the insulating film 131 formed of oxide or nitride of metal (indium, zinc, titanium, aluminum, tungsten, tantalum, or molybdenum) (see FIG. 11C).

Note that the insulating film 131 might be a conductor or a semiconductor in the case where the treatment for adding the oxygen 141 is insufficiently performed, or even in the case where the treatment is sufficiently performed depending on the metal material used for the film 130. Note that since the insulating film 131 is positioned on the back channel side of the transistor 100, when the insulating film 131 is a conductor or a semiconductor, an electron serving as a carrier might be trapped in the insulating film 131; therefore, the insulating film 131 is preferably an insulator.

After that, the insulating film 131 is removed, and the insulating film 118 is formed over the insulating film 116 (see FIG. 11D).

Note that heat treatment may be performed before or after the formation of the insulating film 118, so that excess oxygen included in the insulating films 114 and 116 can diffuse into the oxide semiconductor film 108 to fill oxygen vacancy in the oxide semiconductor film 108. Alternatively, the insulating film 118 may be deposited by heating, so that excess oxygen included in the insulating films 114 and 116 can diffuse into the oxide semiconductor film 108 to fill oxygen vacancy in the oxide semiconductor film 108.

In the case where the insulating film 118 is formed by a PECVD method, the substrate temperature is preferably set to higher than or equal to 300° C. and lower than or equal to 400° C., more preferably higher than or equal to 320° C. and lower than or equal to 370° C., so that a dense film can be formed.

For example, in the case where a silicon nitride film is formed by a PECVD method as the insulating film 118, a deposition gas containing silicon, nitrogen, and ammonia are preferably used as a source gas. A small amount of ammonia

compared to the amount of nitrogen is used, whereby ammonia is dissociated in the plasma and activated species are generated. The activated species cleave a bond between silicon and hydrogen which are included in a deposition gas containing silicon and a triple bond between nitrogen molecules. As a result, a dense silicon nitride film having few defects, in which bonds between silicon and nitrogen are promoted and bonds between silicon and hydrogen is few, can be formed. On the other hand, when the amount of ammonia with respect to nitrogen is large, decomposition of a deposition gas containing silicon and decomposition of nitrogen are not promoted, so that a sparse silicon nitride film in which bonds between silicon and hydrogen remain and defects are increased is formed. Therefore, in the source gas, a flow rate ratio of the nitrogen to the ammonia is set to be greater than or equal to 5 and less than or equal to 50, preferably greater than or equal to 10 and less than or equal to 50.

In this embodiment, with the use of a PECVD apparatus, a 50-nm-thick silicon nitride film is formed as the insulating film 118 using silane, nitrogen, and ammonia as a source gas. The flow rate of silane is 50 sccm, the flow rate of nitrogen is 5000 sccm, and the flow rate of ammonia is 100 sccm. The pressure in the treatment chamber is 100 Pa, the substrate temperature is 350° C., and high-frequency power of 1000 W is supplied to parallel-plate electrodes with a 27.12 MHz high-frequency power source. Note that the PECVD apparatus is a parallel-plate PECVD apparatus in which the electrode area is 6000 cm^2, and the power per unit area (power density) into which the supplied power is converted is 1.7×10^{-1} W/cm^2.

Heat treatment may be performed after the formation of the insulating film 118. The heat treatment is performed typically at a temperature of higher than or equal to 150° C. and lower than or equal to 400° C., preferably higher than or equal to 300° C. and lower than or equal to 400° C., further preferably higher than or equal to 320° C. and lower than or equal to 370° C. When the heat treatment is performed, the amount of hydrogen and water in the insulating films 114 and 116 is reduced and accordingly the generation of defects in the oxide semiconductor film 108 described above is inhibited.

Through the above process, the semiconductor device illustrated in FIGS. 1A to 1C can be manufactured.

Note that the transistor 100A in FIGS. 2A and 2B can be manufactured by forming the insulating film 118 without removal of the insulating film 131.

<Method 2 for Manufacturing Semiconductor Device>

Next, a method for manufacturing the transistor 150 in FIGS. 3A to 3C that is a semiconductor device of one embodiment of the present invention is described below in detail with reference to FIGS. 12A to 12D and FIGS. 13A and 13B.

First, the steps up to the step in FIG. 10B are performed, and then the insulating films 114 and 116 and the film 130 that inhibits release of oxygen are formed over the oxide semiconductor film 108 (see FIG. 12A).

Next, the oxygen 141 is added to the insulating films 114 and 116 and the oxide semiconductor film 108 through the film 130 (see FIG. 12B).

Note that by the addition of the oxygen 141, the film 130 becomes the insulating film 131 formed of oxide or nitride of metal (indium, zinc, titanium, aluminum, tungsten, tantalum, or molybdenum) (see FIG. 12C).

After that, the insulating film 131 is removed, a mask is formed over the insulating film 116 through a lithography process, and the openings 141a and 141b are formed in

desired regions in the insulating films **114** and **116**. Note that the openings **141***a* and **141***b* reach the oxide semiconductor film **108** (see FIG. **12**D).

Next, a conductive film is deposited over the oxide semiconductor film **108** and the insulating film **116** to cover the openings **141***a* and **141***b*, a mask is formed over the conductive film through a lithography process, and the conductive film is processed into desired regions, whereby the conductive films **112***a* and **112***b* are formed (see FIG. **13**A).

Next, the insulating film **118** is formed over the insulating film **116** and the conductive films **112***a* and **112***b* (see FIG. **13**B).

Through the above process, the semiconductor device illustrated in FIGS. **3**A to **3**C can be manufactured.

Note that the transistor **150**A in FIGS. **4**A and **4**B can be manufactured by forming the insulating film **118** without removal of the insulating film **131**.

<Method 3 for Manufacturing Semiconductor Device>

Next, a method for manufacturing the transistor **170** that is a semiconductor device of one embodiment of the present invention is described below in detail with reference to FIGS. **14**A to **14**D and FIGS. **15**A to **15**D.

FIGS. **14**A and **14**C and FIGS. **15**A and **15**C are each a cross-sectional view in the channel length direction of the transistor **170** and FIGS. **14**B and **14**D and FIGS. **15**B and **15**D are each a cross-sectional view in the channel width direction of the transistor **170**.

First, the steps up to the step in FIG. **11**D are performed (see FIGS. **14**A and **14**B).

Next, a mask is formed over the insulating film **118** through a lithography process, and the opening **142***c* is formed in a desired region in the insulating films **114**, **116**, and **118**. In addition, a mask is formed over the insulating film **118** through a lithography process, and the openings **142***a* and **142***b* are formed in desired regions in the insulating films **106**, **107**, **114**, **116**, and **118**. Note that the opening **142***c* reaches the conductive film **112***b*. The openings **142***a* and **142***b* reach the conductive film **104** (see FIGS. **14**C and **14**D).

Note that the openings **142***a* and **142***b* and the opening **140***c* may be formed at a time or may be formed by different steps. In the case where the openings **142***a* and **142***b* and the opening **140***c* are formed at a time, for example, a gray-tone mask or a half-tone mask may be used.

Next, a conductive film **120** is formed over the insulating film **118** to cover the openings **142***a*, **142***b*, and **142***c* (see FIGS. **15**A and **15**B).

For the conductive film **120**, for example, a material including one of indium (In), zinc (Zn), and tin (Sn) can be used. In particular, for the conductive film **120**, a light-transmitting conductive material such as indium oxide including tungsten oxide, indium zinc oxide including tungsten oxide, indium oxide including titanium oxide, indium tin oxide including titanium oxide, indium tin oxide (ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added (ITSO) can be used. The conductive film **120** can be formed by a sputtering method, for example. In this embodiment, a 110-nm-thick ITSO film is formed by a sputtering method.

Next, a mask is formed over the conductive film **120** through a lithography process, and the conductive film **120** is processed into desired regions to form the conductive films **120***a* and **120***b* (see FIGS. **15**C and **15**D).

Through the above process, the transistor **170** illustrated in FIGS. **7**A and **7**B can be manufactured.

<Method 4 for Manufacturing Semiconductor Device>

Next, a method for manufacturing the transistor **100** that is a semiconductor device of one embodiment of the present invention, which is different from that described in <Method 1 for manufacturing semiconductor device>, is described below with reference to FIGS. **16**A to **16**D.

First, the steps up to the step in FIG. **10**C are performed to form the transistor **100**. After that, over the transistor **100**, specifically, over the oxide semiconductor film **108** and the conductive films **112***a* and **112***b*, the insulating film **114** is formed. Then, the film **130** that inhibits release of oxygen is formed over the insulating film **114** (see FIG. **16**A).

Next, the oxygen **141** is added to the insulating film **114** and the oxide semiconductor film **108** through the film **130** (see FIG. **16**B).

Note that by the addition of the oxygen **141**, the film **130** becomes the insulating film **131** formed of oxide or nitride of metal (indium, zinc, titanium, aluminum, tungsten, tantalum, or molybdenum) (see FIG. **16**C).

Next, the insulating film **131** is removed, and the insulating film **116** is formed over the insulating film **114**. After that, the insulating film **118** is formed over the insulating film **116** (see FIG. **16**D).

Through the above process, the semiconductor device illustrated in FIGS. **1**A to **1**C can be manufactured.

Note that in a process for manufacturing the transistor **100**B in FIGS. **2**C and **2**D, the insulating film **116** and the insulating film **118** can be formed without removal of the insulating film **131**.

<Method 5 for Manufacturing Semiconductor Device>

The above-described semiconductor device of one embodiment of the present invention may be formed in combination with a manufacturing method illustrated in FIGS. **17**A to **17**D, as appropriate.

First, an insulating film **101** is formed over the substrate **102**, and the film **130** that inhibits release of oxygen is formed over the insulating film **101** (see FIG. **17**A).

A material which can be used for the insulating film **107** can be used for the insulating film **101**.

Next, the oxygen **141** is added to the insulating film **101** through the film **130** (see FIG. **17**B).

Note that by the addition of the oxygen **141**, the film **130** becomes the insulating film **131** formed of oxide or nitride of metal (indium, zinc, titanium, aluminum, tungsten, tantalum, or molybdenum) (see FIG. **17**C).

Next, the insulating film **131** is removed, and the conductive film **104** is formed over the insulating film **101**. Then, the insulating films **106** and **107** are formed over the insulating film **101** and the conductive film **104** (see FIG. **17**D).

In this manner, the transistor that is the semiconductor device of one embodiment of the present invention may include the base film. In addition, a region including excess oxygen may be formed in the base film by oxygen addition treatment. With such a structure, oxygen in the base film can diffuse into the oxide semiconductor film **108** through the insulating films **106** and **107** to fill oxygen vacancy in the oxide semiconductor film **108**.

<Method 6 for Manufacturing Semiconductor Device>

The above-described semiconductor device of one embodiment of the present invention may be formed in combination with a manufacturing method illustrated in FIGS. **18**A to **18**C, as appropriate.

First, the steps up to the step in FIG. **10**A are performed, and the film **130** that inhibits release of oxygen is formed over the insulating film **107** (see FIG. **18**A).

Next, the oxygen 141 is added to the insulating film 107 through the film 130 (see FIG. 18B).

Note that by the addition of the oxygen 141, the film 130 becomes the insulating film 131 formed of oxide or nitride of metal (indium, zinc, titanium, aluminum, tungsten, tantalum, or molybdenum) (see FIG. 18C).

After that, the insulating film 131 is removed, the oxide semiconductor film 108 is formed over the insulating film 107, and steps after the step of FIG. 10B are performed.

As described above, oxygen addition treatment may be performed on the insulating film 107 serving as part of the gate insulating film to increase the oxygen content of the insulating film 107 in the process for manufacturing the transistor that is the semiconductor device of one embodiment of the present invention.

The structure and method described in this embodiment can be implemented by being combined as appropriate with any of the other structures and methods described in the other embodiments.

Embodiment 2

In this embodiment, the structure of an oxide semiconductor included in a semiconductor device of one embodiment of the present invention is described below in detail.

First a structure which can be included in an oxide semiconductor is described below.

An oxide semiconductor is classified into a single crystal oxide semiconductor and a non-single-crystal oxide semiconductor. Examples of a non-single-crystal oxide semiconductor include a c-axis aligned crystalline oxide semiconductor (CAAC-OS), a polycrystalline oxide semiconductor, a nanocrystalline oxide semiconductor (nc-OS), an amorphous-like oxide semiconductor (a-like OS), and an amorphous oxide semiconductor.

From another perspective, an oxide semiconductor is classified into an amorphous oxide semiconductor and a crystalline oxide semiconductor. In addition, examples of a crystalline oxide semiconductor include a single crystal oxide semiconductor, a CAAC-OS, a polycrystalline oxide semiconductor, and an nc-OS.

It is known that an amorphous structure is generally defined as being metastable and unfixed, and being isotropic and having no non-uniform structure. In other words, an amorphous structure has a flexible bond angle and a short-range order but does not have a long-range order.

This means that an inherently stable oxide semiconductor cannot be regarded as a completely amorphous oxide semiconductor. Moreover, an oxide semiconductor that is not isotropic (e.g., an oxide semiconductor film that has a periodic structure in a microscopic region) cannot be regarded as a completely amorphous oxide semiconductor. Note that an a-like OS has a periodic structure in a microscopic region, but at the same time has a void and has an unstable structure. For this reason, an a-like OS has physical properties similar to those of an amorphous oxide semiconductor.

<CAAC-OS>

First, a CAAC-OS is described.

A CAAC-OS is one of oxide semiconductors having a plurality of c-axis aligned crystal parts (also referred to as pellets).

In a combined analysis image (also referred to as a high-resolution TEM image) of a bright-field image and a diffraction pattern of a CAAC-OS, which is obtained using a transmission electron microscope (TEM), a plurality of pellets can be observed. However, in the high-resolution

TEM image, a boundary between pellets, that is, a grain boundary is not clearly observed. Thus, in the CAAC-OS, a reduction in electron mobility due to the grain boundary is less likely to occur.

The CAAC-OS observed with a TEM is described below. FIG. 19A shows a high-resolution TEM image of a cross section of the CAAC-OS which is observed from a direction substantially parallel to the sample surface. The high-resolution TEM image is obtained with a spherical aberration corrector function. The high-resolution TEM image obtained with a spherical aberration corrector function is particularly referred to as a Cs-corrected high-resolution TEM image. The Cs-corrected high-resolution TEM image can be obtained with, for example, an atomic resolution analytical electron microscope JEM-ARM200F manufactured by JEOL Ltd.

FIG. 19B is an enlarged Cs-corrected high-resolution TEM image of a region (1) in FIG. 19A. FIG. 19B shows that metal atoms are arranged in a layered manner in a pellet. Each metal atom layer has a configuration reflecting unevenness of a surface over which a CAAC-OS film is formed (hereinafter, the surface is referred to as a formation surface) or a top surface of the CAAC-OS, and is arranged parallel to the formation surface or the top surface of the CAAC-OS.

As shown in FIG. 19B, the CAAC-OS has a characteristic atomic arrangement. The characteristic atomic arrangement is denoted by an auxiliary line in FIG. 19C. FIGS. 19B and 19C prove that the size of a pellet is approximately 1 nm to 3 nm, and the size of a space caused by tilt of the pellets is approximately 0.8 nm. Therefore, the pellet can also be referred to as a nanocrystal (nc). Furthermore, a CAAC-OS can be referred to as an oxide semiconductor including c-axis aligned nanocrystals (CANC).

Here, according to the Cs-corrected high-resolution TEM images, the schematic arrangement of pellets 5100 of a CAAC-OS over a substrate 5120 is illustrated by such a structure in which bricks or blocks are stacked (see FIG. 19D). The part in which the pellets are tilted as observed in FIG. 19C corresponds to a region 5161 shown in FIG. 19D.

FIG. 20A shows a Cs-corrected high-resolution TEM image of a plane of the CAAC-OS observed from a direction substantially perpendicular to the sample surface. FIGS. 20B, 20C, and 20D are enlarged Cs-corrected high-resolution TEM images of regions (1), (2), and (3) in FIG. 20A, respectively. FIGS. 20B, 20C, and 20D indicate that metal atoms are arranged in a triangular, quadrangular, or hexagonal configuration in a pellet. However, there is no regularity of arrangement of metal atoms between different pellets.

Next, a CAAC-OS analyzed by X-ray diffraction (XRD) is described. For example, when the structure of a CAAC-OS including an $InGaZnO_4$ crystal is analyzed by an out-of-plane method, a peak appears at a diffraction angle (2θ) of around 31° as shown in FIG. 21A. This peak is derived from the (009) plane of the $InGaZnO_4$ crystal, which indicates that crystals in the CAAC-OS have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS.

Note that in structural analysis of the CAAC-OS by an out-of-plane method, another peak may appear when 2θ is around 36°, in addition to the peak at 2θ of around 31°. The peak of 2θ at around 36° indicates that a crystal having no c-axis alignment is included in part of the CAAC-OS. It is preferable that in the CAAC-OS analyzed by an out-of-plane method, a peak appear when 2θ is around 31° and that a peak not appear when 2θ is around 36°.

On the other hand, in structural analysis of the CAAC-OS by an in-plane method in which an X-ray is incident on a sample in a direction substantially perpendicular to the c-axis, a peak appears when 2θ is around 56°. This peak is derived from the (110) plane of the InGaZnO$_4$ crystal. In the case of the CAAC-OS, when analysis (φ scan) is performed with 2q fixed at around 56° and with the sample rotated using a normal vector of the sample surface as an axis (φ axis), as shown in FIG. 21B, a peak is not clearly observed. In contrast, in the case of a single crystal oxide semiconductor of InGaZnO$_4$, when f scan is performed with 2θ fixed at around 56°, as shown in FIG. 21C, six peaks which are derived from crystal planes equivalent to the (110) plane are observed. Accordingly, the structural analysis using XRD shows that the directions of a-axes and b-axes are irregularly oriented in the CAAC-OS.

Next, a CAAC-OS analyzed by electron diffraction is described. For example, when an electron beam with a probe diameter of 300 nm is incident on a CAAC-OS including an InGaZnO$_4$ crystal in a direction parallel to the sample surface, a diffraction pattern (also referred to as a selected-area transmission electron diffraction pattern) shown in FIG. 50A can be obtained. In this diffraction pattern, spots derived from the (009) plane of an InGaZnO$_4$ crystal are included. Thus, the electron diffraction also indicates that pellets included in the CAAC-OS have c-axis alignment and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS. Meanwhile, FIG. 50B shows a diffraction pattern obtained in such a manner that an electron beam with a probe diameter of 300 nm is incident on the same sample in a direction perpendicular to the sample surface. As shown in FIG. 50B, a ring-like diffraction pattern is observed. Thus, the electron diffraction also indicates that the a-axes and b-axes of the pellets included in the CAAC-OS do not have regular alignment. The first ring in FIG. 50B is considered to be derived from the (010) plane, the (100) plane, and the like of the InGaZnO$_4$ crystal. Furthermore, it is supposed that the second ring in FIG. 50B is derived from the (110) plane and the like.

As described above, the CAAC-OS is an oxide semiconductor with high crystallinity. Entry of impurities, formation of defects, or the like might decrease the crystallinity of an oxide semiconductor. This means that the CAAC-OS has small amounts of impurities and defects (e.g., oxygen vacancy).

Note that the impurity means an element other than the main components of the oxide semiconductor, such as hydrogen, carbon, silicon, or a transition metal element. For example, an element (specifically, silicon or the like) having higher strength of bonding to oxygen than a metal element included in an oxide semiconductor extracts oxygen from the oxide semiconductor, which results in disorder of the atomic arrangement and reduced crystallinity of the oxide semiconductor. A heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (or molecular radius), and thus disturbs the atomic arrangement of the oxide semiconductor and decreases crystallinity.

The characteristics of an oxide semiconductor having impurities or defects might be changed by light, heat, or the like. Impurities included in the oxide semiconductor might serve as carrier traps or carrier generation sources, for example. Furthermore, oxygen vacancy in the oxide semiconductor serves as a carrier trap or serves as a carrier generation source when hydrogen is captured therein.

The CAAC-OS having small amounts of impurities and oxygen vacancy is an oxide semiconductor film with low carrier density (specifically, lower than 8×10^{11}/cm^3, preferably lower than 1×10^{11}/cm^3, further preferably lower than 1×10^{10}/cm^3, and is higher than or equal to 1×10^{-9}/cm^3). Such an oxide semiconductor is referred to as a highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor. A CAAC-OS has a low impurity concentration and a low density of defect states. Thus, the CAAC-OS can be referred to as an oxide semiconductor having stable characteristics.

<nc-OS>

Next, an nc-OS is described.

An nc-OS has a region in which a crystal part is observed and a region in which a crystal part is not clearly observed in a high-resolution TEM image. In most cases, the size of a crystal part included in the nc-OS is greater than or equal to 1 nm and less than or equal to 10 nm, or greater than or equal to 1 nm and less than or equal to 3 nm. Note that an oxide semiconductor including a crystal part whose size is greater than 10 nm and less than or equal to 100 nm is sometimes referred to as a microcrystalline oxide semiconductor. In a high-resolution TEM image of the nc-OS, for example, a grain boundary is not clearly observed in some cases. Note that there is a possibility that the origin of the nanocrystal is the same as that of a pellet in a CAAC-OS. Therefore, a crystal part of the nc-OS may be referred to as a pellet in the following description.

In the nc-OS, a microscopic region (for example, a region with a size greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or equal to 1 nm and less than or equal to 3 nm) has a periodic atomic arrangement. There is no regularity of crystal orientation between different pellets in the nc-OS. Thus, the orientation of the whole film is not observed. Accordingly, the nc-OS cannot be distinguished from an a-like OS and an amorphous oxide semiconductor, depending on an analysis method. For example, when the nc-OS is analyzed by an out-of-plane method using an X-ray beam having a diameter larger than the size of a pellet, a peak which shows a crystal plane does not appear. Furthermore, a diffraction pattern like a halo pattern is observed when the nc-OS is subjected to electron diffraction using an electron beam with a probe diameter (e.g., 50 nm or larger) that is larger than the size of a pellet. Meanwhile, spots appear in a nanobeam electron diffraction pattern of the nc-OS when an electron beam having a probe diameter close to or smaller than the size of a pellet is applied. Moreover, in a nanobeam electron diffraction pattern of the nc-OS, regions with high luminance in a circular (ring) pattern are shown in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS layer, a plurality of spots is shown in a ring-like region in some cases.

Since there is no regularity of crystal orientation between the pellets (nanocrystals) as mentioned above, the nc-OS can also be referred to as an oxide semiconductor including random aligned nanocrystals (RANC) or an oxide semiconductor including non-aligned nanocrystals (NANC).

The nc-OS is an oxide semiconductor that has high regularity as compared to an amorphous oxide semiconductor. Therefore, the nc-OS is likely to have a lower density of defect states than an a-like OS and an amorphous oxide semiconductor. Note that there is no regularity of crystal orientation between different pellets in the nc-OS. Therefore, the nc-OS has a higher density of defect states than the CAAC-OS.

<a-Like OS>

An a-like OS has a structure intermediate between those of the nc-OS and the amorphous oxide semiconductor.

In a high-resolution TEM image of the a-like OS, a void may be observed. Furthermore, in the high-resolution TEM image, there are a region where a crystal part is clearly observed and a region where a crystal part is not observed.

The a-like OS has an unstable structure because it includes a void. To verify that an a-like OS has an unstable structure as compared with a CAAC-OS and an nc-OS, a change in structure caused by electron irradiation is described below.

An a-like OS (sample A), an nc-OS (sample B), and a CAAC-OS (sample C) are prepared as samples subjected to electron irradiation. Each of the samples is an In—Ga—Zn oxide.

First, a high-resolution cross-sectional TEM image of each sample is obtained. The high-resolution cross-sectional TEM images show that all the samples have crystal parts.

Note that which part is regarded as a crystal part is determined as follows. It is known that a unit cell of the $InGaZnO_4$ crystal has a structure in which nine layers including three In—O layers and six Ga—Zn—O layers are stacked in the c-axis direction. The distance between the adjacent layers is equivalent to the lattice spacing on the (009) plane (also referred to as d value). The value is calculated to be 0.29 nm from crystal structural analysis. Accordingly, a portion where the lattice spacing between lattice fringes is greater than or equal to 0.28 nm and less than or equal to 0.30 nm is regarded as a crystal part of $InGaZnO_4$. Each of lattice fringes corresponds to the a-b plane of the $InGaZnO_4$ crystal.

FIG. 51 shows change in the average size of crystal parts (at 22 points to 45 points) in each sample. Note that the crystal part size corresponds to the length of a lattice fringe. FIG. 51 indicates that the crystal part size in the a-like OS increases with an increase in the cumulative electron dose. Specifically, as shown by (1) in FIG. 51, a crystal part of approximately 1.2 nm at the start of TEM observation (the crystal part is also referred to as an initial nucleus) grows to a size of approximately 2.6 nm at a cumulative electron dose of 4.2×10^8 e^-/nm^2. In contrast, the crystal part size in the nc-OS and the CAAC-OS shows little change from the start of electron irradiation to a cumulative electron dose of 4.2×10^8 e^-/nm^2. Specifically, as shown by (2) and (3) in FIG. 51, the average crystal sizes in an nc-OS and a CAAC-OS are approximately 1.4 nm and approximately 2.1 nm, respectively, regardless of the cumulative electron dose.

In this manner, growth of the crystal part in the a-like OS is induced by electron irradiation. In contrast, in the nc-OS and the CAAC-OS, growth of the crystal part is hardly induced by electron irradiation. Therefore, the a-like OS has an unstable structure as compared with the nc-OS and the CAAC-OS.

The a-like OS has a lower density than the nc-OS and the CAAC-OS because it includes a void. Specifically, the density of the a-like OS is higher than or equal to 78.6% and lower than 92.3% of the density of the single crystal oxide semiconductor having the same composition. The density of each of the nc-OS and the CAAC-OS is higher than or equal to 92.3% and lower than 100% of the density of the single crystal oxide semiconductor having the same composition. Note that it is difficult to deposit an oxide semiconductor having a density of lower than 78% of the density of the single crystal oxide semiconductor.

For example, in the case of an oxide semiconductor having an atomic ratio of In:Ga:Zn=1:1:1, the density of single crystal $InGaZnO_4$ with a rhombohedral crystal structure is 6.357 g/cm^3. Accordingly, in the case of the oxide semiconductor having an atomic ratio of In:Ga:Zn=1:1:1,

the density of the a-like OS is higher than or equal to 5.0 g/cm^3 and lower than 5.9 g/cm^3. For example, in the case of the oxide semiconductor having an atomic ratio of In:Ga:Zn=1:1:1, the density of each of the nc-OS and the CAAC-OS is higher than or equal to 5.9 g/cm^3 and lower than 6.3 g/cm^3.

Note that there is a possibility that an oxide semiconductor having a certain composition cannot exist in a single crystal structure. In that case, single crystal oxide semiconductors with different compositions are combined at an adequate ratio, which makes it possible to calculate density equivalent to that of a single crystal oxide semiconductor with the desired composition. The density of a single crystal oxide semiconductor having the desired composition can be calculated using a weighted average according to the combination ratio of the single crystal oxide semiconductors with different compositions. Note that it is preferable to use as few kinds of single crystal oxide semiconductors as possible to calculate the density.

As described above, oxide semiconductors have various structures and various properties. Note that an oxide semiconductor may be a stacked layer including two or more of an amorphous oxide semiconductor, an a-like OS, an nc-OS, and a CAAC-OS, for example.

<Deposition Model>

Deposition models of a CAAC-OS film and an nc-OS film are described below.

FIG. 40A is a schematic diagram of a deposition chamber illustrating a state where the CAAC-OS film is formed by a sputtering method.

A target 1130 is attached to a backing plate. Under the target 1130 and the backing plate, a plurality of magnets are provided. The plurality of magnets cause a magnetic field over the target 1130. A sputtering method in which the disposition speed is increased by utilizing a magnetic field of magnets is referred to as a magnetron sputtering method.

The target 1130 has a polycrystalline structure in which a cleavage plane exists in at least one crystal grain. Note that the details of the cleavage plane are described later.

A substrate 1120 is placed to face the target 1130, and the distance d (also referred to as a target-substrate distance (T-S distance)) is greater than or equal to 0.01 m and less than or equal to 1 m, preferably greater than or equal to 0.02 m and less than or equal to 0.5 m. The deposition chamber is mostly filled with a deposition gas (e.g., an oxygen gas, an argon gas, or a mixed gas containing oxygen at 50 vol % or higher) and controlled to higher than or equal to 0.01 Pa and lower than or equal to 100 Pa, preferably higher than or equal to 0.1 Pa and lower than or equal to 10 Pa. Here, discharge starts by application of a voltage at a certain value or higher to the target 1130, and plasma is observed. Note that the magnetic field over the target 1130 forms a high-density plasma region. In the high-density plasma region, the deposition gas is ionized, so that an ion 1101 is generated. Examples of the ion 1101 include an oxygen cation (O^+) and an argon cation (Ar^+).

The ion 1101 is accelerated to the target 1130 side by an electric field, and collides with the target 1130 eventually. At this time, a pellet 1100a and a pellet 1100b which are flat-plate-like or pellet-like sputtered particles are separated and sputtered from the cleavage plane. Note that structures of the pellet 1100a and the pellet 1100b may be distorted by an impact of collision of the ion 1101.

The pellet 1100a is a flat-plate-like or pellet-like sputtered particle having a triangle plane, e.g., a regular triangle plane. The pellet 1100b is a flat-plate-like or pellet-like sputtered particle having a hexagon plane, e.g., regular hexagon plane.

Note that flat-plate-like or pellet-like sputtered particles such as the pellet 1100a and the pellet 1100b are collectively called pellets 1100. The shape of a flat plane of the pellet 1100 is not limited to a triangle or a hexagon. For example, the flat plane may have a shape formed by combining greater than or equal to 2 and less than or equal to 6 triangles. For example, a square (rhombus) is formed by combining two triangles (regular triangles) in some cases.

The thickness of the pellet 1100 is determined depending on the kind of the deposition gas and the like. The thicknesses of the pellets 1100 are preferably uniform; the reasons thereof are described later. In addition, the sputtered particle preferably has a pellet shape with a small thickness as compared to a dice shape with a large thickness.

The pellet 1100 receives charge when passing through the plasma, so that side surfaces of the pellet 1100 are negatively or positively charged in some cases. The pellet 1100 includes an oxygen atom on its side surface, and the oxygen atom may be negatively charged. For example, a case in which the pellet 1100a includes, on its side surfaces, oxygen atoms that are negatively charged is illustrated in FIG. 42. As in this view, when the side surfaces are charged in the same polarity, charges repel each other, and accordingly, the pellet can maintain a flat-plate shape. In the case where a CAAC-OS is an In—Ga—Zn oxide, there is a possibility that an oxygen atom bonded to an indium atom is negatively charged. There is another possibility that an oxygen atom bonded to an indium atom, a gallium atom, or a zinc atom is negatively charged.

As shown in FIG. 40A, the pellet 1100 flies like a kite in plasma and flutters up to the substrate 1120. Since the pellets 1100 are charged, when the pellet 1100 gets close to a region where another pellet 1100 has already been deposited, repulsion is generated. Here, above the substrate 1120, a magnetic field is generated in a direction parallel to a top surface of the substrate 1120. A potential difference is given between the substrate 1120 and the target 1130, and accordingly, current flows from the substrate 1120 toward the target 1130. Thus, the pellet 1100 is given a force (Lorentz force) on the top surface of the substrate 1120 by an effect of the magnetic field and the current (see FIG. 43). This is explainable with Fleming's left-hand rule. In order to increase a force applied to the pellet 1100, it is preferable to provide, on the top surface, a region where the magnetic field in a direction parallel to the top surface of the substrate 1120 is 10 G or higher, preferably 20 G or higher, further preferably 30 G or higher, still further preferably 50 G or higher. Alternatively, it is preferable to provide, on the top surface, a region where the magnetic field in a direction parallel to the top surface of the substrate is 1.5 times or higher, preferably twice or higher, further preferably 3 times or higher, still further preferably 5 times or higher as high as the magnetic field in a direction perpendicular to the top surface of the substrate 1120.

Furthermore, the substrate 1120 is heated, and resistance such as friction between the pellet 1100 and the substrate 1120 is low. As a result, as illustrated in FIG. 44A, the pellet 1100 glides above the surface of the substrate 1120. The glide of the pellet 1100 is caused in a state where the flat plane faces the substrate 1120. Then, as illustrated in FIG. 44B, when the pellet 1100 reaches the side surface of another pellet 1100 that has been already deposited, the side surfaces of the pellets 1100 are bonded. At this time, the oxygen atom on the side surface of the pellet 1100 is released. With the released oxygen atom, oxygen vacancy in a CAAC-OS is filled in some cases; thus, the CAAC-OS has a low density of defect states.

Further, the pellet 1100 is heated on the substrate 1120, whereby atoms are rearranged, and the structure distortion caused by the collision of the ion 1101 can be reduced. The pellet 1100 whose structure distortion is reduced is substantially single crystal. Even when the pellets 1100 are heated after being bonded, expansion and contraction of the pellet 1100 itself hardly occur, which is caused by turning the pellet 1100 into substantially single crystal. Thus, formation of defects such as a grain boundary due to expansion of a space between the pellets 1100 can be prevented, and accordingly, generation of crevasses can be prevented. Further, the space is filled with elastic metal atoms and the like, whereby the elastic metal atoms have a function, like a highway, of jointing side surfaces of the pellets 1100 which are not aligned with each other.

It is considered that as shown in such a model, the pellets 1100 are deposited over the substrate 1120. Thus, a CAAC-OS film can be deposited even when a surface over which a film is formed (film formation surface) does not have a crystal structure, which is different from film deposition by epitaxial growth. For example, even when a surface (film formation surface) of the substrate 1120 has an amorphous structure, a CAAC-OS film can be formed.

Further, it is found that in formation of the CAAC-OS, the pellets 1100 are arranged in accordance with a surface shape of the substrate 1120 that is the film formation surface even when the film formation surface has unevenness besides a flat surface. For example, in the case where the surface of the substrate 1120 is flat at the atomic level, the pellets 1100 are arranged so that flat planes parallel to the a-b plane face downwards; thus, a layer with a uniform thickness, flatness, and high crystallinity is formed. By stacking n layers (n is a natural number), the CAAC-OS can be obtained (see FIG. 40B).

In the case where the top surface of the substrate 1120 has unevenness, a CAAC-OS where n layers (n is a natural number) in each of which the pellets 1100 are arranged along a convex surface are stacked is formed. Since the substrate 1120 has unevenness, a gap is easily generated between in the pellets 1100 in the CAAC-OS in some cases. Note that owing to intermolecular force, the pellets 1100 are arranged so that a gap between the pellets is as small as possible even on the unevenness surface. Therefore, even when the formation surface has unevenness, a CAAC-OS with high crystallinity can be formed (see FIG. 40C).

As a result, laser crystallization is not needed for formation of a CAAC-OS, and a uniform film can be formed even over a large-sized glass substrate.

Since the CAAC-OS film is deposited in accordance with such a model, the sputtered particle preferably has a pellet shape with a small thickness. Note that in the case where the sputtered particle has a dice shape with a large thickness, planes facing the substrate 1120 are not uniform and thus, the thickness and the orientation of the crystals cannot be uniform in some cases.

According to the deposition model described above, a CAAC-OS with high crystallinity can be formed even on a film formation surface with an amorphous structure.

Further, formation of a CAAC-OS can be described with a deposition model including a zinc oxide particle besides the pellet 1100.

The zinc oxide particle reaches the substrate 1120 before the pellet 1100 does because the zinc oxide particle is smaller than the pellet 1100 in mass. On the surface of the substrate 1120, crystal growth of the zinc oxide particle preferentially occurs in the horizontal direction, so that a thin zinc oxide layer is formed. The zinc oxide layer has

c-axis alignment. Note that c-axes of crystals in the zinc oxide layer are aligned in the direction parallel to a normal vector of the substrate **1120**. The zinc oxide layer serves as a seed layer that makes a CAAC-OS grow and thus has a function of increasing crystallinity of the CAAC-OS. The thickness of the zinc oxide layer is greater than or equal to 0.1 nm and less than or equal to 5 nm, mostly greater than or equal to 1 nm and less than or equal to 3 nm. Since the zinc oxide layer is sufficiently thin, a grain boundary is hardly observed.

Thus, in order to deposit a CAAC-OS with high crystallinity, a target including zinc at a proportion higher than that of the stoichiometric composition is preferably used.

An nc-OS can be understood with a deposition model illustrated in FIG. **41**. Note that a difference between FIG. **41** and FIG. **40**A lies only in the fact that whether the substrate **1120** is heated or not.

Thus, the substrate **1120** is not heated, and a resistance such as friction between the pellet **1100** and the substrate **1120** is high. As a result, the pellets **1100** cannot glide on the surface of the substrate **1120** and are stacked randomly, thereby forming an nc-OS.

<Cleavage Plane>

A cleavage plane that has been mentioned in the deposition model of the CAAC-OS will be described below.

First, a cleavage plane of the target is described with reference to FIGS. **45**A and **45**B. FIGS. **45**A and **45**B show the crystal structure of InGaZnO$_4$. Note that FIG. **45**A shows the structure of the case where an InGaZnO$_4$ crystal is observed from a direction parallel to the b-axis when the c-axis is in an upward direction. Furthermore, FIG. **45**B shows the structure of the case where the InGaZnO$_4$ crystal is observed from a direction parallel to the c-axis.

Energy needed for cleavage at each of crystal planes of the InGaZnO$_4$ crystal is calculated by the first principles calculation. Note that a "pseudopotential" and density functional theory program (CASTEP) using the plane wave basis are used for the calculation. Note that an ultrasoft type pseudopotential is used as the pseudopotential. Further, GGA/PBE is used as the functional. Cut-off energy is 400 eV.

Energy of a structure in an initial state is obtained after structural optimization including a cell size is performed. Further, energy of a structure after the cleavage at each plane is obtained after structural optimization of atomic arrangement is performed in a state where the cell size is fixed.

On the basis of the structure of the InGaZnO$_4$ crystal in FIGS. **45**A and **45**B, a structure cleaved at any one of a first plane, a second plane, a third plane, and a fourth plane is formed and subjected to structural optimization calculation in which the cell size is fixed. Here, the first plane is a crystal plane between a Ga—Zn—O layer and an In—O layer and is parallel to the (001) plane (the a-b plane) (see FIG. **45**A). The second plane is a crystal plane between a Ga—Zn—O layer and a Ga—Zn—O layer and is parallel to the (001) plane (the a-b plane) (see FIG. **45**A). The third plane is a crystal plane parallel to the (110) plane (see FIG. **45**B). The fourth plane is a crystal plane parallel to the (100) plane (the b-c plane) (see FIG. **45**B).

Under the above conditions, the energy of the structure at each plane after the cleavage is calculated. Next, a difference between the energy of the structure after the cleavage and the energy of the structure in the initial state is divided by the area of the cleavage plane; thus, cleavage energy which serves as a measure of easiness of cleavage at each plane is calculated. Note that the energy of a structure indicates energy obtained in such a manner that electronic kinetic

energy of electrons included in the structure and interactions between atoms included in the structure, between the atom and the electron, and between the electrons are considered.

As calculation results, the cleavage energy of the first plane was 2.60 J/m^2, that of the second plane was 0.68 J/m^2, that of the third plane was 2.18 J/m^2, and that of the fourth plane was 2.12 J/m^2 (see Table 1).

TABLE 1

	Cleavage energy [J/m^2]
First plane	2.60
Second plane	0.68
Third plane	2.18
Fourth plane	2.12

From the calculations, in the structure of the InGaZnO$_4$ crystal in FIGS. **45**A and **45**B, the cleavage energy of the second plane is the lowest. In other words, a plane between a Ga—Zn—O layer and a Ga—Zn—O layer is cleaved most easily (cleavage plane). Therefore, in this specification, the cleavage plane indicates the second plane, which is a plane where cleavage is performed most easily.

Since the cleavage plane is the second plane between the Ga—Zn—O layer and the Ga—Zn—O layer, the InGaZnO$_4$ crystals in FIG. **45**A can be separated at a plane equivalent to two second planes. Therefore, in the case where an ion or the like is made to collide with a target, a wafer-like unit (we call this a pellet) which is cleaved at a plane with the lowest cleavage energy is thought to be blasted off as the minimum unit. In that case, a pellet of InGaZnO$_4$ includes three layers: a Ga—Zn—O layer, an In—O layer, and a Ga—Zn—O layer.

The cleavage energies of the third plane (crystal plane parallel to the (110) plane) and the fourth plane (crystal plane parallel to the (100) plane (the b-c plane)) are lower than that of the first plane (crystal plane between the Ga—Zn—O layer and the In—O layer and plane that is parallel to the (001) plane (the a-b plane)), which suggests that most of the flat planes of the pellets have triangle shapes or hexagonal shapes.

Next, through classical molecular dynamics calculation, on the assumption of an InGaZnO$_4$ crystal having a homologous structure as a target, a cleavage plane in the case where the target is sputtered using argon (Ar) or oxygen (O) is examined. FIG. **46**A shows a cross-sectional structure of an InGaZnO$_4$ crystal (2688 atoms) used for the calculation, and FIG. **46**B shows a top structure thereof. Note that a fixed layer in FIG. **46**A prevents the positions of the atoms from moving. A temperature control layer in FIG. **46**A is a layer whose temperature is constantly set to fixed temperature (300 K).

For the classical molecular dynamics calculation, Materials Explorer 5.0 manufactured by Fujitsu Limited. is used. Note that the initial temperature, the cell size, the time step size, and the number of steps are set to be 300 K, a certain size, 0.01 fs, and ten million, respectively. In calculation, an atom to which an energy of 300 eV is applied is made to enter a cell from a direction perpendicular to the a-b plane of the InGaZnO$_4$ crystal under the conditions.

FIG. **47**A shows atomic order when 99.9 picoseconds have passed after argon enters the cell including the InGaZnO$_4$ crystal in FIGS. **46**A and **46**B. FIG. **47**B shows atomic order when 99.9 picoseconds have passed after oxygen enters the cell. Note that in FIGS. **47**A and **47**B, part of the fixed layer in FIG. **46**A is omitted.

According to FIG. **47**A, in a period from entry of argon into the cell to when 99.9 picoseconds have passed, a crack is formed from the cleavage plane corresponding to the second plane in FIG. **45**A. Thus, in the case where argon collides with the InGaZnO$_4$ crystal and the uppermost surface is the second plane (the zero-th), a large crack is found to be formed in the second plane (the second).

On the other hand, according to FIG. **47**B, in a period from entry of oxygen into the cell to when 99.9 picoseconds have passed, a crack is found to be formed from the cleavage plane corresponding to the second plane in FIG. **45**A. Note that in the case where oxygen collides with the cell, a large crack is found to be formed in the second plane (the first) of the InGaZnO$_4$ crystal.

Accordingly, it is found that an atom (ion) collides with a target including an InGaZnO$_4$ crystal having a homologous structure from the upper surface of the target, the InGaZnO$_4$ crystal is cleaved along the second plane, and a flat-plate-like sputtered particle (pellet) is separated. It is also found that the pellet formed in the case where oxygen collides with the cell is smaller than that formed in the case where argon collides with the cell.

The above calculation suggests that the separated pellet includes a damaged region. In some cases, the damaged region included in the pellet can be repaired in such a manner that a defect caused by the damage reacts with oxygen.

Here, difference in size of the pellet depending on atoms which are made to collide is studied.

FIG. **48**A shows trajectories of the atoms from 0 picosecond to 0.3 picoseconds after argon enters the cell including the InGaZnO$_4$ crystal in FIGS. **46**A and **46**B. Accordingly, FIG. **48**A corresponds to a period from FIGS. **46**A and **46**B to FIG. **47**A.

According to FIG. **48**A, when argon collides with gallium (Ga) of the first layer (Ga—Zn—O layer), gallium collides with zinc (Zn) of the third layer (Ga—Zn—O layer) and then, zinc reaches the vicinity of the sixth layer (Ga—Zn—O layer). Note that the argon which collides with the gallium is sputtered to the outside. Accordingly, in the case where argon collides with the target including the InGaZnO$_4$ crystal, a crack is thought to be formed in the second plane (the second) in FIG. **46**A.

FIG. **48**B shows trajectories of the atoms from 0 picosecond to 0.3 picoseconds after oxygen enters the cell including the InGaZnO$_4$ crystal in FIGS. **46**A and **46**B. Accordingly, FIG. **48**B corresponds to a period from FIGS. **46**A and **46**B to FIG. **47**A.

On the other hand, according to FIG. **48**B, when oxygen collides with gallium (Ga) of the first layer (Ga—Zn—O layer), gallium collides with zinc (Zn) of the third layer (Ga—Zn—O layer) and then, zinc does not reach the fifth layer (In—O layer). Note that the oxygen which collides with the gallium is sputtered to the outside. Accordingly, in the case where oxygen collides with the target including the InGaZnO$_4$ crystal, a crack is thought to be formed in the second plane (the first) in FIG. **46**A.

This calculation also shows that the InGaZnO$_4$ crystal with which an atom (ion) collides is separated from the cleavage plane.

In addition, a difference in depth of a crack is examined in view of conservation laws. The energy conservation law and the law of conservation of momentum can be represented by the following formula (1) and the following formula (2). Here, E represents energy of argon or oxygen before collision (300 eV), m$_A$ represents mass of argon or oxygen, v$_A$ represents the speed of argon or oxygen before

collision, v'$_A$ represents the speed of argon or oxygen after collision, m$_{Ga}$ represents mass of gallium, v$_{Ga}$ represents the speed of gallium before collision, and v'$_{Ga}$ represents the speed of gallium after collision.

$$E = \frac{1}{2}m_A v_A^2 + \frac{1}{2}m_{Ga}v_{Ga}^2 \qquad \text{[Formula 1]}$$

$$m_A v_A + m_{Ga}v_{Ga} = m_A v'_A + m_{Ga}v'_{Ga} \qquad \text{[Formula 2]}$$

On the assumption that collision of argon or oxygen is elastic collision, the relationship among v$_A$, v'$_A$, v$_{Ga}$, and v'$_{Ga}$ can be represented by the following formula (3).

$$v'_A - v'_{Ga} = -(v_A - v_{Ga}) \qquad \text{[Formula 3]}$$

From the formulae (1), (2), and (3), on the assumption that v$_{Ga}$ is 0, the speed of gallium v'$_{Ga}$ after collision of argon or oxygen can be represented by the following formula (4).

$$v'_{Ga} = \frac{\sqrt{m_A}}{m_A + m_{Ga}} \cdot 2\sqrt{2E} \qquad \text{[Formula 4]}$$

In the formula (4), mass of argon or oxygen is substituted into m$_A$, whereby the speeds after collision of the atoms are compared. In the case where the argon and the oxygen have the same energy before collision, the speed of gallium in the case where argon collides with the gallium was found to be 1.24 times as high as that in the case where oxygen collides with the gallium. Thus, the energy of the gallium in the case where argon collides with the gallium is higher than that in the case where oxygen collides with the gallium by the square of the speed.

The speed (energy) of gallium after collision in the case where argon collides with the gallium is found to be higher than that in the case where oxygen collides with the gallium. Accordingly, it is considered that a crack is formed at a deeper position in the case where argon collides with the gallium than in the case where oxygen collides with the gallium.

The above calculation shows that separation occurs from the cleavage plane to form a pellet when sputtering is performed using a target including the InGaZnO$_4$ crystal having a homologous structure. On the other hand, even when sputtering is performed on a region having another structure of a target without the cleavage plane, a pellet is not formed, and a sputtered particle with an atomic-level size which is minuter than a pellet is formed. Because the sputtered particle is smaller than the pellet, the sputtered particle is thought to be removed through a vacuum pump connected to a sputtering apparatus. Therefore, a model in which particles with a variety of sizes and shapes fly to a substrate and are deposited hardly applies to the case where sputtering is performed using a target including the InGaZnO$_4$ crystal having a homologous structure. The model illustrated in FIG. **40**A where sputtered pellets are deposited to form a CAAC-OS is a reasonable model.

The CAAC-OS deposited in such a manner has a density substantially equal to that of a single crystal OS. For example, the density of the single crystal OS film having a homologous structure of InGaZnO$_4$ is 6.36 g/cm^3, and the density of the CAAC-OS film having substantially the same atomic ratio is approximately 6.3 g/cm^3.

FIGS. **49**A and **49**B show atomic order of cross sections of an In—Ga—Zn oxide (see FIG. **49**A) that is a CAAC-OS

deposited by sputtering and a target thereof (see FIG. **49**B). For observation of atomic arrangement, a high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) is used. In the case of observation by HAADF-STEM, the intensity of an image of each atom is proportional to the square of its atomic number. Therefore, Zn (atomic number: 30) and Ga (atomic number: 31), whose atomic numbers are close to each other, are hardly distinguished from each other. A Hitachi scanning transmission electron microscope HD-2700 is used for the HAADF-STEM.

When FIG. **49**A and FIG. **49**B are compared, it is found that the CAAC-OS and the target each have a homologous structure and atomic order in the CAAC-OS correspond to that in the target. Thus, as illustrated in the deposition model in FIG. **40**A, the crystal structure of the target is transferred, whereby a CAAC-OS is formed.

Next, a relationship between crystallinity and an oxygen-transmitting property in the case where the oxide semiconductor film is an In—Ga—Zn oxide is described below.

An energy barrier due to movement of excess oxygen (oxygen) in a crystal of an In—Ga—Zn oxide is obtained by calculation. In the calculation, plane-wave basis first-principles calculation software Vienna ab-initio simulation package (VASP) based on density functional theory is used. GGA-PBE is used as a functional. Cut-off energy of a plane wave is 400 eV. The effect of an inner shell electron is included by a projector augmented wave (PAW) method.

Here, the ease of movement of excess oxygen (oxygen) through movement paths 1 to 4 in a crystal of an In—Ga—Zn oxide illustrated in FIG. **22** is calculated.

The movement path 1 is a path through which excess oxygen (oxygen) bonded to oxygen bonded to three indium atoms and one zinc atom is bonded to adjacent oxygen bonded to three indium atoms and one zinc atom. The movement path 2 is a path through which excess oxygen (oxygen) bonded to oxygen bonded to three indium atoms and one gallium atom crosses a layer containing indium and oxygen and is bonded to adjacent oxygen bonded to three indium atoms and one zinc atom. The movement path 3 is a path through which excess oxygen (oxygen) bonded to oxygen bonded to two gallium atoms and one zinc atom is bonded to adjacent oxygen bonded to two zinc atoms and one gallium atom. The movement path 4 is a path through which excess oxygen (oxygen) bonded to oxygen bonded to two gallium atoms and one zinc atom crosses a layer containing gallium, zinc, and oxygen and is bonded to adjacent oxygen bonded to three indium atoms and one gallium atom.

When the frequency of going over an energy barrier E_a per unit time is referred to as a diffusion frequency R, R can be expressed as the following formula.

$$R = v \cdot \exp[-E_a/(k_B T)] \qquad \text{[Formula 5]}$$

Note that v represents the number of heat vibrations of diffusion atoms, k_B represents Boltzmann constant, and T represents the absolute temperature. The diffusion frequency R at 350° C. and 450° C. when 10^{13} [1/sec] is applied to v as Debye frequency is shown in Table 2.

TABLE 2

| | | Diffusion frequency R [1/sec] | |
	Energy barrier [eV]	350° C.	450° C.
Movement path 1	0.50	9.0×10^8	3.3×10^9
Movement path 2	1.97	1.2×10^{-3}	1.9×10^{-1}

TABLE 2-continued

| | | Diffusion frequency R [1/sec] | |
	Energy barrier [eV]	350° C.	450° C.
Movement path 3	0.53	5.2×10^8	2.0×10^9
Movement path 4	0.56	3.0×10^8	1.3×10^9

As shown in Table 2, the movement path 2 across the layer containing indium and oxygen has a higher energy barrier than the other movement paths. This indicates that movement of excess oxygen (oxygen) in the c-axis direction is less likely to occur in a crystal of an In—Ga—Zn oxide. In other words, in the case where crystals have c-axis alignment and the c-axes are aligned in a direction substantially perpendicular to a formation surface or a top surface, like CAAC-OS, movement of excess oxygen (oxygen) is less likely to occur in the direction substantially perpendicular to the formation surface or the top surface.

The structure and method described in this embodiment can be implemented by being combined as appropriate with any of the other structures and methods described in the other embodiments.

Embodiment 3

In this embodiment, oxygen vacancy of an oxide semiconductor film is described in detail below.

<(1) Ease of Formation and Stability of V_oH>

In the case where an oxide semiconductor film (hereinafter referred to as IGZO) is a complete crystal, H preferentially diffuses along the a-b plane at a room temperature. In heat treatment at 450° C., H diffuses along the a-b plane and in the c-axis direction. Here, description is made on whether H easily enters oxygen vacancy V_o if the oxygen vacancy V_o exists in IGZO. A state in which H is in oxygen vacancy V_o is referred to as V_oH.

An $InGaZnO_4$ crystal model shown in FIG. **23** was used for calculation. The activation barrier (E_a) along the reaction path where H in V_oH is released from V_o and bonded to oxygen was calculated by a nudged elastic band (NEB) method. The calculation conditions are shown in Table 3.

TABLE 3

Software	VASP
Calculation method	NEB method
Functional	GGA-PBE
Pseudopotential	PAW
Cut-off energy	500 eV
K points	2 × 2 × 3

In the $InGaZnO_4$ crystal model, there are oxygen sites 1 to 4 as shown in FIG. **23** which differ from each other in metal elements bonded to oxygen and the number of bonded metal elements. Here, calculation was made on the oxygen sites 1 and 2 in which oxygen vacancy V_o is easily formed.

First, calculation was made on the oxygen site in which oxygen vacancy V_o is easily formed: an oxygen site 1 that was bonded to three In atoms and one Zn atom.

FIG. **24**A shows a model in the initial state and FIG. **24**B shows a model in the final state. FIG. **25** shows the calculated activation barrier (E_a) in the initial state and the final state. Note that here, the initial state refers to a state in which H exists in oxygen vacancy V_o (V_oH), and the final state

refers to a structure including oxygen vacancy V_o and a state in which H is bonded to oxygen bonded to one Ga atom and two Zn atoms (H—O).

From the calculation results, bonding of H in oxygen vacancy V_o to another oxygen atom needs an energy of approximately 1.52 eV, while entry of H bonded to O into oxygen vacancy V_o needs an energy of approximately 0.46 eV.

Reaction frequency (Γ) was calculated with use of the activation barriers (E_a) obtained by the calculation and Formula 6. In Formula 6, k_B represents the Boltzmann constant and T represents the absolute temperature.

$$\Gamma = v\exp\left(-\frac{E_a}{k_B T}\right) \qquad \text{[Formula 6]}$$

The reaction frequency at 350° C. was calculated on the assumption that the frequency factor $v=10^{13}$ [1/sec]. The frequency of H transfer from the model shown in FIG. **24A** to the model shown in FIG. **24B** was 5.52×10^9 [1/sec], whereas the frequency of H transfer from the model shown in FIG. **24B** to the model shown in FIG. **24A** was 1.82×10^9 [1/sec]. This suggests that H diffusing in IGZO is likely to form V_oH if oxygen vacancy V_o exists in the neighborhood, and H is unlikely to be released from the oxygen vacancy V_o once V_oH is formed.

Next, calculation was made on the oxygen site in which oxygen vacancy V_o is easily formed: an oxygen site 2 that was bonded to one Ga atom and two Zn atoms.

FIG. **26A** shows a model in the initial state and FIG. **26B** shows a model in the final state. FIG. **27** shows the calculated activation barrier (E_a) in the initial state and the final state. Note that here, the initial state refers to a state in which H exists in oxygen vacancy V_o (V_oH), and the final state refers to a structure including oxygen vacancy V_o and a state in which H is bonded to oxygen bonded to one Ga atom and two Zn atoms (H—O).

From the calculation results, bonding of H in oxygen vacancy V_o to another oxygen atom needs an energy of approximately 1.75 eV, while entry of H bonded to O in oxygen vacancy V_o needs an energy of approximately 0.35 eV.

Reaction frequency (Γ) was calculated with use of the activation barriers (E_a) obtained by the calculation and Formula 6.

The reaction frequency at 350° C. was calculated on the assumption that the frequency factor $v=10^{13}$ [1/sec]. The frequency of H transfer from the model shown in FIG. **26A** to the model shown in FIG. **26B** was 7.53×10^{-2} [1/sec], whereas the frequency of H transfer from the model shown in FIG. **26B** to the model shown in FIG. **26A** was 1.44×10^{10} [1/sec]. This suggests that H is unlikely to be released from the oxygen vacancy V_o once V_oH is formed.

From the above results, it was found that H in IGZO easily diffused in annealing and if oxygen vacancy V_o existed, H was likely to enter the oxygen vacancy V_o to be V_oH.

<(2) Transition Level of V_oH>

The calculation by the NEB method, which was described in <(1) Ease of formation and stability of V_oH>, indicates that in the case where oxygen vacancy V_o and H exist in IGZO, the oxygen vacancy V_o and H easily form V_oH and V_oH is stable. To determine whether V_oH is related to a carrier trap, the transition level of V_oH was calculated.

The model used for calculation is an InGaZnO$_4$ crystal model (112 atoms). V_oH models of the oxygen sites 1 and

2 shown in FIG. **25** were made to calculate the transition levels. The calculation conditions are shown in Table 4.

TABLE 4

Software	VASP
Model	InGaZnO$_4$ crystal model (112 atoms)
Functional	HSE06
Mixture ratio of exchange terms	0.25
Pseudopotential	GGA-PBE
Cut-off energy	800 eV
K points	$1 \times 1 \times 1$

The mixture ratio of exchange terms was adjusted to have a band gap close to the experimental value. As a result, the band gap of the InGaZnO$_4$ crystal model without defects was 3.08 eV that is close to the experimental value, 3.15 eV.

The transition level ($\in$(q/q')) of a model having defect D can be calculated by the following Formula 7. Note that $\Delta E(D^q)$ represents the formation energy of defect D at charge q, which is calculated by Formula 8.

$$\varepsilon(q/q') = \frac{\Delta E(D^q) - \Delta E(D^{q'})}{q' - q} \qquad \text{[Formula 7]}$$

$$\Delta E(D^q) = \qquad \text{[Formula 8]}$$
$$E_{tot}(D^q) - E_{tot}(\text{bulk}) + \sum_i \Delta n_i \mu_i + q(\varepsilon_{VBM} + \Delta V_q + E_F)$$

In Formulae 7 and 8, $E_{tot}(D^q)$ represents the total energy of the model having defect D at the charge q in, $E_{tot}(\text{bulk})$ represents the total energy in a model without defects (complete crystal), Δn_i represents a change in the number of atoms i contributing to defects, μ_i represents the chemical potential of atom i, $\in_{VBM}$ represents the energy of the valence band maximum in the model without defects, ΔV_q represents the correction term relating to the electrostatic potential, and E_F represents the Fermi energy.

FIG. **28** shows the transition levels of V_oH obtained from the above formulae. The numbers in FIG. **28** represent the depth from the conduction band minimum. In FIG. **28**, the transition level of V_oH in the oxygen site 1 is at 0.05 eV from the conduction band minimum, and the transition level of V_oH in the oxygen site 2 is at 0.11 eV from the conduction band minimum. Therefore, these V_oH would be related to electron traps, that is, V_oH was found to behave as a donor. It was also found that IGZO including V_oH had conductivity.

The structure described in this embodiment can be used in appropriate combination with any of the structures described in the other embodiments.

Embodiment 4

In this embodiment, an example of a display device that includes any of the transistors described in the embodiment above is described below with reference to FIG. **29**, FIG. **30**, and FIG. **31**.

FIG. **29** is a top view of an example of a display device. A display device **700** illustrated in FIG. **29** includes a pixel portion **702** provided over a first substrate **701**; a source driver circuit portion **704** and a gate driver circuit portion **706** provided over the first substrate **701**; a sealant **712** provided to surround the pixel portion **702**, the source driver circuit portion **704**, and the gate driver circuit portion **706**; and a second substrate **705** provided to face the first sub-

strate 701. The first substrate 701 and the second substrate 705 are sealed with the sealant 712. That is, the pixel portion 702, the source driver circuit portion 704, and the gate driver circuit portion 706 are sealed with the first substrate 701, the sealant 712, and the second substrate 705. Although not illustrated in FIG. 29, a display element is provided between the first substrate 701 and the second substrate 705.

In the display device 700, a flexible printed circuit (FPC) terminal portion 708 electrically connected to the pixel portion 702, the source driver circuit portion 704, and the gate driver circuit portion 706 is provided in a region different from the region which is surrounded by the sealant 712 and positioned over the first substrate 701. Furthermore, an FPC 716 is connected to the FPC terminal portion 708, and a variety of signals and the like are supplied to the pixel portion 702, the source driver circuit portion 704, and the gate driver circuit portion 706 through the FPC 716. Furthermore, a signal line 710 is connected to the pixel portion 702, the source driver circuit portion 704, the gate driver circuit portion 706, and the FPC terminal portion 708. Various signals and the like are applied to the pixel portion 702, the source driver circuit portion 704, the gate driver circuit portion 706, and the FPC terminal portion 708 via the signal line 710 from the FPC 716.

A plurality of gate driver circuit portions 706 may be provided in the display device 700. An example of the display device 700 in which the source driver circuit portion 704 and the gate driver circuit portion 706 are formed over the first substrate 701 where the pixel portion 702 is also formed is described; however, the structure is not limited thereto. For example, only the gate driver circuit portion 706 may be formed over the first substrate 701 or only the source driver circuit portion 704 may be formed over the first substrate 701. In this case, a substrate where a source driver circuit, a gate driver circuit, or the like is formed (e.g., a driver-circuit substrate formed using a single-crystal semiconductor film or a polycrystalline semiconductor film) may be mounted on the first substrate 701. Note that there is no particular limitation on the method of connecting a separately prepared driver circuit substrate, and a chip on glass (COG) method, a wire bonding method, or the like can be used.

The pixel portion 702, the source driver circuit portion 704, and the gate driver circuit portion 706 included in the display device 700 include a plurality of transistors. As the plurality of transistors, any of the transistors that are the semiconductor devices of embodiments of the present invention can be used.

The display device 700 can include any of a variety of elements. The element includes, for example, at least one of a liquid crystal element, an electroluminescence (EL) element (e.g., an EL element including organic and inorganic materials, an organic EL element, or an inorganic EL element), an LED (e.g., a white LED, a red LED, a green LED, or a blue LED), a transistor (a transistor that emits light depending on current), an electron emitter, electronic ink, an electrophoretic element, a grating light valve (GLV), a plasma display panel (PDP), a display element using micro electro mechanical system (MEMS), a digital micromirror device (DMD), a digital micro shutter (DMS), MIRASOL (registered trademark), an interferometric modulator display (IMOD) element, a MEMS shutter display element, an optical-interference-type MEMS display element, an electrowetting element, a piezoelectric ceramic display, and a display element including a carbon nanotube. Other than the above, display media whose contrast, luminance, reflectivity, transmittance, or the like is changed by an electrical or

magnetic effect may be included. Examples of display devices having EL elements include an EL display. Examples of display devices including electron emitters include a field emission display (FED) and an SED-type flat panel display (SED: surface-conduction electron-emitter display). Examples of display devices including liquid crystal elements include a liquid crystal display (e.g., a transmissive liquid crystal display, a transflective liquid crystal display, a reflective liquid crystal display, a direct-view liquid crystal display, or a projection liquid crystal display). An example of a display device including electronic ink or electrophoretic elements is electronic paper. In the case of a transflective liquid crystal display or a reflective liquid crystal display, some of or all of pixel electrodes function as reflective electrodes. For example, some or all of pixel electrodes are formed to include aluminum, silver, or the like. In such a case, a memory circuit such as an SRAM can be provided under the reflective electrodes, leading to lower power consumption.

As a display method in the display device 700, a progressive method, an interlace method, or the like can be employed. Furthermore, color elements controlled in a pixel at the time of color display are not limited to three colors: R, G, and B (R, G, and B correspond to red, green, and blue, respectively). For example, four pixels of the R pixel, the G pixel, the B pixel, and a W (white) pixel may be included. Alternatively, a color element may be composed of two colors among R, G, and B as in PenTile layout. The two colors may differ among color elements. Alternatively, one or more colors of yellow, cyan, magenta, and the like may be added to RGB. Further, the size of a display region may be different depending on respective dots of the color components. Embodiments of the disclosed invention are not limited to a display device for color display; the disclosed invention can also be applied to a display device for monochrome display.

A coloring layer (also referred to as a color filter) may be used in order to obtain a full-color display device in which white light (W) for a backlight (e.g., an organic EL element, an inorganic EL element, an LED, or a fluorescent lamp) is used. As the coloring layer, red (R), green (G), blue (B), yellow (Y), or the like may be combined as appropriate, for example. With the use of the coloring layer, higher color reproducibility can be obtained than in the case without the coloring layer. In this case, by providing a region with the coloring layer and a region without the coloring layer, white light in the region without the coloring layer may be directly utilized for display. By partly providing the region without the coloring layer, a decrease in luminance due to the coloring layer can be suppressed, and 20% to 30% of power consumption can be reduced in some cases when an image is displayed brightly. Note that in the case where full-color display is performed using a self-luminous element such as an organic EL element or an inorganic EL element, elements may emit light of their respective colors R, G, B, Y, and W. By using a self-luminous element, power consumption can be further reduced as compared to the case of using the coloring layer in some cases.

In this embodiment, a structure including a liquid crystal element and an EL element as display elements is described with reference to FIG. 30 and FIG. 31. Note that FIG. 30 is a cross-sectional view along the dashed-dotted line Q-R shown in FIG. 29 and shows a structure including a liquid crystal element as a display element, whereas FIG. 31 is a cross-sectional view along the dashed-dotted line Q-R shown in FIG. 29 and shows a structure including an EL element as a display element.

Common portions between FIG. 30 and FIG. 31 are described first, and then different portions are described.

<Common Portions in Display Devices>

The display device 700 illustrated in FIG. 30 and FIG. 31 include a lead wiring portion 711, the pixel portion 702, the source driver circuit portion 704, and the FPC terminal portion 708. Note that the lead wiring portion 711 includes a signal line 710. The pixel portion 702 includes a transistor 750 and a capacitor 790. The source driver circuit portion 704 includes a transistor 752.

Any of the transistors described above can be used as the transistors 750 and 752.

The transistors used in this embodiment each include an oxide semiconductor film which is highly purified and in which formation of oxygen vacancies is suppressed. In the transistor, the current in an off state (off-state current) can be made small. Accordingly, an electrical signal such as an image signal can be held for a longer period, and a writing interval can be set longer in an on state. Accordingly, frequency of refresh operation can be reduced, which leads to an effect of suppressing power consumption.

In addition, the transistor used in this embodiment can have relatively high field-effect mobility and thus is capable of high speed operation. For example, with such a transistor which can operate at high speed used for a liquid crystal display device, a switching transistor in a pixel portion and a driver transistor in a driver circuit portion can be formed over one substrate. That is, a semiconductor device formed using a silicon wafer or the like is not additionally needed as a driver circuit, by which the number of components of the semiconductor device can be reduced. In addition, the transistor which can operate at high speed can be used also in the pixel portion, whereby a high-quality image can be provided.

The capacitor 790 includes a dielectric between a pair of electrodes. Specifically, a conductive film which is formed using the same step as a conductive film functioning as a gate electrode of the transistor 750 is used as one electrode of the capacitor 790, and a conductive film functioning as a source electrode or a drain electrode of the transistor 750 is used as the other electrode of the capacitor 790. Furthermore, an insulating film functioning as a gate insulating film of the transistor 750 is used as the dielectric between the pair of electrodes.

In FIG. 30 and FIG. 31, insulating films 764, 766, and 768 and a planarization insulating film 770 are formed over the transistor 750, the transistor 752, and the capacitor 790.

The insulating films 764, 766, and 768 can be formed using materials and methods similar to those of the insulating films 114, 116, and 118 described in the above embodiment, respectively. The planarization insulating film 770 can be formed using a heat-resistant organic material, such as a polyimide resin, an acrylic resin, a polyimide amide resin, a benzocyclobutene resin, a polyamide resin, or an epoxy resin. Note that the planarization insulating film 770 may be formed by stacking a plurality of insulating films formed from these materials. Alternatively, a structure without the planarization insulating film 770 may be employed.

The signal line 710 is formed in the same process as conductive films functioning as a source electrode and a drain electrode of the transistor 750 or 752. Note that the signal line 710 may be formed using a conductive film which is formed in a different process as a source electrode and a drain electrode of the transistor 750 or 752, e.g., a conductive film functioning as a gate electrode may be used. In the case where the signal line 710 is formed using a material

including a copper element, signal delay or the like due to wiring resistance is reduced, which enables display on a large screen.

The FPC terminal portion 708 includes a connection electrode 760, an anisotropic conductive film 780, and the FPC 716. Note that the connection electrode 760 is formed in the same process as conductive films functioning as a source electrode and a drain electrode of the transistor 750 or 752. The connection electrode 760 is electrically connected to a terminal included in the FPC 716 through the anisotropic conductive film 780.

For example, a glass substrate can be used as the first substrate 701 and the second substrate 705. A flexible substrate may be used as the first substrate 701 and the second substrate 705. Examples of the flexible substrate include a plastic substrate.

A structure body 778 is provided between the first substrate 701 and the second substrate 705. The structure body 778 is a columnar spacer obtained by selective etching of an insulating film and provided to control the distance (cell gap) between the first substrate 701 and the second substrate 705. Note that a spherical spacer may be used as the structure body 778. Although the structure in which the structure body 778 is provided on the first substrate 701 side is described as an example in this embodiment, one embodiment of the present invention is not limited thereto. For example, a structure in which the structure body 778 is provided on the second substrate 705 side, or a structure in which both of the first substrate 701 and the second substrate 705 are provided with the structure body 778 may be employed.

Furthermore, a light-blocking film 738 functioning as a black matrix, a coloring film 736 functioning as a color filter, and an insulating film 734 in contact with the light-blocking film 738 and the coloring film 736 are provided on the second substrate 705 side.

Structure Example of Display Device Using Liquid Crystal Element as Display Element

The display device 700 illustrated in FIG. 30 includes a liquid crystal element 775. The liquid crystal element 775 includes a conductive film 772, a conductive film 774, and a liquid crystal layer 776. The conductive film 774 is provided on the second substrate 705 side and functions as a counter electrode. The display device 700 in FIG. 30 is capable of displaying an image in such a manner that transmission or non-transmission is controlled by change in the alignment state of the liquid crystal layer 776 depending on a voltage applied to the conductive film 772 and the conductive film 774.

The conductive film 772 is connected to the conductive films functioning as a source electrode and a drain electrode included in the transistor 750. The conductive film 772 is formed over the planarization insulating film 770 to function as a pixel electrode, i.e., one electrode of the display element. The conductive film 772 has a function of a reflective electrode. The display device 700 in FIG. 30 is what is called a reflective color liquid crystal display device in which external light is reflected by the conductive film 772 to display an image through the coloring film 736.

A conductive film that transmits visible light or a conductive film that reflects visible light can be used for the conductive film 772. For example, a material including one kind selected from indium (In), zinc (Zn), and tin (Sn) is preferably used for the conductive film that transmits visible light. For example, a material including aluminum or silver

may be used for the conductive film that reflects visible light. In this embodiment, the conductive film that reflects visible light is used for the conductive film **772**.

In the case where a conductive film which reflects visible light is used as the conductive film **772**, the conductive film may have a stacked-layer structure. For example, a 100-nm-thick aluminum film is formed as the bottom layer, and a 30-nm-thick silver alloy film (e.g., an alloy film including silver, palladium, and copper) is formed as the top layer. Such a structure makes it possible to obtain the following effects.

(1) Adhesion between the base film and the conductive film **772** can be improved.

(2) The aluminum film and the silver alloy film can be collectively etched depending on a chemical solution.

(3) The conductive film **772** can have a favorable cross-sectional shape (e.g., a tapered shape).

The reason for (3) is as follows: the etching rate of the aluminum film with the chemical solution is higher than that of the copper alloy film, or etching of the aluminum film that is the bottom layer is developed faster than that of the silver alloy film because when the aluminum film that is the bottom layer is exposed after the etching of the silver alloy film that is the top layer, electrons are extracted from metal that is less noble than the silver alloy film, i.e., aluminum that is metal having a high ionization tendency, and thus etching of the silver alloy film is suppressed.

Note that projections and depressions are provided in part of the planarization insulating film **770** of the pixel portion **702** in the display device **700** in FIG. **30**. The projections and depressions can be formed in such a manner that the planarization insulating film **770** is formed using an organic resin film or the like, and projections and depressions are formed on the surface of the organic resin film. The conductive film **772** functioning as a reflective electrode is formed along the projections and depressions. Therefore, when external light is incident on the conductive film **772**, the light is reflected diffusely at the surface of the conductive film **772**, whereby visibility can be improved.

Note that the display device **700** illustrated in FIG. **30** is a reflective color liquid crystal display device given as an example, but a display type is not limited thereto. For example, a transmissive color liquid crystal display device in which the conductive film **772** is a conductive film that transmits visible light may be used. In the case of a transmissive color liquid crystal display device, projections and depressions are not necessarily provided on the planarization insulating film **770**.

Although not illustrated in FIG. **30**, an alignment film may be provided on a side of the conductive film **772** in contact with the liquid crystal layer **776** and on a side of the conductive film **774** in contact with the liquid crystal layer **776**. Although not illustrated in FIG. **30**, an optical member (an optical substrate) and the like such as a polarizing member, a retardation member, or an anti-reflection member may be provided as appropriate. For example, circular polarization may be employed by using a polarizing substrate and a retardation substrate. In addition, a backlight, a sidelight, or the like may be used as a light source.

In the case where a liquid crystal element is used as the display element, a thermotropic liquid crystal, a low-molecular liquid crystal, a high-molecular liquid crystal, a polymer dispersed liquid crystal, a ferroelectric liquid crystal, an anti-ferroelectric liquid crystal, or the like can be used. Such a liquid crystal material exhibits a cholesteric

phase, a smectic phase, a cubic phase, a chiral nematic phase, an isotropic phase, or the like depending on conditions.

Alternatively, in the case of employing a horizontal electric field mode, a liquid crystal exhibiting a blue phase for which an alignment film is unnecessary may be used. A blue phase is one of liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase while temperature of cholesteric liquid crystal is increased. Since the blue phase appears only in a narrow temperature range, a liquid crystal composition in which several weight percent or more of a chiral material is mixed is used for the liquid crystal layer in order to improve the temperature range. The liquid crystal composition which includes liquid crystal exhibiting a blue phase and a chiral material has a short response time and optical isotropy. In addition, the liquid crystal composition which includes liquid crystal exhibiting a blue phase does not need alignment treatment and has a small viewing angle dependence. An alignment film does not need to be provided and rubbing treatment is thus not necessary; accordingly, electrostatic discharge damage caused by the rubbing treatment can be prevented and defects and damage of the liquid crystal display device in the manufacturing process can be reduced.

In the case where a liquid crystal element is used as the display element, a twisted nematic (TN) mode, an in-plane-switching (IPS) mode, a fringe field switching (FFS) mode, an axially symmetric aligned micro-cell (ASM) mode, an optical compensated birefringence (OCB) mode, a ferroelectric liquid crystal (FLC) mode, an antiferroelectric liquid crystal (AFLC) mode, or the like can be used.

Further, a normally black liquid crystal display device such as a transmissive liquid crystal display device utilizing a vertical alignment (VA) mode may also be used. There are some examples of a vertical alignment mode; for example, a multi-domain vertical alignment (MVA) mode, a patterned vertical alignment (PVA) mode, an ASV mode, or the like can be employed.

<Display Device Using Light-Emitting Element as Display Element>

The display device **700** illustrated in FIG. **31** includes a light-emitting element **782**. The light-emitting element **782** includes a conductive film **784**, an EL layer **786**, and a conductive film **788**. The display device **700** shown in FIG. **31** is capable of displaying an image by light emission from the EL layer **786** included in the light-emitting element **782**.

The conductive film **784** is connected to the conductive films functioning as a source electrode and a drain electrode included in the transistor **750**. The conductive film **784** is formed over the planarization insulating film **770** to function as a pixel electrode, i.e., one electrode of the display element. A conductive film which transmits visible light or a conductive film which reflects visible light can be used for the conductive film **784**. The conductive film which transmits visible light can be formed using a material including one kind selected from indium (In), zinc (Zn), and tin (Sn), for example. The conductive film which reflects visible light can be formed using a material including aluminum or silver, for example.

In the display device **700** shown in FIG. **31**, an insulating film **730** is provided over the planarization insulating film **770** and the conductive film **784**. The insulating film **730** covers part of the conductive film **784**. Note that the light-emitting element **782** has a top emission structure. Therefore, the conductive film **788** has a light-transmitting property and transmits light emitted from the EL layer **786**. Although the top-emission structure is described as an

example in this embodiment, one embodiment of the present invention is not limited thereto. A bottom-emission structure in which light is emitted to the conductive film **784** side, or a dual-emission structure in which light is emitted to both the conductive film **784** side and the conductive film **788** side may be employed.

The coloring film **736** is provided to overlap with the light-emitting element **782**, and the light-blocking film **738** is provided to overlap with the insulating film **730** and to be included in the lead wiring portion **711** and in the source driver circuit portion **704**. The coloring film **736** and the light-blocking film **738** are covered with the insulating film **734**. A space between the light-emitting element **782** and the insulating film **734** is filled with the sealing film **732**. Although a structure with the coloring film **736** is described as the display device **700** shown in FIG. **31**, the structure is not limited thereto. In the case where the EL layer **786** is formed by a separate coloring method, the coloring film **736** is not necessarily provided.

The structure described in this embodiment can be used in appropriate combination with any of the structures described in the other embodiments.

Embodiment 5

In this embodiment, a display device that includes a semiconductor device of one embodiment of the present invention is described with reference to FIGS. **32A** to **32C**.

The display device illustrated in FIG. **32A** includes a region including pixels of display elements (hereinafter the region is referred to as a pixel portion **502**), a circuit portion being provided outside the pixel portion **502** and including a circuit for driving the pixels (hereinafter the portion is referred to as a driver circuit portion **504**), circuits each having a function of protecting an element (hereinafter the circuits are referred to as protection circuits **506**), and a terminal portion **507**. Note that the protection circuits **506** are not necessarily provided.

A part or the whole of the driver circuit portion **504** is preferably formed over a substrate over which the pixel portion **502** is formed, in which case the number of components and the number of terminals can be reduced. When a part or the whole of the driver circuit portion **504** is not formed over the substrate over which the pixel portion **502** is formed, the part or the whole of the driver circuit portion **504** can be mounted by COG or tape automated bonding (TAB).

The pixel portion **502** includes a plurality of circuits for driving display elements arranged in X rows (X is a natural number of 2 or more) and Y columns (Y is a natural number of 2 or more) (hereinafter, such circuits are referred to as pixel circuits **501**). The driver circuit portion **504** includes driver circuits such as a circuit for supplying a signal (scan signal) to select a pixel (hereinafter, the circuit is referred to as a gate driver **504a**) and a circuit for supplying a signal (data signal) to drive a display element in a pixel (hereinafter, the circuit is referred to as a source driver **504b**).

The gate driver **504a** includes a shift register or the like. The gate driver **504a** receives a signal for driving the shift register through the terminal portion **507** and outputs a signal. For example, the gate driver **504a** receives a start pulse signal, a clock signal, or the like and outputs a pulse signal. The gate driver **504a** has a function of controlling the potentials of wirings supplied with scan signals (hereinafter, such wirings are referred to as scan lines GL_**1** to GL_X). Note that a plurality of gate drivers **504a** may be provided to control the scan lines GL_**1** to GL_X separately. Alter-

natively, the gate driver **504a** has a function of supplying an initialization signal. Without being limited thereto, the gate driver **504a** can supply another signal.

The source driver **504b** includes a shift register or the like. The source driver **504b** receives a signal (video signal) from which a data signal is derived, as well as a signal for driving the shift register, through the terminal portion **507**. The source driver **504b** has a function of generating a data signal to be written to the pixel circuit **501** which is based on the video signal. In addition, the source driver **504b** has a function of controlling output of a data signal in response to a pulse signal produced by input of a start pulse signal, a clock signal, or the like. Further, the source driver **504b** has a function of controlling the potentials of wirings supplied with data signals (hereinafter such wirings are referred to as data lines DL_**1** to DL_Y). Alternatively, the source driver **504b** has a function of supplying an initialization signal. Without being limited thereto, the source driver **504b** can supply another signal.

The source driver **504b** includes a plurality of analog switches or the like, for example. The source driver **504b** can output, as the data signals, signals obtained by time-dividing the video signal by sequentially turning on the plurality of analog switches. The source driver **504b** may include a shift register or the like.

A pulse signal and a data signal are input to each of the plurality of pixel circuits **501** through one of the plurality of scan lines GL supplied with scan signals and one of the plurality of data lines DL supplied with data signals, respectively. Writing and holding of the data signal to and in each of the plurality of pixel circuits **501** are controlled by the gate driver **504a**. For example, to the pixel circuit **501** in the m-th row and the n-th column (m is a natural number of less than or equal to X, and n is a natural number of less than or equal to Y), a pulse signal is input from the gate driver **504a** through the scan line GL_m, and a data signal is input from the source driver **504b** through the data line DL_n in accordance with the potential of the scan line GL_m.

The protection circuit **506** shown in FIG. **32A** is connected to, for example, the scan line GL between the gate driver **504a** and the pixel circuit **501**. Alternatively, the protection circuit **506** is connected to the data line DL between the source driver **504b** and the pixel circuit **501**. Alternatively, the protection circuit **506** can be connected to a wiring between the gate driver **504a** and the terminal portion **507**. Alternatively, the protection circuit **506** can be connected to a wiring between the source driver **504b** and the terminal portion **507**. Note that the terminal portion **507** means a portion having terminals for inputting power, control signals, and video signals to the display device from external circuits.

The protection circuit **506** is a circuit that electrically connects a wiring connected to the protection circuit to another wiring when a potential out of a certain range is applied to the wiring connected to the protection circuit.

As illustrated in FIG. **32A**, the protection circuits **506** are provided for the pixel portion **502** and the driver circuit portion **504**, so that the resistance of the display device to overcurrent generated by electrostatic discharge (ESD) or the like can be improved. Note that the configuration of the protection circuits **506** is not limited to that, and for example, the protection circuit **506** may be configured to be connected to the gate driver **504a** or the protection circuit **506** may be configured to be connected to the source driver **504b**. Alternatively, the protection circuit **506** may be configured to be connected to the terminal portion **507**.

In FIG. **32A**, an example in which the driver circuit portion **504** includes the gate driver **504a** and the source driver **504b** is shown; however, the structure is not limited thereto. For example, only the gate driver **504a** may be formed and a separately prepared substrate where a source driver circuit is formed (e.g., a driver circuit substrate formed with a single crystal semiconductor film or a poly-crystalline semiconductor film) may be mounted.

Each of the plurality of pixel circuits **501** in FIG. **32A** can have the structure illustrated in FIG. **32B**, for example.

The pixel circuit **501** illustrated in FIG. **32B** includes a liquid crystal element **570**, a transistor **550**, and a capacitor **560**. As the transistor **550**, any of the transistors described in the above embodiment, for example, can be used.

The potential of one of a pair of electrodes of the liquid crystal element **570** is set in accordance with the specifications of the pixel circuit **501** as appropriate. The alignment state of the liquid crystal element **570** depends on written data. A common potential may be supplied to one of the pair of electrodes of the liquid crystal element **570** included in each of the plurality of pixel circuits **501**. Further, the potential supplied to one of the pair of electrodes of the liquid crystal element **570** in the pixel circuit **501** in one row may be different from the potential supplied to one of the pair of electrodes of the liquid crystal element **570** in the pixel circuit **501** in another row.

As examples of a driving method of the display device including the liquid crystal element **570**, any of the following modes can be given: a TN mode, an STN mode, a VA mode, an axially symmetric aligned micro-cell (ASM) mode, an optically compensated birefringence (OCB) mode, a ferroelectric liquid crystal (FLC) mode, an antiferroelectric liquid crystal (AFLC) mode, an MVA mode, a patterned vertical alignment (PVA) mode, an IPS mode, an FFS mode, a transverse bend alignment (TBA) mode, and the like. Other examples of the driving method of the display device include an electrically controlled birefringence (ECB) mode, a polymer dispersed liquid crystal (PDLC) mode, a polymer network liquid crystal (PNLC) mode, and a guest-host mode. Note that the present invention is not limited to these examples, and various liquid crystal elements and driving methods can be applied to the liquid crystal element and the driving method thereof.

In the pixel circuit **501** in the m-th row and the n-th column, one of a source electrode and a drain electrode of the transistor **550** is electrically connected to the data line DL_n, and the other is electrically connected to the other of the pair of electrodes of the liquid crystal element **570**. A gate electrode of the transistor **550** is electrically connected to the scan line GL_m. The transistor **550** has a function of controlling whether to write a data signal by being turned on or off.

One of a pair of electrodes of the capacitor **560** is electrically connected to a wiring to which a potential is supplied (hereinafter referred to as a potential supply line VL), and the other is electrically connected to the other of the pair of electrodes of the liquid crystal element **570**. The potential of the potential supply line VL is set in accordance with the specifications of the pixel circuit **501** as appropriate. The capacitor **560** functions as a storage capacitor for storing written data.

For example, in the display device including the pixel circuit **501** in FIG. **32B**, the pixel circuits **501** are sequentially selected row by row by the gate driver **504a** illustrated in FIG. **32A**, whereby the transistors **550** are turned on and a data signal is written.

When the transistors **550** are turned off, the pixel circuits **501** in which the data has been written are brought into a holding state. This operation is sequentially performed row by row; thus, an image can be displayed.

Alternatively, each of the plurality of pixel circuits **501** in FIG. **32A** can have the structure illustrated in FIG. **32C**, for example.

The pixel circuit **501** illustrated in FIG. **32C** includes transistors **552** and **554**, a capacitor **562**, and a light-emitting element **572**. Any of the transistors described in the above embodiment, for example, can be used as one or both of the transistors **552** and **554**.

One of a source electrode and a drain electrode of the transistor **552** is electrically connected to a wiring to which a data signal is supplied (hereinafter referred to as a signal line DL_n). A gate electrode of the transistor **552** is electrically connected to a wiring to which a gate signal is supplied (hereinafter referred to as a scan line GL_m).

The transistor **552** has a function of controlling whether to write a data signal by being turned on or off.

One of a pair of electrodes of the capacitor **562** is electrically connected to a wiring to which a potential is supplied (hereinafter referred to as a potential supply line VL_a), and the other is electrically connected to the other of the source electrode and the drain electrode of the transistor **552**.

The capacitor **562** functions as a storage capacitor for storing written data.

One of a source electrode and a drain electrode of the transistor **554** is electrically connected to the potential supply line VL_a. Further, a gate electrode of the transistor **554** is electrically connected to the other of the source electrode and the drain electrode of the transistor **552**.

One of an anode and a cathode of the light-emitting element **572** is electrically connected to a potential supply line VL_b, and the other is electrically connected to the other of the source electrode and the drain electrode of the transistor **554**.

As the light-emitting element **572**, an organic electroluminescent element (also referred to as an organic EL element) or the like can be used, for example. Note that the light-emitting element **572** is not limited to an organic EL element; an inorganic EL element including an inorganic material may be used.

A high power supply potential VDD is supplied to one of the potential supply line VL_a and the potential supply line VL_b, and a low power supply potential VSS is supplied to the other.

For example, in the display device including the pixel circuit **501** in FIG. **32C**, the pixel circuits **501** are sequentially selected row by row by the gate driver **504a** illustrated in FIG. **32A**, whereby the transistors **552** are turned on and a data signal is written.

When the transistors **552** are turned off, the pixel circuits **501** in which the data has been written are brought into a holding state. Further, the amount of current flowing between the source electrode and the drain electrode of the transistor **554** is controlled in accordance with the potential of the written data signal. The light-emitting element **572** emits light with a luminance corresponding to the amount of flowing current. This operation is sequentially performed row by row; thus, an image can be displayed.

The structure described in this embodiment can be used in appropriate combination with the structure described in any of the other embodiments.

Embodiment 6

In this embodiment, a display module and electronic appliances that include a semiconductor device of one

embodiment of the present invention are described with reference to FIG. **33** and FIGS. **34**A to **34**H.

In a display module **8000** illustrated in FIG. **33**, a touch panel **8004** connected to an FPC **8003**, a display panel **8006** connected to an FPC **8005**, a backlight unit **8007**, a frame **8009**, a printed board **8010**, and a battery **8011** are provided between an upper cover **8001** and a lower cover **8002**.

The semiconductor device of one embodiment of the present invention can be used for, for example, the display panel **8006**.

The shapes and sizes of the upper cover **8001** and the lower cover **8002** can be changed as appropriate in accordance with the sizes of the touch panel **8004** and the display panel **8006**.

The touch panel **8004** can be a resistive touch panel or a capacitive touch panel and can be formed to overlap the display panel **8006**. A counter substrate (sealing substrate) of the display panel **8006** can have a touch panel function. A photosensor may be provided in each pixel of the display panel **8006** to form an optical touch panel.

The backlight unit **8007** includes a light source **8008**. Note that although a structure in which the light sources **8008** are provided over the backlight unit **8007** is illustrated in FIG. **33**, one embodiment of the present invention is not limited to this structure. For example, a structure in which the light source **8008** is provided at an end portion of the backlight unit **8007** and a light diffusion plate is further provided may be employed. Note that the backlight unit **8007** need not be provided in the case where a self-luminous light-emitting element such as an organic EL element is used or in the case where a reflective panel or the like is employed.

The frame **8009** protects the display panel **8006** and also functions as an electromagnetic shield for blocking electromagnetic waves generated by the operation of the printed board **8010**. The frame **8009** may function as a radiator plate.

The printed board **8010** is provided with a power supply circuit and a signal processing circuit for outputting a video signal and a clock signal. As a power source for supplying power to the power supply circuit, an external commercial power source or a power source using the battery **8011** provided separately may be used. The battery **8011** can be omitted in the case of using a commercial power source.

The display module **8000** may be additionally provided with a member such as a polarizing plate, a retardation plate, or a prism sheet.

FIGS. **34**A to **34**H illustrate electronic appliances. These electronic appliances can include a housing **9000**, a display portion **9001**, a speaker **9003**, an LED lamp **9004**, operation keys **9005** (including a power switch or an operation switch), a connection terminal **9006**, a sensor **9007** (a sensor having a function of measuring or sensing force, displacement, position, speed, acceleration, angular velocity, rotational frequency, distance, light, liquid, magnetism, temperature, chemical substance, sound, time, hardness, electric field, current, voltage, electric power, radiation, flow rate, humidity, gradient, oscillation, odor, or infrared ray), a microphone **9008**, and the like.

FIG. **34**A illustrates a mobile computer that can include a switch **9009**, an infrared port **9010**, and the like in addition to the above components. FIG. **34**B illustrates a portable image reproducing device (e.g., a DVD player) that is provided with a memory medium and can include a second display portion **9002**, a memory medium reading portion **9011**, and the like in addition to the above components. FIG. **34**C illustrates a goggle-type display that can include the

second display portion **9002**, a support **9012**, an earphone **9013**, and the like in addition to the above components. FIG. **34**D illustrates a portable game machine that can include the memory medium reading portion **9011** and the like in addition to the above components. FIG. **34**E illustrates a digital camera that has a television reception function and can include an antenna **9014**, a shutter button **9015**, an image receiving portion **9016**, and the like in addition to the above components. FIG. **34**F illustrates a portable game machine that can include the second display portion **9002**, the memory medium reading portion **9011**, and the like in addition to the above components. FIG. **34**G illustrates a television receiver that can include a tuner, an image processing portion, and the like in addition to the above components. FIG. **34**H illustrates a portable television receiver that can include a charger **9017** capable of transmitting and receiving signals, and the like in addition to the above components.

The electronic appliances illustrated in FIGS. **34**A to **34**H can have a variety of functions, for example, a function of displaying a variety of data (a still image, a moving image, a text image, and the like) on the display portion, a touch panel function, a function of displaying a calendar, date, time, and the like, a function of controlling a process with a variety of software (programs), a wireless communication function, a function of being connected to a variety of computer networks with a wireless communication function, a function of transmitting and receiving a variety of data with a wireless communication function, a function of reading a program or data stored in a memory medium and displaying the program or data on the display portion, and the like. Furthermore, the electronic appliance including a plurality of display portions can have a function of displaying image data mainly on one display portion while displaying text data on another display portion, a function of displaying a three-dimensional image by displaying images on a plurality of display portions with a parallax taken into account, or the like. Furthermore, the electronic appliance including an image receiving portion can have a function of shooting a still image, a function of taking a moving image, a function of automatically or manually correcting a shot image, a function of storing a shot image in a memory medium (an external memory medium or a memory medium incorporated in the camera), a function of displaying a shot image on the display portion, or the like. Note that functions that can be provided for the electronic appliances illustrated in FIGS. **34**A to **34**H are not limited to those described above, and the electronic appliances can have a variety of functions.

The electronic appliances described in this embodiment each include the display portion for displaying some sort of data. Note that the semiconductor device of one embodiment of the present invention can also be used for an electronic appliance that does not have a display portion.

The electronic appliances described in this embodiment each include the display portion for displaying some sort of data. Note that the semiconductor device of one embodiment of the present invention can also be used for an electronic appliance that does not have a display portion.

Example 1

In this example, the amount of oxygen released from an insulating film included in a semiconductor device of one embodiment of the present invention was measured. Samples 1 to 10 described below were used for evaluation in this example.

(Sample 1)

Sample 1 was formed in such a manner that a 100-nm-thick silicon oxide film was formed over a glass substrate with a sputtering apparatus. The silicon oxide film was deposited under the conditions where the substrate temperature was 100° C., an oxygen gas at a flow rate of 50 sccm was introduced into a chamber, the pressure was 0.5 Pa, and a DC power of 6000 W was supplied to a silicon sputtering target.

(Sample 2)

Sample 2 was formed in such a manner that a 100-nm-thick silicon nitride film and a 400-nm-thick silicon oxynitride film over the 100-nm-thick silicon nitride film were formed over a glass substrate with a PECVD apparatus and subjected to heat treatment.

(Sample 3)

Sample 3 was formed in such a manner that a 100-nm-thick silicon nitride film and a 400-nm-thick silicon oxynitride film over the 100-nm-thick silicon nitride film were formed over a glass substrate with a PECVD apparatus and subjected to heat treatment. Then, oxygen addition treatment is performed on the silicon oxynitride film.

(Sample 4)

Sample 4 was formed in such a manner that a 100-nm-thick silicon nitride film and a 400-nm-thick silicon oxynitride film over the 100-nm-thick silicon nitride film were formed over a glass substrate with a PECVD apparatus and subjected to heat treatment. Next, a 5-nm-thick oxide semiconductor film (an IGZO film with In:Ga:Zn=1:1:1) was formed with a sputtering apparatus. Then, oxygen addition treatment was performed through the oxide semiconductor film. After that, the oxide semiconductor film was removed to expose the silicon oxynitride film.

(Sample 5)

Sample 5 was formed in such a manner that a 100-nm-thick silicon nitride film and a 400-nm-thick silicon oxynitride film over the 100-nm-thick silicon nitride film were formed over a glass substrate with a PECVD apparatus and subjected to heat treatment. Next, a 5-nm-thick tungsten film was formed with a sputtering apparatus. Then, oxygen addition treatment was performed through the tungsten film. After that, the tungsten film was removed to expose the silicon oxynitride film.

(Sample 6)

Sample 6 was formed in such a manner that a 100-nm-thick silicon nitride film and a 400-nm-thick silicon oxynitride film over the 100-nm-thick silicon nitride film were formed over a glass substrate with a PECVD apparatus and subjected to heat treatment. Next, a 5-nm-thick tantalum nitride film was formed with a sputtering apparatus. Then, oxygen addition treatment was performed through the tantalum nitride film. After that, the tantalum nitride film was removed to expose the silicon oxynitride film.

(Sample 7)

Sample 7 was formed in such a manner that a 100-nm-thick silicon nitride film and a 400-nm-thick silicon oxynitride film over the 100-nm-thick silicon nitride film were formed over a glass substrate with a PECVD apparatus and subjected to heat treatment. Next, a 5-nm-thick titanium film was formed with a sputtering apparatus. Then, oxygen addition treatment was performed through the titanium film. After that, the titanium film was removed to expose the silicon oxynitride film.

(Sample 8)

Sample 8 was formed in such a manner that a 100-nm-thick silicon nitride film and a 400-nm-thick silicon oxynitride film over the 100-nm-thick silicon nitride film were

formed over a glass substrate with a PECVD apparatus and subjected to heat treatment. Next, a 5-nm-thick aluminum film was formed with a sputtering apparatus. Then, oxygen addition treatment was performed through the aluminum film. After that, the aluminum film was removed to expose the silicon oxynitride film.

(Sample 9)

Sample 9 was formed in such a manner that a 100-nm-thick silicon nitride film and a 400-nm-thick silicon oxynitride film over the 100-nm-thick silicon nitride film were formed over a glass substrate with a PECVD apparatus and subjected to heat treatment. Next, a 5-nm-thick ITSO film was formed with a sputtering apparatus. Then, oxygen addition treatment was performed through the ITSO film. After that, the ITSO film was removed to expose the silicon oxynitride film. Note that the composition ratio of In_2O_3 to SnO_2 and SiO_2 in the target used for forming the ITSO film was 85:10:5 [wt %].

(Sample 10)

Sample 10 was formed in such a manner that a 100-nm-thick silicon nitride film was formed over a glass substrate with a PECVD apparatus.

The heat treatment performed on each of Samples 2 to 9 was performed at 650° C. for 6 minutes in a nitrogen atmosphere with an RTA apparatus. By the heat treatment, oxygen included in the silicon oxynitride film at the time of deposition is released from the silicon oxynitride film.

The silicon nitride film used in each of Samples 2 to 10 was deposited under the conditions where the substrate temperature was 350° C.; a silane gas at a flow rate of 200 sccm, a nitrogen gas at a flow rate of 2000 sccm, and an ammonia gas at a flow rate of 2000 sccm were introduced into a chamber; the pressure was 100 Pa; and an RF power of 2000 W was supplied between parallel-plate electrodes provided in a PECVD apparatus.

The silicon oxynitride film in each of Samples 2 to 9 was deposited under the conditions where the substrate temperature was 220° C., a silane gas at a flow rate of 160 sccm and a dinitrogen monoxide gas at a flow rate of 4000 sccm were introduced into a chamber, the pressure was 200 Pa, and an RF power of 1500 W was supplied between parallel-plate electrodes provided in a PECVD apparatus.

The oxygen addition treatment performed on each of Samples 3 to 9 was conducted with an etching apparatus under the conditions where the substrate temperature was 40° C., an oxygen gas (^{16}O) at a flow rate of 250 sccm was introduced into a chamber, the pressure was 15 Pa, and an RF power of 4500 W was supplied between parallel-plate electrodes provided in the etching apparatus so that a bias would be applied to the substrate side.

The amount of a gas having a mass-to-charge ratio (M/z) of 32, i.e., oxygen (O_2), released from each of Samples 1 to 10 was measured. A TDS analysis apparatus was used for measuring the amount of released gas.

FIG. **35** shows the TDS measurement results of Samples 1 to 10. In FIG. **35**, the horizontal axis shows the name of the sample, and the vertical axis represents the amount of released gas with M/z=32.

According to the results in FIG. **35**, the amount of a gas with M/z=32 released from Sample 1 was $5×10^{20}/cm^3$. The amount of a gas with M/z=32 released from Sample 2 was $3×10^{18}/cm^3$. The amount of a gas with M/z=32 released from Sample 3 was $2×10^{19}/cm^3$. The amount of a gas with M/z=32 released from Sample 4 was $3×10^{20}/cm^3$. The amount of a gas with M/z=32 released from Sample 5 was $5×10^{19}/cm^3$. The amount of a gas with M/z=32 released from Sample 6 was $2×10^{21}/cm^3$. The amount of a gas with

M/z=32 released from Sample 7 was $1 \times 10^{21}/cm^3$. The amount of a gas with M/z=32 released from Sample 8 was $5 \times 10^{20}/cm^3$. The amount of a gas with M/z=32 released from Sample 9 was $8 \times 10^{20}/cm^3$. The amount of a gas with M/z=32 released from Sample 10 was $3 \times 10^{18}/cm^3$.

The results indicate that such an amount of oxygen was released from Sample 1 because a sputtering apparatus was used for depositing the silicon oxide film in Sample 1 and thus the silicon oxide film had excess oxygen, and further, heat treatment was not performed. In addition, the amount of oxygen released from Sample 2 was smaller than those of oxygen released from the other samples because heat treatment was performed after formation of the silicon oxynitride film in Sample 2 to release oxygen from the silicon oxynitride film. Furthermore, the amount of oxygen released from each of Samples 3 to 9 was larger than that of oxygen released from Sample 2 because oxygen addition treatment was performed on each of Samples 3 to 9 after heat treatment. Moreover, the amount of oxygen released from each of Samples 4 to 9 was larger than that of oxygen released from Sample 3 because the metal film, the metal nitride film, or the metal oxide film was provided over the silicon oxynitride film, and oxygen was added to the silicon oxynitride film through the metal film, the metal nitride film, or the metal oxide film. In particular, the amount of oxygen released from Sample 6, i.e., the structure that included a silicon oxynitride film and a tantalum nitride film over the silicon oxynitride film and was subjected to oxygen addition treatment, was the largest of those of oxygen released from the samples. Furthermore, the amount of oxygen released from Sample 10 was small because a gas containing oxygen was not used for deposition.

As described above, it is proved that Sample 1 and Samples 3 to 9 are each capable of releasing oxygen by heating, and the amount of oxygen released from each of Sample 1 and Samples 3 to 9 was greater than or equal to $1 \times 10^{19}/cm^3$, which is estimated as oxygen molecules. Therefore, these samples can be used as the third insulating film of the semiconductor device of one embodiment of the present invention. Furthermore, Sample 2 and Sample 10 can each be used as the fourth insulating film.

The structure described above in this example can be combined with any of the structures described in the other embodiments and examples as appropriate.

Example 2

In this example, the oxygen concentration of an insulating film included in the semiconductor device of one embodiment of the present invention, here, a silicon oxynitride film, was measured. Sample A1 and Sample A2 described below were formed and used for evaluation in this example.
(Sample A1)

Sample A1 was formed as follows. A 100-nm-thick silicon nitride film was formed over a glass substrate, a 400-nm-thick silicon oxynitride film was formed over the silicon nitride film, and heat treatment was performed. Then, a 5-nm-thick tantalum nitride film was formed with a sputtering apparatus. After that, the tantalum nitride film was removed to expose the silicon oxynitride film. Note that Sample A1 is for comparison.
(Sample A2)

Sample A2 was formed as follows. A 100-nm-thick silicon nitride film was formed over a glass substrate, a 400-nm-thick silicon oxynitride film was formed over the silicon nitride film, and heat treatment was performed. Then, a 5-nm-thick tantalum nitride film was formed with a sput-

tering apparatus, and oxygen addition treatment was performed. After that, the tantalum nitride film was removed to expose the silicon oxynitride film.

The deposition conditions of the silicon nitride film in each of Samples A1 and A2 were the same as those described in Example 1. The heat treatment conditions for each of Samples A1 and A2 were the same as those described in Example 1.

The oxygen addition treatment performed on Sample A2 was conducted with an etching apparatus under the conditions where the substrate temperature was 40° C., an oxygen gas (^{16}O) at a flow rate of 150 sccm and an oxygen gas (^{18}O) at a flow rate of 100 sccm were introduced into a chamber, the pressure was 15 Pa, and an RF power of 4500 W was supplied between parallel-plate electrodes provided in the etching apparatus so that a bias would be applied to the substrate side. Since the silicon oxynitride film included oxygen (^{16}O) at a main component level when deposited, an oxygen gas (^{18}O) was used to exactly measure the amount of oxygen added by the oxygen addition treatment.

The oxygen concentrations of Samples A1 and A2 were measured. A SIMS analysis apparatus was used for measuring the oxygen concentration, and oxygen to be measured was ^{18}O.

FIGS. 36A and 36B show SIMS measurement results of Sample A1 and Sample A2, respectively.

In FIGS. 36A and 36B, the vertical axis and the horizontal axis represent ^{18}O concentration and depth, respectively. A dashed line in FIGS. 36A and 36B denotes the vicinity of the interface between the silicon oxynitride film and the silicon nitride film. Furthermore, in FIGS. 36A and 36B, "SiON" denotes the silicon oxynitride film, and "SiN" denotes the silicon nitride film.

Since Sample A1 for comparison was not subjected to oxygen addition treatment, the silicon oxynitride film includes oxygen (^{18}O) at approximately 1.0×10^{20} atoms/cm³ as shown in FIG. 36A. This is substantially equal to the natural abundance of oxygen (^{18}O) (0.2%), which means that the silicon oxynitride film of Sample A1 hardly includes oxygen (^{18}O). Meanwhile, the silicon oxynitride film included in the semiconductor device of one embodiment of the present invention includes oxygen (^{18}O) at higher than or equal to 8.0×10^{20} atoms/cm³ and lower than or equal to 1×10^{22} atoms/cm³ as shown in FIG. 36B. Thus, the oxygen concentration of the silicon oxynitride film can be increased by oxygen addition treatment. In addition, it was found that the oxygen introduced into the silicon oxynitride film by the oxygen addition treatment was substantially uniformly included in the silicon oxynitride film.

The structure described above in this example can be combined with any of the structures described in the other embodiments as appropriate.

Example 3

In this example, a transistor corresponding to the transistor 170 in FIGS. 7A to 7C was formed and tests for electrical characteristics and reliability were performed. In this example, Sample B1, Sample B2, Sample C1, and Sample C2 were formed and used for evaluation. Note that Samples B1 and B2 are transistors for comparison, and Samples C1 and C2 are transistors of one embodiment of the present invention. To form each of Samples B1, B2, C1, and C2, 20 transistors were formed over a substrate.

The samples formed in this example are described below. Note that the reference numerals used for the transistor 170 in FIGS. 7A to 7C are used in the following description.

(Sample B1 and Sample B2)

Sample B1 included 20 transistors each having a channel length L of 2 μm and a channel width W of 50 μm, and Sample B2 included 20 transistors each having a channel length L of 6 μm and a channel width W of 50 μm. Thus, both the samples had the same structure by the same method, except for the channel length L.

First, the conductive film 104 was formed over the substrate 102. As the substrate 102, a glass substrate was used. Furthermore, as the conductive film 104, a 100-nm-thick tungsten film was formed with a sputtering apparatus.

Next, the insulating films 106 and 107 were formed over the substrate 102 and the conductive film 104. As the insulating film 106, a 400-nm-thick silicon nitride film was formed with a PECVD apparatus. As the insulating film 107, a 50-nm-thick silicon oxynitride film was formed with a PECVD apparatus.

Then, the oxide semiconductor film 108 was formed over the insulating film 107. As the oxide semiconductor film 108, a 35-nm-thick IGZO film was formed with a sputtering apparatus. Note that the oxide semiconductor film 108 was deposited under the conditions where the substrate temperature was 170° C., an argon gas at a flow rate of 100 sccm and an oxygen gas at a flow rate of 100 sccm were introduced into a chamber, the pressure was 0.6 Pa, and an AC power of 2500 W was applied to a metal oxide sputtering target (In:Ga:Zn=1:1:1).

Then, first heat treatment was performed. As the first heat treatment, heat treatment was performed at 450° C. for 1 hour in a nitrogen atmosphere and then heat treatment was performed at 450° C. for 1 hour in a mixed atmosphere of nitrogen and oxygen.

Next, the conductive films 112a and 112b were formed over the insulating film 107 and the oxide semiconductor film 108. As the conductive films 112a and 112b, a 50-nm-thick tungsten film, a 400-nm-thick aluminum film, and a 100-nm-thick titanium film were successively formed in vacuum with a sputtering apparatus.

After that, the insulating film 114 and the insulating film 116 were formed over the insulating film 107, the oxide semiconductor film 108, and the conductive films 112a and 112b. As the insulating film 114, a 50-nm-thick silicon oxynitride film was formed with a PECVD apparatus. As the insulating film 116, a 400-nm-thick silicon oxynitride film was formed with a PECVD apparatus. Note that the insulating film 114 and the insulating film 116 were formed successively in vacuum with a PECVD apparatus.

The insulating film 114 was deposited under the conditions where the substrate temperature was 220° C., a silane gas at a flow rate of 50 sccm and a dinitrogen monoxide gas at a flow rate of 2000 sccm were introduced into a chamber, the pressure was 20 Pa, and an RF power of 100 W was supplied between parallel-plate electrodes provided in a PECVD apparatus. The insulating film 116 was deposited under the conditions where the substrate temperature was 220° C., a silane gas at a flow rate of 160 sccm and a dinitrogen monoxide gas at a flow rate of 4000 sccm were introduced into a chamber, the pressure was 200 Pa, and an RF power of 1500 W was supplied between parallel-plate electrodes provided in a PECVD apparatus.

Then, second heat treatment was performed. The second heat treatment was performed at 350° C. for 1 hour in a mixed gas atmosphere of nitrogen and oxygen.

Next, the insulating film 118 was formed over the insulating film 116. As the insulating film 118, a 100-nm-thick silicon nitride film was formed with a PECVD apparatus. The insulating film 118 was deposited under the conditions

where the substrate temperature was 350° C., a silane gas at a flow rate of 50 sccm, a nitrogen gas at a flow rate of 5000 sccm, and an ammonia gas at a flow rate of 100 sccm were introduced into a chamber, the pressure was 100 Pa, and an RF power of 1000 W was supplied between parallel-plate electrodes provided in a PECVD apparatus.

Next, the opening 142c reaching the conductive film 112b and the openings 142a and 142b reaching the conductive film 104 were formed. The openings 142a, 142b, and 142c were formed with a dry etching apparatus.

Next, a conductive film was formed over the insulating film 118 to cover the openings 142a, 142b, and 142c and processed to form the conductive films 120a and 120b. For the conductive films 120a and 120b, a 100-nm-thick ITSO film was formed with a sputtering apparatus. The composition of a target used for forming the ITSO film was the same as that described in Example 1.

Then, third heat treatment was performed. The third heat treatment was performed at 250° C. for 1 hour in a nitrogen atmosphere.

Through the above process, Samples B1 and Sample B2 were formed.

(Sample C1 and Sample C2)

Sample C1 included 20 transistors each having a channel length L of 2 μm and a channel width W of 50 μm, and Sample C2 included 20 transistors each having a channel length L of 6 μm and a channel width W of 50 μm. Thus, both the samples had the same structure except for the channel length L and were formed by the same formation method.

The process for forming Samples C1 and C2 are different from that for forming Samples B1 and B2 described above in the following steps. The steps other than the following steps are the same as those for Samples B1 and B2.

After the second heat treatment, the film 130 capable of inhibiting release of oxygen was formed over the insulating film 116. As the film 130, a 5-nm-thick tantalum oxide film was formed with a sputtering apparatus.

Next, oxygen addition treatment was performed on the oxide semiconductor film 108 and the insulating films 114 and 116 through the film 130. The film 130 became the insulating film 131 owing to the oxygen addition treatment. As the insulating film 131, a tantalum oxide film was formed. The conditions of the oxygen addition treatment were the same as those described in Example 1.

Next, the insulating film 118 was formed over the insulating film 131. As the insulating film 118, a 100-nm-thick silicon nitride film was formed with a PECVD apparatus. In this manner, in Samples C1 and C2 of this example, the insulating film 131 was not removed. That is, Samples C1 and C2 each have a structure of the transistor 170 in FIGS. 7A to 7C in which the insulating film 131 is provided between the insulating film 116 and the insulating film 118.

Through the above processes, Samples B1, B2, C1, and C2 were formed.

FIGS. 37A and 37B and FIGS. 38A and 38B show electrical characteristics of Samples B1, B2, C1, and C2.

Note that FIG. 37A shows electrical characteristics of Sample B1, FIG. 37B shows electrical characteristics of Sample B2, FIG. 38A shows the electrical characteristics of Sample C1, and FIG. 38B shows electrical characteristics of Sample C2. In FIGS. 37A and 37B and FIGS. 38A and 38B, the horizontal axis and the vertical axis represent gate voltage (VG) and drain current (ID), respectively, and data of the 20 transistors are superimposed on each other. Furthermore, voltage between the source electrode and the drain

electrode (the voltage is expressed as VD) was set at 10 V, and VG was applied from −15 V to 20 V at intervals of 0.5 V.

The results in FIGS. **37**A and **37**B and FIGS. **38**A and **38**B show that variation among the transistors is large in Samples B1 and B2. In particular, variation in characteristics among the transistors having a channel length L of 2 μm in Sample B1 is large and the transistors have normally-on characteristics. In contrast, variation in characteristics among the transistors is small in Samples C1 and C2. Furthermore, Samples C1 and C2 have favorable rising characteristics in the vicinity of 0 V.

Next, reliability tests were performed on Samples B1, C1, and C2. For the reliability tests, a bias-temperature stress test (hereinafter, referred to as gate bias temperature (GBT) test) was used.

Note that the GBT test is one kind of accelerated test and a change in characteristics, caused by long-term usage, of transistors can be evaluated in a short time. In particular, the amount of shift in threshold voltage (ΔVth) of the transistor between before and after a GBT test is an important indicator for examining reliability. The smaller the shift in the threshold voltage (ΔVth) between before and after a GBT test is, the higher the reliability of the transistor is.

The GBT tests in this example were performed under the conditions where the gate voltage (VG) was ±30 V; the drain voltage (VD) and the source voltage (VS) were 0 V (COMMON); the stress temperature was 60° C.; the time for stress application was one hour; and two kinds of measurement environments, a dark environment and a photo environment (irradiation with light having approximately 10000 lx with a white LED), were employed. In other words, the source electrode and the drain electrode of the transistor were set at the same potential, and a potential different from that of the source and drain electrodes was applied to the gate electrode for a certain time (one hour, here). A case where the potential applied to the gate electrode is higher than that of the source and drain electrodes is called positive stress, and a case where the potential applied to the gate electrode is lower than that of the source and drain electrodes is called negative stress. Therefore, in combination with the measurement environments, the GBT stress test was performed under four stress conditions: dark positive stress, dark negative stress, photo positive stress, and photo negative stress.

FIG. **39** shows the GBT test results of Samples B1, C1, and C2. In FIG. **39**, the horizontal axis shows the name of the sample and the vertical axis represents the amount of change in the threshold voltage (ΔVth) of the transistor.

The results in FIG. **39** show that the amount of change in the threshold voltage (ΔVth) in the GBT stress test is small in Samples C1 and C2 of one embodiment of the present invention. In particular, under the conditions of the GBT stress test with light irradiation (photo positive stress and photo negative stress), the amount of change in the threshold voltage (ΔVth) in Samples C1 and C2 is smaller than that in Sample B1, which is a comparative example.

Accordingly, the transistors of Samples C1 and C2 of this example have small variation in electrical characteristics and high reliability.

The structure described above in this example can be combined with any of the structures described in the other embodiments and examples as appropriate.

This application is based on Japanese Patent Application serial no. 2014-039151 filed with Japan Patent Office on Feb. 28, 2014, the entire contents of which are hereby incorporated by reference.

What is claimed is:

1. A semiconductor device comprising:
a transistor comprising:
　a gate electrode;
　a first insulating film over the gate electrode;
　a second insulating film over the first insulating film;
　an oxide semiconductor film over the second insulating film;
　a source electrode electrically connected to the oxide semiconductor film; and
　a drain electrode electrically connected to the oxide semiconductor film;
a third insulating film over the transistor;
a fourth insulating film over the third insulating film; and
a fifth insulating film on and in direct contact with the fourth insulating film,
wherein the fourth insulating film comprises oxygen,
wherein the fifth insulating film comprises nitrogen,
wherein the third insulating film has a spin density corresponding to a signal that appears at g=2.001 lower than or equal to 3×10^{17} spins/cm³ by electron spin resonance measurement,
wherein an amount of oxygen molecules released from the fourth insulating film is greater than or equal to 1×10^{19}/cm³ when measured by thermal desorption spectroscopy, and
wherein an amount of oxygen molecules released from the fifth insulating film is less than 1×10^{19}/cm³ when measured by the thermal desorption spectroscopy.

2. The semiconductor device according to claim **1**, wherein the fourth insulating film further comprises nitrogen and silicon.

3. The semiconductor device according to claim **1**, wherein the fifth insulating film further comprises silicon.

4. The semiconductor device according to claim **1**, wherein the first insulating film comprises nitrogen and silicon.

5. The semiconductor device according to claim **1**,
wherein the oxide semiconductor film comprises O, In, Zn, and M and
wherein the M is one selected from the group consisting of Ti, Ga, Y, Zr, La, Ce, Nd, and Hf.

6. The semiconductor device according to claim **1**,
wherein the oxide semiconductor film includes a crystal part, and
wherein the crystal part includes a portion whose c-axis is a parallel to a normal vector of a surface where the oxide semiconductor film is formed.

7. A display device comprising:
the semiconductor device according to claim **1**; and
a display element.

8. An electronic appliance comprising:
the semiconductor device according to claim **1**; and
an operation key or a battery.

9. A semiconductor device comprising:
a transistor comprising:
　a gate electrode;
　a first insulating film over the gate electrode;
　a second insulating film over the first insulating film;
　an oxide semiconductor film over the second insulating film;
　a third insulating film over the oxide semiconductor film;
　a fourth insulating film over the third insulating film;
　a source electrode electrically connected to the oxide semiconductor film; and

a drain electrode electrically connected to the oxide semiconductor film; and

a fifth insulating film on and in direct contact with the fourth insulating film;

wherein the fourth insulating film comprises oxygen,

wherein the fifth insulating film comprises nitrogen,

wherein the third insulating film has a spin density corresponding to a signal that appears at g=2.001 lower than or equal to 3×10^{17} spins/cm^3 by electron spin resonance measurement,

wherein an amount of oxygen molecules released from the third insulating film is greater than or equal to 1×10^{19}/cm^3 when measured by thermal desorption spectroscopy, and

wherein an amount of oxygen molecules released from the fourth insulating film is less than 1×10^{19}/cm^3 when measured by the thermal desorption spectroscopy.

10. The semiconductor device according to claim **9**, wherein the fourth insulating film further comprises nitrogen and silicon.

11. The semiconductor device according to claim **9**, wherein the fifth insulating film further comprises silicon.

12. The semiconductor device according to claim **9**, wherein the first insulating film comprises nitrogen and silicon.

13. The semiconductor device according to claim **9**, wherein the oxide semiconductor film comprises O, In, Zn, and M and

wherein the M is one selected from the group consisting of Ti, Ga, Y, Zr, La, Ce, Nd, and Hf.

14. A display device comprising:

the semiconductor device according to claim **9**; and

a display element.

15. A display module comprising:

the display device according to claim **14**; and

a touch sensor.

16. An electronic appliance comprising:

the semiconductor device according to claim **9**; and

an operation key or a battery.

17. The semiconductor device according to claim **1**,

wherein the fifth insulating film is silicon nitride or aluminum nitride.

18. The semiconductor device according to claim **1**,

wherein the fourth insulating film is silicon nitride oxide or silicon oxide,

wherein the fifth insulating film is silicon nitride or aluminum nitride.

19. The semiconductor device according to claim **9**,

wherein the fifth insulating film is silicon nitride or aluminum nitride.

20. The semiconductor device according to claim **9**,

wherein the fourth insulating film is silicon nitride oxide or silicon oxide,

wherein the fifth insulating film is silicon nitride or aluminum nitride.

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