



US009536847B2

(12) **United States Patent**
Wei et al.

(10) **Patent No.:** **US 9,536,847 B2**
(45) **Date of Patent:** ***Jan. 3, 2017**

(54) **BUMP PAD STRUCTURE**

(71) Applicant: **Taiwan Semiconductor Manufacturing Company, Ltd.**,
Hsin-Chu (TW)

(72) Inventors: **Hsiu-Ping Wei**, Dajia Town (TW);
Hsien-Wei Chen, Hsin-Chu (TW);
Hao-Yi Tsai, Hsin-Chu (TW); **Ying-Ju Chen**,
Hsin-Chu (TW); **Yu-Wen Liu**, Hsin-Chu (TW)

(73) Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.**,
Hsin-Chu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/884,438**

(22) Filed: **Oct. 15, 2015**

(65) **Prior Publication Data**

US 2016/0035684 A1 Feb. 4, 2016

Related U.S. Application Data

(60) Continuation of application No. 14/512,895, filed on Oct. 13, 2014, now Pat. No. 9,171,811, which is a (Continued)

(51) **Int. Cl.**
H01L 23/00 (2006.01)
H01L 21/768 (2006.01)
H01L 23/48 (2006.01)

(52) **U.S. Cl.**
CPC **H01L 24/05** (2013.01); **H01L 21/768** (2013.01); **H01L 21/76877** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 24/05; H01L 24/03; H01L 21/76877; H01L 24/13
See application file for complete search history.

(56) **References Cited**
U.S. PATENT DOCUMENTS

7,196,428 B2 3/2007 Chen
7,622,309 B2 11/2009 Su et al.
(Continued)

FOREIGN PATENT DOCUMENTS

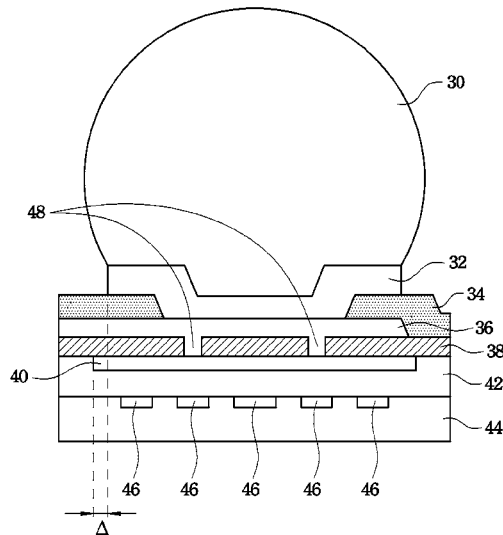
TW 200616125 5/2006
TW 200705632 2/2007

Primary Examiner — Roy Potter
(74) *Attorney, Agent, or Firm* — Slater Matsil, LLP

(57) **ABSTRACT**

An embodiment is a bump bond pad structure that comprises a substrate comprising a top layer, a reinforcement pad disposed on the top layer, an intermediate layer above the top layer, an intermediate connection pad disposed on the intermediate layer, an outer layer above the intermediate layer, and an under bump metal (UBM) connected to the intermediate connection pad through an opening in the outer layer. Further embodiments may comprise a via mechanically coupling the intermediate connection pad to the reinforcement pad. The via may comprise a feature selected from the group consisting of a solid via, a substantially ring-shaped via, or a five by five array of vias. Yet, a further embodiment may comprise a secondary reinforcement pad, and a second via mechanically coupling the reinforcement pad to the secondary reinforcement pad.

20 Claims, 16 Drawing Sheets



Related U.S. Application Data

division of application No. 13/786,045, filed on Mar. 5, 2013, now Pat. No. 8,907,478, which is a continuation of application No. 12/726,449, filed on Mar. 18, 2010, now Pat. No. 8,405,211.

(60) Provisional application No. 61/176,522, filed on May 8, 2009.

(52) **U.S. Cl.**

CPC **H01L 23/48** (2013.01); **H01L 23/481** (2013.01); **H01L 24/03** (2013.01); **H01L 24/13** (2013.01); **H01L 2224/0401** (2013.01); **H01L 2224/0509** (2013.01); **H01L 2224/05012** (2013.01); **H01L 2224/05092** (2013.01); **H01L 2224/05094** (2013.01); **H01L 2224/05095** (2013.01); **H01L 2224/05096** (2013.01); **H01L 2224/05124** (2013.01); **H01L 2224/05147** (2013.01); **H01L 2224/05552** (2013.01); **H01L**

2224/05569 (2013.01); **H01L 2224/05572** (2013.01); **H01L 2224/05599** (2013.01); **H01L 2224/131** (2013.01); **H01L 2924/00013** (2013.01); **H01L 2924/00014** (2013.01); **H01L 2924/01002** (2013.01); **H01L 2924/014** (2013.01); **H01L 2924/01005** (2013.01); **H01L 2924/01006** (2013.01); **H01L 2924/01013** (2013.01); **H01L 2924/01019** (2013.01); **H01L 2924/01029** (2013.01); **H01L 2924/01033** (2013.01); **H01L 2924/01075** (2013.01); **H01L 2924/01078** (2013.01)

(56)

References Cited

U.S. PATENT DOCUMENTS

7,777,333 B2 8/2010 Bachman et al.
8,405,211 B2* 3/2013 Tsai H01L 24/13
257/737

* cited by examiner

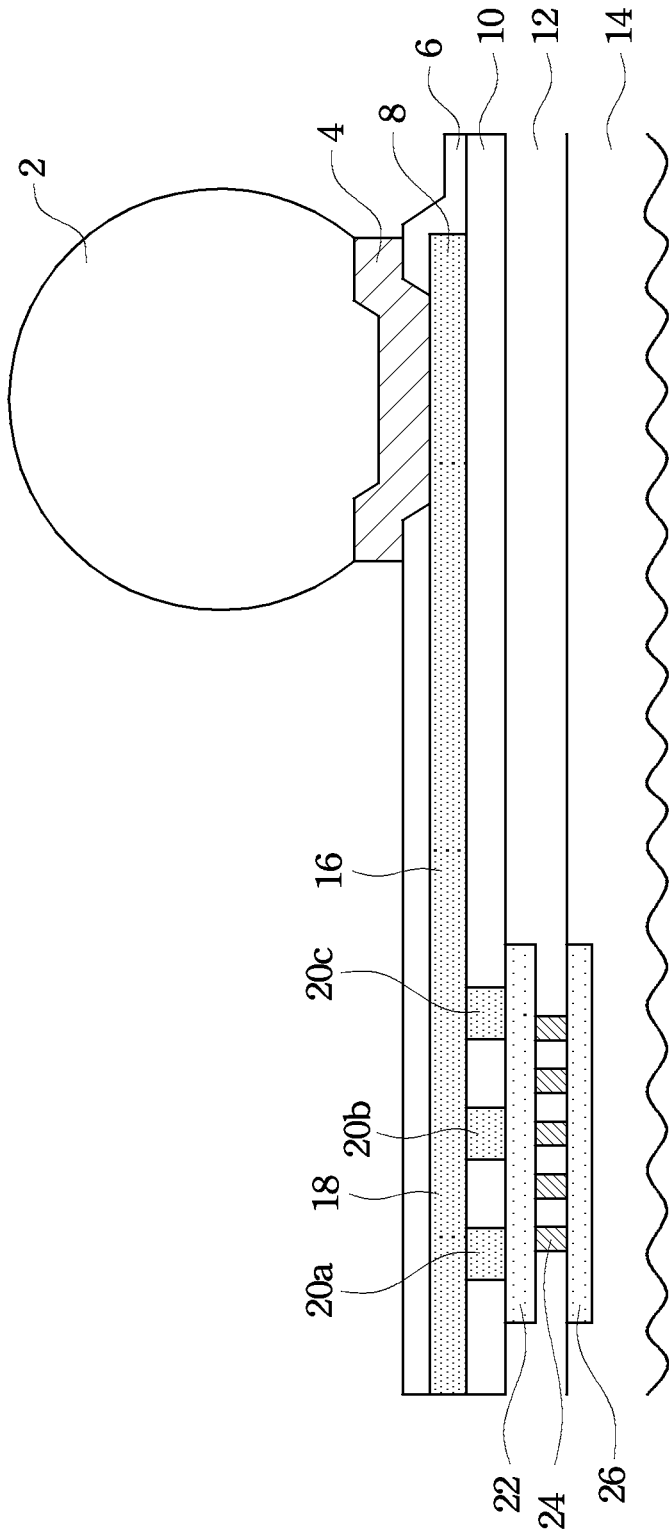


Fig. 1A
(Prior Art)

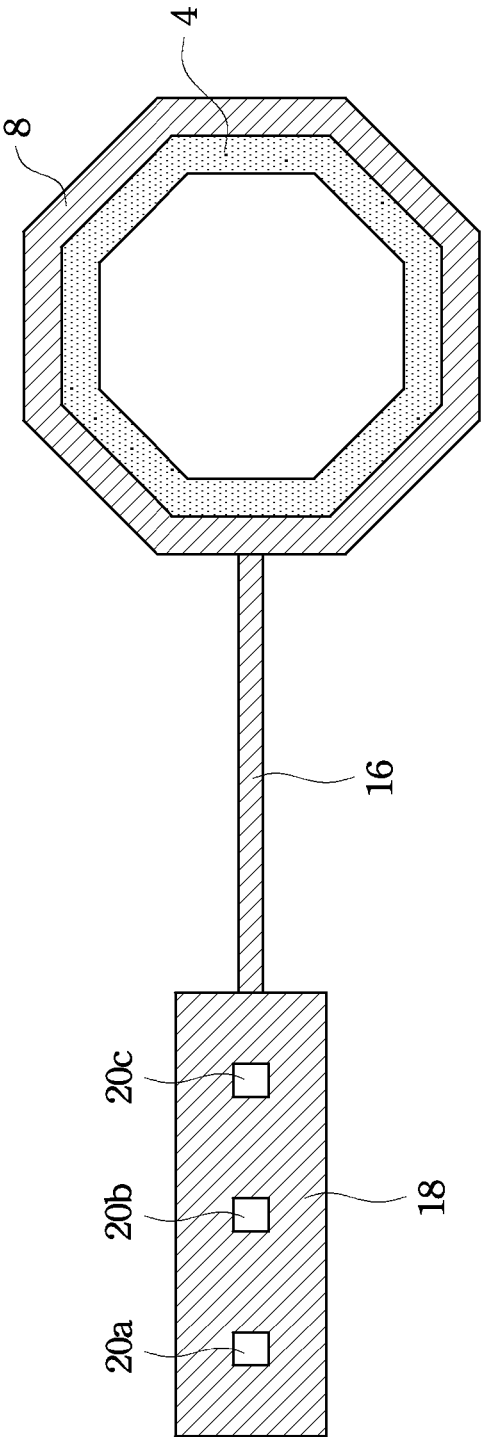


Fig. 1B
(Prior Art)

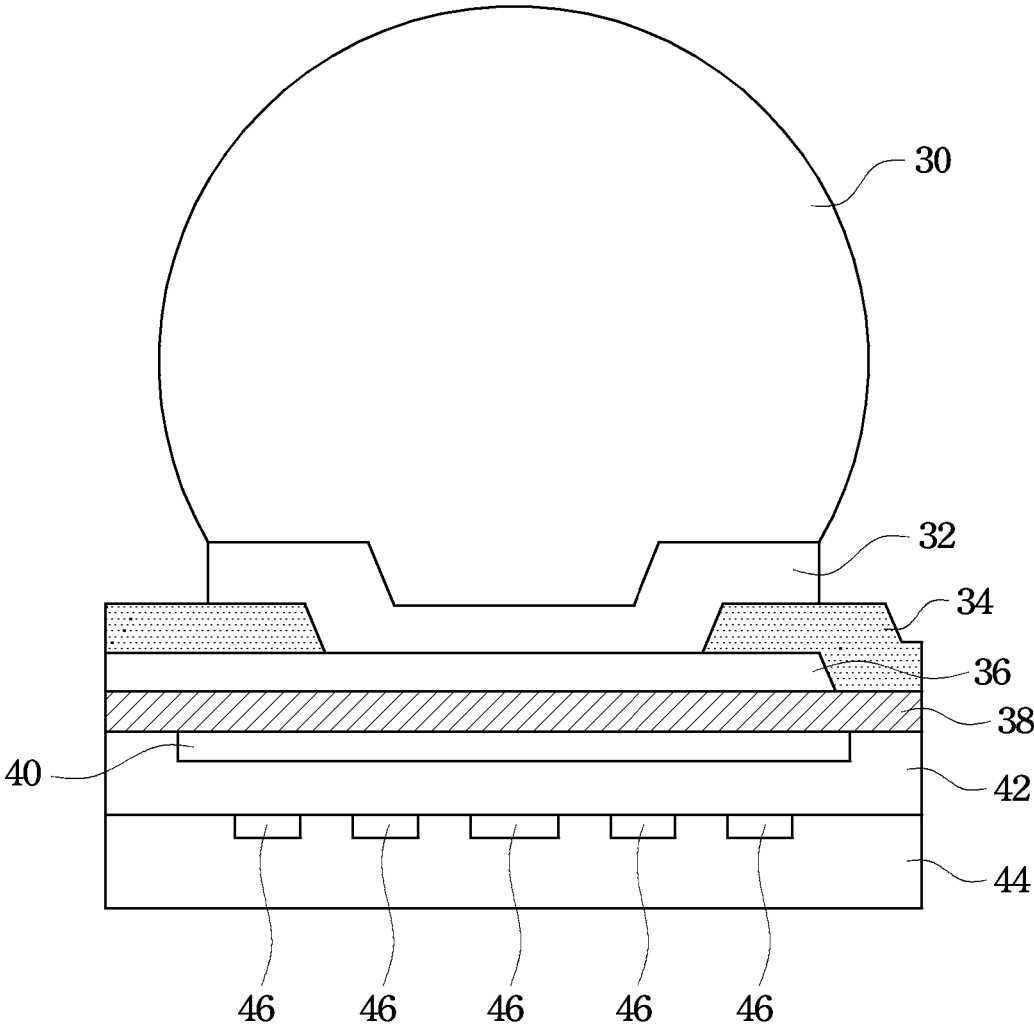


Fig. 2

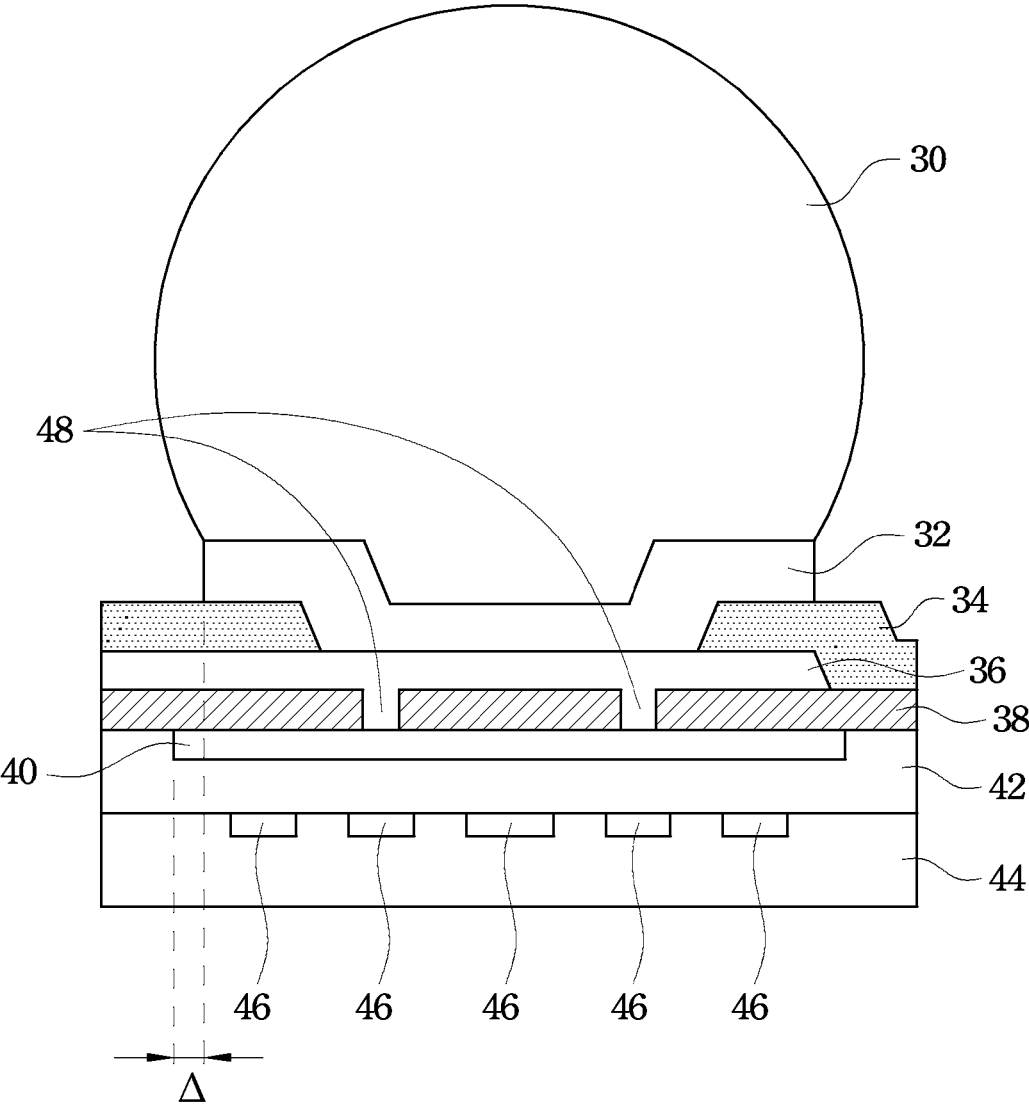


Fig. 3

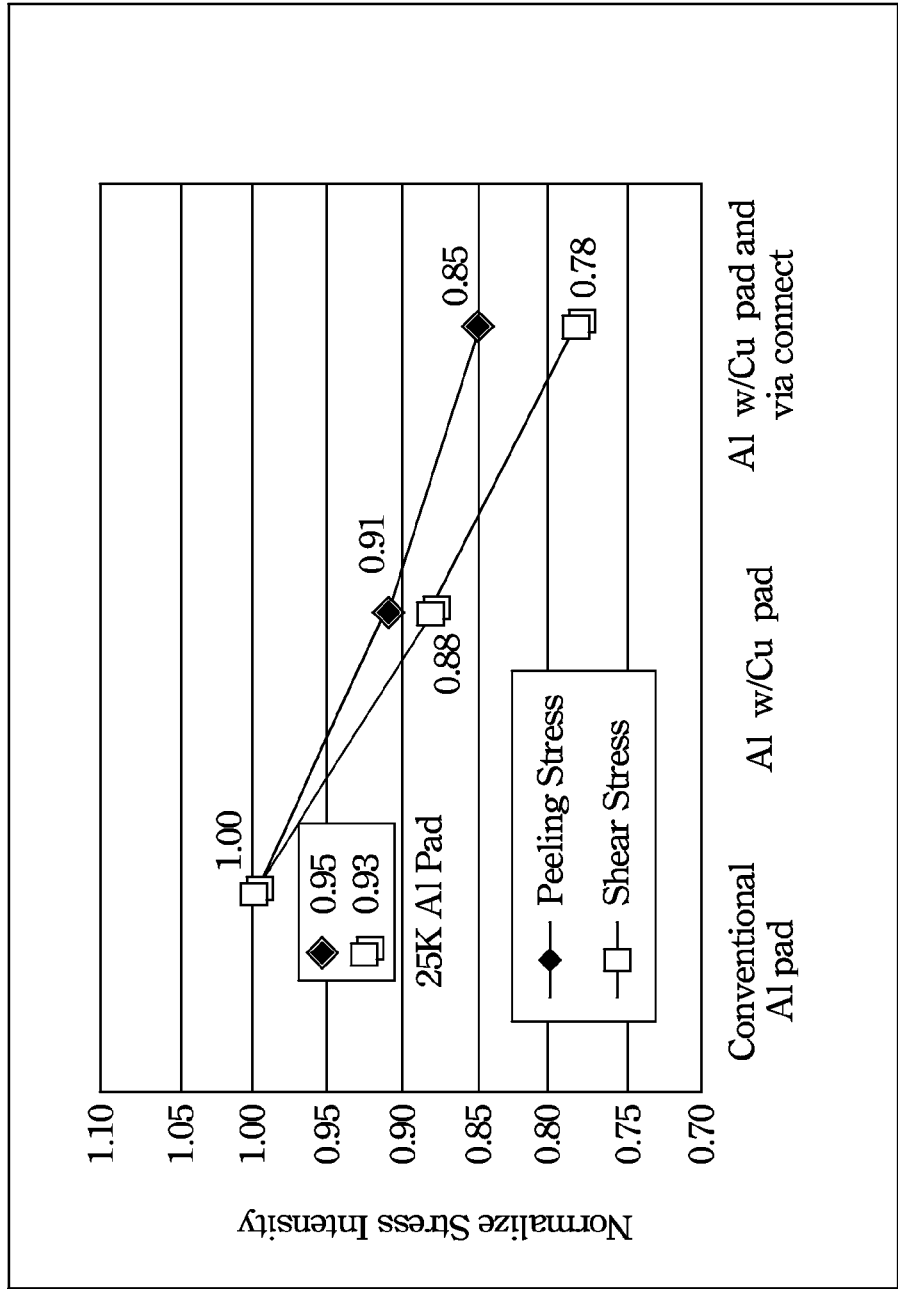


Fig. 4

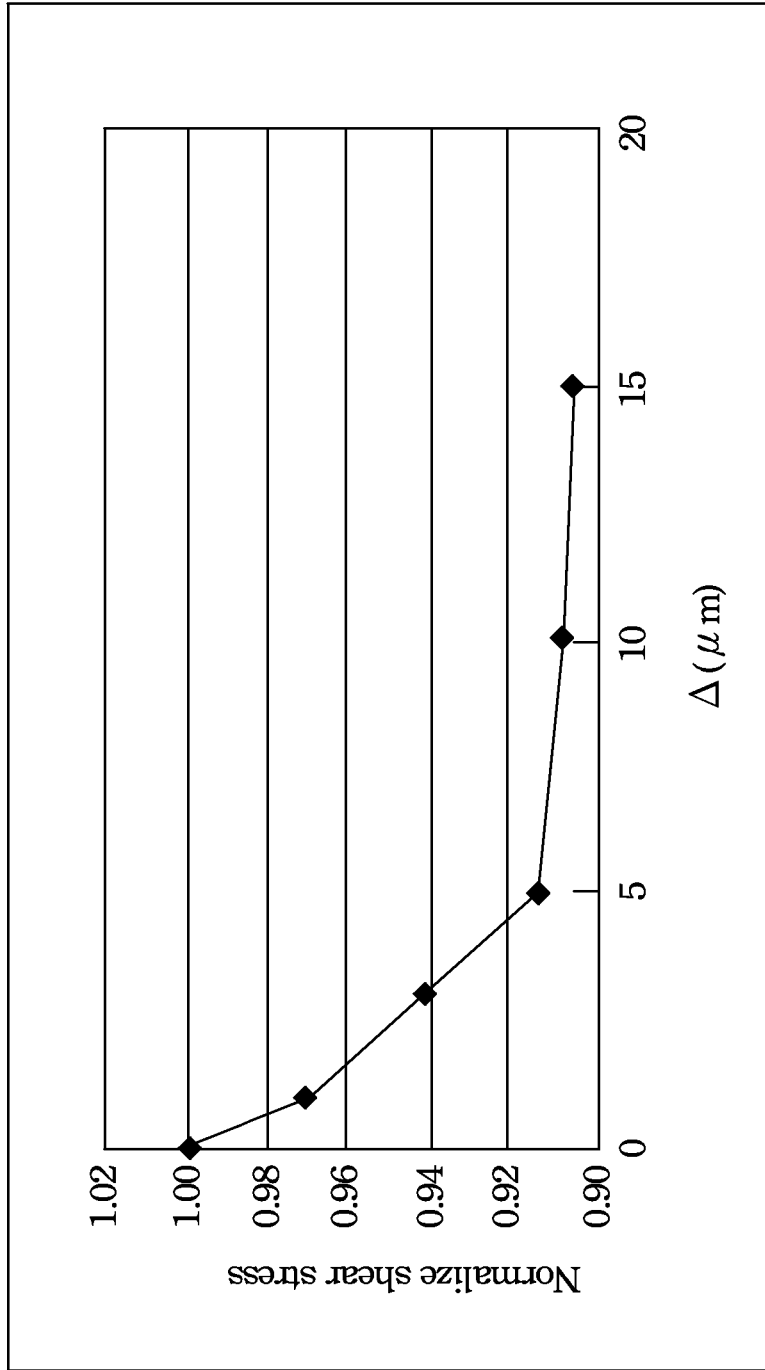


Fig. 5

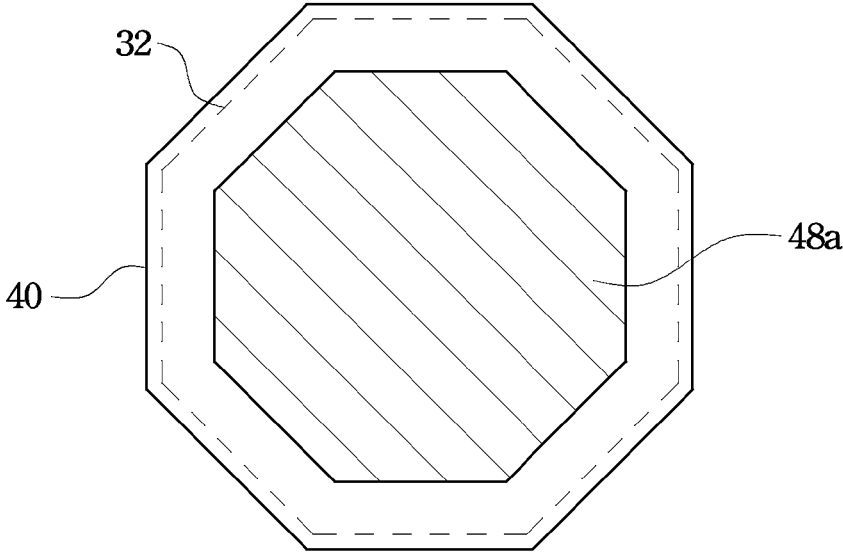


Fig. 6A

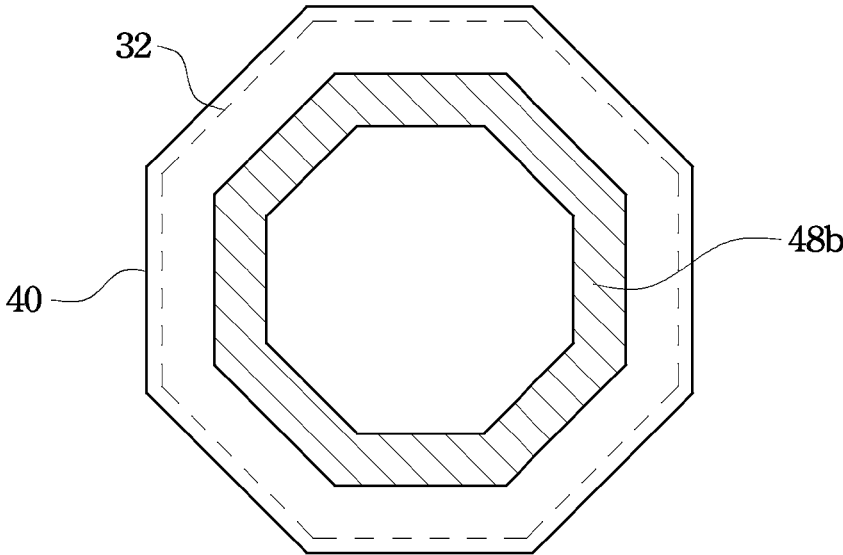


Fig. 6B

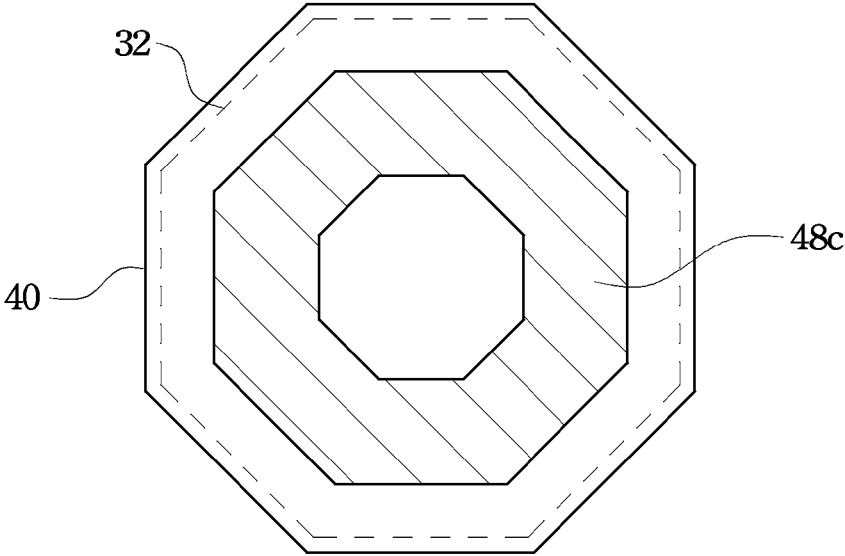


Fig. 6C

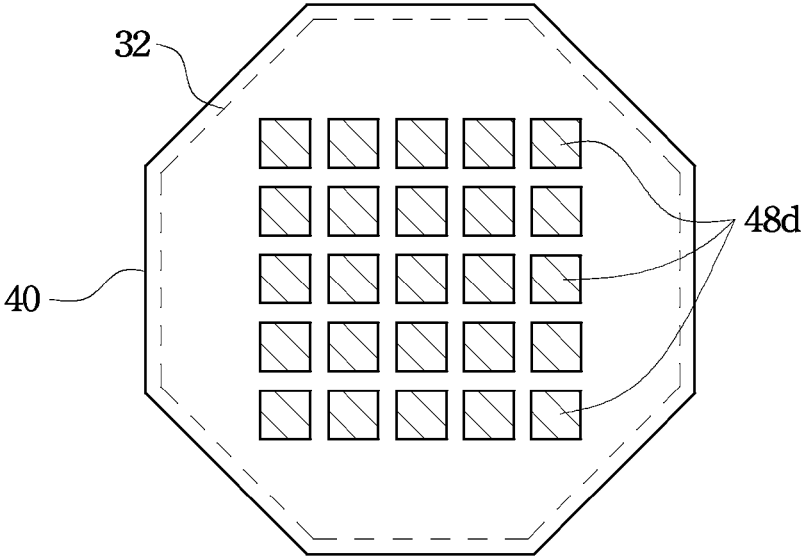


Fig. 6D

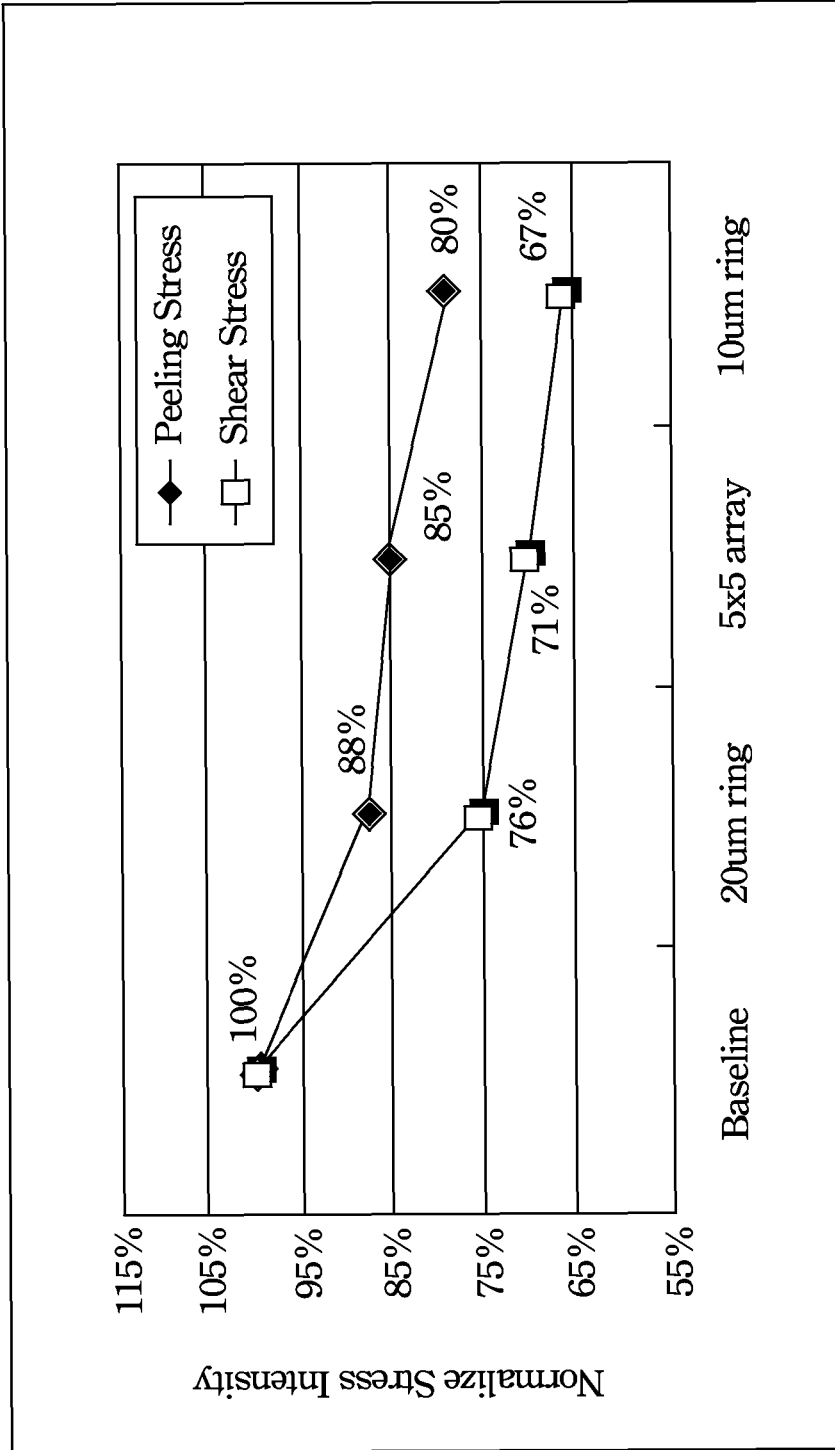


Fig. 7

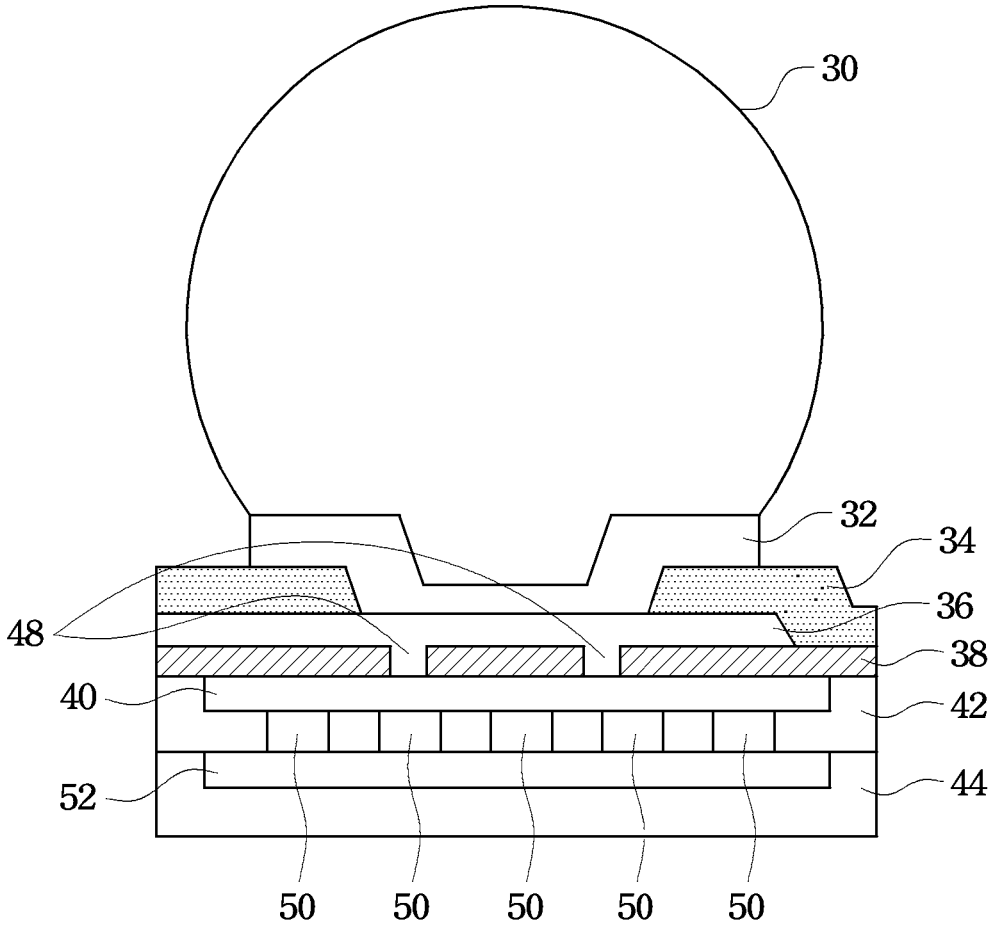


Fig. 8

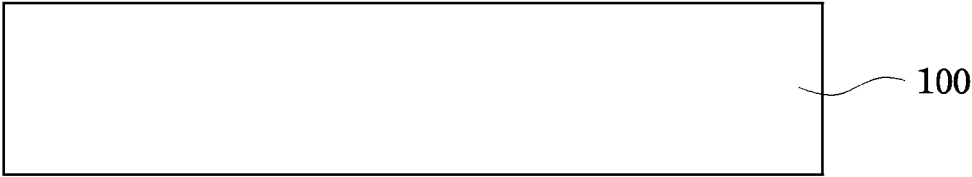


Fig. 9A

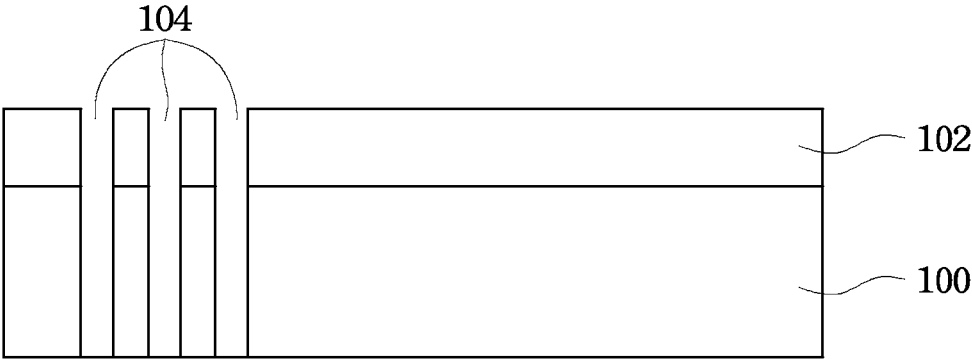


Fig. 9B

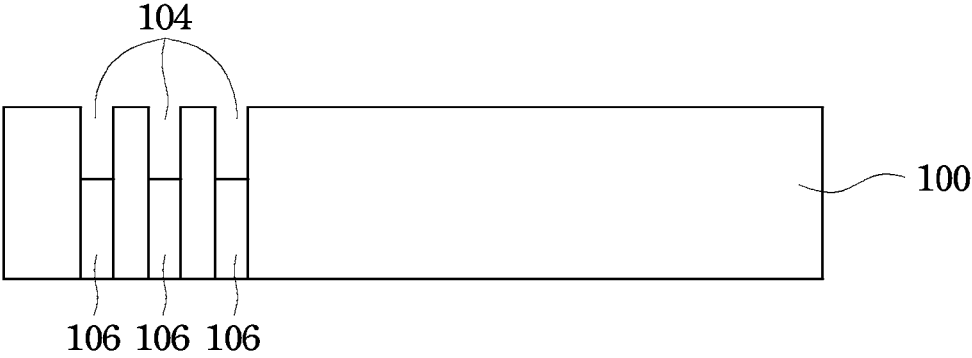


Fig. 9C

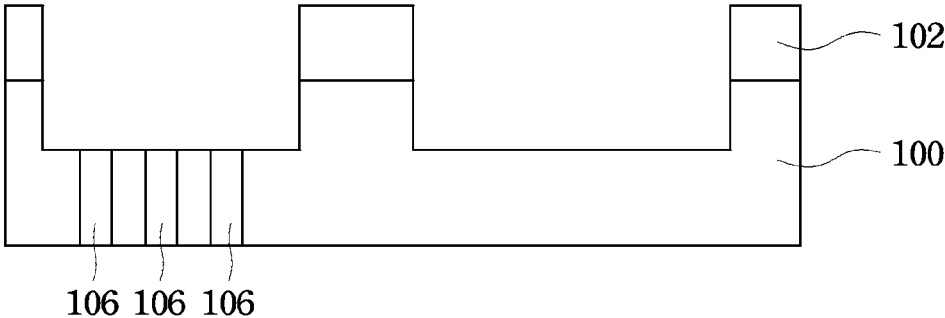


Fig. 9D

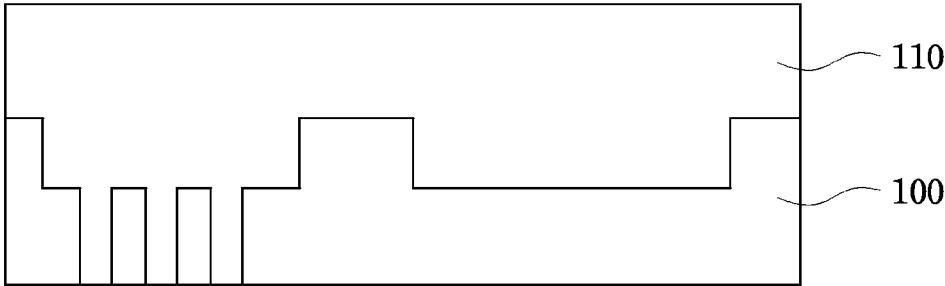


Fig. 9E

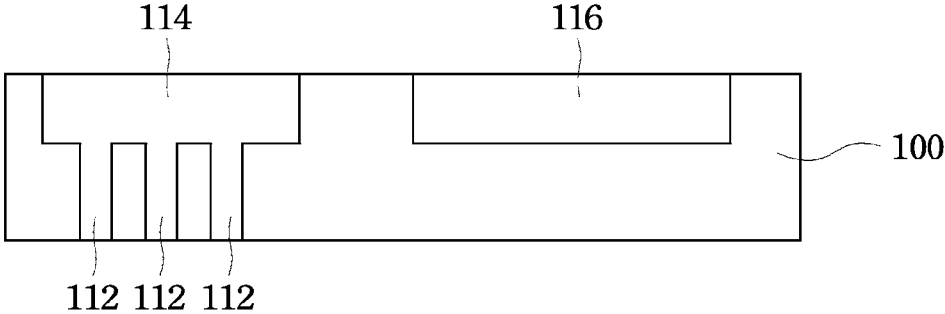


Fig. 9F

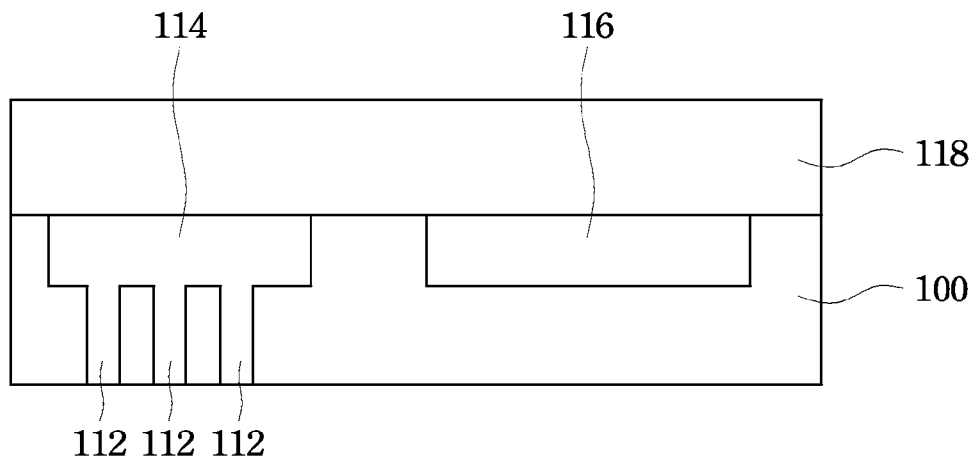


Fig. 9G

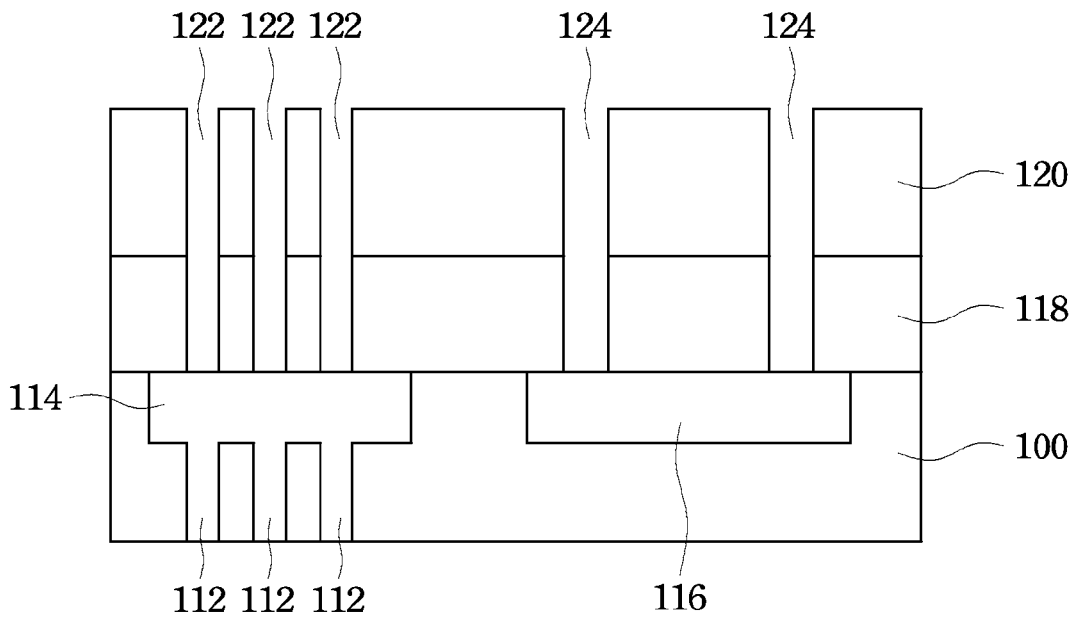


Fig. 9H

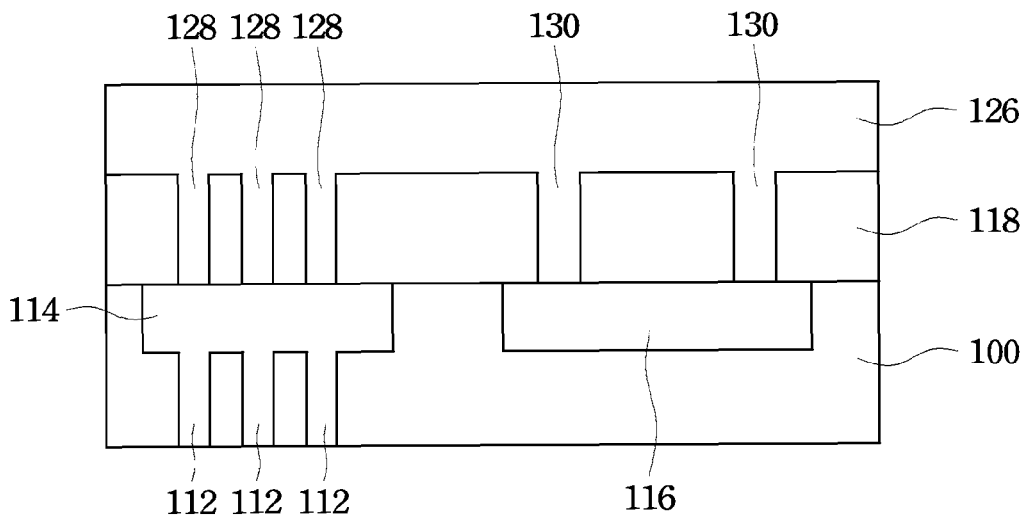


Fig. 9I

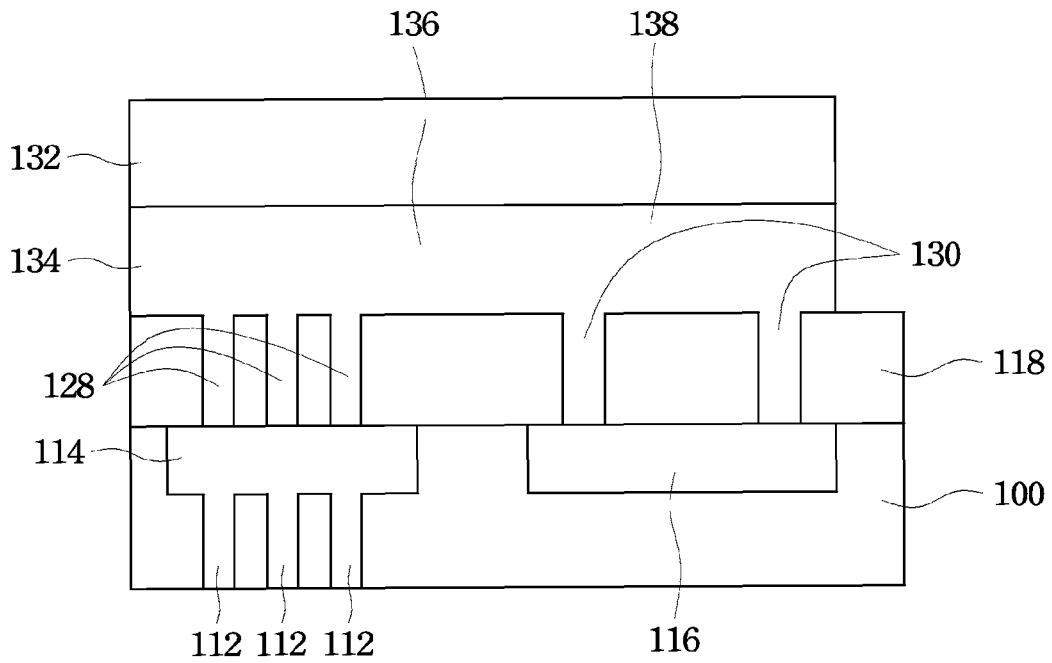


Fig. 9J

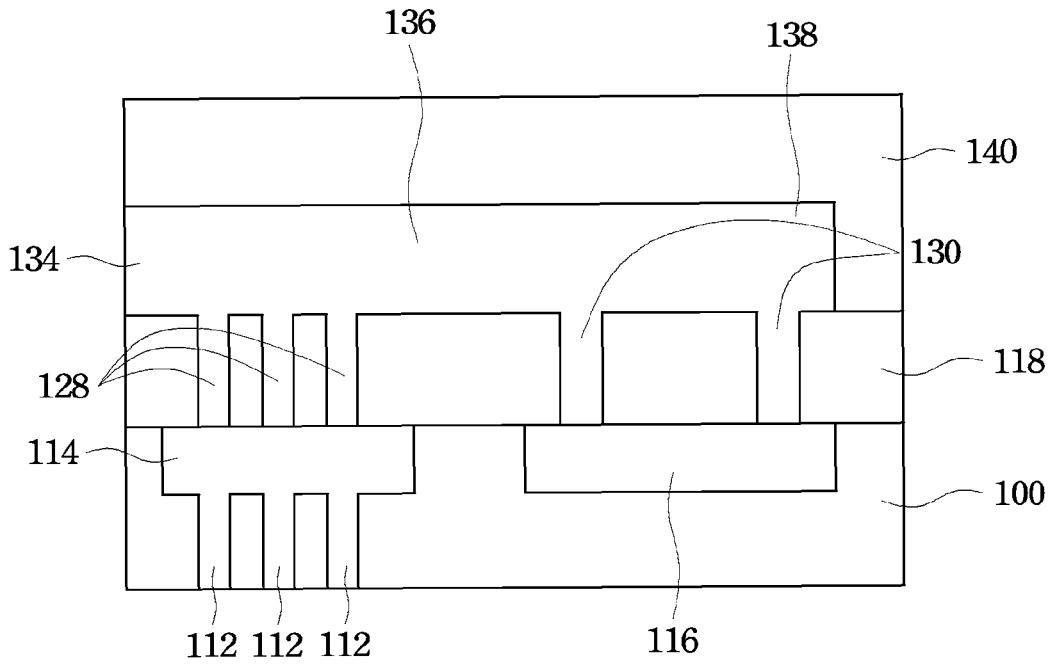


Fig. 9K

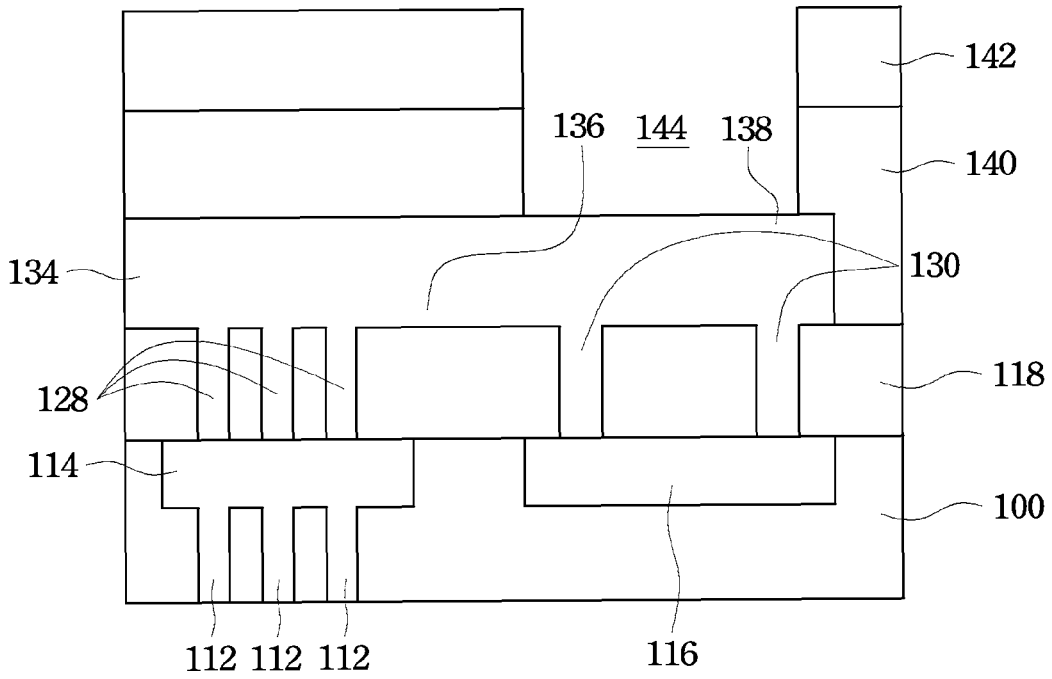


Fig. 9L

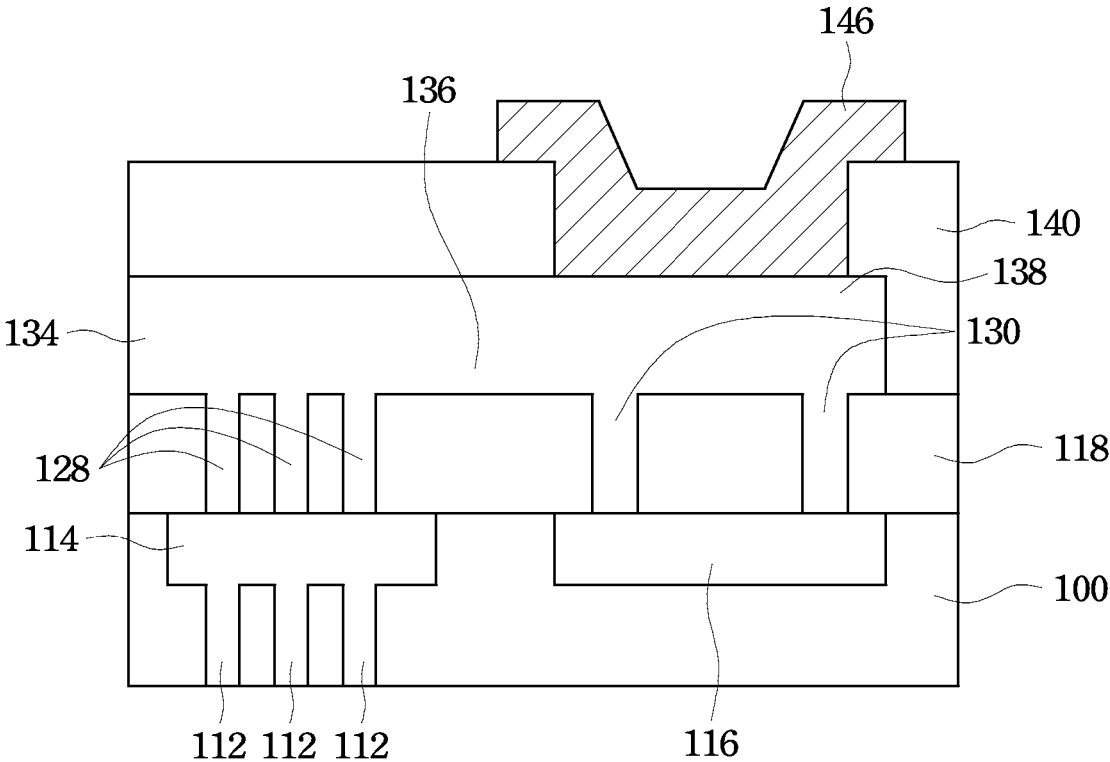


Fig. 9M

1

BUMP PAD STRUCTURE

This application is a continuation of U.S. patent application Ser. No. 14/512,895, filed on Oct. 13, 2014, and entitled “Bump Pad Structure,” which is a divisional of U.S. patent application Ser. No. 13/786,045, filed on Mar. 5, 2013, and entitled “Bump Pad Structure,” which is a continuation of U.S. patent application Ser. No. 12/726,449, filed on Mar. 18, 2010, and entitled “Bump Pad Structure,” which claims the benefit of U.S. Provisional Patent Application Ser. No. 61/176,522, filed on May 8, 2009, and entitled “Bump Pad Structure,” which applications are incorporated herein by reference in their entireties.

TECHNICAL FIELD

The present invention relates generally to a bump pad structure for a semiconductor device, and more particularly to a bump pad structure for a flip chip assembly.

BACKGROUND

A flip chip package includes a downward facing semiconductor chip electrically and mechanically attached to a substrate by solder bumps. Flip chip packages are usually preferred over other conventional packages because of the scalability of flip chip packages that allows their use in smaller applications. But as the sizes of flip chip packages decrease and as the uses of low-k dielectrics increase, problems with the bump pad metal and low-k dielectric may occur from mechanical stresses on the flip chip package.

FIG. 1A is a cross-sectional view of a solder bump pad and a portion of its underlying interconnect structure. A solder bump **2** is physically connected to an under bump metal (UBM) pad **4** that is connected to an aluminum pad **8** through an opening in an outer passivation layer **6** on a semiconductor chip. The aluminum pad **8** rests on an inner passivation layer **10**. The inner passivation layer **10** is above an undoped silicon glass (USG) layer **12** that is on a low-k dielectric layer **14**. The USG layer **12** may comprise multiple individual metal layers that comprise circuitry. An aluminum trace **16** electrically couples the aluminum pad **8** to an aluminum contact **18** in the interconnect structure. Vias **20a**, **20b**, and **20c** through the inner passivation layer **10** connect the aluminum contact **18** to a contact **22**. The contact **22** is coupled to another contact **26** through vias **24**. Additional contacts and vias may comprise the interconnect structure as required by the semiconductor device.

FIG. 1B is a layout of the UBM pad **4**, the aluminum pad **8**, the aluminum trace **16**, the aluminum contact **18**, and vias **20a**, **20b**, and **20c**. The outer octagonal area represents the aluminum pad **8**. The middle octagonal area represents the UBM pad **4**. The inner octagonal area represents the depressed portion of the UBM pad **4**.

The bump pad illustrated in FIGS. 1A and 1B are generally used on flip chip assemblies. Flip chip assemblies are preferred in modern technologies because of their scalability for use in smaller technologies. Yet, as the assembly size decreases, particularly to 22 nm technology, and as low-k dielectric usage becomes more prevalent, particularly when the k value is less than 2.5, the impact of the mechanical stresses arising from the bump pad increases. Stresses on the bump pad, such as peeling or shear forces caused by coefficient of thermal expansion (CTE) mismatch between the semiconductor device and the attached package substrate, can cause mechanical failures of the semiconductor

2

device, such as cracking of the USG, low-k dielectric, or solder bump, due to the weakened bump pad.

Another structure commonly used in flip chip technology is the direct bump on copper (DBOC) structure. In the DBOC structure, the UBM is in direct contact with the copper metal of the top metallization layer. No aluminum pad or inner passivation layer is used in the DBOC structure. Without an aluminum pad or an inner passivation layer to act as a buffer, a DBOC structure generally has less mechanical strength and suffers from the same problems as discussed above. Accordingly, there is a need in the prior art for a bump pad with increased mechanical strength to overcome the deficiencies of the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

FIG. 1A is a cross-sectional view of a conventional bump pad structure and interconnect;

FIG. 1B is a plan view of a conventional bump pad structure and interconnect;

FIG. 2 is a cross-sectional view of a bump pad structure in accordance with an embodiment of the present invention;

FIG. 3 is a cross-sectional view of a bump pad structure in accordance with a further embodiment of the present invention;

FIG. 4 is a chart comparing the stresses at the interface of the undoped silicon glass (USG) layer and the low-k dielectric layer between the conventional structure and embodiments of the present invention;

FIG. 5 is a chart illustrating the effects of the dimensions of the copper pad on the stresses at the interface of the USG layer and the low-k dielectric layer;

FIGS. 6A through 6D are plan views of vias and a bump pad structure in accordance with embodiments of the present invention;

FIG. 7 is a chart illustrating how different via layouts affect the stress at the interface of the USG layer and the low-k dielectric layer;

FIG. 8 is a cross-sectional view of a bump pad structure in accordance with a further embodiment of the present invention; and

FIGS. 9A through 9M illustrate a process to create a bump pad structure in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the present embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

The present invention will be described with respect to embodiments in a specific context, namely a bump pad for a flip chip assembly. The invention may also be applied, however, to any packaging assembly that uses solder bump pads, such as a DBOC structure.

FIG. 2 illustrates a first embodiment of the invention. A solder bump **30** is physically connected to an under bump metal (UBM) pad **32** that is connected to an aluminum pad

36 through an opening in an outer passivation layer 34 on a semiconductor chip. The aluminum pad 36 rests on an inner passivation layer 38. The inner passivation layer 38 is above an undoped silicon glass (USG) layer 42 that is on a low-k dielectric layer 44. A solid copper pad 40 is on the USG layer 42 beneath the aluminum pad 36. The low-k dielectric layer 44 may also comprise circuitry 46. The layers may also comprise any other known configuration or material. For example, the low-k dielectric layer 44 may instead be another USG layer. Further, not shown in FIG. 2, and subsequent FIGS. 3 and 8, is an aluminum trace electrically coupling an interconnect structure to the aluminum pad 36.

FIG. 3 represents another embodiment. FIG. 3 is the same structure as FIG. 2, except the structure in FIG. 3 has vias 48 connecting the aluminum pad 36 to the copper pad 40.

These embodiments reduce the stresses on the USG layer 42 and low-k dielectric layer 44. FIG. 4 is a chart illustrating the reduction of stresses at the interface of the USG layer 42 and the low-k dielectric layer 44. The conventional aluminum pad is represented in FIG. 1A. The aluminum pad with a copper pad is illustrated in FIG. 2, and the aluminum pad with the copper pad and via connection is in FIG. 3. The stresses on the interface are normalized using the conventional pad as a baseline. The aluminum pad and copper pad structure (FIG. 2) had a reduction in peeling stress of nine percent and in shear stress of twelve percent from the normalized baseline. The aluminum pad and copper pad with vias structure (FIG. 3) had a reduction in peeling stress of fifteen percent and in shear stress of twenty-two percent from the baseline.

The reduction in stresses on the interface is generally caused by an increase in the Young's modulus caused by adding the copper pad 40. The Young's modulus of the low-k dielectric is approximately 10 GPa, and the Young's modulus of the USG is approximately 70 GPa. However, the Young's modulus of copper is approximately 128 GPa. Accordingly, inserting copper into the structure will generally increase the Young's modulus of the structure to increase the mechanical strength to better protect the interface.

Not only can the type of structure used affect the stresses on the USG layer 42 and the low-k dielectric layer 44, but also the dimensions of the copper pad 40 can affect the stresses. FIG. 5 is a chart of how the dimensions of the copper pad 40 can affect the stresses. The x-axis of the chart is delta Δ in micrometers. Delta Δ represents the difference of the circumradius of the UBM pad 32 from the circumradius of the copper pad 40 as illustrated in FIG. 3. In FIG. 5, the stresses on the interface of the USG layer 42 and the low-k dielectric layer 44 are normalized to a baseline of when the circumradius of the copper pad 40 equals the circumradius of the UBM pad 32 such that delta Δ is zero. As the chart shows, the stresses decrease as delta Δ increases, yet the decrease in normalized stress is relatively small once delta Δ exceeds five micrometers. Thus, the delta Δ can be said to become saturated at five micrometers. Accordingly, delta Δ is preferred to be about five micrometers although delta could be any possible size.

Further, the layout of the vias 48 used to connect the aluminum pad 36 to the copper pad 40 can affect the stresses on the USG layer 42 and the low-k dielectric layer 44. FIGS. 6A through 6D are exemplary layouts of vias 48. FIG. 6A shows a layout with a solid octagonal via 48a. The dashed line represents the layout of the UBM pad 32, and the solid line is the copper pad 40. Generally, the circumradius of the UBM pad 32 is between approximately seventy-five and one hundred twenty micrometers, and the circumradius of the

aluminum pad 36 (not shown) is approximately four micrometers larger than the circumradius of the UBM pad 32. FIG. 6B shows an octagonal ring via 48b in which the outer circumradius of the via 48b is ten micrometers larger than the inner circumradius of the via 48b. FIG. 6C shows an octagonal ring via 48c in which the outer circumradius of the via 48c is twenty micrometers larger than the inner circumradius of the via 48c. The vias in FIGS. 6B and 6C have surface areas of 28.4 percent and 52.1 percent, respectively, of the surface area of the aluminum pad 36. Further, the difference of the inner and outer circumradii of the octagonal ring vias 48b and 48c may be increased or decreased, such as to five micrometers or to twenty-five micrometers. With a five micrometer difference, the surface area of the via is 14.8 percent of the aluminum pad 36, and with a twenty-five micrometer difference, the surface area of the via is 62.1 percent of the aluminum pad 36. FIG. 6D shows a five by five array of vias 48b.

FIG. 7 is a chart illustrating how these different layouts affect the stress at the interface of the USG layer 42 and the low-k dielectric layer 44. The solid octagonal via 48a in FIG. 6A is used as a baseline, and all other layouts are normalized to it. From the chart, one can see that the normalized stresses decrease from the baseline to the twenty micrometer octagonal ring via 48c in FIG. 6C to the five by five array of vias 48d in FIG. 6D to the ten micrometer octagonal ring via 48b in FIG. 6B.

The disadvantage of the foregoing embodiments is that more area is needed for the copper pad 40 in the USG layer 42 or that an extra metal layer must be included in the USG layer 42. As compared to the bump pad in FIG. 1A, embodiments of the invention would require an area on the top metal layer within the USG layer 42 in which to place the copper pad 40. This may necessitate re-routing circuitry on the top metal layer to clear the area for the copper pad 40. Alternatively, an extra metal layer could be added within the USG layer 42 in which to place the copper pad 40. This would not require re-routing circuitry in an existing semiconductor device design, but would cost more in terms of added processing and materials to add the extra metal layer.

FIG. 8 is another embodiment similar to that illustrated in FIG. 3, except a second copper pad 52 is under the USG layer 42 and on the low-k dielectric layer 44. Vias 50 connect the copper pad 40 to the second copper pad 52. The vias 50 may be one or many individual vias or may be a via in accordance with the layouts of vias in FIGS. 6A through 6D. Further, more copper pads may be added to the structure in FIG. 8. The copper pads may be within the multiple metal layers that comprise the USG layer 42 or may be within the USG layer 42 and the low-k dielectric layer 44. The multiple copper pads may be connected by vias or may not be connected. The addition of the second copper pad 52 further increases the Young's modulus of the structure, thus increasing the overall mechanical strength of the structure.

Other features of embodiments include a thicker aluminum pad 36 and/or aluminum trace, a thicker USG layer 42, or merely having vias 48 through the inner passivation layer 38 without an underlying copper pad. Generally, an aluminum pad 36 is about 1.45 μm thick. Increasing this thickness, for example to 2.5 μm , may increase the mechanical strength of the structure and will protect the USG layer 42 and low-k dielectric layer 44 more. Likewise, increasing the thickness of the USG layer 42 may increase the mechanical strength of the USG layer 42 to increasingly protect the USG layer 42 and the low-k dielectric layer 44. The USG layer 42 may be thickened by increasing the thickness of existing layers within the USG layer 42 or by adding new layers within the

5

USG layer 42. Further, vias 48 through the inner passivation layer 38 alone without an underlying copper pad may increase the mechanical strength of the structure over conventional bump pads.

FIGS. 9A through 9M illustrate a process to build the bump pad structure in FIG. 3 according to another embodiment. In FIG. 9A, the USG layer 100 is formed on a low-k dielectric layer (not shown). In FIG. 9B, a photoresist layer 102 is patterned on the USG layer 100 to expose the USG layer 100 where interconnect via openings 104 are to be etched. Then, the interconnect via openings 104 are etched using known photolithography techniques. In FIG. 9C, the interconnect via openings 104 are then partially filled with plugs 106 and the photoresist layer 102 is removed. In FIG. 9D, another photoresist layer 108 is formed on the USG layer 100 and patterned to expose the USG layer 100 where an interconnect contact is to be formed over the interconnect via openings 104 and where a copper pad is to be formed. The USG layer 100 is then etched to a depth of at least to the top of the plugs 106 using known photolithography techniques.

In FIG. 9E, the photoresist layer 108 and plugs 106 are removed. Next, copper 110 is deposited on the USG layer 100. A diffusion barrier layer may be formed using physical vapor deposition before depositing the copper 110. Also, a copper seed layer may be formed for electroplating after forming the diffusion barrier layer but before depositing the copper 110. In FIG. 9F, any excess copper 110 is removed, such as by chemical mechanical polish. This forms the interconnect vias 112, the interconnect contact 114, and the copper pad 116. Alternatively, conventional dual damascene process steps may be employed to form the interconnect vias 112, the interconnect contact 114, and the copper pad 116.

In FIG. 9G, a first passivation layer 118 is deposited over the USG layer 100. In FIG. 9H, a photoresist layer 120 is formed on the first passivation layer 118. The photoresist layer 120 is patterned to expose portions of the first passivation layer 118 that overlie the interconnect contact 114 and the copper pad 116. The first passivation layer 118 is then etched using known photolithography techniques leaving via openings 122 and 124. In FIG. 9I, the photoresist layer 120 is removed and aluminum 126 is deposited. The aluminum 126 fills the via openings 122 to form aluminum interconnect vias 128 and fills the via openings 124 to form aluminum vias 130. In FIG. 9J, a photoresist layer 132 is formed over the aluminum 126 and patterned to form an aluminum interconnect contact 134, an aluminum trace 136, and an aluminum pad 138. The aluminum 126 is then etched to form those components.

In FIG. 9K, the photoresist layer 132 is removed, and a second passivation layer 140 is deposited on the structure. In FIG. 9L, a photoresist layer 142 is formed on the second passivation layer 140 and patterned to expose a portion of the second passivation layer 140 above the aluminum pad 138. The second passivation layer 140 is then etched down to the aluminum pad 138 leaving a UBM opening 144. In FIG. 9M, the photoresist layer 142 is removed, and a UBM pad 146 is formed in the UBM opening 144 and is connected to the aluminum pad 138.

In accordance with an embodiment of the present invention, a bump bond pad structure comprises a substrate comprising a top layer, a reinforcement pad disposed on the top layer, an intermediate layer above the top layer, an intermediate connection pad disposed on the intermediate layer, an outer layer above the intermediate layer, and an under bump metal (UBM) connected to the intermediate connection pad through an opening in the outer layer.

6

In accordance with another embodiment of the present invention, a bump bond pad structure comprises a copper pad on a top layer of a substrate, an aluminum pad on an inner passivation layer, a via mechanically coupling the copper pad to the aluminum pad, and an UBM mechanically and electrically coupled to the aluminum pad through an opening in an outer passivation layer. The inner passivation layer is on the top layer of the substrate.

In accordance with another embodiment of the present invention, a method for creating a bump bond pad structure, the method comprises forming a reinforcement pad on a top layer of a substrate, forming an intermediate layer on the top layer of the substrate, forming an intermediate connection pad on the intermediate layer and a via through the intermediate layer to couple the intermediate connection pad to the reinforcement pad, forming an outer layer over the substrate, and forming an UBM in an opening of the outer layer to couple the UBM to the intermediate connection pad.

An advantage of an embodiment of the present invention is generally a reduction in stresses on an interface between an USG layer and a low-k dielectric layer caused by an increase in the Young's modulus of the structure. The increase in the Young's modulus generally causes the entire structure to have more mechanical strength.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, although many of the features of the embodiments describe above have comprised either copper or aluminum, each feature may comprise copper instead of the described aluminum, or vice versa. As another example, it will be readily understood by those skilled in the art that the layers described above, i.e. the passivation layers, the USG layer, and the low-k dielectric layer, are not necessarily the layers present in a structure in accordance with the foregoing embodiments.

Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A structure comprising:

- a substrate comprising a first dielectric layer;
- a reinforcement pad disposed in the first dielectric layer, the reinforcement pad having first outer edges configured in a first shape in a first plane parallel to a top surface of the first dielectric layer, the first shape having a first circumradius;
- a second dielectric layer over the first dielectric layer;
- an intermediate connection pad disposed on the second dielectric layer;
- a passivation layer over the second dielectric layer; and
- an under bump metal (UBM) connected to the intermediate connection pad through an opening in the passivation layer, the UBM having second outer edges configured in a second shape in a second plane parallel

to the top surface of the first dielectric layer, the second shape having a second circumradius, the first circumradius exceeding the second circumradius by at least 4.167%.

2. The structure of claim 1 further comprising:
at least one first via in the second dielectric layer, the at least one first via directly connecting the reinforcement pad and the intermediate connection pad.

3. The structure of claim 2, wherein the at least one first via consists of a single solid via in the second dielectric layer between the intermediate connection pad and the reinforcement pad.

4. The structure of claim 2, wherein the at least one first via comprises a substantially ring-shaped via.

5. The structure of claim 2, wherein the at least one first via comprises an array of discrete vias.

6. The structure of claim 1 further comprising:
a secondary reinforcement pad, wherein the substrate further comprises a third dielectric layer under the first dielectric layer, the secondary reinforcement pad being disposed in the third dielectric layer.

7. The structure of claim 6 further comprising:
a first via connected between the intermediate connection pad and the reinforcement pad, the first via being in the second dielectric layer; and
a second via connected between the reinforcement pad and the secondary reinforcement pad, the second via being in the first dielectric layer.

8. The structure of claim 1, wherein the reinforcement pad comprises copper, and wherein the intermediate connection pad comprises aluminum.

9. The structure of claim 1, wherein the first circumradius is at least 5 μm larger than the second circumradius.

10. A structure comprising:
a first metal pad over a substrate;
a first passivation layer over the first metal pad, at least one via in the first passivation layer;
a second metal pad on the first passivation layer, the second metal pad having a different material composition than the first metal pad, the at least one via directly connecting the first metal pad and the second metal pad;
a second passivation layer over the first passivation layer; and
an under bump metal (UBM) connected to the second metal pad through an opening in the second passivation layer.

11. The structure of claim 10, wherein a circumradius of the first metal pad is at least 5 μm larger than a circumradius of the UBM.

12. The structure of claim 10, wherein the first metal pad comprises copper, and wherein the second metal pad comprises aluminum.

13. The structure of claim 10, wherein the at least one via: is a substantially ring-shaped via, is an array of individual vias, or consists of a single solid via between the first metal pad and the second metal pad.

14. A method comprising:
forming a first material in a first recess of a first dielectric layer to form a reinforcement pad, the reinforcement pad having a first circumradius;
forming a second dielectric layer over the first dielectric layer;
forming a second material on the second dielectric layer to form an intermediate connection pad;
forming a passivation layer over the intermediate connection pad;
forming an opening in the passivation layer to the intermediate connection pad; and
forming an under bump metal (UBM) in the opening and partially on the passivation layer, the UBM having a second circumradius, the first circumradius exceeding the second circumradius by at least 4.167%.

15. The method of claim 14, wherein the reinforcement pad comprises first outer edges, the first outer edges forming a first shape in a first plane parallel to a top surface of the first dielectric layer, and the UBM has second outer edges, the second outer edges forming a second shape in a second plane parallel to the top surface of the first dielectric layer, the second shape corresponding to the first shape.

16. The method of claim 14, wherein the first material comprises copper, and the second material comprises aluminum.

17. The method of claim 14 further comprising:
etching a first opening through the second dielectric layer to the reinforcement pad, the second material being formed in the first opening to form a first via.

18. The method of claim 17, wherein the first opening is an array of individual openings or consists of a single opening between the reinforcement pad and the intermediate connection pad.

19. The method of claim 14 further comprising:
etching a third dielectric layer to form a second recess;
forming a third material in the second recess to form a secondary reinforcement pad;
forming the first dielectric layer over the third dielectric layer; and
etching a second opening through the first dielectric layer in the first recess to the secondary reinforcement pad, wherein forming the first material in the first recess further comprising forming the first material in the second opening to form a second via.

20. The method of claim 14, wherein the first circumradius is at least 5 μm larger than the second circumradius.

* * * * *