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(54) MEMORY CELLS AND METHODS OF (2013.01); *H01L 45/1233* (2013.01); *H01L* FORMING MEMORY CELLS (2013.01); *A01L 45/1266* (2013.01); *H01L 45/141* (2013.01);

- (71) Applicant: **Micron Technology, Inc.**, Boise, ID (58) $(1S)$
- (72) Inventors: **Martin Schubert**, Sunnyvale, CA (US); See application file for complete search history. **Shu Qin**, Boise, ID (US); Scott E. Sills, Boise, ID (US); Durai Vishak Nirmal Ramaswamy, Boise, ID (US);
Allen McTeer, Eagle, ID (US); Yongjun Jeff Hu, Boise, ID (US)
- (73) Assignee: Micron Technology, Inc., Boise, ID
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(65) Prior Publication Data

- Related U.S. Application Data - (57) ABSTRACT (60) Division of application No. 14/884,035, filed on Oct.
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- (52) U.S. Cl. CPC *H01L 45/1608* (2013.01); *H01L 45/085* 9 Claims, 3 Drawing Sheets

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Field of Classification Search (US) CPC H01L 45/00; H01L 31/00; H01L

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(74) Attorney, Agent, or Firm — Wells St. John P.S.

15, 2015, now Pat. No. 9,385,317, which is a Some embodiments include a memory cell having a first
continuation of annication No. 14/618,936, filed on electrode, and an intermediate material over and directly continuation of application No. 14/618,936, filed on electrode, and an intermediate material over and directly
Eeh 10, 2015, now Pat No. 9.257.646, which is a against the first electrode. The intermediate material Feb. 10, 2015, now Pat. No. 9,257,646, which is a against the first electrode. The intermediate material division of application No. 14/070.407, filed on Nov includes stabilizing species corresponding to one or both of division of application No. 14/070,407, filed on Nov. includes stabilizing species corresponding to one or both of carbon and boron. The memory cell also has a switching 1, 2013, now Pat. No. 8,981,334. carbon and boron. The memory cell also has a switching material,

an ion reservoir material over the switching material, and a

an ion reservoir material over the switching material, and a Int. Cl. an ion reservoir material over the switching material, and a
H01L 21/20 (2006.01) second electrode over the ion reservoir material. Some HOIL 21/20 (2006.01) second electrode over the ion reservoir material. Some
HOIL 45/00 (2006.01) embodiments include methods of forming memory cells. embodiments include methods of forming memory cells.

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MEMORY CELLS AND METHODS OF FORMING MEMORY CELLS

RELATED PATENT DATA

This patent resulted from a divisional of U.S. patent application Ser. No. 14/884,035, which was filed Oct. 15, 2015, and which is hereby incorporated herein by reference: which resulted from a continuation of U.S. patent applica tion Ser. No. 14/618,936, which was filed Feb. 10, 2015, 10 which issued as U.S. Pat. No. 9,257,646, and which is hereby incorporated herein by reference; which resulted from a divisional of U.S. patent application Ser. No. 14/070, 407, which was filed Nov. 1, 2013, which issued as U.S. Pat. No. 8,981,334, and which is hereby incorporated herein by ¹⁵ reference.

TECHNICAL FIELD

Memory cells and methods of forming memory cells.

BACKGROUND

Integrated memory may be used in computer systems for storing data. Integrated memory is usually fabricated in one 25 or more arrays of individual memory cells. The memory cells are configured to retain or store memory in at least two different selectable states. In a binary system, the states are considered as either a "0" or a "1". In other systems, at least some individual memory cells may be configured to store 30 more than two levels or states of information.

An example memory cell is a programmable metallization cell (PMC). Such may be alternatively referred to as con ductive bridging random access memory (CBRAM), nano bridge memory, or electrolyte memory. APMC may use ion 35 conductive Switching material (for instance, a suitable chal cogenide or any of various suitable oxides) and an ion reservoir material proximate the Switching material. The ion reservoir material and Switching material may be provided between a pair of electrodes. A suitable voltage applied 40 across the electrodes can cause ions to migrate from the ion reservoir material into the switching material to thereby create one or more current-conductive paths through the switching material. An opposite voltage applied across the electrodes essentially reverses the process and thus removes 45 the current-conductive paths. APMC thus comprises a high resistance state (corresponding to the state lacking a con ductive bridge extending through a switching material) and a low resistance state (corresponding to the state having the conductive bridge extending through the switching mate- 50 rial), with such states being reversibly interchangeable with one another.

Although there has been effort toward development of PMCs and other memory cells, there remains a need for improved memory cells.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows an example embodiment PMC in cross sectional side view reversibly transitioning between a low 60 resistance state (LRS) and a high resistance state (HRS).

FIG. 2 shows an example embodiment memory cell in cross-sectional side view.

FIGS. 3-7 show a semiconductor construction in cross sectional side view, and illustrate process stages of an 65 example embodiment process for forming an example embodiment memory cell.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

5 through the electrodes, with higher conductivity electrodes A performance aspect of PMCs can be conductivity being desired. Another performance aspect can be stability of a conductive bridge. Some embodiments provided herein utilize an intermediate material between a switching material and an adjacent electrode to enable characteristics of a memory cell to be tailored to achieve a desired balance between conductive bridge stability and electrode conduc tivity. The intermediate material comprises one or both of carbon and boron. The intermediate material may improve reliability of the memory cell as compared to conventional memory cells, may improve memory state retention, and may improve durability of the memory cell as compared to conventional memory cells. Example embodiments are described with reference to FIGS. 1-7.

Referring to FIG. 1, a PMC (i.e., memory cell) 10 is illustrated in two modes corresponding to a high resistance state (HRS) and a low resistance state (LRS). The two modes are reversibly interchanged with one another through appli cation of electric fields EF⁺ and EF⁻, with EF⁻ being of opposite polarity relative to EF.

The PMC comprises a pair of electrodes 12 and 14, which in some embodiments may be referred to as a first electrode and a second electrode respectively. The PMC also com prises a switching material 16 and an ion reservoir material 18 between the electrodes. Additionally, the PMC comprises an intermediate material 20 between the first electrode 12 and the switching material 16. In the shown embodiment, the intermediate material 20 is directly against an upper surface of the electrode 12, and directly against a lower surface of the switching material 16.

Electrodes 12 and 14 may comprise any suitable conduc tive composition or combination of compositions; and may be the same composition as one another or may be different compositions relative to one another. In some embodiments, the electrodes may comprise, consist essentially of, or consist of one or more of various metals (for example, tungsten, titanium, ruthenium, tantalum, etc.) or metal containing compositions (for instance, metal nitride, metal carbide, metal silicide, etc.). For instance, in some embodiments the electrode 12 may comprise, consist essentially of or consist of a titanium-containing composition (for instance, titanium nitride); and the electrode 14 may com prise, consist essentially of, or consist of tungsten. As other illustrative examples, in some embodiments the electrode 12 may comprise one or more of ruthenium, tungsten and tantalum nitride.

In the shown embodiment, the electrode 12 extends through a dielectric material 13. In some embodiments, such dielectric material may comprise, consist essentially of, or consist of silicon nitride.

The memory cell 10 is shown to have the bottom electrode 12 connected to a conductive line 30 , and to have the top electrode 14 connected to a conductive line 32 (diagrammatically illustrated with a box). The lines 30 and 32 may be sense and/or access lines coupled to the electrodes, and configured for providing appropriate electric fields across the memory cell during read/write operations. In some embodiments, the illustrated memory cell may be one of a plurality of memory cells of a memory array, and the lines 30 and 32 may be part of a circuit configuration utilized to uniquely address each of the memory cells of the array. In some embodiments, a "select device' (not shown) may be provided adjacent the memory cell 10 to reduce undesired current leakage to and/or from the memory cell during utilization of the memory cell in a memory array. Example select devices include diodes, transistors, ovonic threshold switches, etc. The select device may be provided between electrode 12 and the line 30 in some embodiments.

Although the electrodes 12 and 14 are shown to comprise homogeneous compositions, in other embodiments one or both of the electrodes may comprise multiple discrete com positions; and in some embodiments one or both of the electrodes may be a laminate of multiple electrically con- 10 ductive compositions.

The line 30 may be supported by a semiconductor sub strate (not shown). Such substrate may comprise, for example, monocrystalline silicon and/or other suitable semiconductor materials, and may be part of a semiconductor 15 die. Accordingly the memory cell 10 may be part of an integrated circuit Supported by a semiconductor chip.

The switching region 16 may be a solid, gel, or any other suitable phase, and may comprise chalcogenide-type materials (for instance, materials comprising one or more of tellurium, sulfur and selenium), oxides (for instance, aluminum oxide, zirconium oxide, hafnium oxide, tungsten oxide, silicon oxide, etc.) and/or any other suitable materials.

The ion reservoir material 18 contributes ions which ultimately form one or more conductive bridges 25 across 25 the switching material 16. The ion reservoir material may comprise any suitable composition or combination of com positions. In some embodiments, the ion reservoir material may comprise one or more of aluminum, copper, silver and chalcogen (for instance, tellurium); and may be configured 30 for contributing aluminum cations, copper cations and/or silver cations for formation of one or more conductive bridges. The conductive bridges may have any suitable configuration and may be filaments of conductive particles (for instance ions or ion clusters) in some embodiments. 35

In the shown embodiment, the conductive bridge 25 is diagrammatically illustrated as being entirely absent in the high resistance state (HRS) configuration of the memory cell. In other embodiments, a portion of the conductive cell.

Although the ion reservoir material is shown comprising a single composition, in other embodiments the ion reservoir material may comprise two or more different compositions.
Similarly, although the switching material is shown com-45 prising only a single composition, in other embodiments the Switching material may comprise two or more different compositions.

The intermediate material 20 may stabilize the memory cell. For instance, the intermediate material may stabilize the 50 conductive bridge 25 to improve retention and reliability of the memory cell relative to conventional memory cells lacking the intermediate material. Additionally, or alterna tively, the intermediate material may function as a barrier between the switching material 16 and the electrode 12 to 55 alleviate or preclude migration of chemical constituents from electrode 12 into switching material 16 and/or vice versa (for instance, the barrier may preclude undesired oxygen migration from an aluminum oxide-containing Switching material to a metal-containing electrode). The 60 intermediate material may comprise stabilizing species cor responding to one or both of carbon and boron. In some embodiments, the intermediate material may comprise, con sist essentially of, or consist of one or both of carbon and boron. 65

In some embodiments, the stabilization provided by inter mediate material 20 may improve durability of a memory cell (i.e., may extend the lifetime of the memory cell) as compared to conventional memory cells lacking the inter mediate material 20. For instance, carbon of the intermediate material may form metal carbide when it interacts with metal of electrode 12; and such metal carbide may function, at least in part, as a protective layer proximate the interface of the electrode and the switching material. Similarly, boron of the intermediate material may form a protective metal boride.

The provision of stabilizing species corresponding to carbon and/or boron within the intermediate material 20, rather than dispersing such species throughout electrode 12, may enable conductive properties of electrode 12 to be maintained. Such may improve cell performance as com pared to applications in which carbon and/or boron are dispersed throughout the entirety of the electrode 12.

The conductive bridge 25 is shown to extend to an upper surface of intermediate material 20, and in the illustrated embodiment does not penetrate into or through intermediate material 20. In other embodiments, the conductive bridge may extend at least partially through the intermediate mate rial 20.

The intermediate material 20 may be kept thin so that resistive properties of the intermediate material impact cell performance only marginally, if at all. For instance, in some embodiments the intermediate material may comprise a thickness within a range of from greater than 0 Å to less than or equal to about 50 Å ; and in some embodiments may comprise a thickness within a range of from greater than or equal to about 10 A to less than or equal to about 50 A.

In some embodiments, utilization of the intermediate material 20 may enable conductivity of electrode 12 to be enhanced by enabling relatively exotic materials to be utilized in the electrode 12. Specifically, the barrier proper ties of intermediate material 20 may enable materials to be utilized for electrode 12 that could not be utilized in con ventional memory cells lacking intermediate material 20.

bridge may remain in the HRS configuration of the memory 40 be formed only over electrode 12 and not over dielectric In some embodiments, the intermediate material 20 may material 13. In some embodiments, the intermediate material 20 may be deposited across both of electrode 12 and dielectric material 13, and may have a same composition across the dielectric material as across the electrode. In some embodiments, at least a portion of the intermediate material may be formed by implanting carbon and/or boron into materials 12 and 13. In such embodiments, the intermediate material 20 may comprise a first composition over electrode 12 containing the stabilizing species interspersed with mate rial of electrode 12, and may comprise a second composition over dielectric 13 containing the stabilizing species inter spersed with material of dielectric 13. Accordingly, the intermediate material 20 may comprise two different types of regions 31 and 33 (as shown), which differ in composition relative to one another. For instance, if electrode 12 com prises titanium nitride, the region 33 may comprise boron and/or carbon interspersed with titanium nitride; and if dielectric 13 comprises silicon nitride, the region 31 may comprise boron and/or carbon interspersed with silicon nitride. The composition within region 33 may comprise a total concentration of stabilizing species (i.e. boron and/or carbon) within a range of from about 15 atomic percent to about 100 atomic percent; in some embodiments within a range of from about 90 atomic percent to about 100 atomic percent; and in some embodiments about 100 atomic per cent. The composition within region 31 may comprise a similar total concentration of the stabilizing species.

In some embodiments, the region 33 may comprise a uniform composition of the stabilizing species. In other embodiments, the region 33 may comprise a gradient of the stabilizing species composition as shown in FIG. 2. Spe cifically, FIG. 2 shows a memory cell $10a$ comprising a 5 gradient of stabilizing species concentration (indicated by the arrow 40) within an intermediate material 20a. The illustrated gradient increases in a direction from the first electrode 12 to the switching material 16. In some embodi ments, an upper surface of the intermediate material 20*a* 10 directly against the switching material 16 may comprise a total concentration of Stabilizing species (i.e., carbon and/or boron) of from about 90 atomic percent to about 100 atomic percent, and a bottom surface of the intermediate material directly against the first electrode 12 may comprise a total 15 concentration of the stabilizing species of from about 0 atomic percent to less than or equal to about 10 atomic percent (and in some embodiments to less than or equal to about 5 atomic percent). Similarly, an upper portion of region 31 of the intermediate material may comprise from 20 about 95% to about 100 atomic percent of stabilizing species, and a lower portion may comprise from about zero atomic percent to less or equal to about 10 atomic percent of the stabilizing species, with the stabilizing species in the lower portion being dispersed within a dielectric composi- 25 tion of material 13.

The region 33 of the intermediate material $20a$ may comprise stabilizing species implanted over and within the composition of electrode 12. The gradient of FIG. 2 may enable a thin upper region of the intermediate material to 30 have the stabilizing properties associated with a high con centration of boron and/or carbon, and may enable a remain der of the intermediate material to have higher conductivity associated with an increased concentration of the composiassociated with an increased concentration of the composition of electrode 12. Thus, the gradient of FIG. 2 may enable 35 an intermediate material to be formed having improved conductive properties relative to the homogeneous interme diate material of FIG. 1.

The memory cell $10a$ is illustrated in a high resistance state, and accordingly the conductive bridge 25 (FIG. 1) is 40 not shown.

The memory cells described above may be formed uti lizing any suitable processing. An example method of forming memory cell 10 is described with reference to FIGS. 3-7.

Referring to FIG. 3 , a construction **bu** is shown at a 45 processing stage in which an opening 62 has been formed to extend through dielectric material 13 to an upper surface of the electrically conductive line 30. The opening 62 may be formed with any suitable processing. For instance, a mask (not shown) may be formed over material 13 to define a 50 location of opening 62, the opening may be transferred through material 13 with one or more suitable etches, and then the mask may be removed to leave the shown con struction of FIG. 3. The mask may comprise any suitable mask; including, for example, a photolithographically-pat- 55 terned photoresist mask and/or a mask formed utilizing pitch multiplication methodologies.

Referring to FIG. 4, material 64 is formed within opening 62. The material 64 may comprise any of the compositions discussed above with reference to FIG. 1 as being suitable 60 for electrode 12.

Referring to FIG. 5, material 64 is subjected to planariza tion (for instance, chemical-mechanical polishing) to form a planarized surface 65 extending across materials 13 and 64. Such patterns material 64 into the electrode 12.

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Referring to FIG. 6, intermediate material 20 is formed over materials 13 and 64; with such intermediate material 6

comprising one or both of carbon and boron. The interme diate material may be formed utilizing any suitable processing, including, for example, one or more of atomic layer deposition (ALD), chemical vapor deposition (CVD) and physical vapor deposition (PVD). In some embodiments, at least some of material 20 may be formed utilizing plasma doping (PLAD). Specifically, construction 60 may be pro vided within a plasma and then suitable ions of the stabi lizing species (specifically, carbon and/or boron) are implanted into the construction to form intermediate mate rial 20. Such implant may form a homogeneous material, or may form a non-homogeneous material. In some embodi ments, the implant may form a gradient of the type described above with reference to FIG. 2. If it is desired to have the upper Surface of material 20 having a higher concentration of the stabilizing species than is achieved by the implant, a deposition may be conducted after the implant to form an upper surface of material 20 comprising about 100 atomic percent of the stabilizing species.

In some embodiments, the plasma doping may utilize an energy of from about 30 electron volts (eV) to about 10,000 eV; such as, for example, from about 100 eV to about 500 eV. In some embodiments the plasma doping may utilize a dose of from about 1×10^{13} ions/cm² to about 1×10^{17} ions/ cm²; such as, for example, a dose of about 1×10^{15} ions/cm².
In some embodiments, low energy PLAD may provide desired capabilities of tuning and implant characteristics, particularly in a sub-3 KeV regime.

Referring to FIG. 7, the switching material 16 is formed over and directly against the intermediate material 20, the ion reservoir material 18 is formed over the switching material 16, and the top electrode 14 is formed over the ion reservoir material 18. Accordingly, the memory cell 10 is formed.

The memory cells discussed above may be incorporated into electronic systems. Such electronic systems may be used in, for example, memory modules, device drivers, power modules, communication modems, processor mod ules, and application-specific modules, and may include multilayer, multichip modules. The electronic systems may be any of a broad range of systems, such as, for example, clocks, televisions, cell phones, personal computers, auto mobiles, industrial control systems, aircraft, etc.

Unless specified otherwise, the various materials, sub stances, compositions, etc. described herein may be formed with any suitable methodologies, either now known or yet to be developed, including, for example, atomic layer deposi tion (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), etc.

The terms "dielectric" and "electrically insulative" are both utilized to describe materials having insulative electri cal properties. Both terms are considered synonymous in this disclosure. The utilization of the term "dielectric' in some instances, and the term "electrically insulative' in other instances, is to provide language variation within this disclosure to simplify antecedent basis within the claims that follow, and is not utilized to indicate any significant chemi cal or electrical differences.

The particular orientation of the various embodiments in the drawings is for illustrative purposes only, and the embodiments may be rotated relative to the shown orienta tions in some applications. The description provided herein, and the claims that follow, pertain to any structures that have the described relationships between various features, regard less of whether the structures are in the particular orientation of the drawings, or are rotated relative to such orientation.

The cross-sectional views of the accompanying illustra tions only show features within the planes of the cross sections, and do not show materials behind the planes of the cross-sections in order to simplify the drawings.

When a structure is referred to above as being "on" or 5 "against" another structure, it can be directly on the other structure or intervening structures may also be present. In contrast, when a structure is referred to as being "directly on" or "directly against" another structure, there are no intervening structures present. When a structure is referred to as being "connected" or "coupled" to another structure, it can be directly connected or coupled to the other structure, or intervening structures may be present. In contrast, when a structure is referred to as being "directly connected" or arectly coupled to another structure, there are no inter- 15 vening structures present. 10

In some embodiments, a memory cell comprises a first electrode, and an intermediate material over and directly against the first electrode. The intermediate material comprises stabilizing species corresponding to one or both of carbon and boron. The memory cell also comprises a switching material over and directly against the intermediate material, an ion reservoir material over the switching material, and a second electrode over the ion reservoir material.

In some embodiments, a memory cell comprises a first electrode, and an intermediate material over and directly against the first electrode. The intermediate material com prising stabilizing species corresponding to one or both of carbon and boron. The memory cell also comprises a switching material over and directly against the intermediate 30 material, an ion reservoir material over the switching material, and a second electrode over the ion reservoir material. The intermediate material comprises a gradient of stabilizing species concentration, with said concentration being lowest directly adjacent the first electrode and being highest 35 directly adjacent the switching material. 25

In some embodiments, a method of forming a memory cell comprises forming an intermediate material over and directly against a first electrode, with the intermediate mate rial comprising stabilizing species corresponding to one or 40 both of carbon and boron. A switching material is formed over and directly against the intermediate material. An ion reservoir material is formed over the switching material. A second electrode is formed over the ion reservoir material.

In compliance with the statute, the subject matter dis- 45 closed herein has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the claims are not limited to the specific features shown and described, since the means herein disclosed comprise example embodiments. The 50 claims are thus to be afforded full scope as literally worded, and to be appropriately interpreted in accordance with the doctrine of equivalents.

We claim:

1. A method of forming a memory cell, comprising:

forming a first electrode material within an opening in an electrically insulative material and over the electrically insulative material;

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removing the first electrode material from over the elec trically insulative material with a planarization process; 60 the planarization process forming a first electrode from the first electrode material and forming a planarized surface extending across the first electrode and the electrically insulative material;

- forming an intermediate material across the planarized surface, the intermediate material comprising stabilizing species corresponding to one or both of carbon and boron;
- forming a switching material over and directly against the intermediate material;
- forming an ion reservoir material over the switching material;
- forming a second electrode over the ion reservoir mate rial; and
- wherein the intermediate material comprise a bottom surface directly against the first electrode, and an upper surface above the bottom surface; and wherein the upper Surface comprises a total concentration of said stabilizing species of from about 15 atomic percent to about 100 atomic percent.

2. The method of claim 1 wherein the upper surface comprises a total concentration of said stabilizing species of from about 90 atomic percent to about 100 atomic percent. 3. A method of forming a memory cell, comprising:

- forming a first electrode material within an opening in an electrically insulative material and over the electrically insulative material;
- removing the first electrode material from over the elec trically insulative material with a planarization process; the planarization process forming a first electrode from the first electrode material and forming a planarized surface extending across the first electrode and the electrically insulative material;
- forming an intermediate material along the planarized surface, the intermediate material comprising stabilizing species corresponding to one or both of carbon and boron;
- forming a Switching material over and directly against the intermediate material;
- forming an ion reservoir material over the switching material;
- forming a second electrode over the ion reservoir mate
- rial; and
wherein the intermediate material is formed utilizing plasma doping of the stabilizing species.

4. The method of claim 3 wherein the intermediate material comprises a gradient of stabilizing species concen tration, with said concentration being lowest at a bottom surface of the intermediate material along the planarized surface, and highest at an upper surface of the intermediate material.

5. The method of claim 4 wherein the upper surface of the intermediate material comprises a total concentration of said stabilizing species of from about 15 atomic percent to about 100 atomic percent.
6. The method of claim 4 wherein the upper surface of the

6. The method of claim 4 wherein the upper surface of the intermediate material comprises a total concentration of said stabilizing species of from about 90 atomic percent to about 100 atomic percent.

7. The method of claim 3 wherein the stabilizing species includes carbon.

8. The method of claim 3 wherein the stabilizing species includes boron.

9. The method of claim 3 wherein the stabilizing species includes carbon and boron.

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