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Tzeng et al.

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(54) **DECOUPLING MIM CAPACITOR DESIGNS FOR INTERPOSERS AND METHODS OF MANUFACTURE THEREOF**

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Related U.S. Application Data

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H01L 49/02 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 28/40*** (2013.01)

(58) **Field of Classification Search**
CPC ... H01L 21/20; H01L 23/147; H01L 23/3114; H01L 23/49822; H01L 27/06; H01L 27/0805; H01L 28/40; H01L 28/55; H01L 28/65; H01L 28/91
See application file for complete search history.

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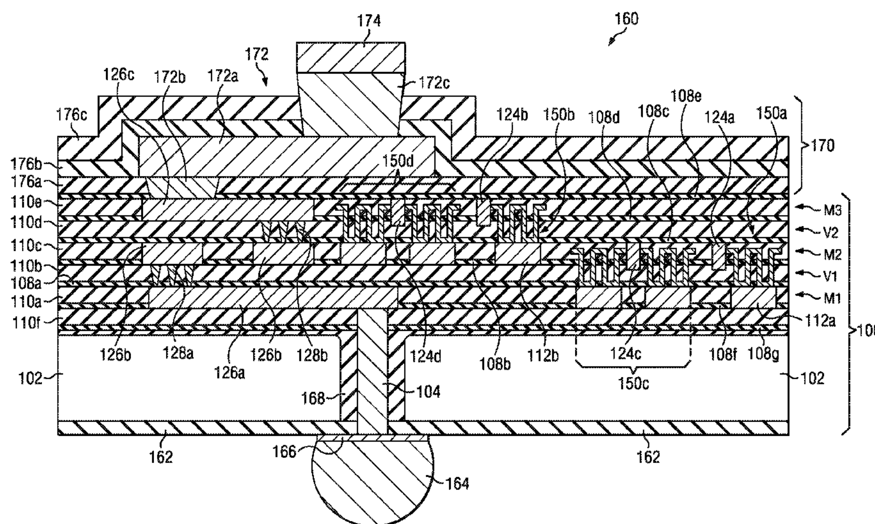
Primary Examiner — Kyoung Lee
(74) *Attorney, Agent, or Firm* — Slater Matsil, LLP

(57) **ABSTRACT**

Decoupling metal-insulator-metal (MIM) capacitor designs for interposers and methods of manufacture thereof are disclosed. In one embodiment, a method of forming a decoupling capacitor includes providing a packaging device, and forming a decoupling MIM capacitor in at least two metallization layers of the packaging device.

20 Claims, 24 Drawing Sheets



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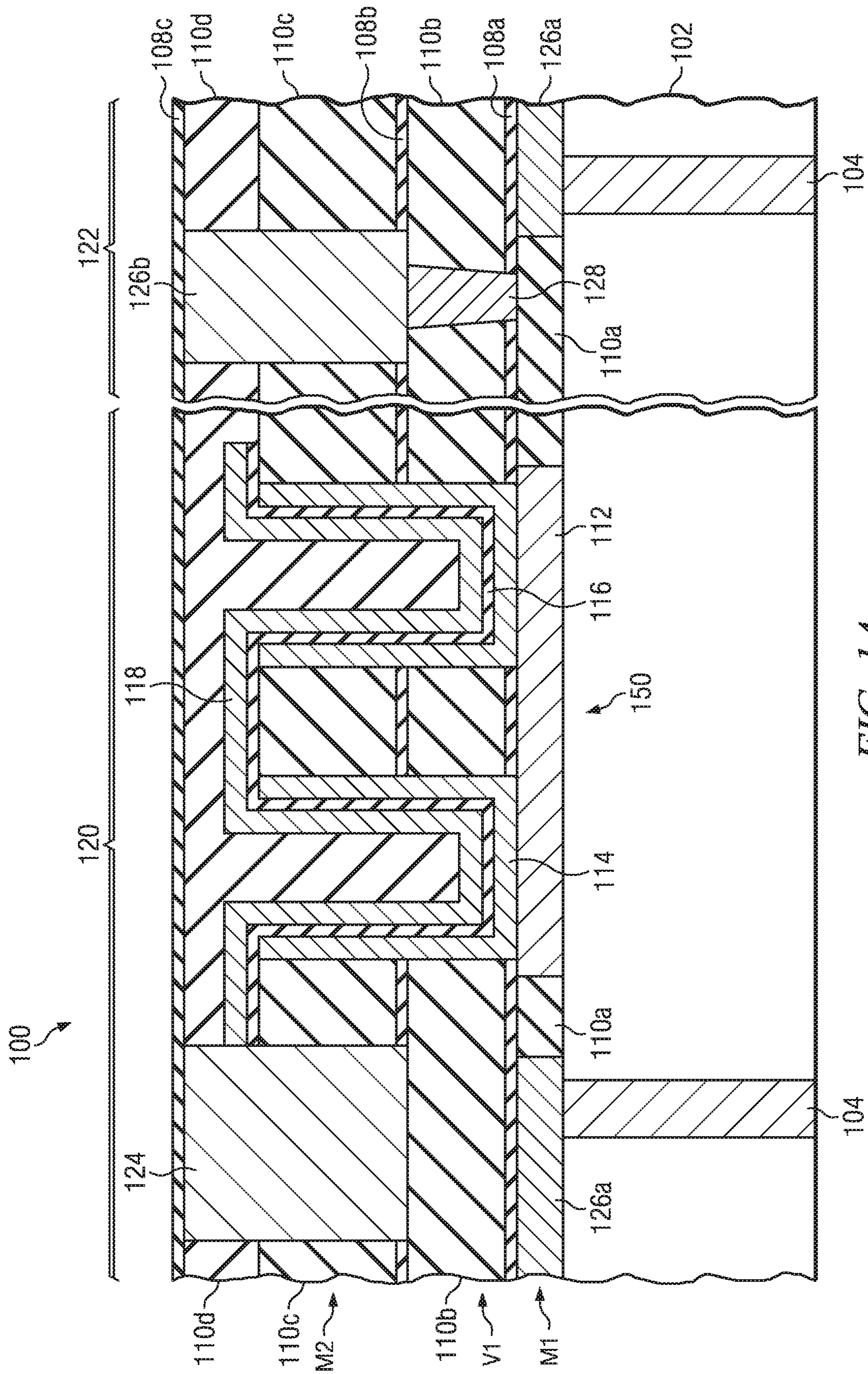

FIG. 1A

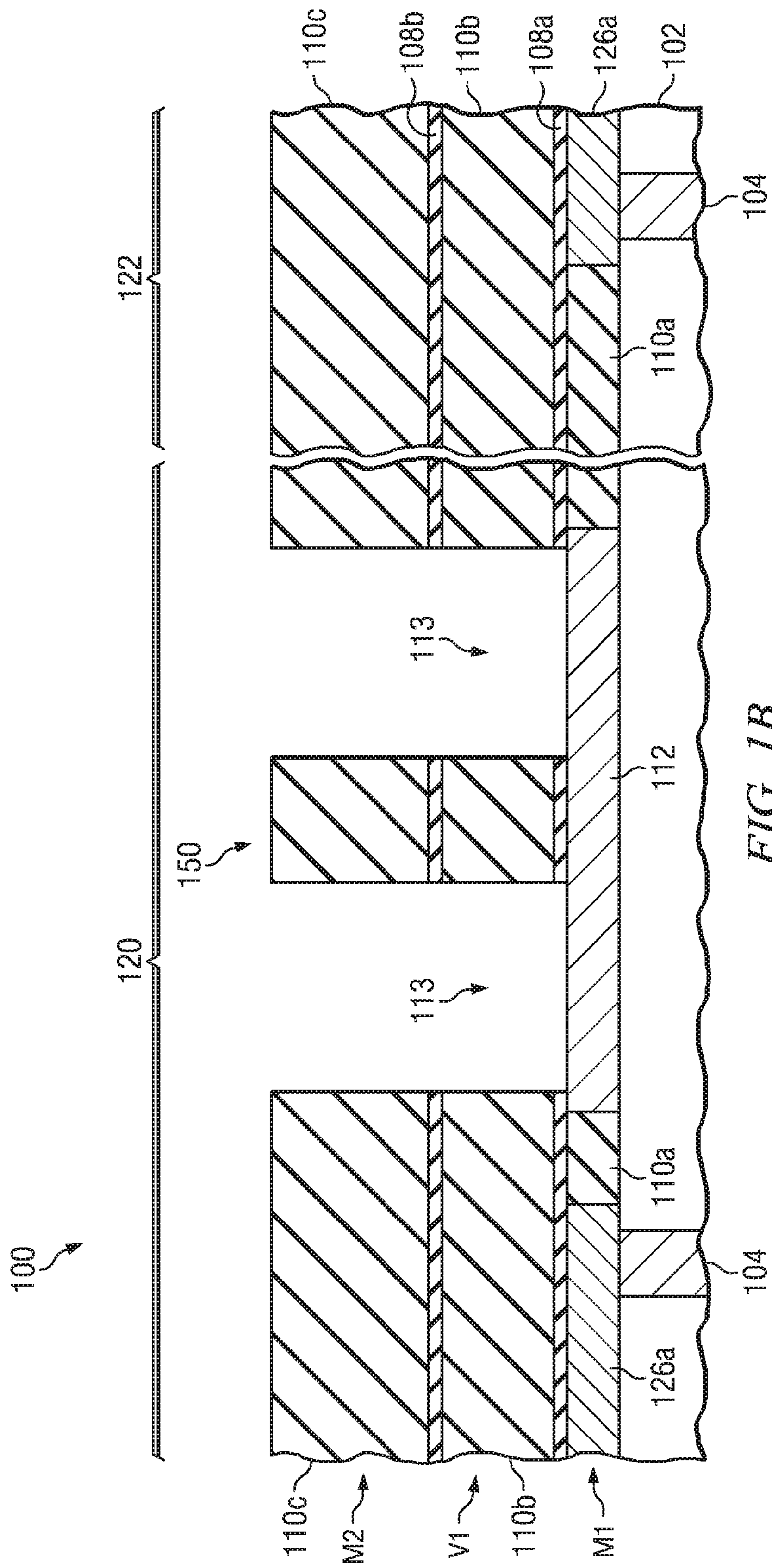

FIG. 1B

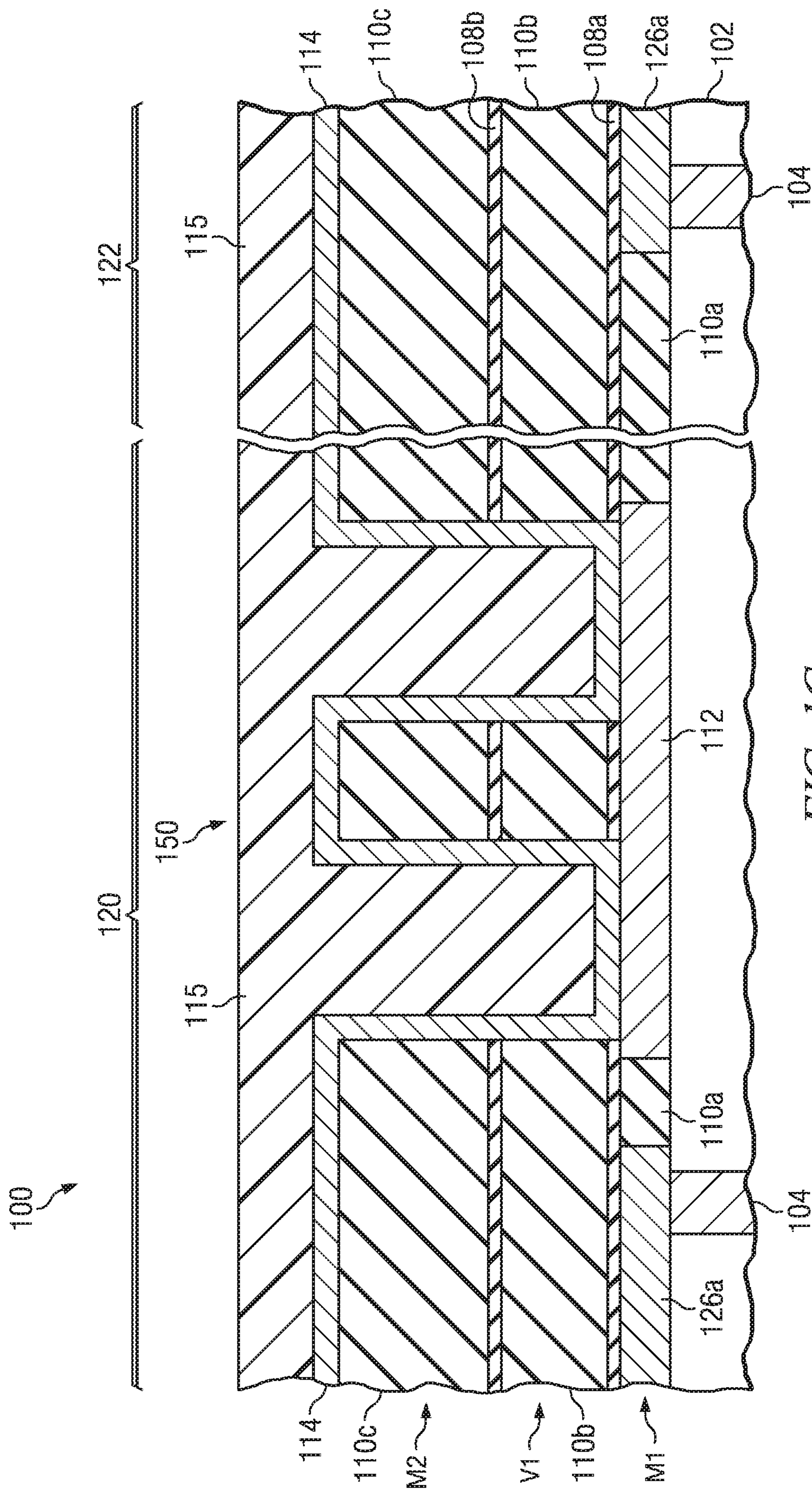

FIG. 1C

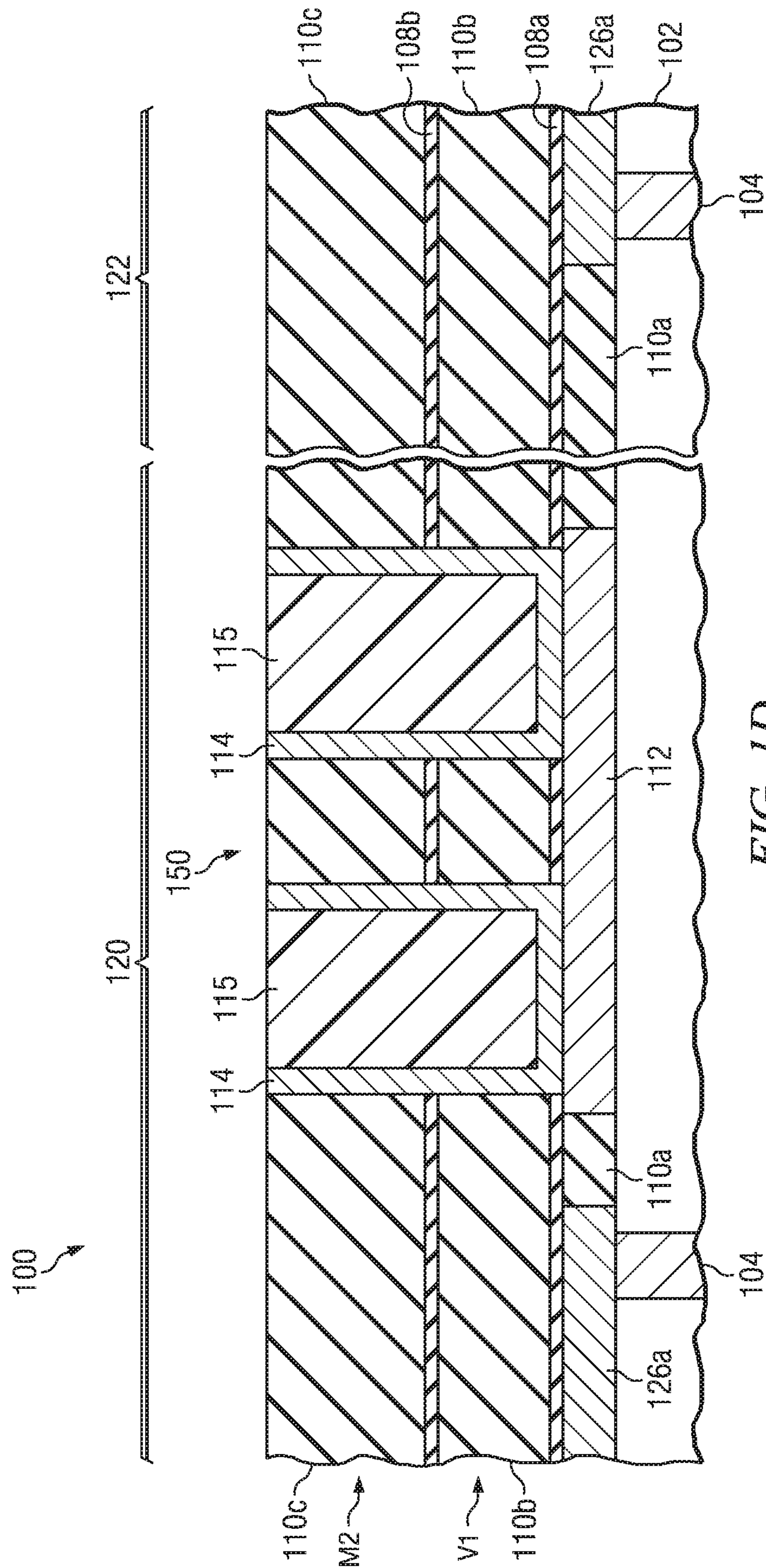

FIG. 1D

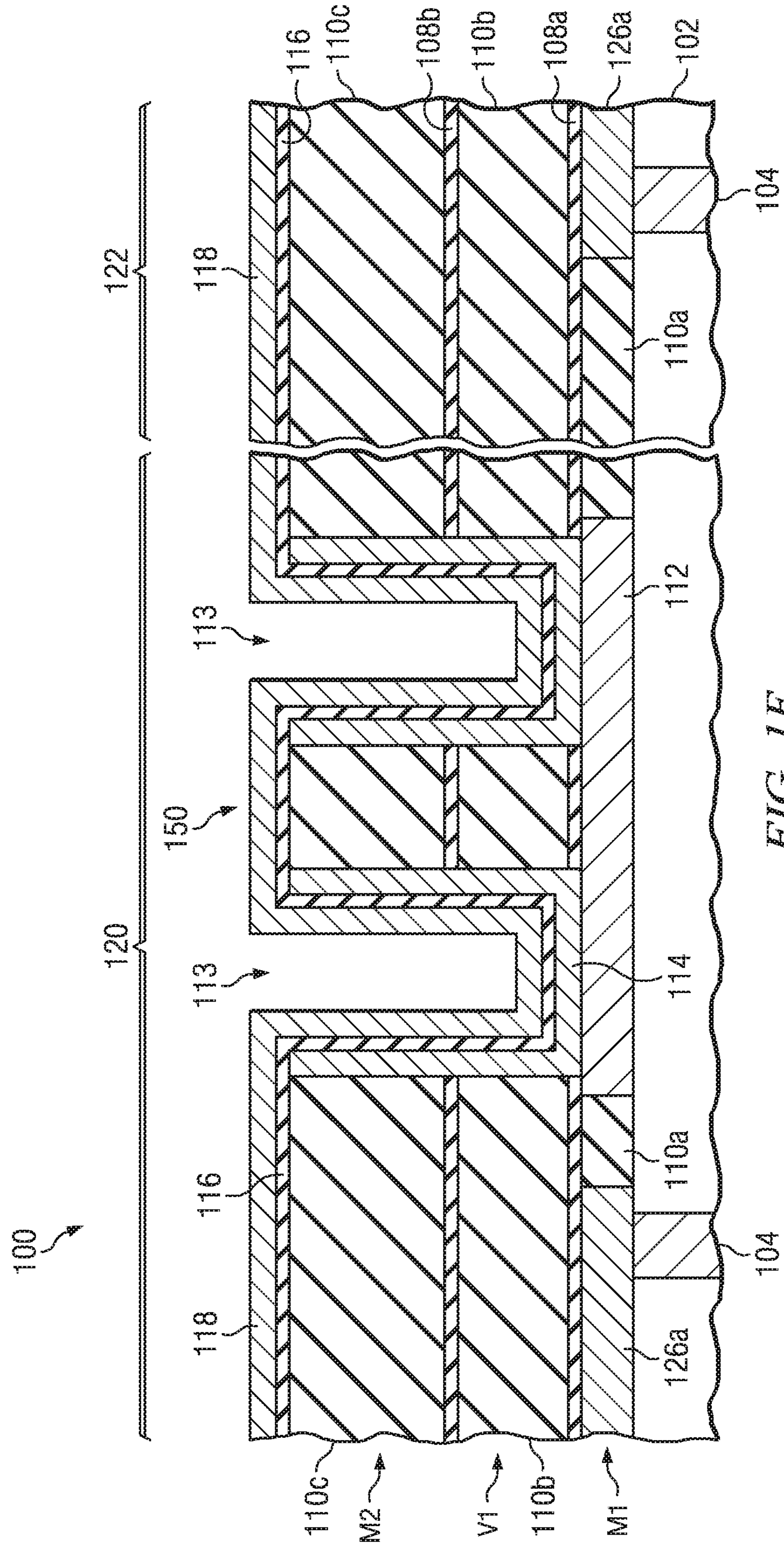

FIG. 1E

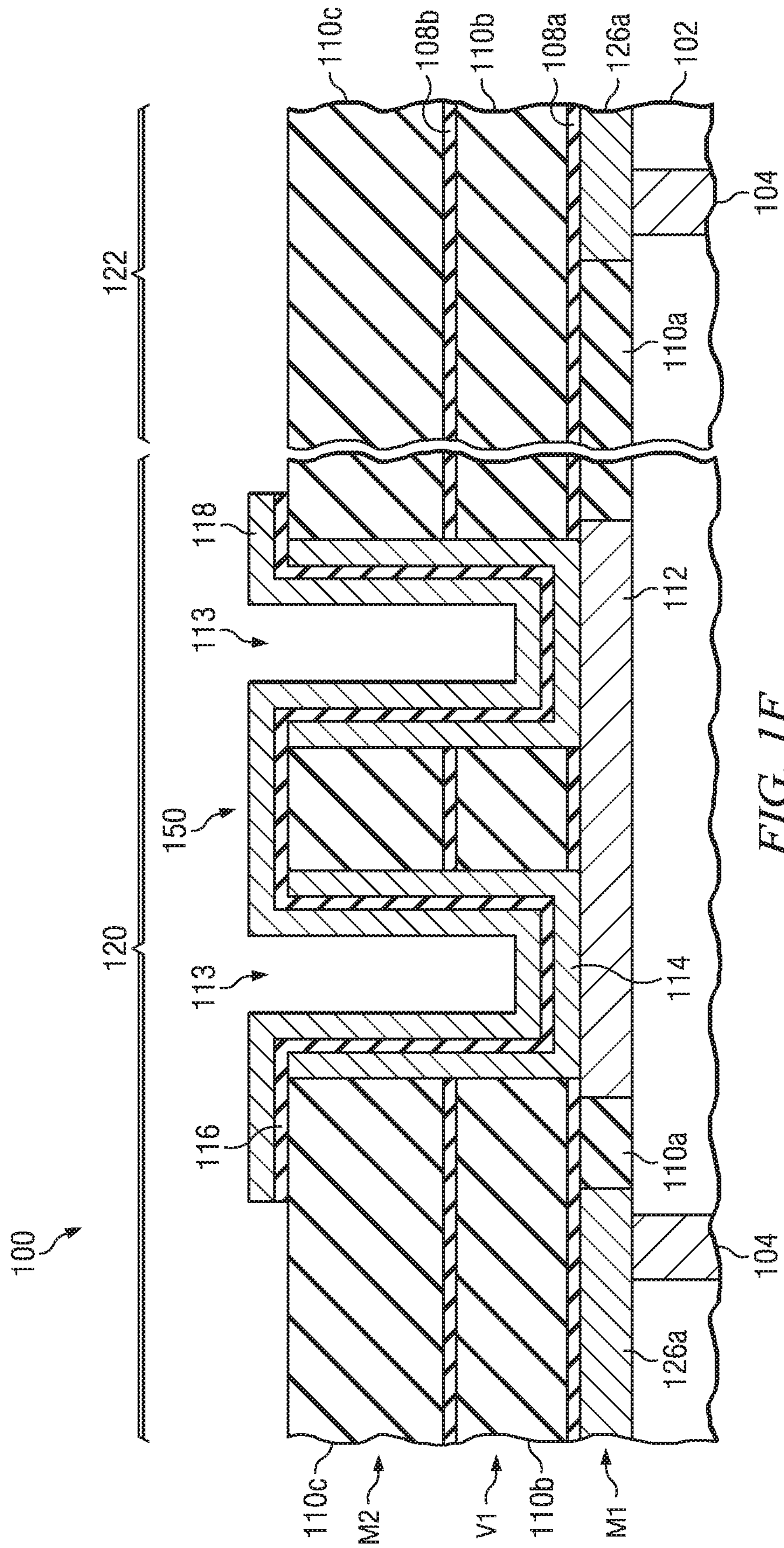

FIG. 1F

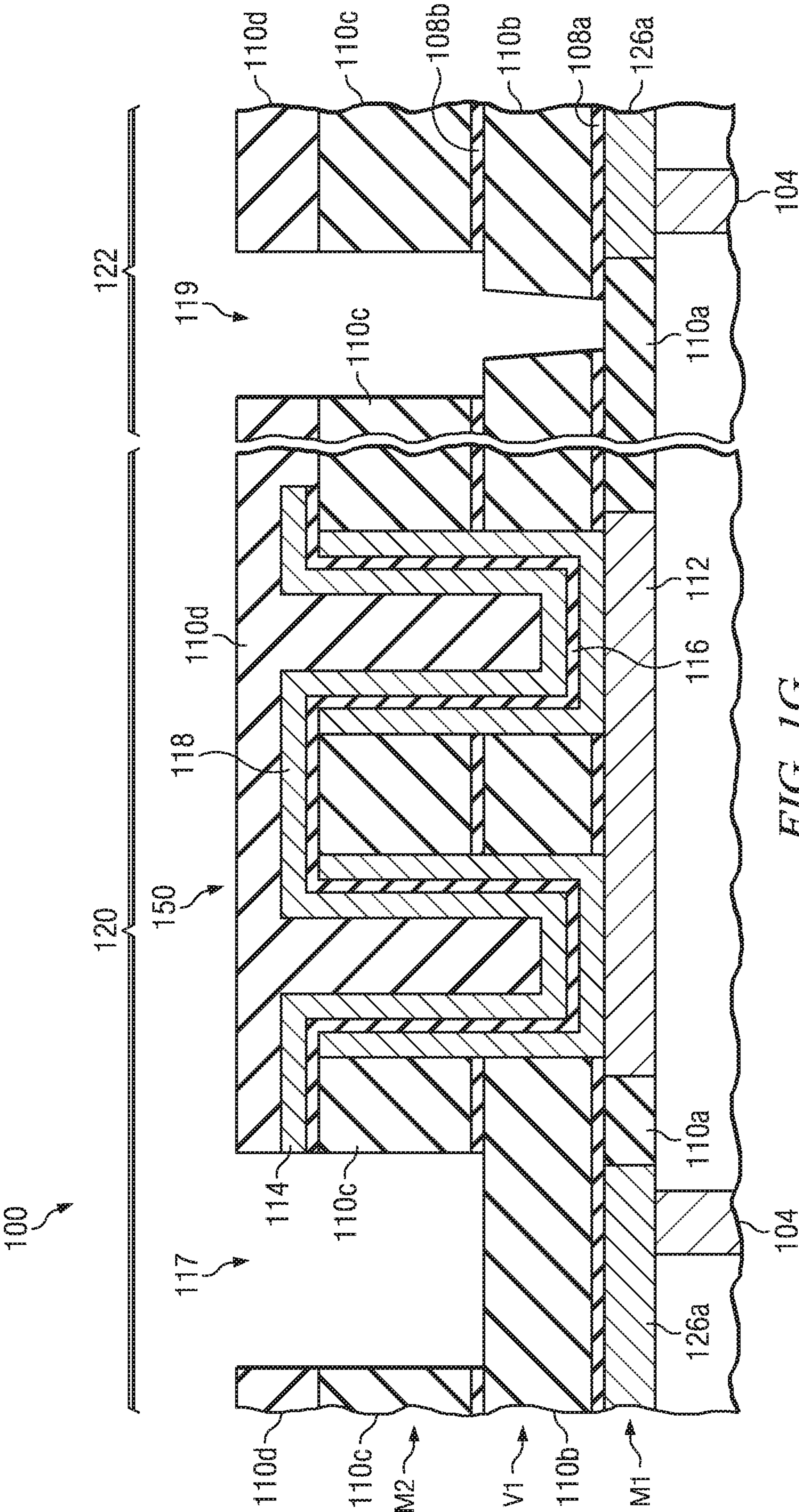

FIG. 1G

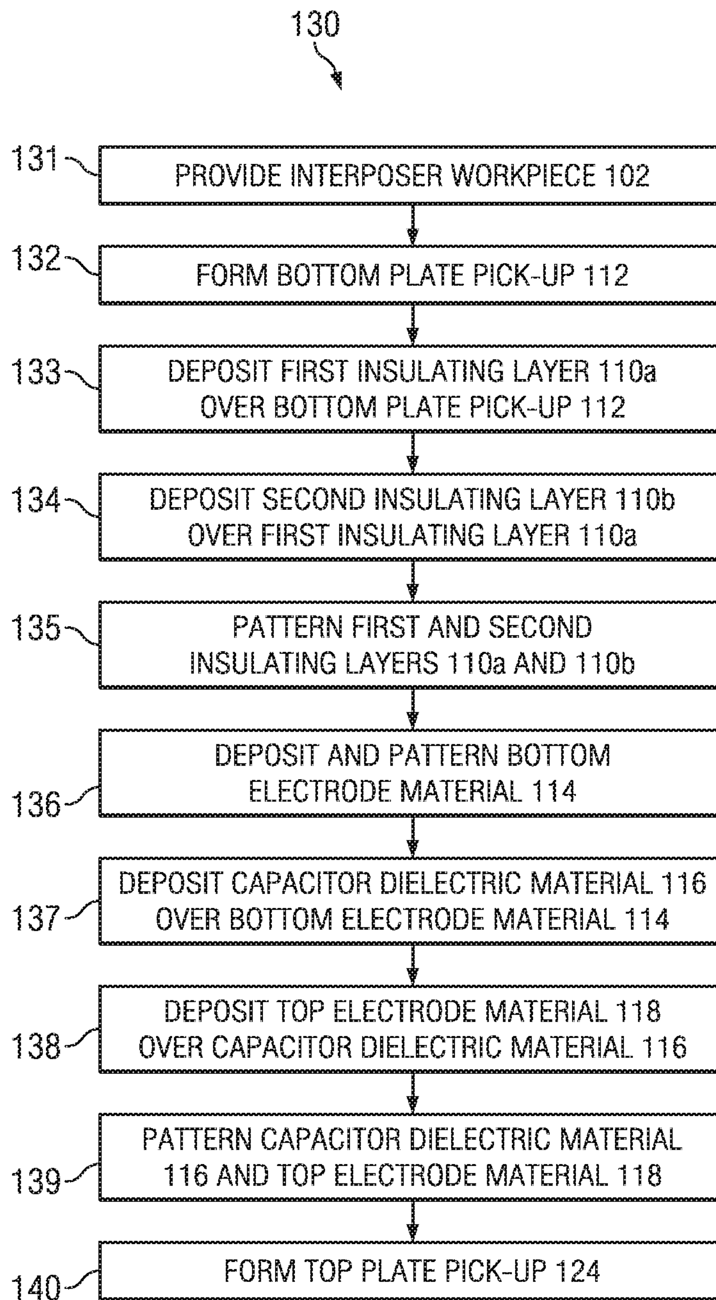

FIG. 2

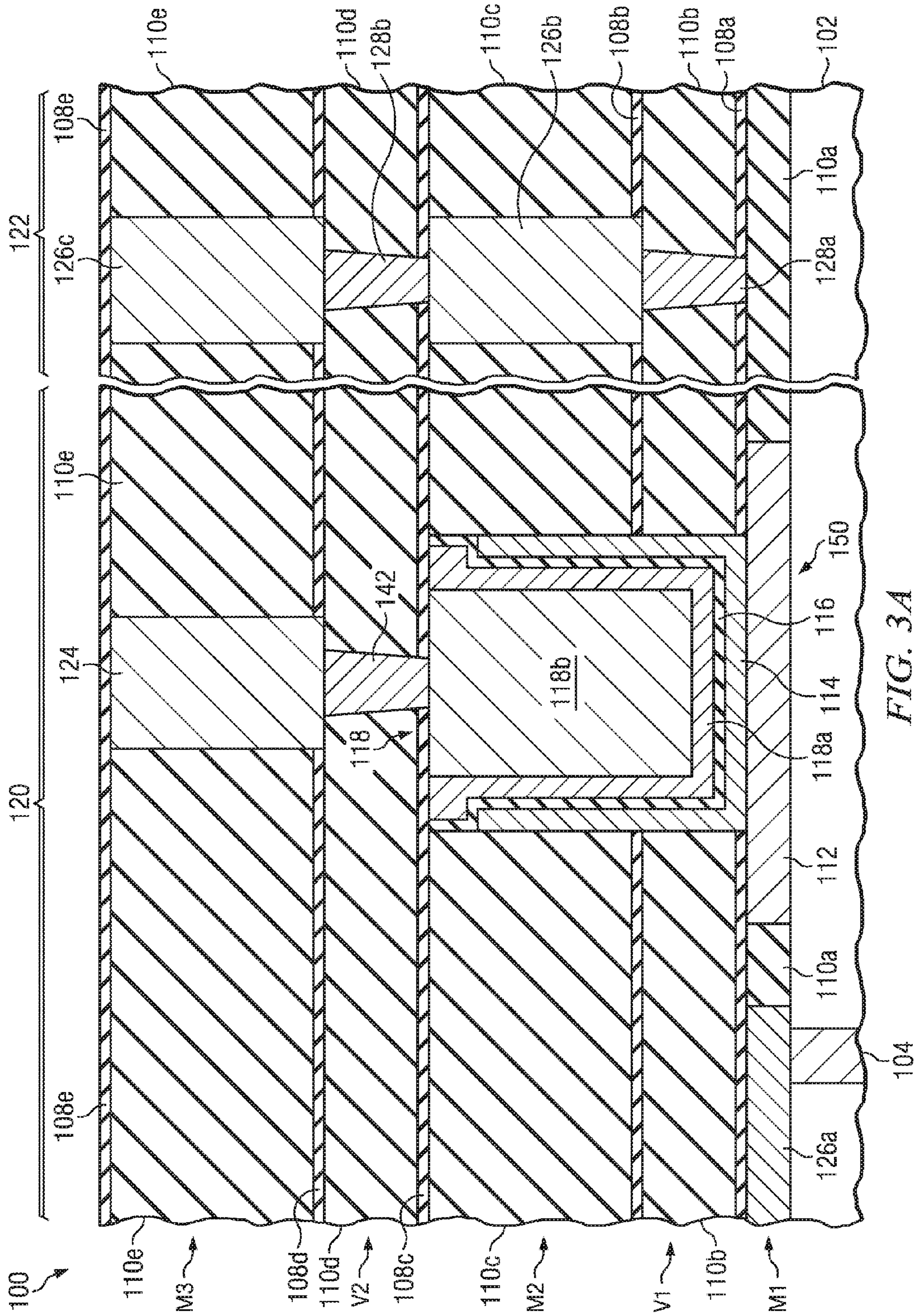

FIG. 3A

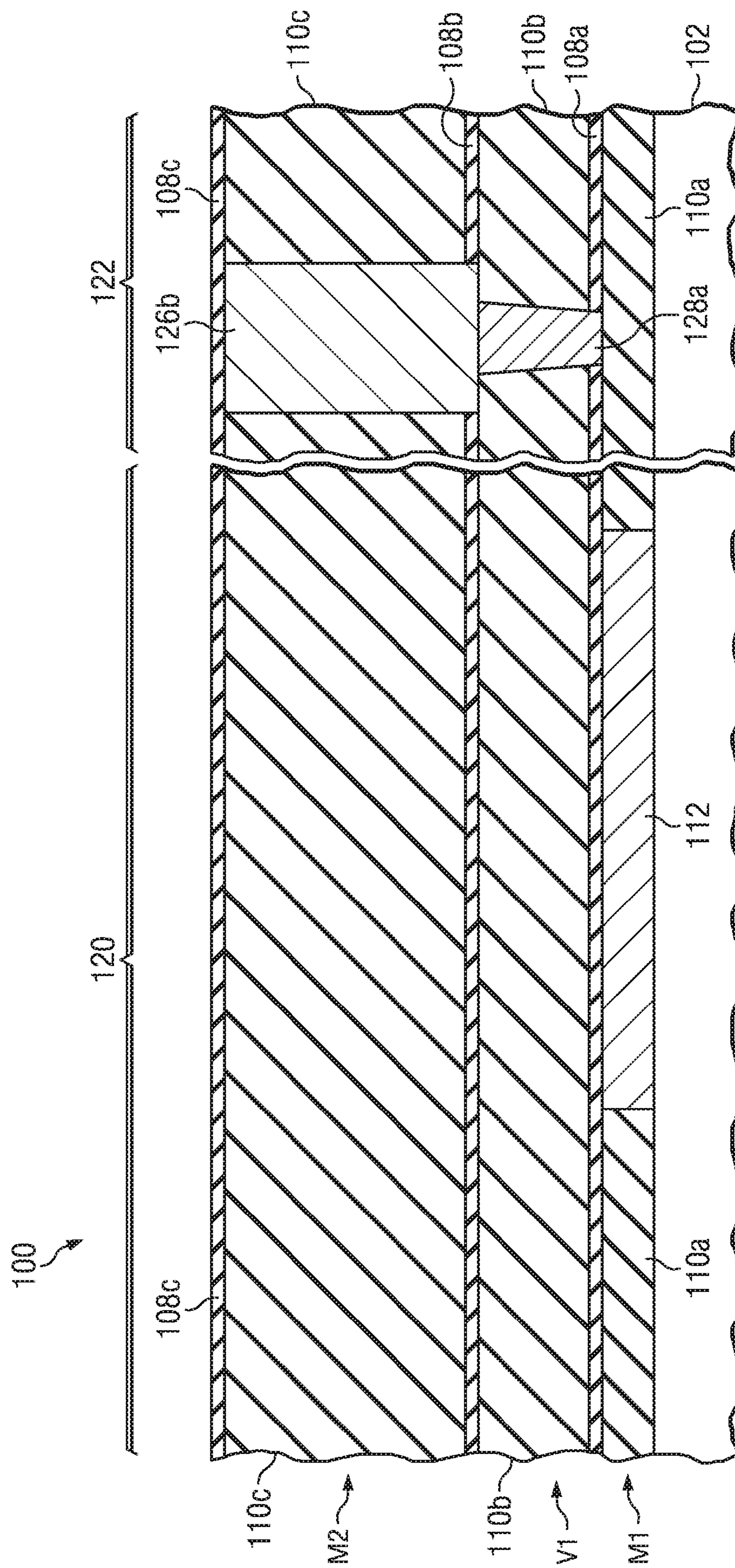

FIG. 3B

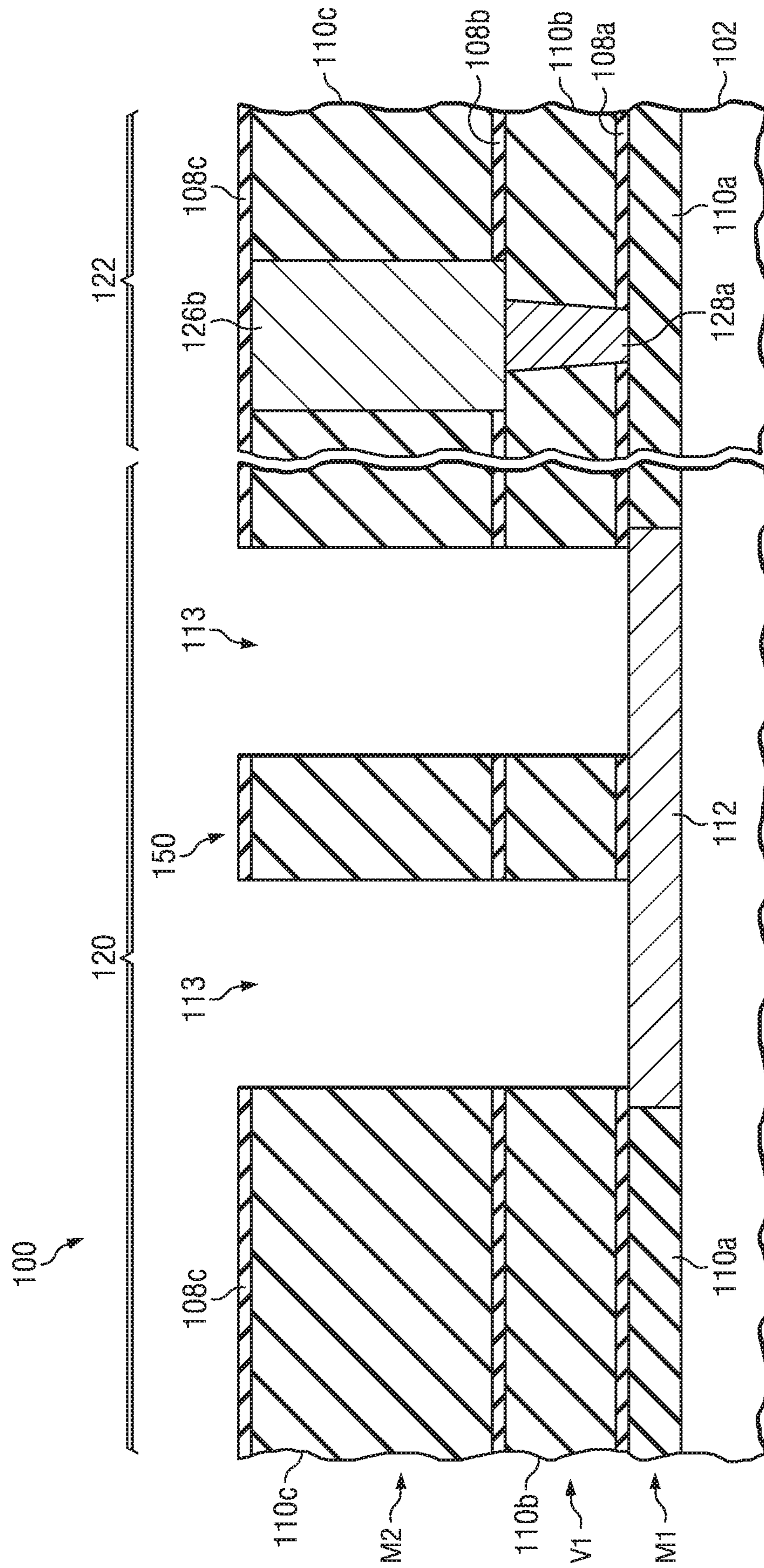

FIG. 3C

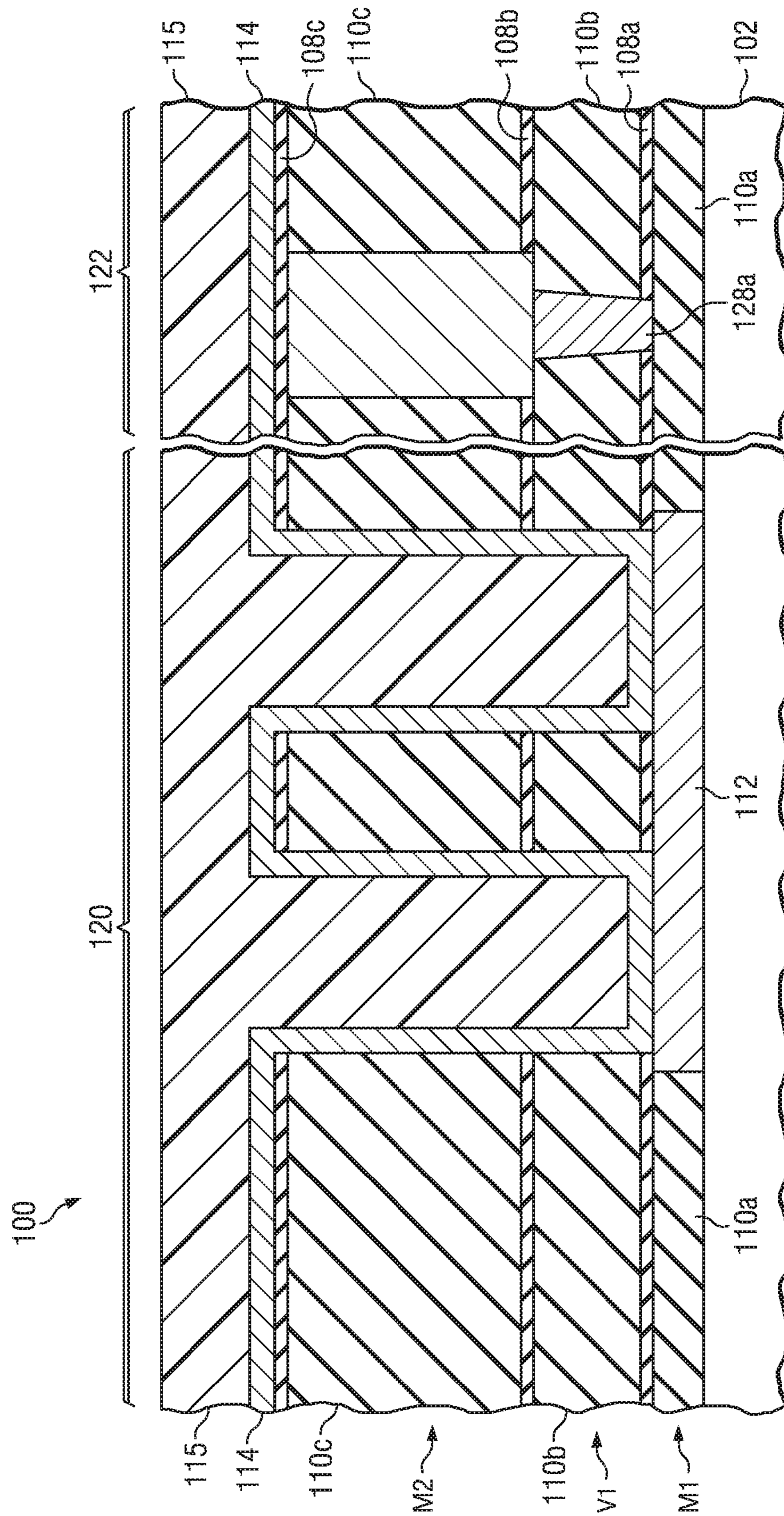

FIG. 3D

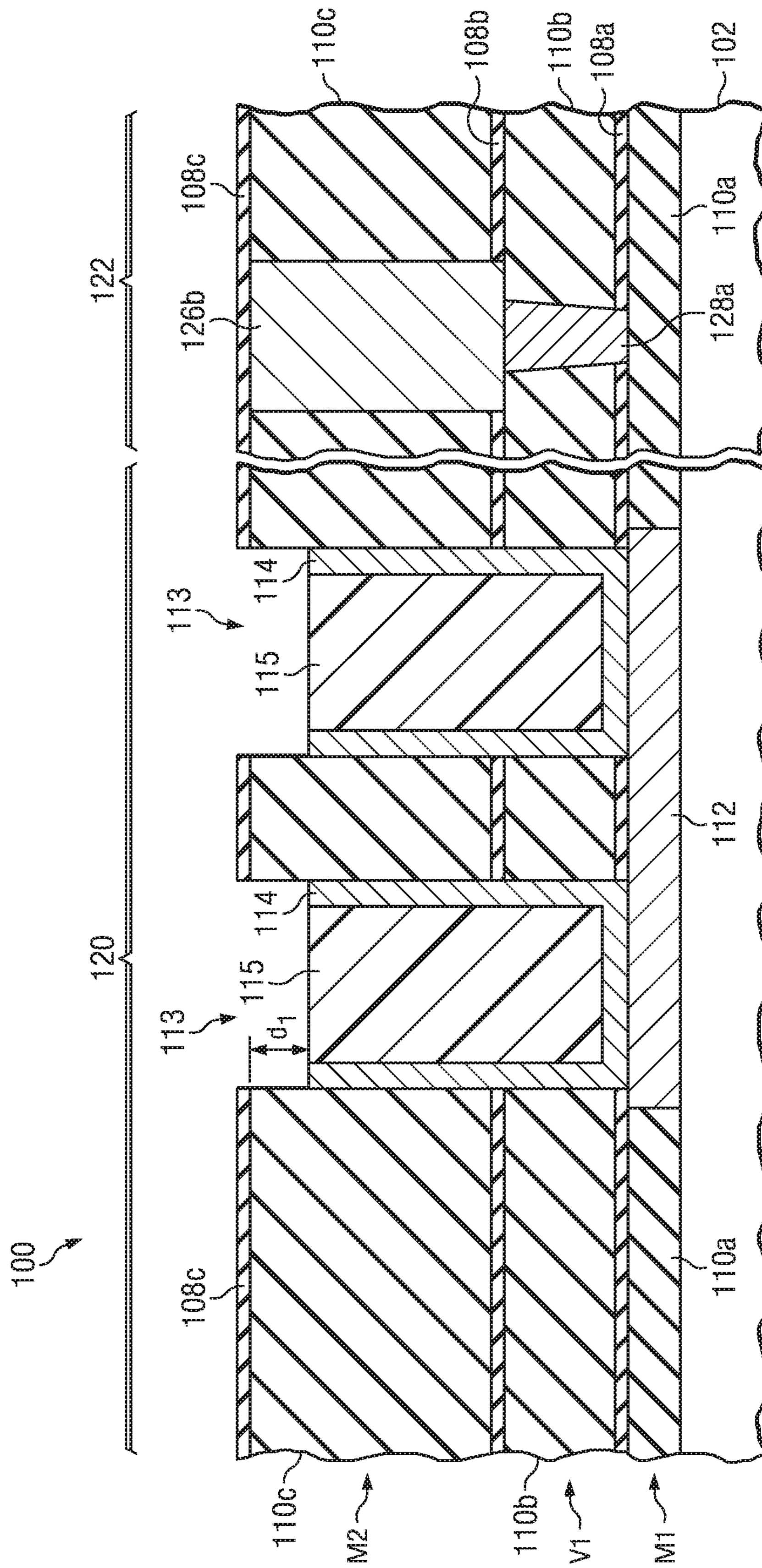

FIG. 3E

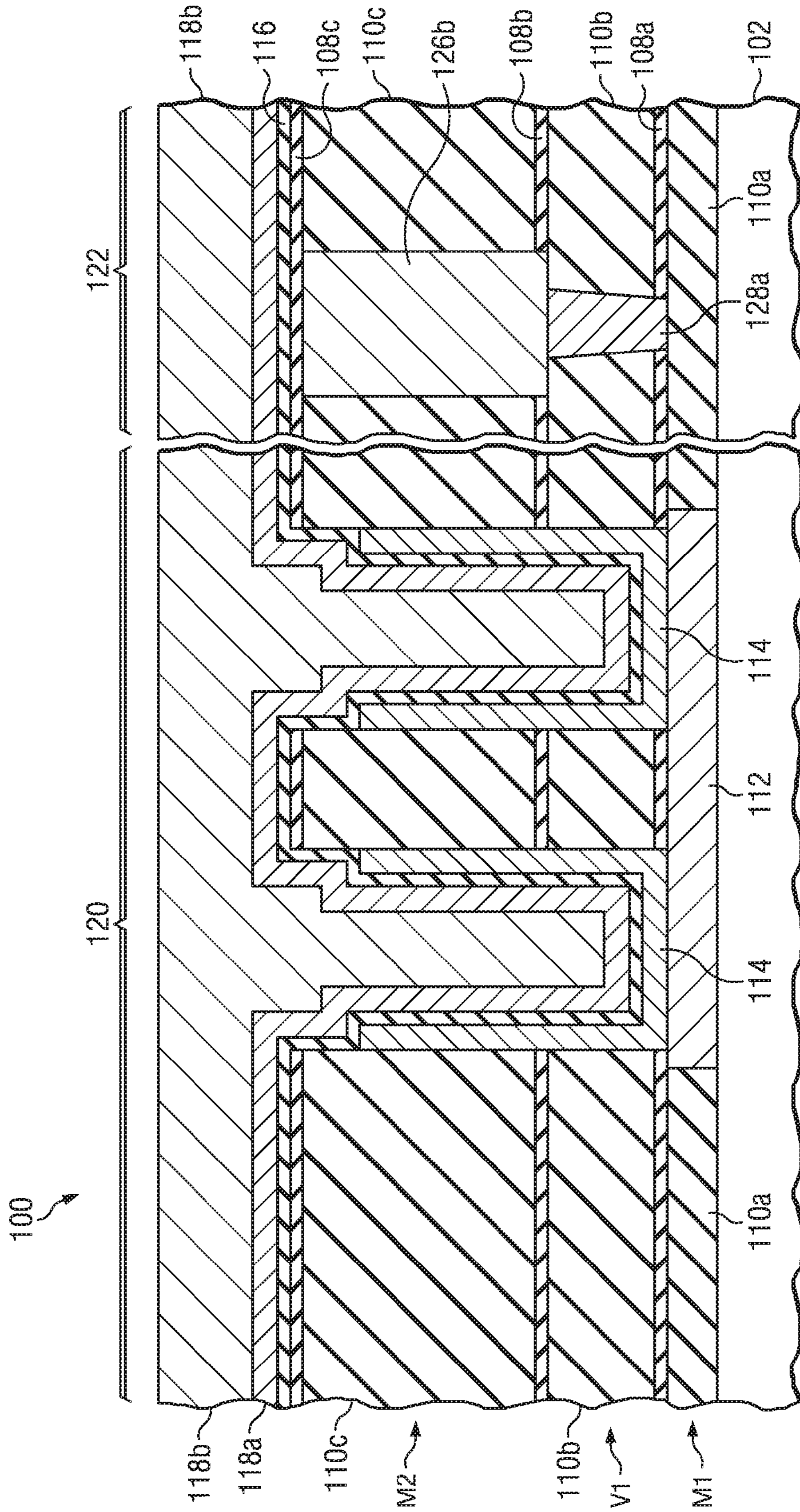

FIG. 3F

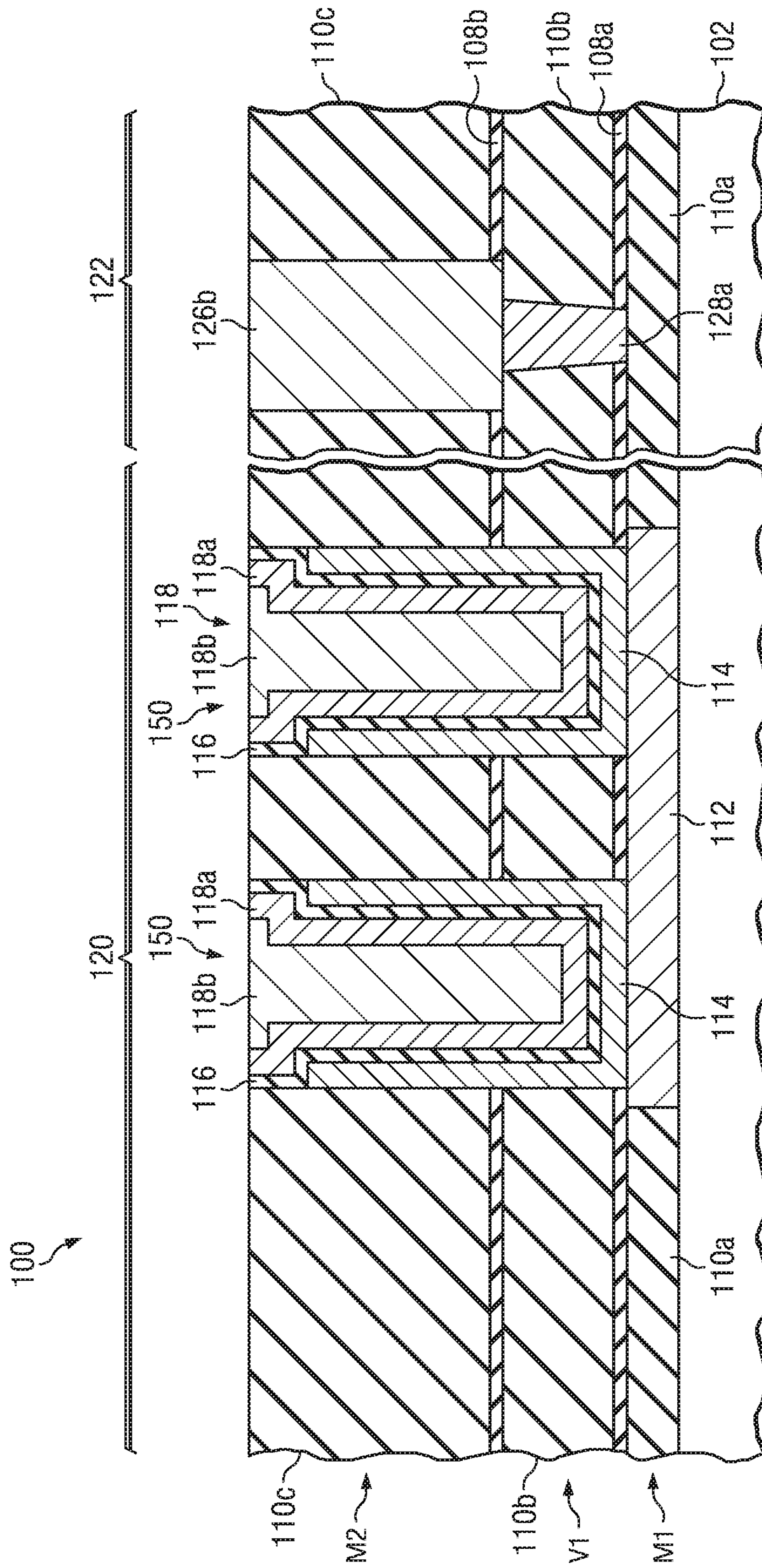

FIG. 3G

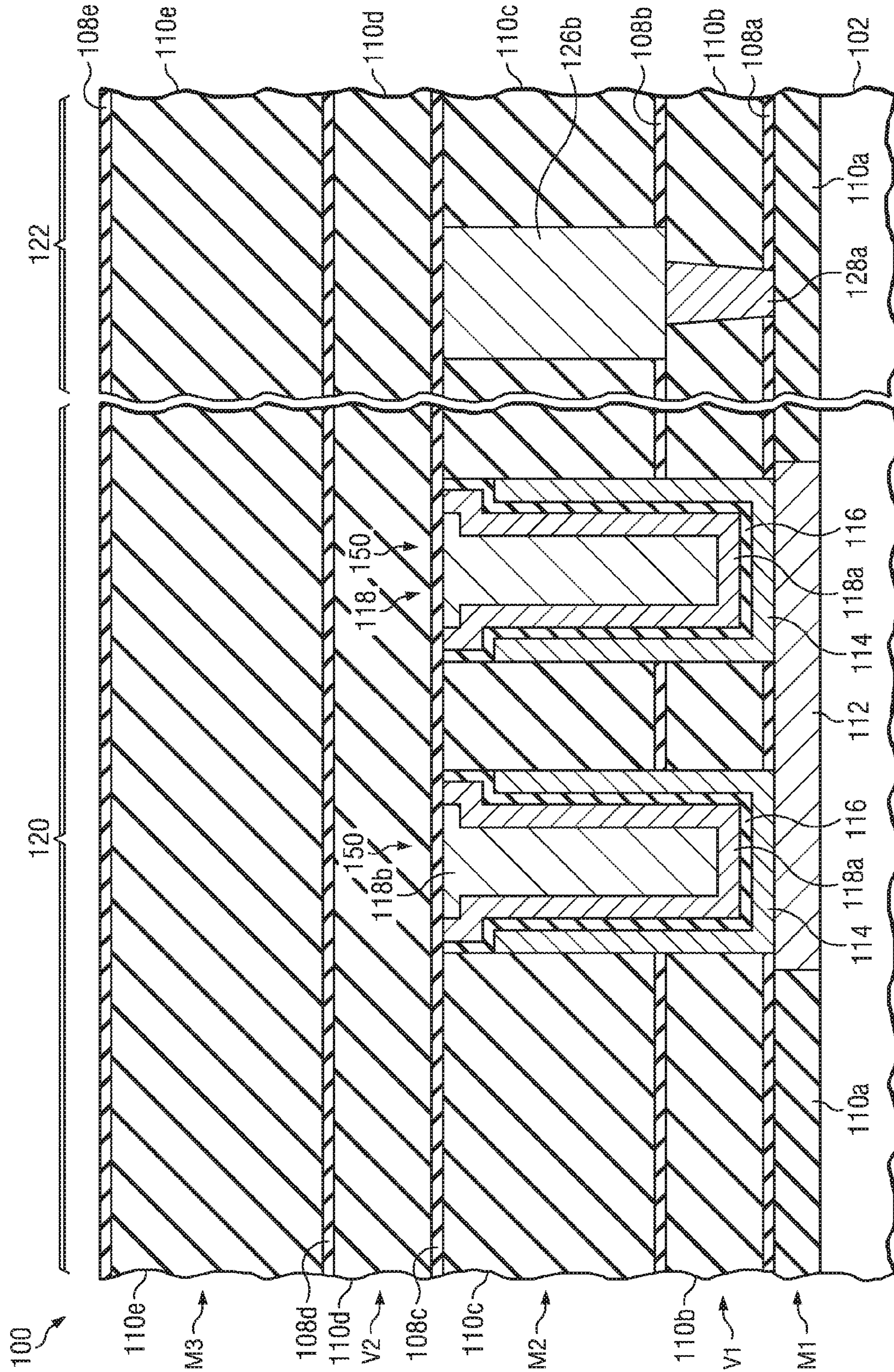

FIG. 3H

FIG. 4A

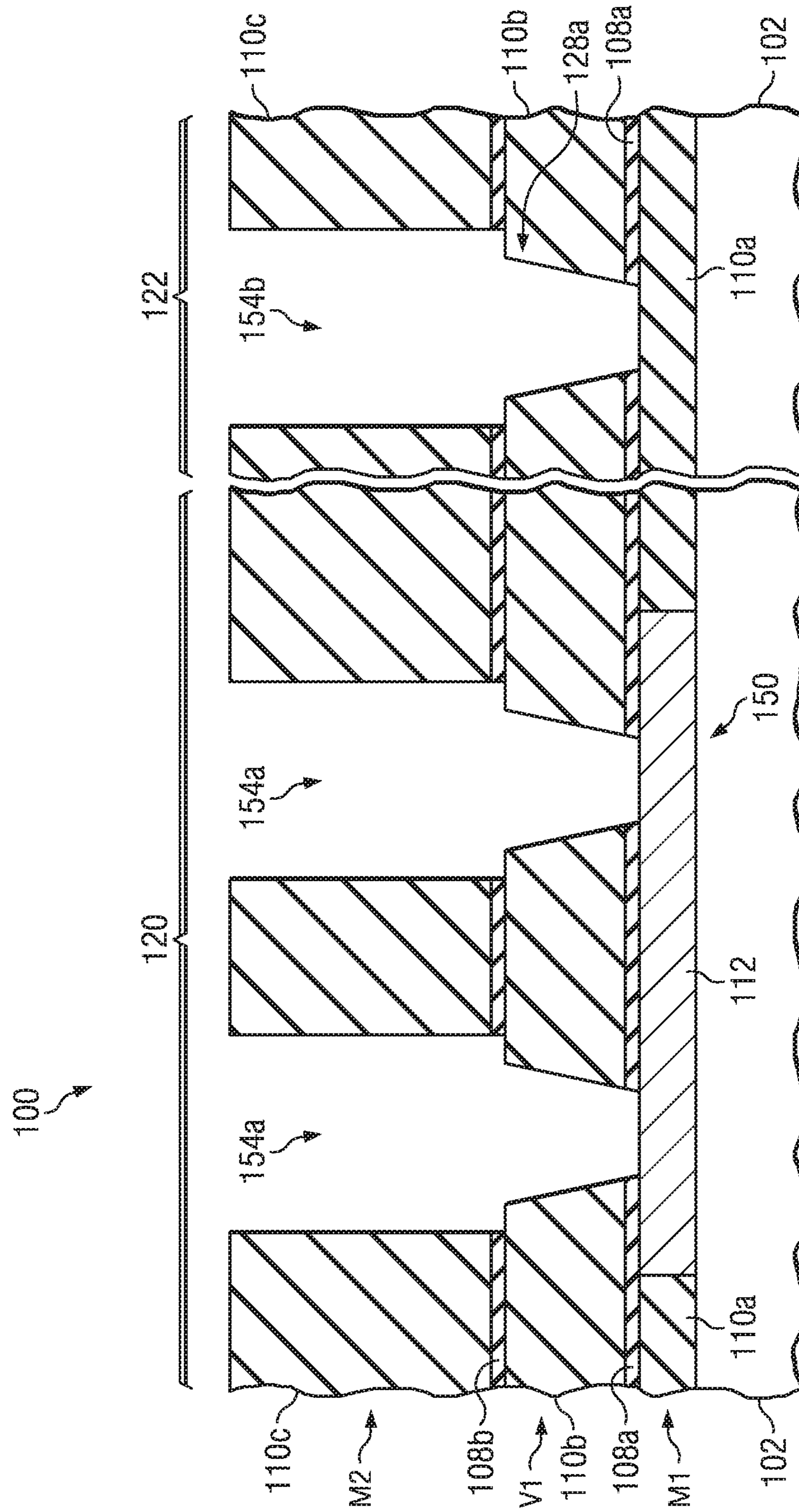

FIG. 4B

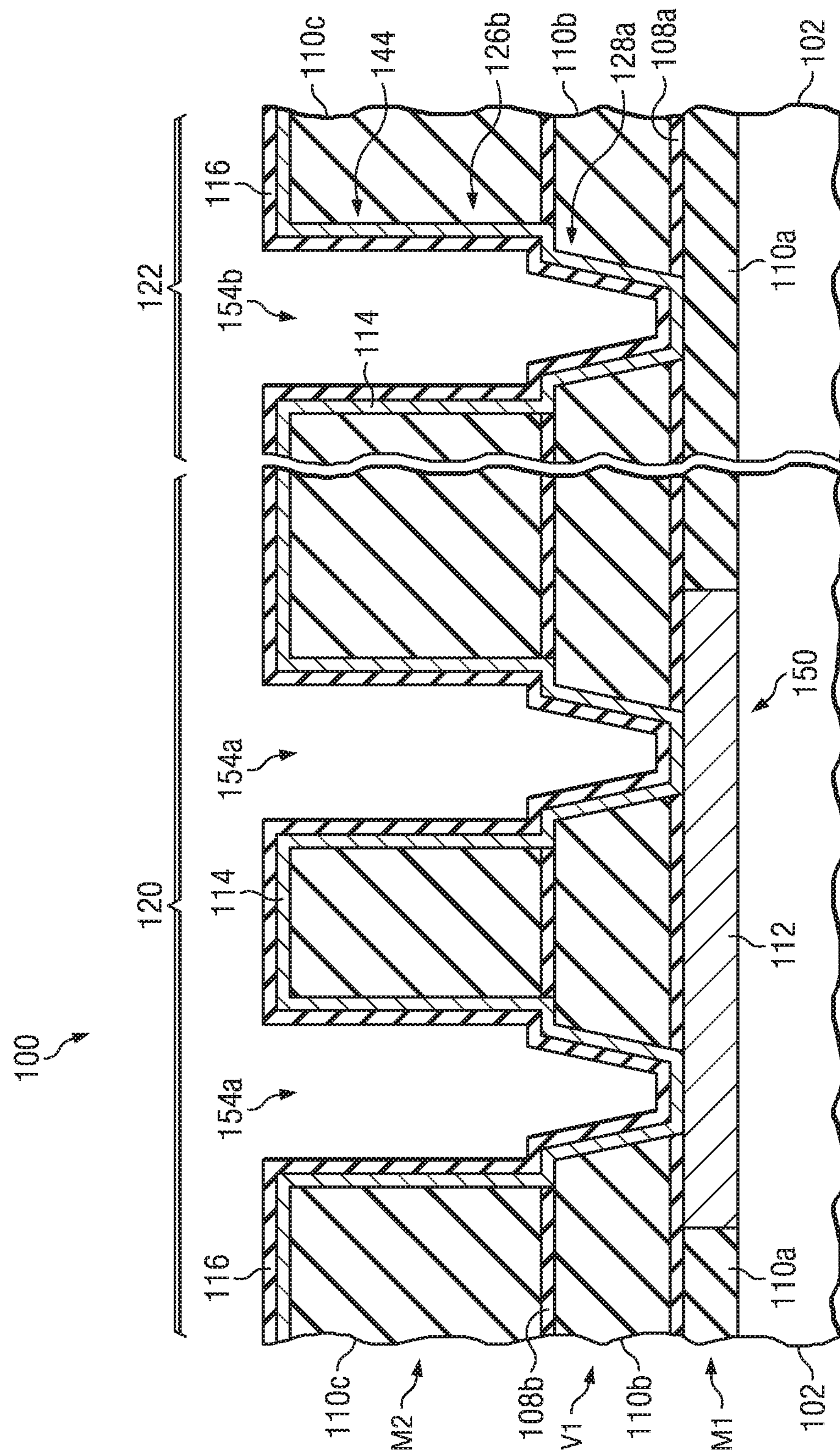

FIG. 4C

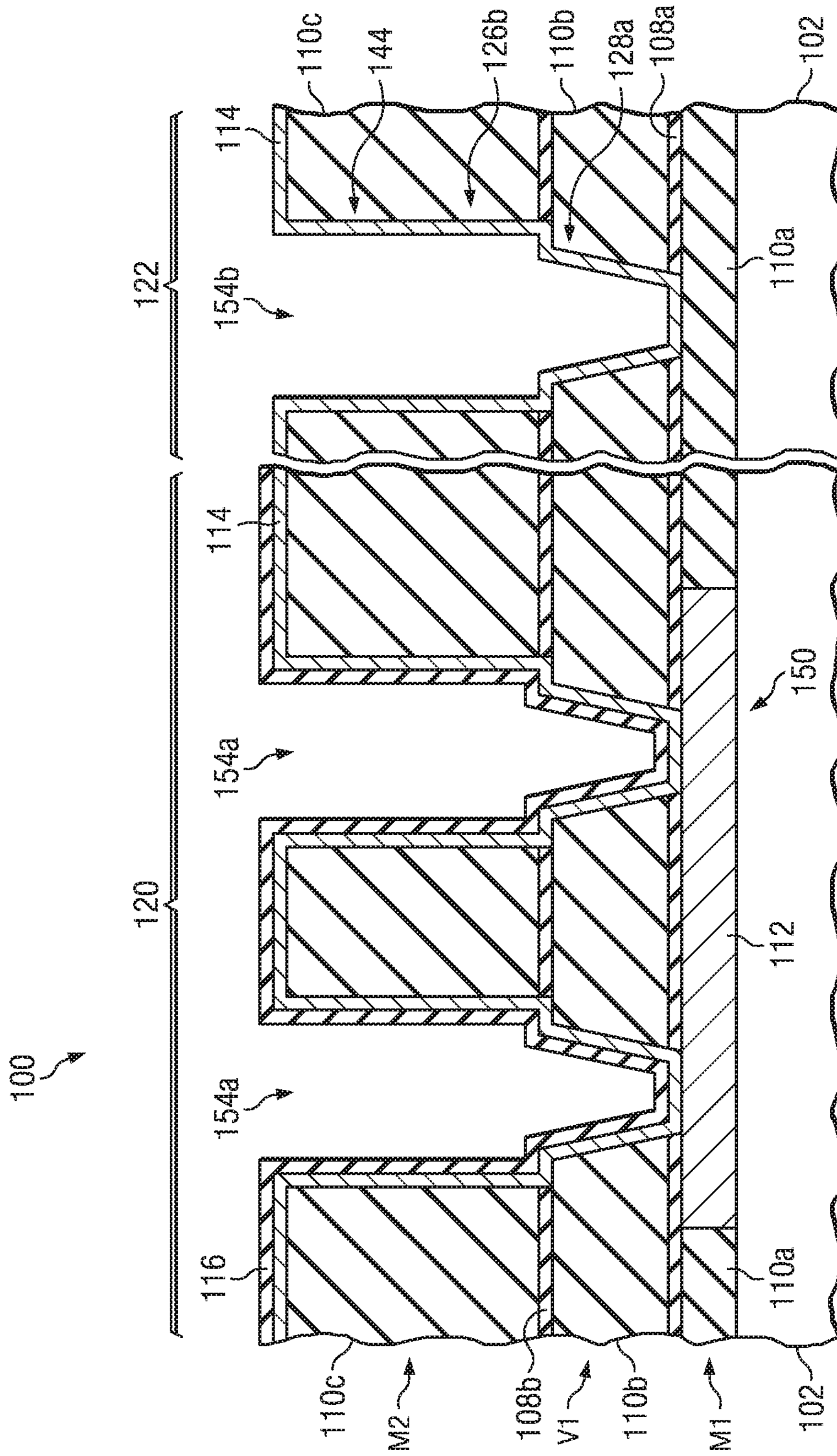

FIG. 4D

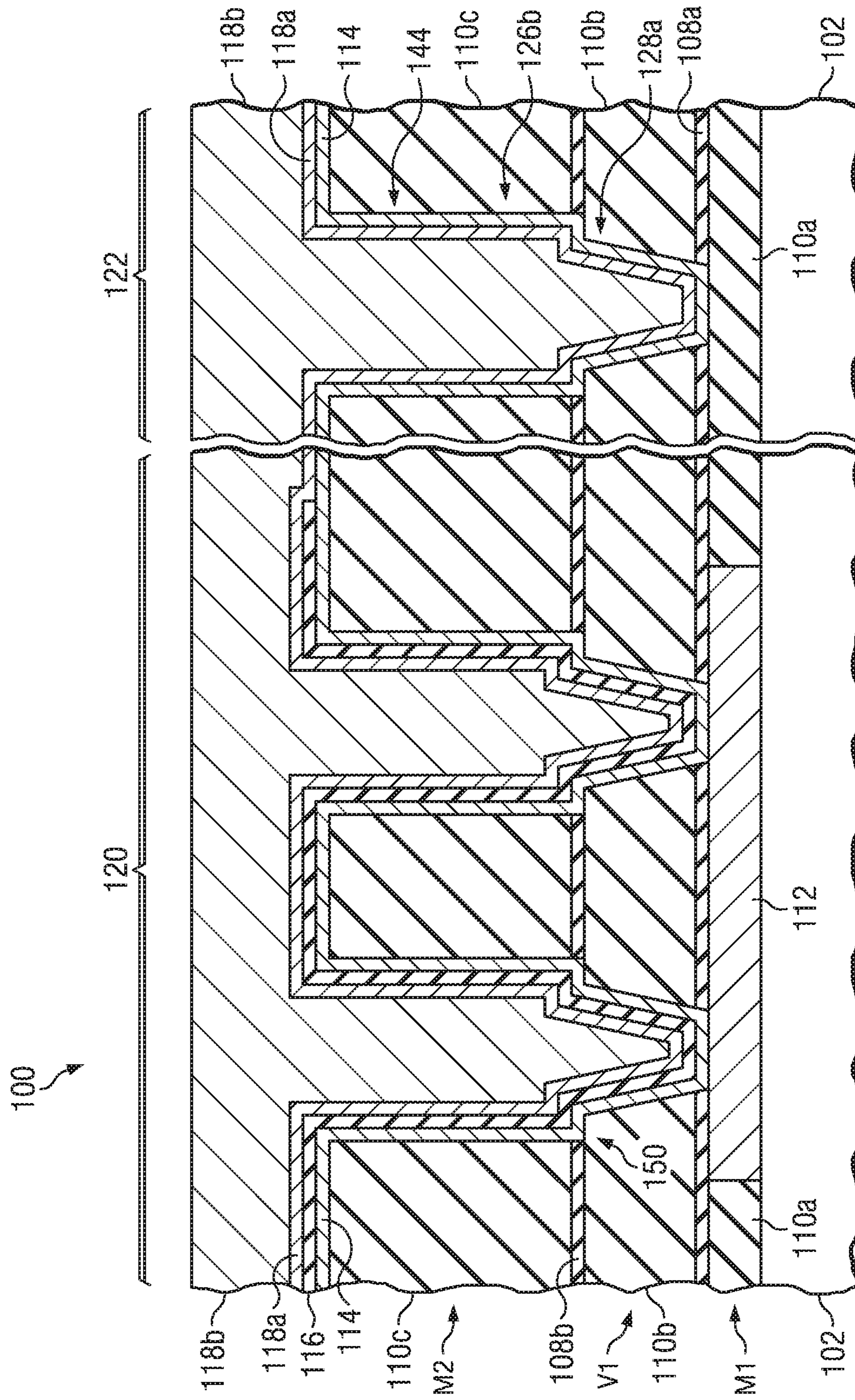

FIG. 4E

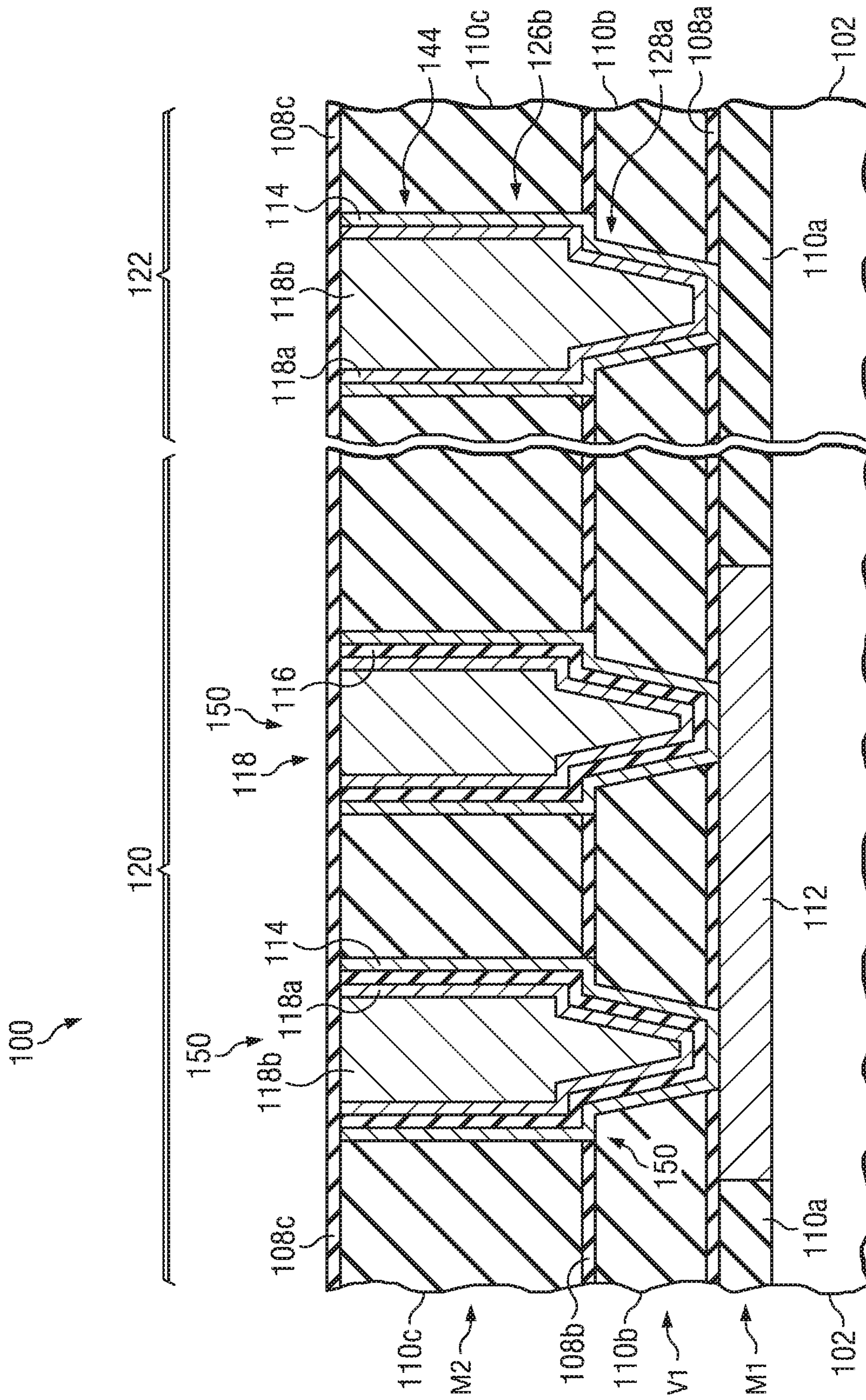

FIG. 4F

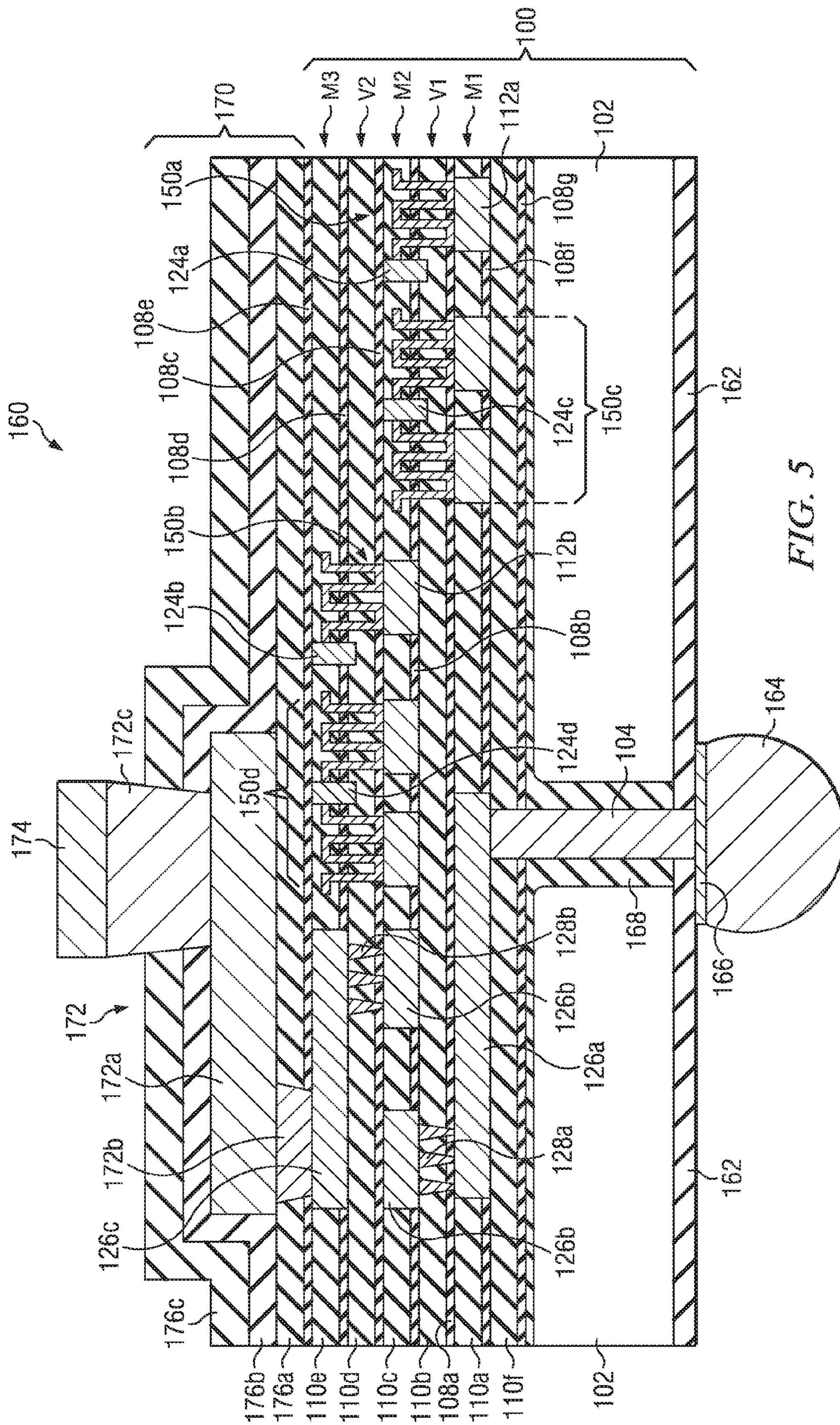

FIG. 5

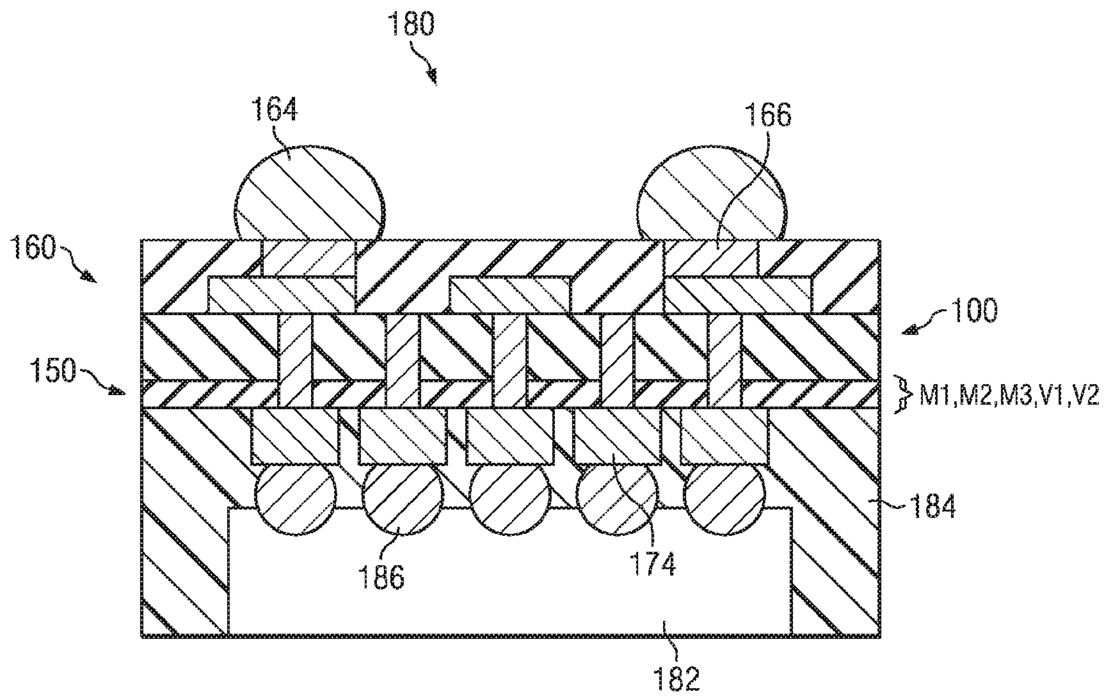

FIG. 6

DECOUPLING MIM CAPACITOR DESIGNS FOR INTERPOSERS AND METHODS OF MANUFACTURE THEREOF

PRIORITY CLAIM AND CROSS-REFERENCE

This application is a continuation of, and claims the benefit of, U.S. patent application Ser. No. 14/265,223, filed on filed Apr. 29, 2014, titled "Decoupling MIM Capacitor Designs for Interposers and Methods of Manufacture Thereof," which is a continuation of U.S. patent application Ser. No. 14/248,186, filed on filed Apr. 8, 2014, titled "Decoupling MIM Capacitor Designs for Interposers and Methods of Manufacture Thereof," which is a divisional of U.S. patent application Ser. No. 13/209,195, filed on Aug. 12, 2011, titled "Decoupling MIM Capacitor Designs for Interposers and Methods of Manufacture Thereof," all of which are hereby incorporated herein by reference.

BACKGROUND

Semiconductor devices are used in a variety of electronic applications, such as personal computers, cell phones, digital cameras, and other electronic equipment, as examples. The semiconductor industry continues to improve the integration density of various electronic components (e.g., transistors, diodes, resistors, capacitors, etc.) by continual reductions in minimum feature size, which allow more components to be integrated into a given area. These smaller electronic components also require smaller packages that utilize less area than packages of the past, in some applications. One type of smaller packaging that has been developed is three-dimensional (3D) ICs, in which two die or ICs are bonded together and electrical connections are formed between the die and contact pads on an interposer.

Typically, power and ground lines are routed to logic gates and other devices in integrated circuits. The current from a power supply flows through the power lines, logic gates, and finally to ground. During the switching of the logic gates, a large amount of change in the current may occur within a short period of time. Decoupling capacitors are used to absorb these glitches during current switching. Decoupling capacitors function as charge reservoirs by maintaining a constant voltage between the supply voltage and ground, preventing momentary drops in the supplied voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIGS. **1**A through **1**G show cross-sectional views of a decoupling MIM capacitor formed in two metallization layers of an interposer in accordance with an embodiment of the present disclosure at various stages of manufacturing.

FIG. **2** is a flow chart for forming decoupling MIM capacitors in an interposer in accordance with an embodiment.

FIGS. **3**A through **3**H are cross-sectional views of a decoupling MIM capacitor formed in an interposer in accordance with another embodiment at various stages.

FIGS. **4**A through **4**F are cross-sectional views of a decoupling MIM capacitor formed in an interposer in accordance with yet another embodiment at various stages.

FIG. **5** shows a cross-sectional view of several decoupling MIM capacitors formed in an interposer.

FIG. **6** shows a cross-sectional view of an integrated circuit packaged with a novel interposer having decoupling MIM capacitors described herein formed therein.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

Embodiments of the present disclosure are related to packages for semiconductor devices that utilize an interposer as a component, such as 3DICs. Novel methods of forming decoupling MIM capacitors in interposers will be described herein.

Referring first to FIG. **1**A, a cross-sectional view is shown of a decoupling MIM capacitor **150** formed in two adjacent metallization layers M**2** and V**1** of an interposer **100** in accordance with an embodiment of the present disclosure. A method of manufacturing the decoupling MIM capacitor **150** at various stages is shown in FIGS. **1**B through **1**G. First, an interposer workpiece or substrate **102** is provided that has a plurality of through-silicon vias (TSVs) **104** formed therein, as shown in FIG. **1**B. The TSVs **104** are also referred to herein as through-substrate vias. The TSVs **104** are conductive and provide a connection from a front side of the interposer substrate **102** to the back side. The substrate **102** may comprise silicon or other semiconductive materials, for example.

Metallization layer M**1** is formed over the substrate **102**. The metallization layer M**1** may be formed by depositing a metal layer and patterning the metal layer to form conductive lines **126***a*. An insulating layer **110***a* may then be formed over the patterned metal layer. Alternatively, the metallization layer M**1** may be formed using a damascene process, wherein the insulating layer **110***a* is deposited over the substrate **102** and then patterned and filled with a metal layer to form conductive lines **126***a*. Excess metal may be removed from the top surface of the insulating layer **110***a* using a chemical-mechanical polishing (CMP) process, for example, using a single damascene process. The insulating layer **110***a* may

comprise silicon dioxide or other insulators, and the conductive lines **126***a* may comprise copper, copper alloys, or other conductors, as examples.

In accordance with some embodiments, a bottom plate pick-up **112** is also formed in the metallization layer M**1** when the conductive lines **126***a* are formed. The bottom plate pick-up **112** provides electrical connection to the bottom electrode of the decoupling MIM capacitor **150**, e.g., bottom electrode material **114**, as shown in FIG. **1**A. The bottom plate pick-up **112** is formed in an adjacent metallization layer M**1** to the decoupling MIM capacitor **150** in some embodiments, e.g., in a metallization layer M**1** disposed beneath a metallization layer V**1** that a portion of the decoupling MIM capacitor **150** is formed in.

Next, an etch stop layer **108***a* may be formed over the metallization layer M**1**, as shown in FIG. **1**B. The etch stop layer **108***a* may comprise SiC in some embodiments, although alternatively, the etch stop layer **108***a* may comprise SiN or other insulating materials. Insulating layer **110***b* is then deposited or formed over the workpiece **102**, e.g., over the etch stop layer **108***a*. The insulating layer **110***b* is also referred to herein as a first insulating layer, for example. An etch stop layer **108***b* is then formed over the insulating layer **110***b*. The etch stop layer **108***b* may comprise SiN or other insulating materials. An insulating layer **110***c* is then deposited or formed over the etch stop layer **108***b*. The insulating layer **110***c* is also referred to herein as a second insulating layer. Insulating layers **110***b* and **110***c* may comprise undoped silicon glass (USG) oxide or other insulating materials, as examples.

In the embodiment shown in FIGS. **1**A through **1**G, a pattern for at least one decoupling MIM capacitor is formed using a separate lithography mask to pattern insulating layers **110***c* and **110***b*. After the insulating layer **110***c* is formed or deposited, insulating layers **110***c* and **110***b* are patterned, as shown in FIG. **1**B, forming patterns **113** having a desired shape for the at least one decoupling MIM capacitor **150** within the insulating layers **110***c* and **110***b*. The width of the patterns **113** in the insulating layers **110***c* and **110***b* may comprise about 50 nm to 500 nm, for example, and the patterns **113** may be substantially circular, oval, square, or round in a top view (not shown), as examples.

Next, a bottom electrode material **114** is formed over the second insulating layer **110***c*, as shown in FIG. **1**C, lining the patterns **113** formed in the first and second insulating layers **110***b* and **110***c* for the at least one decoupling MIM capacitor **150**. The bottom electrode material **114** may comprise a layer of TaN or TiN deposited in a thickness of about 10 nm to 30 nm, for example although alternatively, the bottom electrode material **114** may comprise other conductive materials and dimensions. The bottom electrode material **114** is removed from a top surface of the second insulating layer **110***c*, e.g., using one or more etch processes, CMP processes, or a combination thereof. The bottom electrode material **114** may be removed from the top surface of the second insulating layer **110***c* using a layer of photoresist **115** and an etch process, for example, shown in FIGS. **1**C and **1**D. The layer of photoresist **115** is then removed.

A dielectric material **116** is then formed over the bottom electrode material **114** and over the top surface of the second insulating layer **110***c*, as shown in FIG. **1**E. The dielectric material **116** comprises a capacitor dielectric material for the at least one decoupling MIM capacitor **150**. The dielectric material **116** may comprise a high dielectric constant (k) material having a dielectric constant greater than the dielectric constant of SiO2, for example, such as ZrO, HfO, Si3N4, or BST, although alternatively, the capacitor dielectric material **116** may comprise other materials. The dielectric material **116** may comprise a thickness of about 5 nm to 20 nm or other dimensions. A top electrode material **118** comprising similar materials and dimensions as described for the bottom electrode material **114** is then formed over the capacitor dielectric material **116**, also shown in FIG. **1**E.

The top electrode material **118** and the capacitor dielectric material **116** are then patterned using an additional lithography mask to remove the top electrode material **118** and capacitor dielectric material **116** from other regions **122** that may comprise logic regions or other connection regions of the interposer **100**, for example, as shown in FIG. **1**F. Portions of the top electrode material **118** and the capacitor dielectric material **116** may also be removed in region **120** of the interposer **100** to form a desired shape of the top capacitor plate of the decoupling MIM capacitor **150** comprising the top electrode material **118**, which may comprise an array region, for example. The top electrode material **118**, capacitor dielectric material **116**, and bottom electrode material **114** form at least one decoupling MIM capacitor **150** for the interposer **100** in region **120**, advantageously.

The manufacturing process is then continued to complete the fabrication of the metallization layers V**1** and M**2**. For example, insulating layer **110***d* may be formed over the decoupling MIM capacitors **150** and insulating layer **110***c*, as shown in FIG. **1**G. The insulating layer **110***d* may comprise USG oxide film or similar materials as described for insulating layers **110***c* and **110***b*. The insulating layer **110***d* may be exposed to a CMP process to return the total thickness of insulating layers **110***b*, **110***c*, and **110***d* to the original total thickness of layers **110***b* and **110***c* before the CMP process used to form the decoupling MIM capacitors **150**, for example.

Manufacturing processes may then be continued to form conductive lines **126***b* and vias **128** in metallization layers M**2** and V**1**, within insulating layers **110***d*/**110***c* and **110***b*, respectively, in region **122**, as shown in FIG. **1**A. An additional etch stop layer **108***c* may be formed over insulating layer **110***d*, as shown. Patterns **117** and **119** for a top plate pick-up **124** and the conductive lines **126***b* and vias **128**, respectively, shown in FIG. **1**G, may be formed using a dual damascene process, for example. Conductive material is then deposited over the insulating layer **110***d* to fill the patterns **117** and **119**, and excess conductive material is removed using one or more etch processes or CMP processes, leaving the structure shown in FIG. **1**A. In accordance with some embodiments, a top plate pick-up **124** is also formed in insulating layer **110***c*/**110***d*. The top plate pick-up **124** is coupled to a portion of the top electrode material **118** of the decoupling MIM capacitor **150**, as shown. Advantageously, an additional lithography mask is not required to form the top plate pick-up **124** or the bottom plate pick-up **112** : these pick-ups **124** and **112** may be patterned by altering an existing mask used to pattern metallization layers M**2** and M**1**, respectively.

FIG. **2** is a flow chart **130** for forming decoupling MIM capacitors **150** in an interposer **100** in accordance with an embodiment of the present disclosure. To form decoupling MIM capacitors **150**, first, an interposer workpiece **102** is provided (step **131**). A bottom plate pick-up **112** is formed over the workpiece **102** (step **132**). A first insulating layer **110***a* is deposited over the bottom plate pick-up **112** (step **133**). A second insulating layer **110***b* is deposited over the first insulating layer **110***a* (step **134**). The first and second insulating layers **110***a* and **110***b* are patterned (step **135**). A bottom electrode material **114** is then deposited and patterned (step **136**). A decoupling capacitor dielectric material **116** is deposited over the bottom electrode material **114** (step **137**).

A top electrode material **118** is deposited over the capacitor dielectric material **116** (step **138**). The capacitor dielectric material **116** and the top electrode material **118** are patterned (step **139**) to form the decoupling MIM capacitor **150**. The pattern may be achieved by lithography masks and processes, as described with respect to FIGS. **1**A through **1**G, or the patterning may be achieved by CMP processes, to be described further herein. A top plate pick-up **124** is formed (step **140**) that is coupled to the top electrode material **118**.

In the embodiment shown in FIGS. **1**A through **1**G, two additional lithography masks are used: a first lithography mask that is used to pattern the bottom electrode material **114** and a second lithography mask that is used to pattern the top electrode material **118** and the capacitor dielectric material **116**. FIGS. **3**A through **3**H are cross-sectional views of a method of forming a decoupling MIM capacitor **150** in an interposer **100** in accordance with another embodiment, wherein only one additional lithography mask is required to form the decoupling MIM capacitor **150**. Like numerals are used for the various elements in FIGS. **3**A through **3**H that were used to describe FIGS. **1**A through **1**G, and to avoid repetition, each reference number shown in FIGS. **3**A through **3**H is not described again in detail herein.

In the embodiment shown in FIGS. **3**A through **3**H, insulating layers **110***c* and **110***b* are patterned using a lithography mask for a desired pattern for the decoupling MIM capacitor **150**. First, insulating layers **110***c* and **110***b* and etch stop layers **108***a*, **108***b*, and **108***c* are formed over the first metallization layer M**1**, as shown in FIG. **3**B, and conductive lines **126***b* and vias **128***a* are formed in region **122**. A separate lithography mask is then used to form patterns **113** in region **120** for the decoupling MIM capacitor **150**, as shown in FIG. **3**C. A bottom electrode material **114** is then formed or deposited over the second insulating layer **110***c*, as shown in FIG. **3**D, lining the patterns **113** in the first and second insulating layers **110***b* and **110***c*. A top portion of the bottom electrode material **114** is removed from an upper part of sidewalls of the second insulating layer **110***c*, using a layer of photoresist **115**, as shown in FIGS. **3**D and **3**E, and the bottom electrode material **114** is also removed from a top surface of the second insulating layer **110***c* in this embodiment. The portions of the bottom electrode material **114** removed may be removed using a photoresist **115** etch-back process that may recess the bottom electrode by a dimension d**1** comprising about 3,000 Angstroms from the top surface of the second insulating layer **110***c*, for example, as shown in FIG. **3**E. Alternatively, portions of the bottom electrode material **114** may be removed using other methods and comprising other dimensions d**1**.

Next, the capacitor dielectric material **116** is formed over the bottom electrode material **114**, over the top surface of the second insulating layer **110***c*, and over the exposed sidewalls of the second insulating layer **110***c*, as shown in FIG. **3**F. A first top electrode material **118***a* is formed over the capacitor dielectric material **114**, and a second top electrode material **118***b* is formed over the first top electrode material **118***a*, also shown in FIG. **3**F. The first top electrode material **118***a* may comprise TiN or TaN and may function as a seed layer or liner for plating of the second top electrode material **118***b* that may comprise copper, for example. One or more CMP processes and/or etch processes are then used to remove the first and second top electrode materials **118***a*/**118***b* and the capacitor dielectric material **116** from the top surface of the second insulating material **110***c*, as shown in FIG. **3**G, forming at least one decoupling MIM capacitor **150** in metallization layers M**2** and V**1**. The first top electrode material **118***a* and the second top electrode material **118***b* comprise the top electrode **118** of the decoupling MIM capacitor **150**. Insulating layers **110***d* and **110***e* and etch stop layers **108***c*, **108***d* and **108***e* are formed over the at least one decoupling MIM capacitor **150**, (e.g., etch stop layer **108***c* is redeposited after being removed in the step shown in FIG. **3**G) as shown in FIG. **3**H, and conductive lines **126***c* and vias **128***b* are formed in region **122** as shown in FIG. **3**A.

In this embodiment, connections to the top electrode material **118***b* are made in metallization layers V**2** and M**3** disposed over the metallization layers M**2** and V**1** that the capacitor **150** is formed in. For example, top plate pick-up **124** is formed in metallization layer M**3** that comprises a conductive line **126***c* layer, as shown in FIG. **3**A. The top plate pick-up **124** is coupled to the top electrode material **118***b* by a via **142** formed in metallization layer V**2** that comprises a via **128***b* layer for the interposer **100**. Insulating layers **110***d* and **110***e* and etch stop layers **108***d* and **108***e* may comprise similar materials mentioned herein for layers **110***a*, **110***b*, and **110***c*, and **108***a*, **108***b*, and **108***c*, respectively, for example.

FIGS. **4**A through **4**F show cross-sectional views of decoupling MIM capacitors **150** formed in an interposer **100** in accordance with yet another embodiment of the present disclosure. In this embodiment, no additional lithography masks may be required to manufacture the novel decoupling MIM capacitors **150**. Rather, another lithography mask already used in the manufacturing process flow having non-critical alignment dimensions may be used, such as a mask used to open the region **120** which may comprise an array region, if such a mask is available, for example. The second insulating layer **110***c* and the first insulating layer **110***b* are patterned with a pattern **154***a* for at least one decoupling MIM capacitor **150** in region **120** during a lithography process used to pattern the second insulating layer **110***c* and the first insulating layer **110***b* with a pattern **154***b* for a plurality of conductive lines **126***b* and a plurality of vias **128***a*, respectively, in region **122**, in this embodiment, as shown in FIG. **4**B.

The bottom electrode material **114** is formed over the patterned second insulating layer **110***c* and first insulating layer **110***b*, lining the pattern **154***a* for the at least one decoupling MIM capacitor **150** and the pattern **154***b* for the conductive lines **126***b* and vias **128***a* in the first and second insulating layers **110***b* and **110***c*, as shown in FIG. **4**C. The capacitor dielectric material **116** is formed over the bottom electrode material **114**. The capacitor dielectric material **116** is removed from the pattern **154***b* for the plurality of conductive lines **126***b* and plurality of vias **128***a* in region **122**, using the lithography mask described herein for this embodiment, as shown in FIG. **4**D.

A first top electrode material **118***a* is formed over the capacitor dielectric material **116** in region **120** and over the bottom electrode material **114** in the pattern **154***b* for the plurality of vias **128***a* and plurality of conductive lines **126***b* in region **122**, as shown in FIG. **4**E. Layer **144** in region **122** comprises a first layer comprising bottom electrode material **114** and a second layer comprising top electrode material **118***a*. A second top electrode material **118***b* is formed over the first top electrode material **114**, filling in the patterns **154** with conductive material and forming decoupling MIM capacitors **150** in region **120** and forming vias **128***a* and conductive lines **126***b* in region **122**, as shown in FIG. **4**E. Advantageously, the bottom electrode material **114** and first top electrode material **118***a* can be used as liners and/or seed layers **144** for the plating of conductive material of the second top electrode material **118***b* for conductive lines **126***b* and vias **128***a* in region **122**, in this embodiment. The first top electrode material **118***a* and the second top electrode material **118***b* comprise the top electrode **118** of the decoupling MIM capacitors **150**.

Next, one or more CMP processes and/or etch processes is used to remove the first and second top electrode materials **118***a* and **118***b*, the capacitor dielectric material **116**, and the bottom electrode material **114** from the top surface of the second insulating material **110***c*, forming at least one decoupling MIM capacitor **150** in region **120**, as shown in FIG. **4**F. Etch stop layers **108***c*, **108***d*, **108***e* and insulating layers **110***d* and **110***e* are formed over the decoupling MIM capacitor **150** and conductive lines **126***b*, as shown in FIGS. **4**F and **4**A. As in the embodiment shown in FIG. **3**, the top plate pick-up **124** is formed in a metallization layer M**3** disposed over the decoupling MIM capacitor **150** and is coupled to the top electrodes **118** of the decoupling MIM capacitors **150** by vias **142**.

FIG. **5** shows a cross-sectional view of several decoupling MIM capacitors **150***a*, **150***b*, **150***c*, and **150***d* formed in an interposer **100**. The interposer **100** includes metallization layers M**1**, V**1**, M**2**, V**2**, and M**3**. FIG. **5** shows a package **160** for a semiconductor device that includes the interposer **100** described herein. The package **160** includes an insulating material **162** formed on a side opposite the metallization layers M**1**, V**1**, M**2**, V**2**, and M**3**. The insulating material **162** may comprise SiN, as an example, although other materials may be used. A plurality of solder balls **164** may be coupled to the TSVs **104** of the interposer **100**, as shown. Contact pads **166** may be formed over the exposed ends of the TSVs **104**, and the solder balls **164** may be formed on the contact pads **166**, for example. The solder balls **164** may be used to couple the package **160** to another integrated circuit, circuit board, or other package, as examples.

A wiring layer **170** may be formed on the interposer **100** in some embodiments proximate the metallization layers M**1**, V**1**, M**2**, V**2**, and M**3**. The wiring layer **170** may include a redistribution layer (RDL) **172**. The RDL **172** may comprising wiring such as conductive lines **172***a* and vias **172***b* formed in insulating layers **176***a*, **176***b*, and **176***c*. The conductive lines **172***a* of the RDL **172** may be coupled to conductive lines **126***c* in upper metallization layer M**3**. The RDL **172** may include conductive regions **172***c* that are coupleable to microbumps **174** which may be formed thereon. The microbumps **174** may be used to couple the package **160** to integrated circuits **182** for packaging, as shown in a cross-sectional view in FIG. **6**, which illustrates an integrated circuit **182** packaged using a novel interposer **100** including the decoupling MIM capacitors **150** described herein. A molding compound **184** may be disposed over the integrated circuit **182** which may comprise a die. The molding compound **184** also covers exposed portions of the interposer **100**, as shown. The integrated circuit **182** may be bonded to the interposer using metal balls **186** that may comprise solder, gold, or other metals, as examples.

The decoupling MIM capacitors **150** may comprise single capacitors as shown in FIG. **3**A, or the decoupling MIM capacitors **150** may comprise one or more capacitors coupled together in parallel or series, or positioned proximate one another, as shown in FIGS. **1**A, **1**F, **1**G, **3**G, **3**H, **4**A and **4**F, depending on the application. The decoupling MIM capacitors **150** may also be configured in a single stage (see **150***a* and **150***b* of FIG. **5**) or two stages (see **150***c* and **150***d* of FIG. **5**). Two stages may be used to achieve a large bias, by coupling two decoupling MIM capacitors **150** in series, for example.

Advantages of embodiments of the disclosure include providing novel decoupling MIM capacitor **150** designs for interposers **100**. The decoupling MIM capacitors **150** may be formed in any two adjacent metallization layers and provide a large amount of capacitance density. The decoupling MIM capacitors **150** reduce noise and stabilize power signals. The decoupling MIM capacitors **150** are particularly useful in low VDD applications where the signal-noise ratio can be sensitive. The novel decoupling MIM capacitor **150** structures and designs are easily implementable in manufacturing process flows for interposers **100**.

Very high MIM capacitance densities are achievable by embodiments of the present disclosure. For example, if high k materials are used for the capacitor dielectric material **116**, capacitances of about 60 to 200 fF/μm2 may be achieved with an effective oxide thickness (EOT) of the capacitor dielectric material **116** of about 13 Angstroms. Furthermore, the thicknesses of the metallization layers M**1**, V**1**, M**2**, V**2**, and M**3** of the interposers **100** are sufficient, e.g., around 10,000 Angstroms to 20,000 Angstroms in some embodiments, to produce decoupling MIM capacitors **150** having a high capacitance.

Embodiments of the present disclosure include methods of forming decoupling MIM capacitors **150**, and also include interposers **100** and packages **160** that include the decoupling MIM capacitors **150**. Embodiments of the present disclosure also include packaged semiconductor devices **180** that have been packaged using the novel interposers **100** and packages **160** described herein.

In accordance with one embodiment of the present disclosure, a method of forming a decoupling capacitor includes providing a packaging device, and forming a decoupling MIM capacitor in at least two metallization layers of the packaging device.

In accordance with another embodiment, a method of forming a decoupling capacitor in an interposer includes providing a workpiece and forming a first metallization layer over the workpiece. A second metallization layer is formed over the first metallization layer. A decoupling MIM capacitor is formed in the first metallization layer and the second metallization layer.

In accordance with yet another embodiment, an interposer for packaging a semiconductor device includes a workpiece and a plurality of metallization layers disposed over the workpiece. At least one decoupling MIM capacitor is disposed in at least two of the plurality of metallization layers.

In accordance with an embodiment, a method for forming a semiconductor device, the method comprises providing an interposer, the interposer having a first plurality of contact pads and a second plurality of contact pads, the interposer having a decoupling metal-insulator-metal (MIM) capacitor formed thereon, wherein the decoupling MIM capacitor comprises a bottom electrode, a capacitor dielectric over the bottom electrode, and a top electrode over the capacitor dielectric. The method further comprises mounting an integrated circuit die to the second plurality of contact pads, the decoupling MIM capacitor being electrically interposed between the integrated circuit die and a first contact pad of the first plurality of contact pads.

In accordance with another embodiment, a method for forming a semiconductor device, the method comprises providing an interposer. The interposer comprises a first contact pad on a first side of the interposer and a second contact pad on a second side of the interposer, the first contact pad being electrically coupled to the second contact pad. The interposer further comprises a decoupling metal-insulator-metal (MIM) capacitor, the decoupling MIM capacitor being electrically coupled between the first contact pad and the second contact pad, wherein the decoupling MIM capacitor comprises a bottom electrode, a capacitor dielectric over the bottom electrode, and a top electrode over the capacitor dielectric. The

method further comprises electrically coupling an integrated circuit die to the first contact pad on the interposer.

In accordance with yet another embodiment, a method for forming a semiconductor device, the method comprises providing an interposer. The interposer comprises a substrate, one or more metallization layers over the substrate, and a decoupling metal-insulator-metal (MIM) capacitor in the one or more metallization layers, the decoupling MIM capacitor having a first electrode, a second electrode, and a dielectric layer interposed between the first electrode and the second electrode. The interposer further comprises a first contact pad electrically coupled to the first electrode, and a second contact pad electrically coupled to the second electrode. The method further comprises electrically coupling an integrated circuit die to the first contact pad.

In yet another embodiment, a device is provided. The device includes an interposer, a first contact pad, and an integrated circuit die. The interposer includes a substrate, a first metallization layer over the substrate and a second metallization layer over the first metallization layer, and a capacitor in the second metallization layer, the capacitor comprising a bottom electrode, a dielectric over the bottom electrode, and a top electrode over the dielectric. The first contact pad is electrically coupled to the bottom electrode, and the capacitor is electrically coupled between the integrated circuit die and the first contact pad.

In yet another embodiment, a device is provided. The device includes an interposer substrate, a first dielectric layer over the interposer substrate, a second dielectric layer over the first dielectric layer, a first electrode in the second dielectric layer and extending through the first dielectric layer, a capacitor dielectric over the first electrode in the first dielectric layer and the second dielectric layer, and a second electrode over the capacitor dielectric in the first dielectric layer and the second dielectric layer. The device further includes a first via extending through the first dielectric layer, a first conductive line extending through the second dielectric layer, the first conductive line coupled to the first via, and an integrated circuit die electrically coupled to the first conductive line, the first conductive line being interposed between the integrated circuit die and the interposer substrate.

In yet another embodiment, a device is provided. The device includes an interposer having an interposer substrate, a plurality of dielectric layers on a first side of the interposer substrate, contact pads on a second side of the interposer substrate, a capacitor extending through at least a first dielectric layer and a second dielectric layer of the plurality of dielectric layers, and an interconnect extending through the first dielectric layer and the second dielectric layer, the interconnect comprising a via extending through the first dielectric layer and a conductive line extending through the second dielectric layer.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A device comprising:

an interposer, the interposer comprising:

a substrate;

a first metallization layer over the substrate and a second metallization layer over the first metallization layer;

a capacitor in the second metallization layer, the capacitor comprising a bottom electrode, a dielectric over the bottom electrode, and a top electrode over the dielectric; and

a first contact pad electrically coupled to the bottom electrode; and

an integrated circuit die, wherein the capacitor is electrically coupled between the integrated circuit die and the first contact pad.

2. The device of claim **1**, wherein the interposer further comprises a through via, wherein the capacitor is electrically coupled between the integrated circuit die and the through via.

3. The device of claim **1**, further comprising a first via layer interposed between the first metallization layer and the second metallization layer.

4. The device of claim **3**, wherein the bottom electrode extends through the first via layer.

5. The device of claim **4**, further comprising a conductive interconnect, the conductive interconnect comprising a first conductive line in the second metallization layer and a first conductive via extending through the first via layer.

6. The device of claim **1**, further comprising a top plate pick-up, wherein the top plate pick-up extends into the second metallization layer.

7. The device of claim **1**, wherein the interposer is free of active devices.

8. A device comprising:

an interposer substrate;

a first dielectric layer over the interposer substrate;

a second dielectric layer over the first dielectric layer;

a first electrode in the second dielectric layer and extending through the first dielectric layer;

a capacitor dielectric over the first electrode in the first dielectric layer and the second dielectric layer;

a second electrode over the capacitor dielectric in the first dielectric layer and the second dielectric layer;

a first via extending through the first dielectric layer;

a first conductive line extending through the second dielectric layer, the first conductive line coupled to the first via; and

an integrated circuit die electrically coupled to the first conductive line, the first conductive line being interposed between the integrated circuit die and the interposer substrate.

9. The device of claim **8**, wherein the first electrode does not extend to an upper surface of the second dielectric layer.

10. The device of claim **8**, wherein the second electrode extends over a top surface of the second dielectric layer.

11. The device of claim **10**, further comprising a top plate pickup in the second dielectric layer.

12. The device of claim **11**, wherein the second electrode extends laterally over the second dielectric layer to the top plate pickup.

13. The device of claim **8**, wherein an upper surface of the second dielectric layer is level with an upper surface of the second electrode and the capacitor dielectric.

14. The device of claim **13**, wherein the upper surface of the second dielectric layer is level with an upper surface of the first electrode.

15. The device of claim **8**, wherein the second electrode comprises a first metal layer and a second metal layer,

wherein the first metal layer and the second metal layer completely fills an area interposed between opposing sidewalls of the capacitor dielectric.

16. The device of claim **8**, further comprising a third dielectric layer over the second electrode, wherein the third dielectric layer extends into the second dielectric layer.

17. A device comprising:

an interposer, the interposer comprising:

an interposer substrate;

a plurality of dielectric layers on a first side of the interposer substrate;

contact pads on a second side of the interposer substrate;

a capacitor extending through at least a first dielectric layer and a second dielectric layer of the plurality of dielectric layers; and

an interconnect extending through the first dielectric layer and the second dielectric layer, the interconnect comprising a via extending through the first dielectric layer and a conductive line extending through the second dielectric layer.

18. The device of claim **17**, wherein the capacitor comprises:

a first electrode extending along sidewalls and a bottom of an opening in the first dielectric layer and the second dielectric layer, the first electrode not extending to an upper surface of the second dielectric layer;

a capacitor dielectric layer over the first electrode, the capacitor dielectric layer extending to the upper surface of the second dielectric layer; and

a second electrode over the capacitor dielectric layer, the second electrode extending to the upper surface of the second dielectric layer.

19. The device of claim **17**, wherein the capacitor comprises:

a first electrode extending along sidewalls and a bottom of an opening in the first dielectric layer and the second dielectric layer;

a capacitor dielectric layer over the first electrode; and

a second electrode over the capacitor dielectric layer, upper surfaces of the first electrode, the capacitor dielectric layer, and the second electrode being level with an upper surface of the second dielectric layer.

20. The device of claim **17**, wherein the capacitor comprises:

a first electrode extending along sidewalls and a bottom of an opening in the first dielectric layer and the second dielectric layer;

a capacitor dielectric layer over the first electrode, the capacitor dielectric layer extending over an upper surface of the second dielectric layer; and

a second electrode over the capacitor dielectric layer, the second electrode extending over an upper surface of the second dielectric layer.

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