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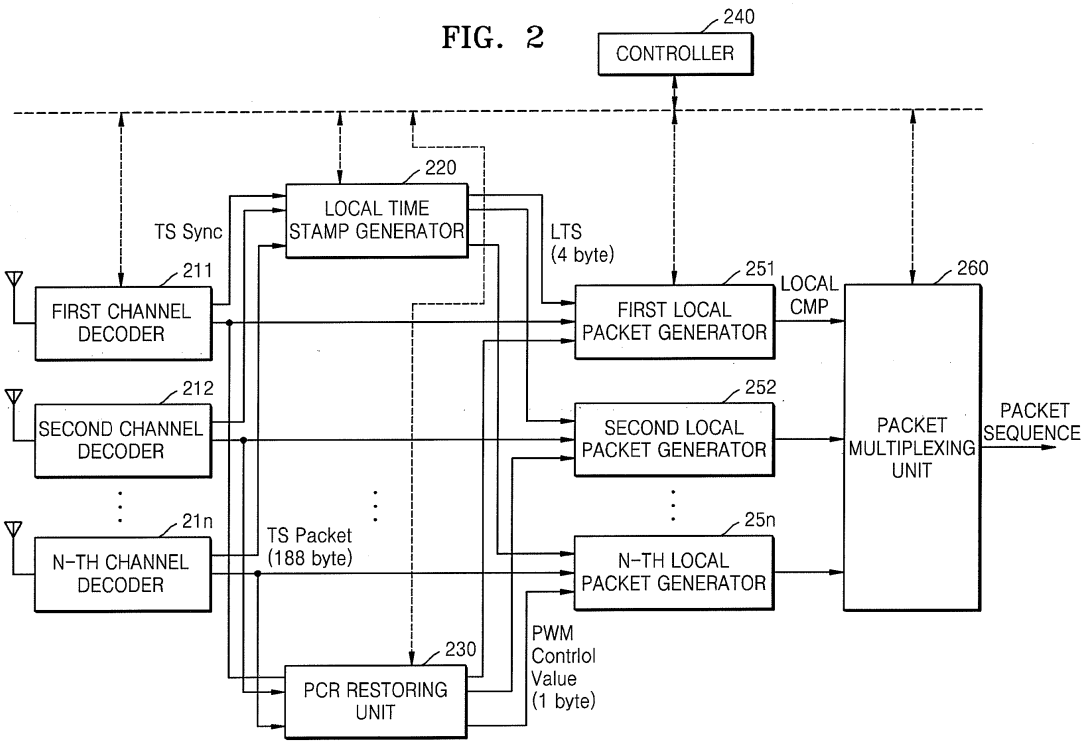
(54) Method and apparatus for multiplexing/de-multiplexing multi-programs

(57) A multi-channel multiplexing/demultiplexing method and apparatus for preventing MPEG jitters from being generated in a digital broadcast, and a multi-channel receiver using the multi-channel multiplexing/demultiplexing apparatus are provided. The multi-channel multiplexing method comprises: extracting a plurality of transport stream packets from a plurality of channel decoders; comparing a reference clock value of each transport stream packet with a system clock value latched by the reference clock value, and generating a system clock control value; inserting the system clock value into a local packet of each channel; and multiplexing a plurality of local packets of a plurality of channels and generating a multi-channel packet.

FIG. 2



EP 1 933 562 A2

Description

[0001] Methods and apparatuses consistent with the present invention relate to a digital broadcast reception/transmission system, and more particularly, to a multi-program multiplexing/demultiplexing method and apparatus for preventing MPEG jitters from being generated in digital broadcasts, and a multimedia receiver performing the multi-program multiplexing/demultiplexing method.

[0002] As digital video/audio compression and digital transmission technologies have been enhanced, digital broadcasts which can provide broadcast services having a higher picture quality, compared to analog broadcasts, and which have high interoperability with digital communication media, digital storage media, etc, have been developed.

[0003] In general, a digital broadcast is transmitted in the form of a transport stream encoded based on the MPEG-2 standard.

[0004] Recently, the number of broadcast channels has gradually been increasing. Accordingly, a system which can store a plurality of broadcast programs received through a plurality of channels while the programs are being watched is needed. In order to meet the need, broadcast receivers having a Picture In Picture (PIP) function and a double window function are being commercialized.

[0005] In general, a cable broadcast system multiplexes programs received through a plurality of channels, and transmits multiplexed transmission streams to a broadcast receiver. At this time, there is a need to minimize Program Clock Reference (PCR) jitters of the multiplexed transmission streams. The PCR is time information for setting a System Time Clock (STC) value of a system decoder to a value suitable for an encoder side.

[0006] FIG. 1 is a timing diagram for explaining a related art multi-program multiplexing method which is performed in a related art cable broadcasting system.

[0007] Referring to FIG. 1, a plurality of channel decoders (not shown) output a plurality of transport stream packets TS1 to TSn, respectively, according to channel characteristics (for example, their transport stream rates). A Cable Card MPEG Packet (CMP) generator (not shown) adds control information to a transport stream of each channel and generates a CMP. A multiplexer (not shown) then multiplexes CMPs of the respective channels and generates a packet sequence.

[0008] The output timing of the multiplexed packet sequence depends on the input order of transport stream packets and the duration of each transport stream packet. However, in the related art multi-program multiplexing method, since uniform time intervals between local transport streams cannot be ensured, MPEG jitters occur. Accordingly, in the related art multi-program multiplexing method, errors occur in clock (27MHz) locking of an MPEG system, due to such MPEG jitters.

[0009] Exemplary embodiments of the present invention overcome the above disadvantages and other disadvantages not described above. Also, the present invention is not required to overcome the disadvantages described above, and an exemplary embodiment of the present invention may not overcome any of the problems described above.

[0010] The present invention provides a multi-program multiplexing/demultiplexing method and apparatus for preventing MPEG jitters from being generated by inserting a system clock control value for each channel into a multi-program packet, in a receiver which receives multi-programs.

[0011] The present invention also provides a digital signal receiver including a multi-program multiplexer/demultiplexer, for preventing MPEG jitters from being generated.

[0012] According to an aspect of the present invention, there is provided a multi-program multiplexing method comprising: extracting a plurality of transport stream packets from a plurality of channel decoders; comparing a reference clock value of each transport stream packet with a system clock value latched by the reference clock value, and generating a system clock control value; inserting the system clock value into a local packet of each channel; and multiplexing a plurality of local packets of a plurality of channels and generating a multi-program packet.

[0013] According to another aspect of the present invention, there is provided a multi-program demultiplexing method comprising: receiving a multi-program packet into which a system clock control value for each channel is inserted; extracting the system clock control value and a local transport identifier (ID) from the multi-program packet; extracting a local transport stream packet according to the local transport ID, and linking the local transport stream packet with a corresponding system clock control value; and controlling a system clock signal with reference to a system clock control value corresponding to the local transport stream packet.

[0014] According to another aspect of the present invention, there is provided a multi-program multiplexing apparatus comprising: at least one channel decoder unit selecting a broadcast signal of a desired channel from among a plurality of broadcast signals of a plurality of channels, and extracting a transport stream packet from the broadcast signal of the desired channel; a local time stamp generating unit generating a local time stamp according to a synchronization signal of the transport stream packet; a reference clock restoring unit comparing a reference clock value of the transport stream packet, with a system clock value latched by the reference clock value, and generating a system clock control value; a local packet generating unit generating a local packet for each channel, on the basis of the transport stream packet, the local time stamp, and the system clock control value; and a multiplexing unit receiving and multiplexing a plurality of local packets for a plurality of channels, and generating a packet sequence which is synchronized at

an output frequency.

[0015] According to another aspect of the present invention, there is provided a multi-program demultiplexing apparatus comprising: a packet demultiplexing unit extracting a local transport ID and a system clock control value, from a multi-program packet into which a system clock control value for each channel is inserted; a transport stream demultiplexing unit extracting a local transport stream packet according to the local transport ID; and a clock controller controlling a system clock signal for each channel according to the system clock control value for each channel.

[0016] The above and other aspects of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a timing diagram for explaining a related art multi-program multiplexing method which is performed by a related art cable broadcast system;

FIG. 2 is a block diagram of a multi-program multiplexing apparatus according to an exemplary embodiment of the present invention;

FIG. 3 illustrates a signal format generated by local packet generators, according to an exemplary embodiment of the present invention;

FIG. 4 is a detailed block diagram of a Program Clock Reference (PCR) restoring unit illustrated in FIG. 2;

FIG. 5 is a flowchart of a multi-program multiplexing method according to an exemplary embodiment of the present invention;

FIG. 6 is a block diagram of a multi-program demultiplexing apparatus according to an exemplary embodiment of the present invention; and

FIG. 7 is a flowchart of a multi-program demultiplexing method according to an exemplary embodiment of the present invention.

[0017] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the appended drawings.

[0018] A multi-program multiplexing/demultiplexing apparatus according to an exemplary embodiment of the present invention is installed in a receiver. Accordingly, the receiver inserts a clock control value into each transport stream (TS) packet received through a plurality of channels in order to multiplex transport stream packets, and then demultiplexes the multiplexed TS packets. The receiver then generates a system time clock signal (hereinafter, referred to as a system clock signal) of 27 MHz that is to be synchronized with an oscillation frequency of 27 MHz which is used in a transmitter, in order to correctly restore a received signal. Accordingly, the transmitter transmits a Program Clock Reference (PCR) signal to the receiver so that a Phase Locked Loop (PLL) circuit of the receiver that will restore the system clock signal of 27 MHz can use the PCR signal as a reference clock signal.

[0019] FIG. 2 is a block diagram of a multi-program multiplexing apparatus according to an exemplary embodiment of the present invention.

[0020] Referring to FIG. 2, the multi-program multiplexing apparatus includes first, second, through to n-th channel decoders 211, 212, through to 21n, a local time stamp generator 220, a Program Clock Reference (PCR) restoring unit 230, first, second, through to n-th local packet generators 251, 252, through to 25n, a controller 240, and a packet multiplexing unit 260.

[0021] The first through n-th channel decoders 211 through 21n select broadcast signals of desired channels from among a plurality of broadcast signals received through a plurality of antennas, and extracts MPEG TS packets from the broadcast signals. Each MPEG TS packet includes a header area and a payload area. The header area includes 4 bits of a header and an additional header having a PCR value, and the payload area includes 188 bytes of video/audio signals. The header also includes a synchronization signal indicating a start location of the MPEG TS packet.

[0022] The local time stamp generator 220 generates a local time stamp value for the MPEG TS packet of each channel extracted by the first through n-th channel decoders 211 through 21n, according to the synchronization signal of the MPEG TS packet of each channel. Here, 4 bytes are assigned to the local time stamp value.

[0023] The PCR restoring unit 230 extracts a PCR value from the MPEG TS packet extracted by the first through n-th decoders 211 through 21n, compares a System Time Clock (STC) value latched (e.g., stored or saved) when the PCR value is extracted, and generates a Pulse Width Modulation (PWM) control value. The STC value is system clock information for lip synchronization of a received audio/video signal. The PWM control value represents the characteristic of a system clock signal for each channel.

[0024] The first through n-th packet generators 251 through 25n generate a local packet for each channel, using the 188 bytes of the MPEG TS packets generated by the first through n-th channel decoders 211 through 21n, the local time stamp value for each channel generated by the local time stamp generator 220, the PWM control value generated by the PCR restoring unit 230, and additional information generated by the controller 240. The local packet may be a Cable Card MPEG Packet (CMP) which is applied to a cable broadcast receiver.

[0025] The packet multiplexing unit 260 multiplexes local packets of n channels generated by the first though n-th local packet generators 251 through 25n, and generates a packet sequence which is synchronized at an output frequency.

[0026] The controller 240 controls the operation of the first through n-th channel decoders 211 through 21n, the local time stamp generator 220, the reference clock restoring unit 230, the first through n-th local packet generators 251 through 25n, and the packet multiplexing unit 260, and generates additional information.

[0027] FIG. 3 illustrates a signal format of a local packet generated by the first through n-th local packet generators 251 through 25n, according to an exemplary embodiment of the present invention.

[0028] Referring to FIG. 3, the local packet includes a header and an MPEG TS packet. The header includes 8 bits of a local TS ID area (LTSID), 24 bits of a reserved area (Res), 32 bits of a local time stamp area (LTS), 16 bits of a reserved area (Res), 8 bits of a PWM control value area (PWMV), and 8 bits of a Cyclic Redundancy Check (CRC) value. The MPEG TS packet includes 188 bytes of payload data.

[0029] FIG. 4 is a detailed view of the PCR restoring unit 230 illustrated in FIG. 2.

[0030] Referring to FIG. 4, the PCR restoring unit 230 includes first, second, through to n-th PCR extractors 410, 411, through to 41n, first, second, through to n-th STC generators 421, 422, through to 42n, and first, second, through to n-th PWM control value generators 431, 432, through to 43n.

[0031] The first through n-th PCR extractors 410 through 41n extract PCR values from the 188 bytes of TS packets received through a plurality of channels.

[0032] The first through n-th STC generators 421 through 42n latch STC values, when the PCR values extracted by the first through n-th PCR extractors 410 through 41n are output.

[0033] The first through n-th PWM control value generators 431 through 43n compare the PCR values extracted by the first through n-th PCR extractors 410 through 41 n with the STC values latched by the first through n-th STC generators 421 through 42n, generate error values according to the comparison result, and convert the error values into PWM control values. Accordingly, the first through n-th PWM control value generators 431 through 43n generate PWM control values, each PWM control value having 1 byte corresponding to a clock control value for each channel.

[0034] FIG. 5 is a flowchart of a multi-program multiplexing method according to an exemplary embodiment of the present invention.

[0035] First, a plurality of TS packets are respectively extracted from a plurality of channel decoders (operation 510).

[0036] Successively, it is determined whether a PCR value exists in each TS packet (operation 520).

[0037] If a PCR value exists in a TS packet, the PCR value is extracted from the TS packet (operation 530). Meanwhile, if no PCR value exists in any TS packet, packet multiplexing is performed (operation 560).

[0038] When the PCR value is extracted, a STC value is latched (operation 530).

[0039] Then, the PCR value extracted for each channel is compared with the latched STC value, an error value is generated according to the comparison result, and a PWM control value corresponding to the error value is calculated (operation 540). The PWM control value corresponds to a control value of a system clock signal.

[0040] Then, the PWM control value is inserted into the corresponding local packet (operation 550).

[0041] Accordingly, a local packet, as illustrated in FIG. 3, includes an MPEG TS packet generated by the corresponding channel decoder, a local time stamp value LTS, a PWM control value PWMV, etc.

[0042] Successively, local packets of a plurality of channels are multiplexed, and a multi-program packet which is synchronized at an output frequency is generated (operation 560).

[0043] FIG. 6 is a block diagram of a multi-program demultiplexing apparatus according to an exemplary embodiment of the present invention.

[0044] Referring to FIG. 6, the multi-program demultiplexing apparatus includes a packet demultiplexing unit 610, first, second, through to n-th TS demultiplexing units 621, 622, through to 62n, first, second, through to n-th PWM controllers 631, 632, through to 63n, first, second, through to n-th buffer units 641, 642, through to 64n, and first, second, through to n-th system clock units 651, 652, through to 65n.

[0045] The packet demultiplexing unit 610 extracts a header from a received multi-packet sequence, and divides the multi-packet sequence into a plurality of local TS packets according to LTSID. Also, the packet demultiplexing unit 610 extracts a PWM control value for each local channel from the header.

[0046] The first through n-th TS demultiplexing units 621 through 62n parse the TS packets for respective channels extracted by the packet demultiplexing unit 610, to Elementary Streams (ESs), section streams, etc., according to audio data, video data, Program Specific Information (PSI), etc.

[0047] Each of the first through n-th PWM controllers 631 through 63n includes a PWM generator (not shown) and a Low Pass Filter (LPF) (not shown), generates a PWM signal according to a PWM control value of each channel extracted by the packet demultiplexing unit 610, performs low-pass filtering on the PWM signal, and generates an analog voltage signal.

[0048] The first through n-th system clock units 651, 652, through to 65n drive a voltage controlled crystal oscillator (VCXO) (not shown) according to analog voltage signals generated by the first through n-th PWM controllers 631 through 63n, and generate system clock signals for the respective local channels through the VCXO. The system clock signals restore video/audio signals for the respective local channels.

[0049] The first through n-th buffer units 641 through 64n store the ESs or section streams parsed by the first through n-th TS demultiplexing units 621 through 62n.

[0050] FIG. 7 is a flowchart of a multi-program demultiplexing method according to an exemplary embodiment of the present invention.

[0051] First, a multi-program packet into which a PWM control value is inserted for each channel is received (operation 710).

[0052] Successively, a local TS ID and a PWM control

value are extracted from the multi-program packet (operation 720).

[0053] A local TS packet is then extracted according to the local TS ID (operation 730), and the local TS packet is linked with the corresponding PWM control value (operation 740).

[0054] Next, a system clock signal is controlled using a PWM control value corresponding to the local TS packet that is to be reproduced (operation 750).

[0055] The exemplary embodiments of the present invention can also be embodied as computer readable codes on a computer readable recording medium. The computer readable recording medium is any data storage device that can store data which can be thereafter read by a computer system. Examples of the computer readable recording medium include read-only memory (ROM), random-access memory (RAM), CD-ROMs, magnetic tapes, floppy disks, and optical data storage devices. The computer readable recording medium can also be distributed over network coupled computer systems so that the computer readable code is stored and executed in a distributed fashion.

[0056] As described above, according to the exemplary embodiments of the present invention, in a receiver which receives multi-programs through a plurality of channels, compares a PCR with an STC for each channel and inserts a PWM control value corresponding to a clock error into a multi-program packet, it is possible to prevent clock locking errors from being generated due to MPEG jitters generated in multi-program multiplexing.

[0057] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the scope of the present invention as defined by the following claims.

Claims

1. A multi-channel multiplexing method comprising:

extracting a plurality of transport stream packets from a plurality of channel decoders (211, 212... 21n) each corresponding to a channel;
comparing reference clock values of the plurality of transport stream packets with system clock values, and generating system clock control values;
generating a plurality of local pakets from the transport stream packets for each channel;
inserting the system clock values into the local packets; and
multiplexing local packets of the plurality of channels to generate a multi-channel packet.

2. The multi-channel multiplexing method of claim 1, wherein the system clock control values are pulse-width modulation (PWM) control values.

3. The multi-channel multiplexing method of claim 1 or 2 further comprising:

extracting the reference clock values from the plurality of transport stream packets and;
latching the system clock values when the reference clock values are extracted, wherein the comparing comprises comparing the reference clock values with the system clock values and generating error values according to a result of the comparing; and
the generating the system clock control values comprises generating the system clock control values for the channels based on the error values.

4. The multi-channel multiplexing method of any one of the preceding claims, wherein the system clock control values are pulse-width modulation (PWM) control values for controlling errors of system clock signals.

5. The multi-channel multiplexing method of any one of the preceding claims, wherein each one of the plurality of the local packets includes a transport stream, a local time stamp, and a system clock control value, for one of the channels.

6. A multi-channel demultiplexing method comprising:

receiving a multi-channel packet into which a system clock control value for a channel is inserted;
extracting the system clock control value and a local transport identifier (ID) from the multi-channel packet;
extracting a local transport stream packet according to the local transport ID, and linking the local transport stream packet with the system clock control value; and
controlling a system clock signal with reference to the system clock control value corresponding to the local transport stream packet.

7. A multi-channel multiplexing apparatus comprising:

a plurality of channel decoder units (211, 212... 21n) configured to select a broadcast signal of a plurality of desired channels respectively from among a plurality of broadcast signals, each configured to extract a transport stream packet from the broadcast signal of one of the desired channels;
a local time stamp generating unit (220) configured to generate a local time stamp, according

to a synchronization signal of each extracted transport stream packet;
a reference clock restoring unit (230) configured to compare a reference clock value of each transport stream packet, with a system clock value, and generate a system clock control value;
a local packet generating unit (251, 252 ... 25n) configured to generate a local packet for each desired channel, based on each transport stream packet, local time stamp, and system clock control value; and
a multiplexing unit (260) configured to receive and multiplex a plurality of local packets for a plurality of desired channels, and generate a packet sequence which is synchronized at an output frequency.

8. The multi-channel multiplexing apparatus of claim 7, wherein the reference clock restoring unit (230) comprises:

a reference clock extracting unit (410, 411 ... 41n) configured to extract the reference clock value from each transport stream packet for each desired channel;
a system clock generator (421, 422 ... 32n) configured to latch the system clock value when the reference clock value is extracted; and
a clock control value generator (431, 432 ... 43n) configured to compare the reference clock value with the system clock value to generate a result, generate an error value according to the result, and generate the system clock control value for the one desired channel based on the error value.

9. A multi-channel demultiplexing apparatus comprising:

a packet demultiplexing unit (610) configured to extract a local transport identifier (ID) and a system clock control value, from a multi-channel packet into which a system clock control value for a desired channel is inserted;
a transport stream demultiplexing unit (621, 622 ... 62n) configured to extract a local transport stream packet according to the local transport ID; and
a clock controller (631, 632 ... 63n) configured to control a system clock signal for the desired channel, according to the system clock control value for the desired channel.

10. The multi-channel demultiplexing apparatus of claim 9, wherein the clock controller (631, 632 ... 63n) comprises:

a pulse-width modulator (PWM) generator configured to generate a pulse-width modulation signal, according to the system clock control value for the desired channel; and
a low-pass filter configured to perform low-pass filtering on the PWM signal.

11. A multi-channel receiving apparatus comprising:

a multiplexing unit configured to extract transport stream packets through a plurality of channel decoders, compare reference clock values of the plurality of transport stream packets with system clock values to generate a comparison result, generate system clock control values according to the comparison result, insert the system clock control values into local packets for desired channels, multiplexe the local packets of the desired channels, and generate a multi-channel packet; and
a demultiplexing unit configured to receive the multi-channel packet into which the system clock control values for the desired channels are inserted, from the multiplexing unit, extract local transport identifiers (IDs) and the system clock control values from the multi-channel packet, extract the local packets according to the local transport IDs, link the local packets with the system clock control values, and control system clock signals with reference to the system clock control values which correspond to the local packets.

FIG. 1 (RELATED ART)

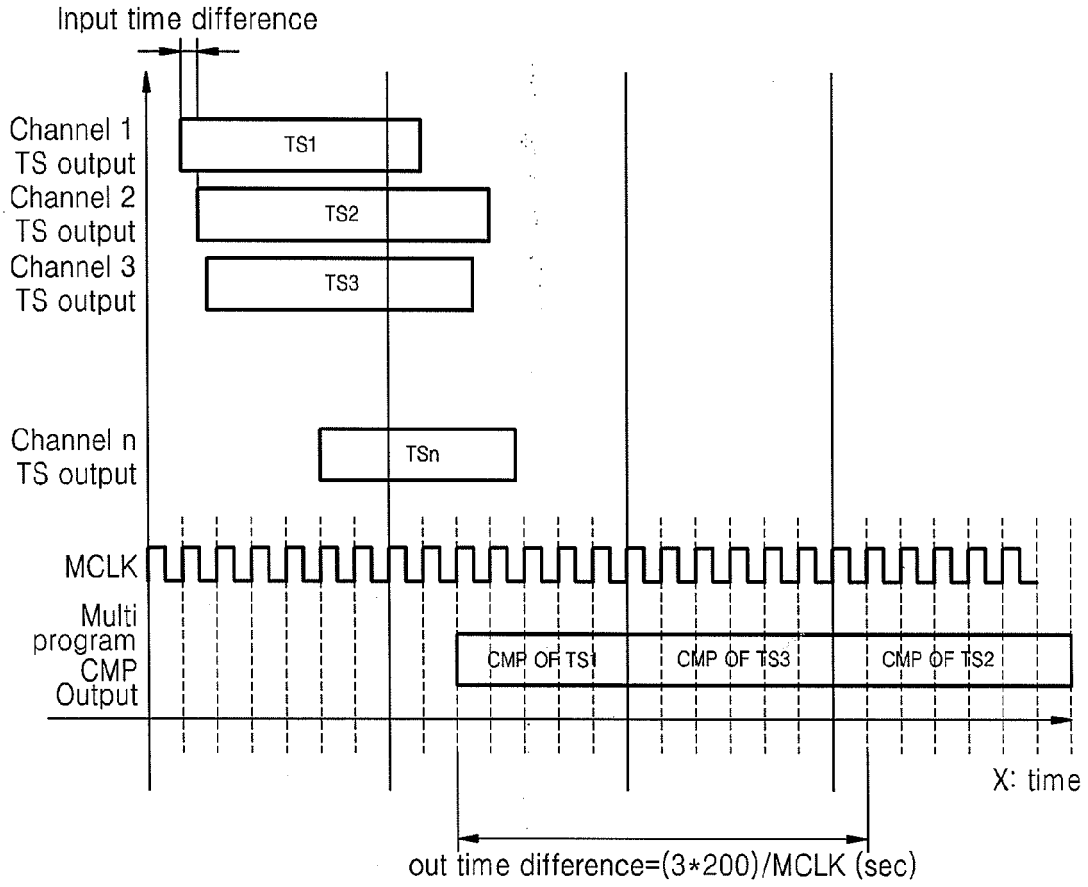


FIG. 2

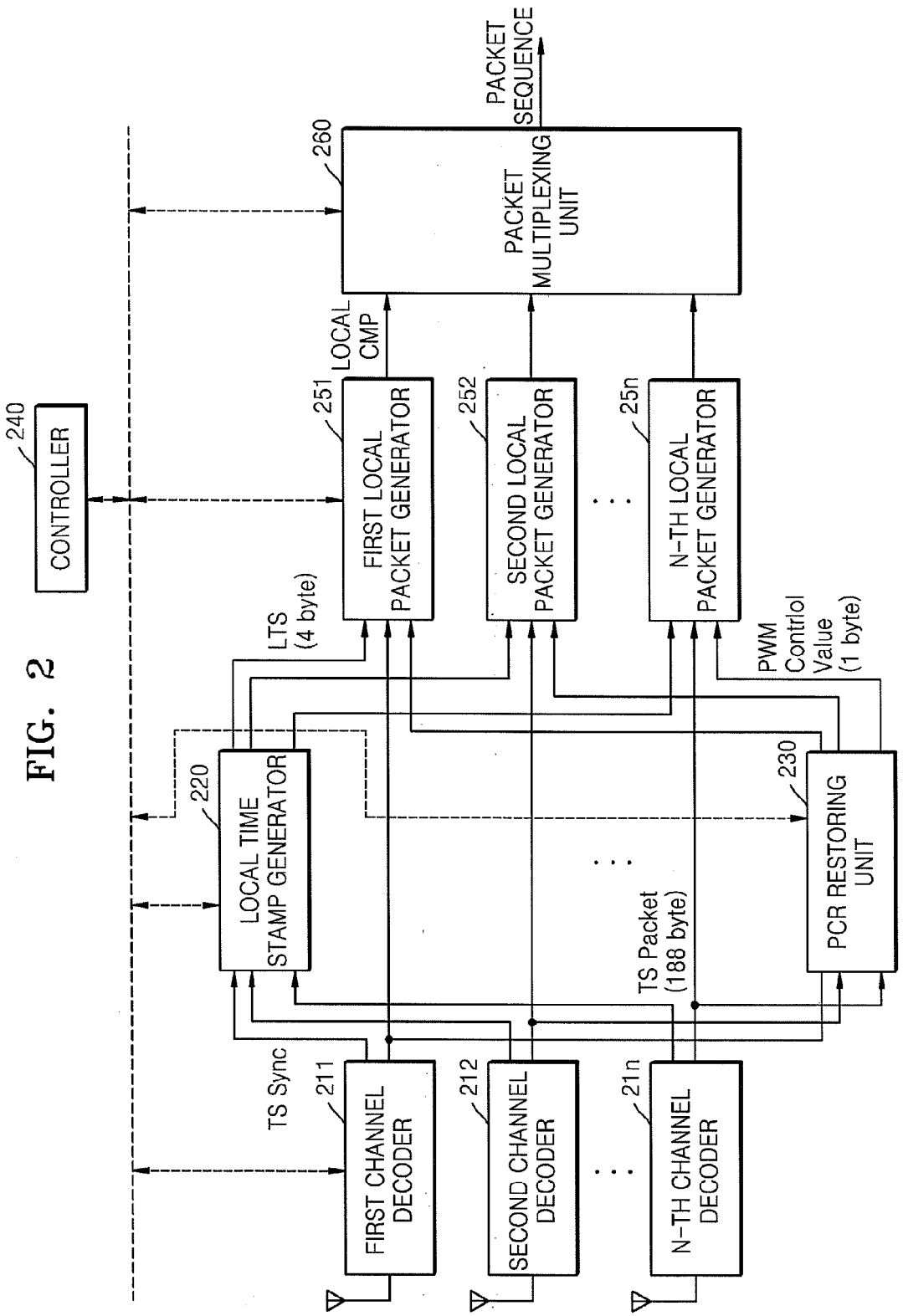

PACKET SEQUENCE
260
PACKET MULTIPLEXING UNIT
LOCAL CMP
240
CONTROLLER
251
FIRST LOCAL PACKET GENERATOR
252
SECOND LOCAL PACKET GENERATOR
25n
N-TH LOCAL PACKET GENERATOR
LTS (4 byte)
PWM Control Value (1 byte)
220
LOCAL TIME STAMP GENERATOR
230
PCR RESTORING UNIT
TS Packet (188 byte)
TS Sync
211
FIRST CHANNEL DECODER
212
SECOND CHANNEL DECODER
21n
N-TH CHANNEL DECODER

FIG. 3

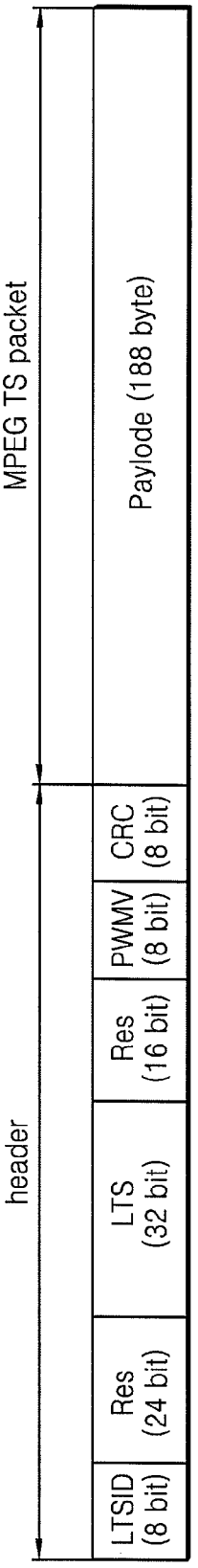

MPEG TS packet
header
LTSID (8 bit)
Res (24 bit)
LTS (32 bit)
Res (16 bit)
PWMV (8 bit)
CRC (8 bit)
Paylode (188 byte)

FIG. 4

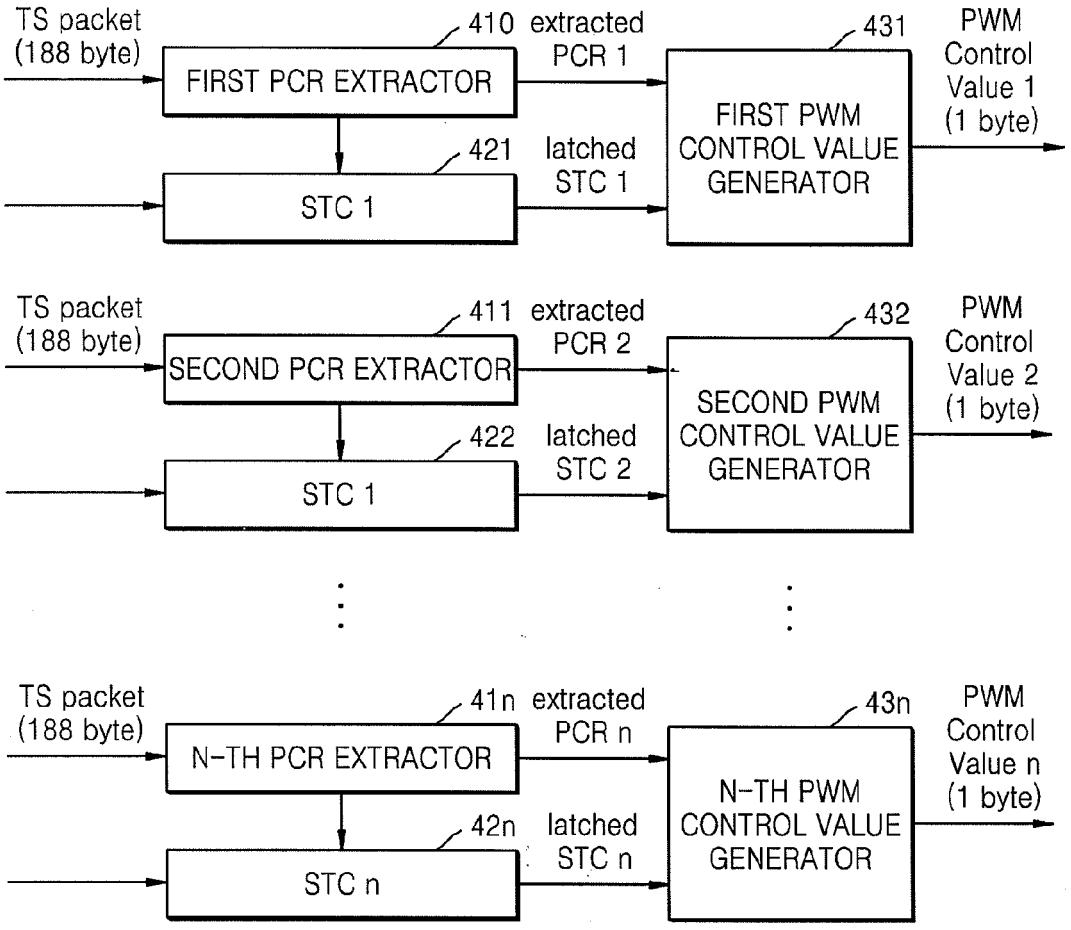

TS packet
(188 byte)
410
FIRST PCR EXTRACTOR
extracted
PCR 1
431
FIRST PWM
CONTROL VALUE
GENERATOR
PWM
Control
Value 1
(1 byte)
421
STC 1
latched
STC 1
TS packet
(188 byte)
411
SECOND PCR EXTRACTOR
extracted
PCR 2
432
SECOND PWM
CONTROL VALUE
GENERATOR
PWM
Control
Value 2
(1 byte)
422
STC 1
latched
STC 2
TS packet
(188 byte)
41n
N-TH PCR EXTRACTOR
extracted
PCR n
43n
N-TH PWM
CONTROL VALUE
GENERATOR
PWM
Control
Value n
(1 byte)
42n
STC n
latched
STC n

FIG. 5

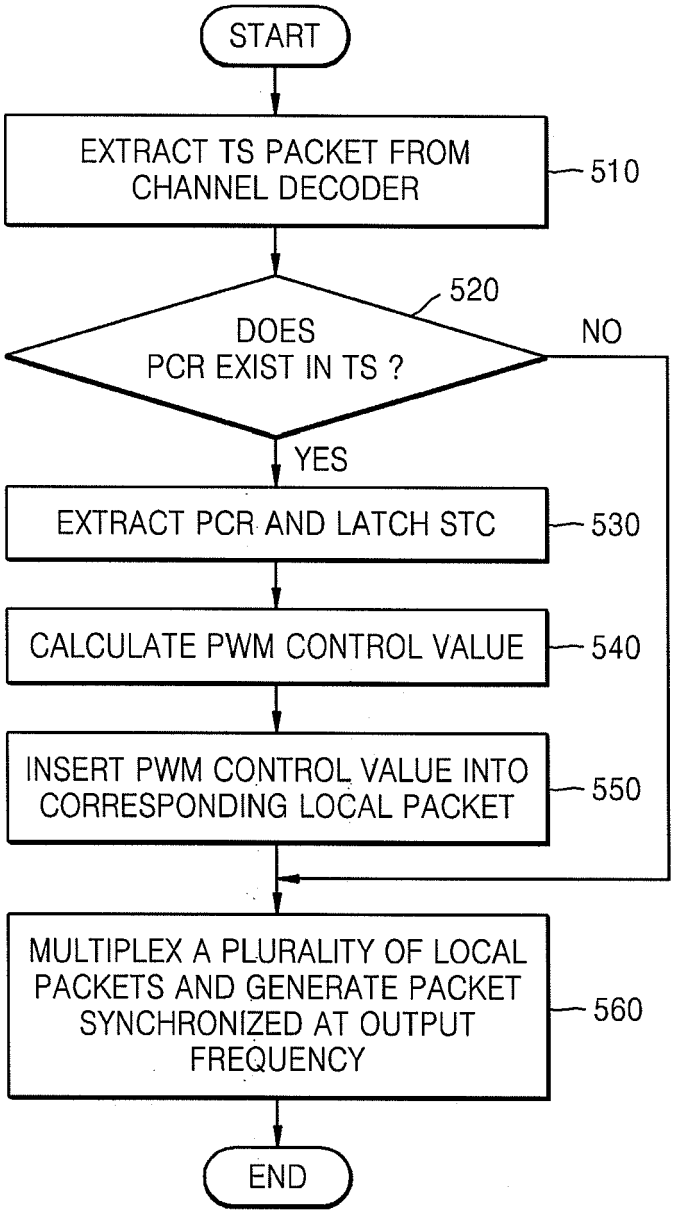

START
EXTRACT TS PACKET FROM CHANNEL DECODER
510
DOES PCR EXIST IN TS ?
520
NO
YES
EXTRACT PCR AND LATCH STC
530
CALCULATE PWM CONTROL VALUE
540
INSERT PWM CONTROL VALUE INTO CORRESPONDING LOCAL PACKET
550
MULTIPLEX A PLURALITY OF LOCAL PACKETS AND GENERATE PACKET SYNCHRONIZED AT OUTPUT FREQUENCY
560
END

FIG. 6

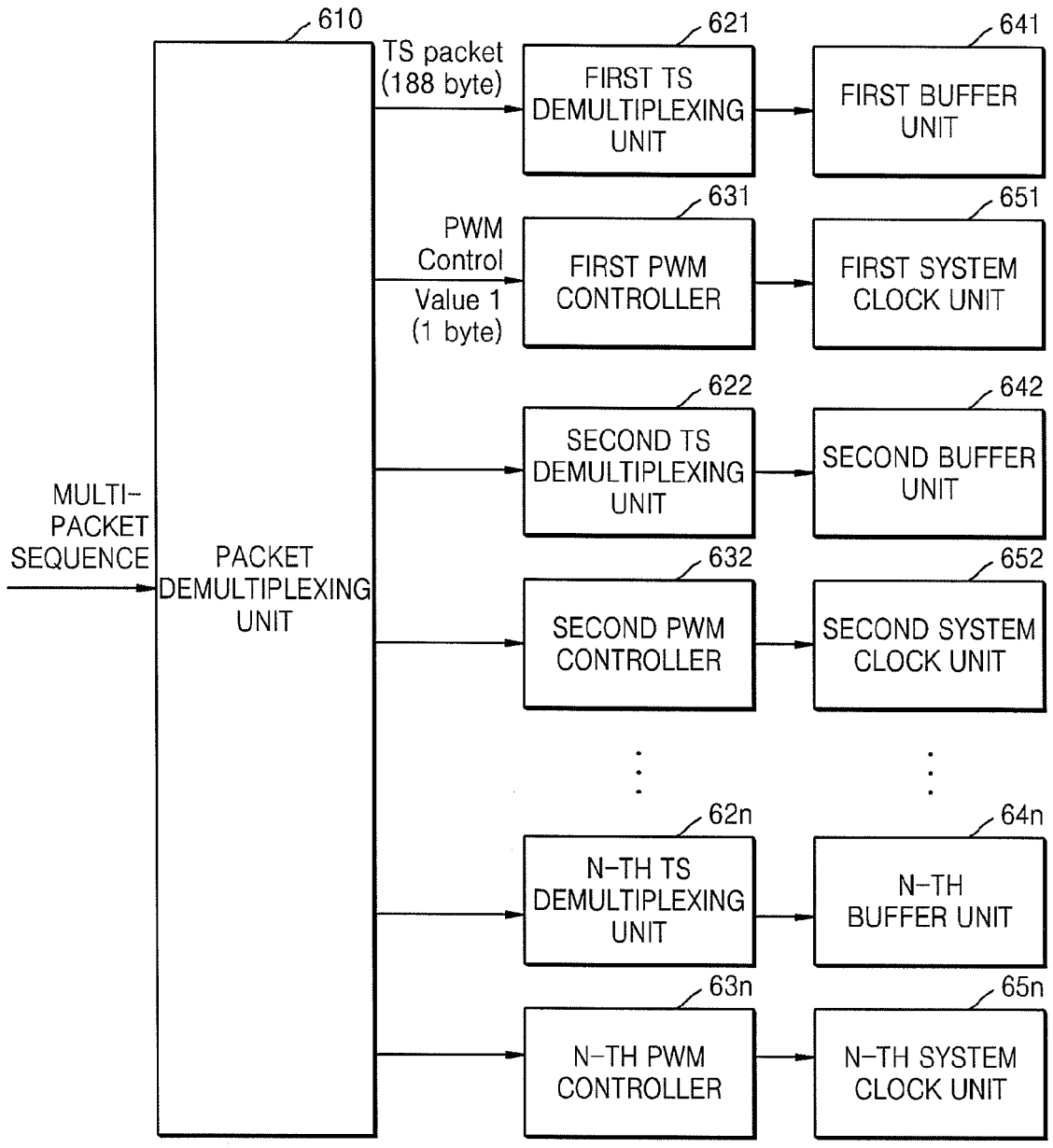
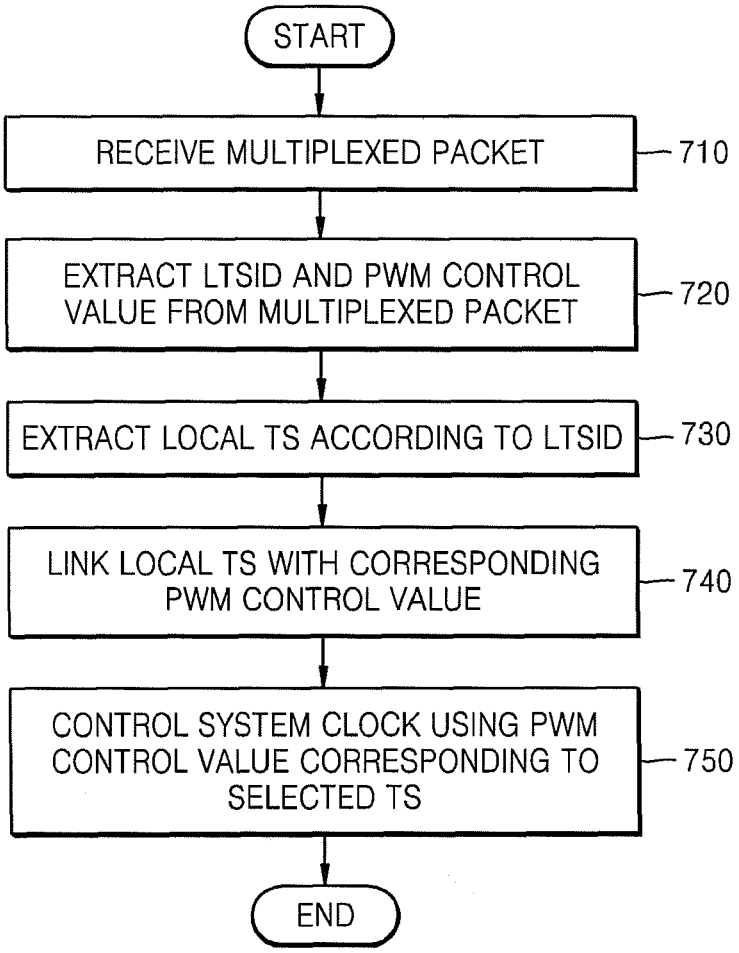

610
MULTI-PACKET SEQUENCE
PACKET DEMULTIPLEXING UNIT
TS packet (188 byte)
PWM Control Value 1 (1 byte)
621
FIRST TS DEMULTIPLEXING UNIT
641
FIRST BUFFER UNIT
631
FIRST PWM CONTROLLER
651
FIRST SYSTEM CLOCK UNIT
622
SECOND TS DEMULTIPLEXING UNIT
642
SECOND BUFFER UNIT
632
SECOND PWM CONTROLLER
652
SECOND SYSTEM CLOCK UNIT
62n
N-TH TS DEMULTIPLEXING UNIT
64n
N-TH BUFFER UNIT
63n
N-TH PWM CONTROLLER
65n
N-TH SYSTEM CLOCK UNIT

FIG. 7


START
RECEIVE MULTIPLEXED PACKET
710
EXTRACT LTSID AND PWM CONTROL VALUE FROM MULTIPLEXED PACKET
720
EXTRACT LOCAL TS ACCORDING TO LTSID
730
LINK LOCAL TS WITH CORRESPONDING PWM CONTROL VALUE
740
CONTROL SYSTEM CLOCK USING PWM CONTROL VALUE CORRESPONDING TO SELECTED TS
750
END