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(54) **BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANAR INTRINSIC GETTERING ZONE**

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Related U.S. Application Data

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(51) **Int. Cl.**⁷ **H01L 27/01**; H01L 27/12; H01L 31/0392

(52) **U.S. Cl.** **257/347**; 438/455; 438/458; 438/474; 438/977

(58) **Field of Search** 148/33, 33.2-33.5; 27/347, 349, 352; 438/455, 458, 459, 474, 475, 514, 518, 526, 530, 531, 977

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,608,096 A 8/1986 Hill

5,063,113 A	11/1991	Wada	
5,229,305 A *	7/1993	Baker	438/459
5,334,273 A	8/1994	Short et al.	
5,374,564 A	12/1994	Bruel	
5,661,044 A	8/1997	Holland et al.	
5,731,637 A	3/1998	Hori et al.	
5,882,987 A	3/1999	Srikrishnan	
6,046,095 A *	4/2000	Horikawa	438/471
6,083,324 A *	7/2000	Henley et al.	148/33.2
6,245,161 B1 *	6/2001	Henley et al.	148/33.4
6,255,195 B1 *	7/2001	Linn et al.	438/455
6,368,938 B1 *	4/2002	Usenko	438/407

* cited by examiner

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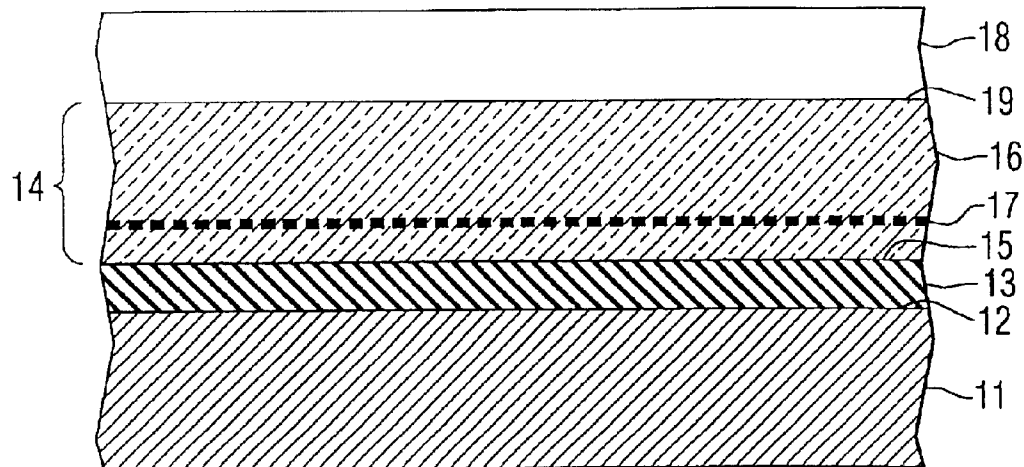
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(57) **ABSTRACT**

A bonded semiconductor-on-insulator substrate for an integrated circuit. The bonded semiconductor-on-insulator substrate includes a wafer, a handle wafer and an insulating bond layer. The wafer has a first layer of monocrystalline semiconductor material adjacent a first surface of the wafer. The wafer also has a second layer of undamaged by implantation monocrystalline semiconductor material adjacent a second surface of the wafer. The wafer further has a substantially planar intrinsic gettering zone of substantially pure semiconductor material and active gettering sites positioned between the first and second layers formed by implanting ions of the semiconductor material through the first layer of monocrystalline semiconductor material. The insulating bond layer bonds the handle wafer to the first surface of the wafer.

32 Claims, 4 Drawing Sheets



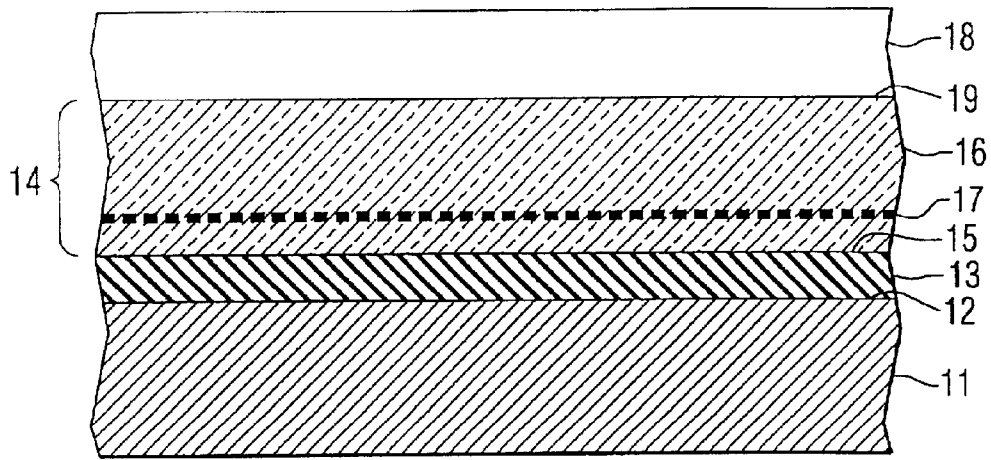


FIG. 1 10

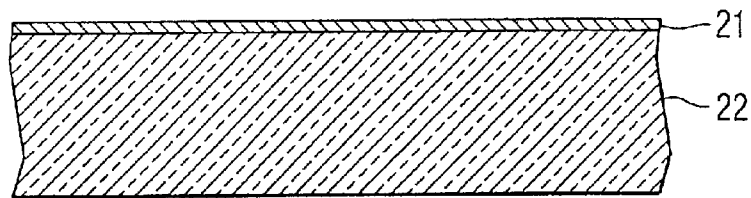


FIG. 2A

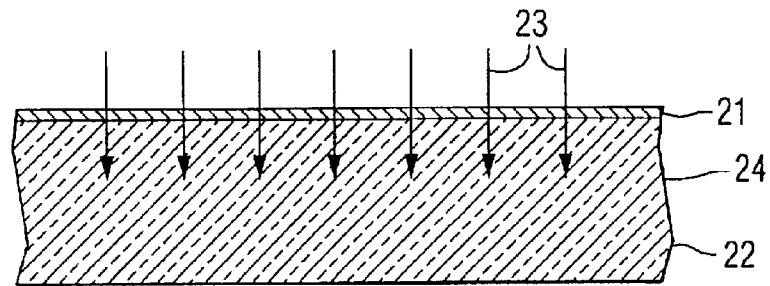


FIG. 2B

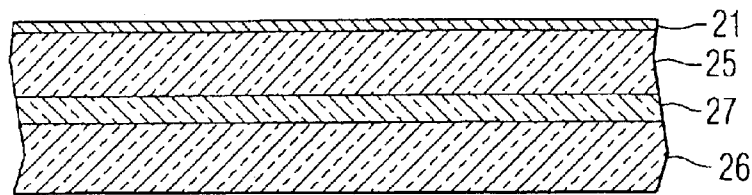


FIG. 2C

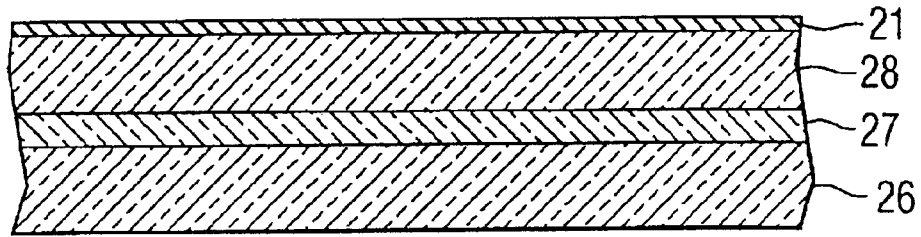


FIG. 2D

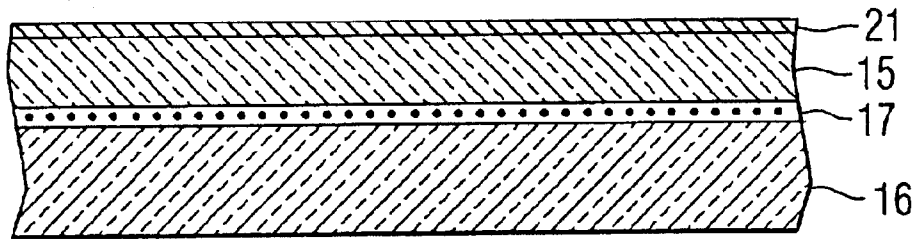


FIG. 2E

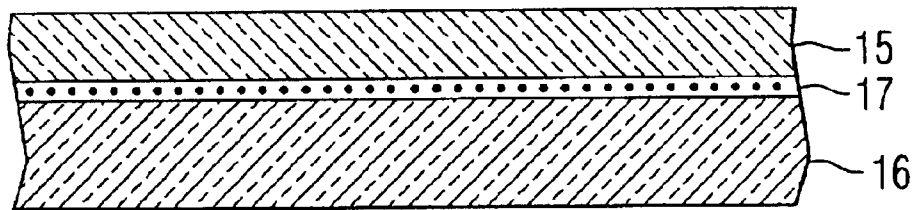


FIG. 2F

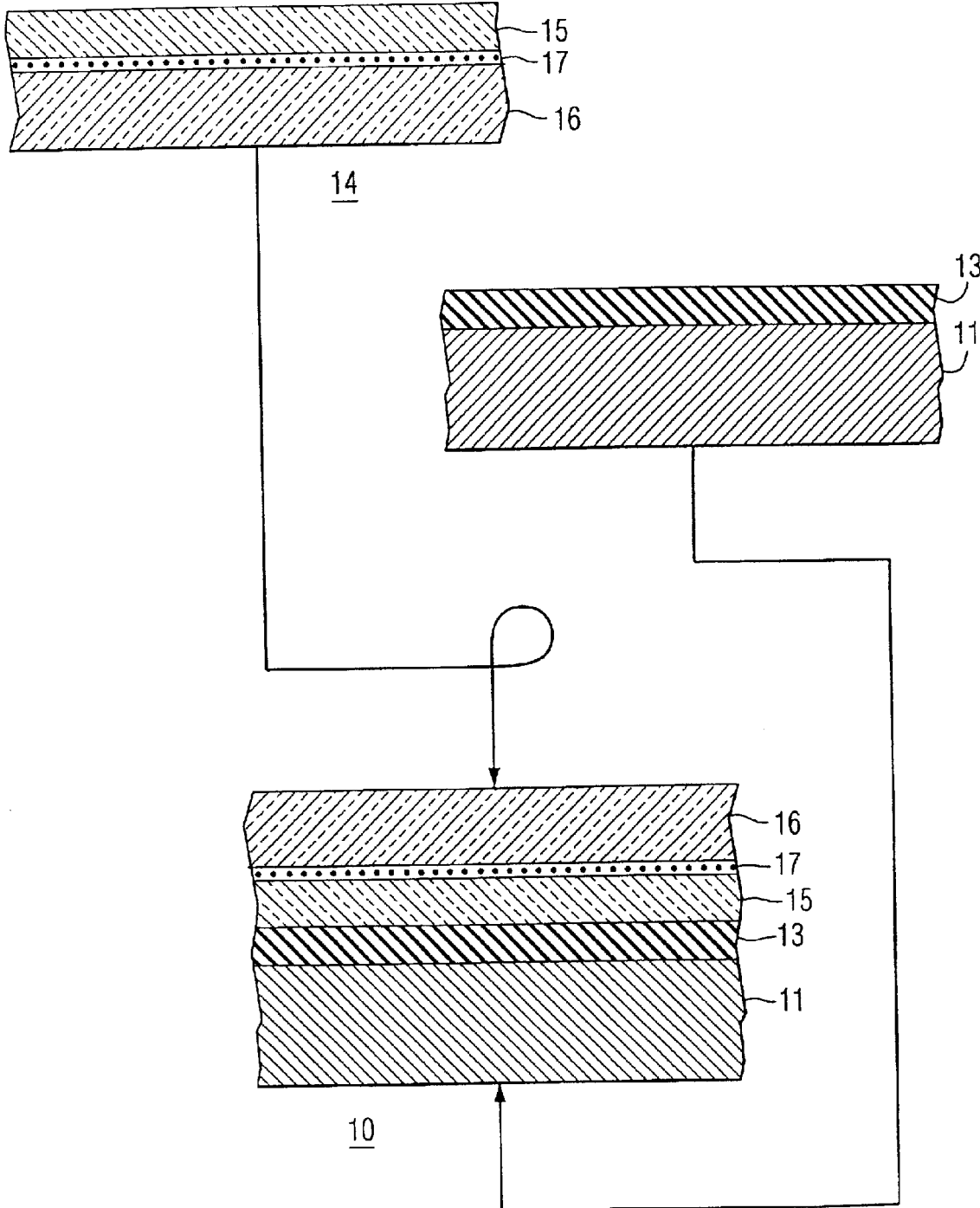


FIG. 3

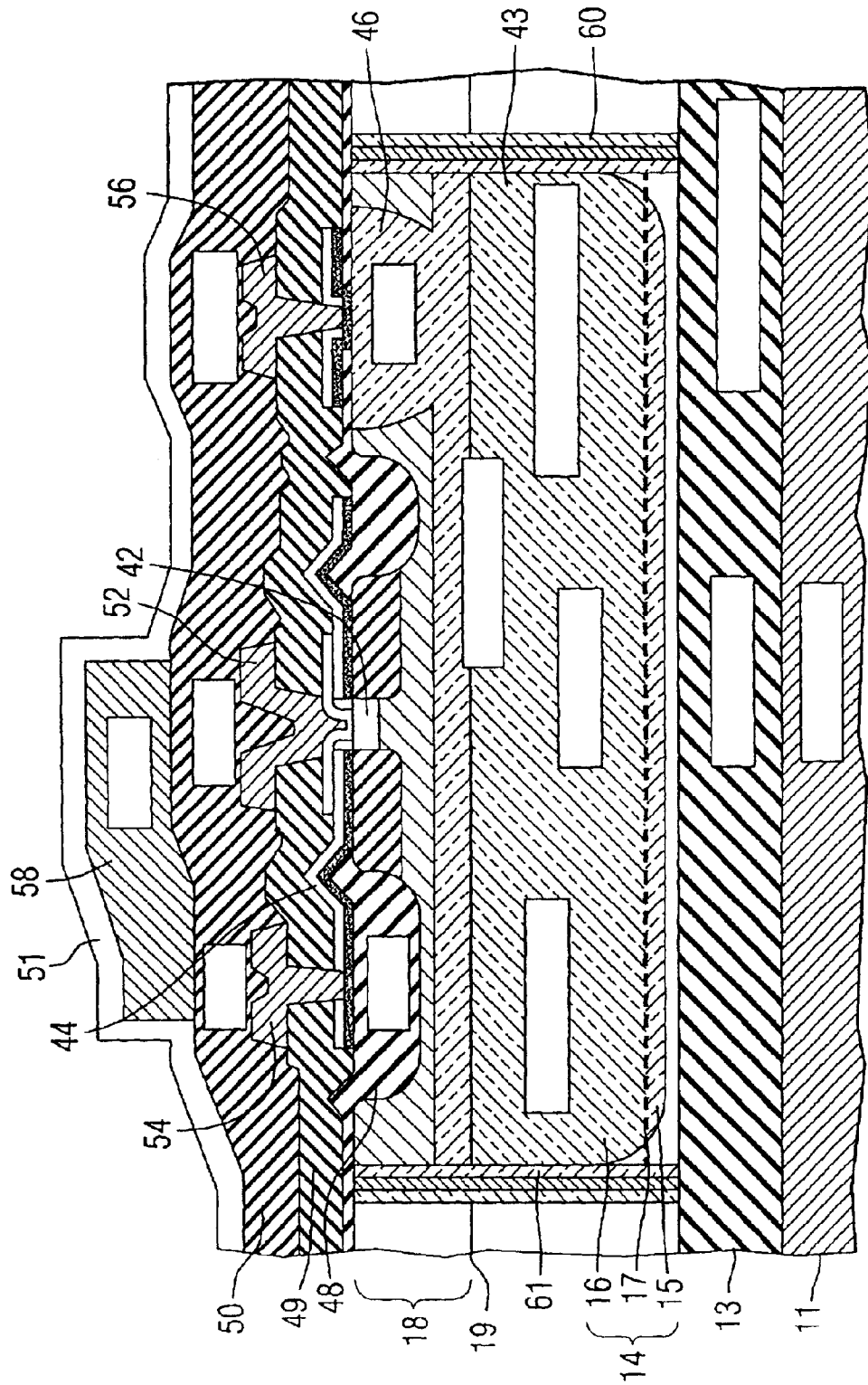


FIG. 4

BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANAR INTRINSIC GETTERING ZONE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional application of U.S. patent application Ser. No. 09/255,231, filed Feb. 22, 1999 now U.S. Pat. No. 6,255,195.

FIELD OF THE INVENTION

The present invention relates to gettering in a semiconductor device and, more particularly, to a process for forming a bonded semiconductor-on-insulator substrate containing a planar intrinsic gettering zone and to a semiconductor device and an integrated circuit formed on the bonded substrate.

BACKGROUND OF THE INVENTION

During integrated circuit manufacture and processing, a silicon wafer may be exposed to metallic contaminants such as iron, nickel, zinc, chromium, and the like that may ultimately degrade the final product yield, performance, or reliability. This contamination may occur through contact with stainless steel wafer handlers and tools, diffusion of metallic substances from heater coils or lamps in high temperature processing chambers, or sputter debris dislodging from plasma chamber walls.

Gettering is a term that refers generally to any mechanism by which contaminating impurities, typically transition metals, are removed from sensitive semiconductor device regions and entrapped in other relatively benign domains of the wafer. Gettering is described in Wolf and Tauber, *Silicon Processing in the VLSI Era*, Vol. 1, 1986, Lattice Press, pp 61-70.

Gettering typically proceeds in three steps: 1) release of a contaminating element from its originating stable state and locale in the wafer into solid solution in the semiconductor crystal lattice; 2) diffusion of the contaminant through the crystal away from sensitive device structures or areas where susceptible structures are ultimately to be formed; and 3) capture of the contaminants by extended defects such as dislocations or precipitates at a position far enough away from devices to avoid interference with their operation and stable enough to prevent future liberation or discharge into the wafer during ensuing thermal, chemical and plasma treatments.

There are two basic categories of gettering mechanisms: extrinsic, or external, and intrinsic, or internal. These categories are discussed in U.S. Pat. No. 4,608,096 to Hill, the disclosure of which is incorporated herein by reference.

Extrinsic gettering entails the use of external means (usually on the wafer back surface) to create damage or stress in the silicon lattice, leading to the creation of extended defects capable of mobile metal capture. Examples of extrinsic gettering approaches include: diffused backside phosphorus or arsenic doping to tie up nickel, gold, iron, copper, etc., and mechanical or physical backside wafer damage produced by abrasion, grooving, sandblasting, laser deformation, ion implantation, polysilicon deposition, etc.

Intrinsic gettering is typically accomplished by the localized capture of impurities at extended defects that exist within the bulk material of the silicon wafer, for example, a Czochralski grown monocrystalline wafer containing interstitial oxygen (5-25 ppma). Intrinsic gettering usually

involves the supersaturation of a region or zone of the silicon wafer with oxygen that will separate from solid solution and form clusters of silicon dioxide during thermal treatment. The stresses resulting from the agglomerate clusters cause stacking faults and dislocation loops that are capable of trapping impurities. To be effective, the clusters must be formed in the bulk of the wafer away from active device sites. Oxygen levels above the precipitation threshold must therefore be avoided in regions where active devices will be later be formed and permanently reside.

Various approaches have been taken in the past to provide gettering regions in a bonded semiconductor-on insulator substrate. For example, in U.S. Pat. No. 5,063,113 to Wada, the disclosure of which is incorporated herein by reference, defects for gettering sites are induced in a semiconductor layer by thermal treatment. However the defects are distributed vertically throughout the layer, extending even to the exterior surface, where they may adversely affect bonding of the layer with other layers. In addition, grinding and polishing of the layer results in substantial loss of the gettering sites.

U.S. Pat. No. 5,229,305 to Baker, the disclosure of which is incorporated herein by reference, describes a method for implanting boron, argon, krypton or, preferably, oxygen ions into a polished surface of a semiconductor layer, followed by thermal treatment, to create gettering sites in the layer. The polished surface of the semiconductor layer is then bonded to a handle substrate. Baker does not show implanting silicon ions into the silicon substrate. To create a high density gettering zone, Baker requires a large implant dose. Such a dose of non-semiconductor ions would alter the electrical characteristics of the semiconductor substrate.

Commonly employed gettering techniques are inadequate for use with many desired semiconductor devices. For example, the formation of gettering sites by treatment of the back surface of a device is generally unsuited for application to semiconductor-on-insulator structures. Also, defects that provide gettering sites are often generated in an indiscriminate, scattered fashion throughout the wafer and may thus adversely affect the performance of a device subsequently formed in the wafer.

There is a need for a method for making a bonded semiconductor-on-insulator substrate for integrated circuits that includes a high quality semiconductor device wafer having a smooth surface to promote its bonding integrity to a handle wafer and containing a well-defined, restricted intrinsic gettering zone close to but not detrimentally overlapping sites of devices that are particularly susceptible to metal contamination. There is a further need for a semiconductor substrate whose electrical characteristics are substantially unchanged by the formation of a gettering zone therein. The present invention meets these needs.

SUMMARY OF THE INVENTION

The present invention is directed to a method for forming a bonded semiconductor-on-insulator substrate for the fabrication of semiconductor devices and integrated circuits. Into a surface of a wafer of a monocrystalline semiconductor material, ions of the semiconductor material are implanted to a selected depth in the wafer to form, adjacent to the surface, an amorphous layer of the semiconductor material. The layer of amorphous semiconductor material extends to a substantially planar zone disposed at substantially the selected depth and comprising the monocrystalline semiconductor material damaged by lattice defects, i.e., end-of-range implant damage. Undamaged material below the selected

depth comprises a first layer of the monocrystalline semiconductor material.

The wafer is heated under conditions effective to convert the amorphous layer to a second layer of the monocrystalline semiconductor material and to coalesce the zone of damaged monocrystalline semiconductor material, thereby forming a substantially planar intrinsic gettering zone of substantially pure semiconductor material that includes active gettering sites disposed at substantially the selected depth.

An insulating bond layer on one surface of a handle wafer is bonded to the surface of the wafer to form a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a device wafer of monocrystalline semiconductor material. The device wafer includes a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites.

Also in accordance with the present invention is a bonded semiconductor-on-insulator substrate that includes a wafer comprising two layers of a monocrystalline semiconductor material separated by a planar intrinsic gettering zone that comprises substantially pure semiconductor material and contains active gettering sites. Further in accordance with the invention is a semiconductor device or integrated circuit formed on the described substrate.

The bonded substrate of the present invention includes a narrowly restricted gettering zone located in near proximity to device regions, which increases the efficiency of contaminant removal from those regions and facilitates small geometry manufacture. Because the gettering zone comprises substantially pure semiconductor material, its formation affects only the structural characteristics and not the electrical characteristics of the wafer. The bonded substrate of the invention is reliably constructed and provides excellent structural stability to devices formed on it over a wide range of processing temperature and conditions.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic cross-section of the bonded semiconductor-on-insulator substrate of the present invention.

FIGS. 2A–F is a schematic representation of the steps of forming a device wafer containing a planar intrinsic gettering zone.

FIG. 3 is a schematic representation of the bonding of a handle wafer and a device wafer containing a planar intrinsic gettering zone to form the bonded substrate of the present invention.

FIG. 4 is a schematic cross-section of a bipolar junction transistor (BJT) formed on the bonded substrate of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. 1, a bonded substrate 10 of the present invention includes a handle wafer 11 having on one surface 12 an insulating bond layer 13 and a semiconductor device wafer 14 bonded to insulating layer 13. Semiconductor device wafer 14 has a first layer 15 of monocrystalline semiconductor material adjacent to insulating layer 13 and a second layer 16 of monocrystalline semiconductor material overlying first layer 15. Second monocrystalline semiconductor layer 16 is separated from first monocrystalline semiconductor layer 15 by an intervening substantially planar intrinsic gettering zone 17 comprising gettering sites

in the monocrystalline semiconductor material. A further optional epitaxial monocrystalline semiconductor layer 18 can be deposited on surface 19 of layer 16.

FIGS. 2A–F depict the method of the invention for forming the device wafer 14 shown in FIG. 1. As depicted in FIG. 2A, an oxide layer 21 having a thickness preferably of about 1 nm to about 50 nm is optionally formed on a wafer 22 of monocrystalline semiconductor material. The oxide of layer 21 may be a native oxide, a chemically grown oxide, a thermally grown oxide, or a deposited oxide. Ions 23 of the semiconductor material at a dose of about 10^{14} to 10^{18} ions/cm² are implanted, through oxide layer 21 if present, to a selected depth 24 in wafer 22, as shown in FIG. 2B. The depth 24 of ion implantation can be controlled by the energy employed; for example, about 185 keV causes implantation of silicon ions at a depth 24 of about 0.4 μ m, while a lower energy of about 90 keV results in a depth 24 of about 0.2 μ m. In accordance with the present invention, the depth of ion implantation in the monocrystalline semiconductor wafer preferably is about 0.1 μ m to 2.0 μ m, preferably about 0.2 μ m to 0.6 μ m, and the implantation energy preferably is about 50 keV to 250 keV. Ion implantation is well described in Giles, "Ion Implantation," Chapter 8 in Sze, editor, *VLSI Technology*, Second Edition, McGraw-Hill, Inc., 1988, the disclosure of which is incorporated herein by reference.

As depicted in FIG. 2C, ion implantation results in formation of an amorphous semiconductor layer 25. If oxide layer 21 is present, amorphous layer 25 may contain oxygen atoms that originated from layer 21. A layer 26 of undamaged monocrystalline semiconductor material is separated from amorphous layer 25 by a substantially planar latent getter zone 27 of monocrystalline semiconductor material containing lattice defects, i.e., end-of-range implant damage. Amorphous layer 25 is heated under conditions effective to convert it by solid phase epitaxial annealing to a layer 28 of monocrystalline semiconductor material, as shown in FIG. 2D. The annealing of amorphous layer 25 to produce monocrystalline semiconductor layer 28 is achieved by heating to a temperature of about 450° C. to 1200° C. for about 15 minutes to 8 hours, preferably about 550° C. to 620° C. for about 2 hours to 6 hours in a non-oxidizing atmosphere such as nitrogen, argon, or hydrogen. Annealing removes from layer 28 sufficient oxygen to preclude the formation of defect sites.

Further heating at about 800° C. to 1200° C. for about 1 hour to 6 hours, preferably about 1000° C. to 1150° C. for about 2 hours to 4 hours, causes coalescence of zone 27 of monocrystalline semiconductor material damaged by lattice defects to form a gettering zone 17 containing active gettering sites. It must be emphasized that gettering zone 17, unlike that described in the previously mentioned U.S. Pat. No. 5,229,305, comprises substantially pure semiconductor material containing dislocations that provide active gettering sites. Because implantation is carried out with ions 23 of the semiconductor material, e.g., silicon ions, no dopants or other contaminants that can affect the electrical properties of the semiconductor wafer 14 are introduced during ion implantation.

The annealing of layer 25 and the coalescence of zone 27 can be carried out in a single step under effective temperature-time conditions, but it is preferred that a two-stage procedure first at lower temperature, then at higher be employed. The coalescence of zone 27 produces a substantially planar intrinsic gettering zone 17 separating a first layer 15 and a second layer 16, each comprising monocrystalline semiconductor material, as depicted in FIG. 2E. Zone

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27 can have an initial thickness of about 0.2 μm to 0.4 μm , coalescing to form a gettering zone 17 having a thickness of about 0.05 μm to about 0.2 μm , preferably about 0.1 μm . First monocrystalline semiconductor layer 15 has a thickness of about 0.1 μm to about 0.8 μm , preferably about 0.2 μm to about 0.4 μm . Second monocrystalline semiconductor layer 16, which is much thicker than layer 15, can have a thickness of 100 μm or greater prior to being thinned to a desired final thickness of about 0.2 μm to 20 μm .

Removal of oxide layer 21, if present, produces device wafer 14, as shown in FIG. 2F. It should be noted that the structure of wafer 14 as shown in FIG. 2F is inverted relative to its orientation in FIG. 1.

FIG. 3 is a schematic representation of the formation of the bonded semiconductor-on-insulator substrate of the present invention by inverting device wafer 14, as shown in FIG. 2F, and bonding it to insulating bond layer 13 on handle wafer 11. Following bonding of wafer 14 to layer 12, thick second monocrystalline semiconductor layer 16 can be thinned to a desired thickness. An epitaxial monocrystalline semiconductor layer 18 can be deposited on thinned layer 16, as shown in FIG. 1, and active devices can be fabricated within epitaxial layer 18.

Those skilled in the art will appreciate that the planar gettering zone 17 can be precisely positioned at a depth 24 within device wafer 14. Likewise, the thickness of second monocrystalline semiconductor layer 16 can be controlled by chemical or mechanical material removal means, including etching, lapping, grinding, and polishing. As a result, gettering zone 17 can also be precisely positioned with respect to devices formed on the surface 19 of layer 16 or in epitaxial layer 18.

The method of the present invention is applicable to any substrate having a semiconductor-on-insulator structure. Preferably, however, the semiconductor material comprising device wafer 14 is monocrystalline silicon, in which gettering zone 17 is produced by implanting silicon ions 23 through a layer 22 of silicon dioxide. Semiconductor material comprising device wafer 14 can further be germanium, and gettering zone 17 can be produced by implanting germanium ions 23 through a layer 22 of germanium oxide.

Handle wafer 11 can be formed from a metal, an insulator, silicon carbide, polysilicon or, preferably, monocrystalline silicon. Insulating bond layer can be formed of any insulating material but preferably comprises silicon dioxide. Thus, the method of the present invention is especially useful for forming silicon-on-insulator (SOI) bonded substrates on which semiconductor devices and integrated circuits can be fabricated.

FIG. 4 schematically depicts the cross-section of a bipolar junction transistor (BJT) 40 formed in an epitaxial layer 18 formed on a bonded SOI substrate 10 containing a planar intrinsic gettering zone 17 in accordance with the present invention. Transistor 40 includes an emitter diffusion 42, a base diffusion 44, and a collector sinker diffusion 46. The polarity of emitter diffusion 42 and sinker diffusion 46 are the same, i.e., n or p, the polarity of base diffusion 44 being the opposite, i.e., p or n. Sinker diffusion 46 is connected to a buried layer 43 in a manner well known in the art. Insulating layers 48, 49, 50 isolate the respective metal contacts 52, 54, 56 for emitter, base, and sinker diffusions 42, 44, 46. Surface insulator 51 protects an interconnect metal line 58 and otherwise seals the surface of transistor 40. Lateral isolation trenches 60, 61, which have oxide sidewalls and are filled with polysilicon, extend from the surface of transistor 40 to buried oxide insulating layer 13 and serve to isolate transistor 40 from adjacent devices.

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In addition to BJTs, many other types of devices can be constructed on the bonded substrate of the present invention: resistors, capacitors, diodes, field effect transistors (FETs), including junction and MOSFETs, thyristors, and the like.

The invention has been described in detail for the purpose of illustration, but it is understood that such detail is solely for that purpose, and variations can be made therein by those skilled in the art without departing from the spirit and scope of the invention, which is defined by the following claims.

What is claimed:

1. A semiconductor device formed by the method comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafers thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged by implantation monocrystalline semiconductor material below said selected depth comprising a second layer of the undamaged by implantation monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a first layer of the monocrystalline semiconductor material;

heating the wafer under conditions defective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering, zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

forming a semiconductor device on said second layer of undamaged by implantation monocrystalline semiconductor material or on layer of epitaxial monocrystalline semiconductor material deposited on said second layer; and

wherein the said semiconductor device is formed on said epitaxial layer.

2. The semiconductor device of claim 1 wherein said device is selected from the group consisting of a bipolar junction transistor, a field effect transistor, a capacitor, a resistor, a thyristor and combinations thereof comprising integrated circuits.

3. A semiconductor device formed by the process comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent

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to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged by implantation monocrystalline semiconductor material below said selected depth comprising a second layer of the undamaged by implantation monocrystalline semiconductor material; heating said wafer under conditions effective to convert said amorphous semiconductor layer to a first layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth between the first layer of monocrystalline semiconductor material and the second layer of undamaged by implantation monocrystalline semiconductor material;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer adjacent the first layer of monocrystalline semiconductor material, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicon ions;

wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide; and forming a semiconductor device on said bonded substrate.

4. The semiconductor device of claim 3 wherein said device is selected from the group consisting of a bipolar junction transistor, a field effect transistor, a capacitor, a resistor, a thyristor, and combinations thereof comprising integrated circuits.

5. A bonded semiconductor-on-insulator substrate for semiconductor devices and integrated circuits, said substrate comprising:

a wafer comprising a monocrystalline semiconductor material and having a first surface and a second surface, said wafer comprising a first layer of the monocrystalline semiconductor material adjacent to said first surface and a second layer of undamaged by implantation monocrystalline semiconductor material adjacent to said second surface, and interposed between said first and second layers of the monocrystalline semiconductor material, a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites,

an insulating bond layer disposed on said first surface of said wafer; and

a handle wafer bonded to said insulating bond layer.

6. The substrate of claim 5 wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicon ions.

7. The substrate of claim 5 wherein the monocrystalline semiconductor material comprises silicon and the substan-

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tially planar intrinsic gettering zone is formed by implanting ions of silicon through the first layer of monocrystalline semiconductor material.

8. The substrate of claim 5 wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide.

9. The substrate of claim 5 wherein said first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm .

10. The substrate of claim 5 wherein said second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm .

11. The substrate of claim 5 wherein said gettering zone has a thickness of about 0.05 μm to about 0.2 μm .

12. The substrate of claim 5 further comprising two or more devices and one or more trenches surrounding at least one of said devices for laterally isolating the surrounded device from the other device(s).

13. A semiconductor device formed on the second layer of monocrystalline semiconductor material of the substrate of claim 5 or on a layer of epitaxial monocrystalline semiconductor material deposited on said second layer.

14. The semiconductor device of claim 13 wherein said device is selected from the group consisting of a bipolar junction transistor, field effect transistor, capacitor, a resistor, a thyristor, and combinations thereof comprising integrated circuits.

15. A bonded semiconductor-on-insulator substrate for an integrated circuit comprising:

a wafer, the wafer having a first layer of monocrystalline semiconductor material adjacent a first surface of the wafer, the wafer further having a second layer of undamaged by implantation monocrystalline semiconductor material adjacent a second surface of the wafer, the wafer further having a substantially planar intrinsic gettering zone of substantially pure semiconductor material and active gettering sites positioned between the first and second layers formed by implanting ions of the semiconductor material through the first layer of monocrystalline semiconductor material;

a handle wafer; and

an insulating bond layer bonding the handle wafer to the first surface of the wafer.

16. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 15, wherein the first and second layers of monocrystalline semiconductor material comprises silicon and the ions implanted through the first layer are silicon ions.

17. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 15, wherein the second layer of undamaged monocrystalline semiconductor material is a device layer upon which semiconductor devices are formed.

18. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 15, wherein the handle wafer comprises silicon and the insulating bond layer comprises silicon dioxide.

19. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 15, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm .

20. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 15, wherein the second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm .

21. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 15, wherein the gettering zone has a thickness of about 0.05 μm to about 0.2 μm .

22. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 15, further comprising:

a layer of epitaxial monocrystalline semiconductor material deposited on the second layer.

23. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 22, further comprising: two or more semiconductor devices formed in the epitaxial monocrystalline semiconductor material, wherein the semiconductor devices are laterally isolated from each other.

24. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 15, further comprising:

two or more semiconductor devices formed in the bonded semiconductor-on-insulator substrate, wherein each semiconductor device is laterally isolated from each other.

25. A bipolar junction transistor for an integrated circuit comprising:

wafer, the wafer having a first layer of monocrystalline semiconductor material adjacent a first surface of the wafer, the wafer further having a second layer of undamaged by implantation monocrystalline semiconductor material adjacent a second surface of the wafer, the wafer further having a substantially planar intrinsic gettering zone of substantially pure semiconductor material and active gettering sites positioned between the first and second layers formed by implanting ions of the semiconductor material through the first layer of monocrystalline semiconductor material;

a handle wafer;

an insulating bond layer bonding the handle wafer to the first surface of the wafer;

a layer of epitaxial monocrystalline semiconductor material deposited on the first layer;

an emitter diffusion formed in the epitaxial monocrystalline semiconductor material;

a base diffusion formed in the epitaxial monocrystalline semiconductor material; and

a collector sinker diffusion formed in the epitaxial monocrystalline semiconductor material, wherein the emitter, base and collector sinker diffusions are laterally isolated from other devices formed in the epitaxial monocrystalline semiconductor material of the integrated circuit.

26. The bipolar junction transistor for an integrated circuit of claim 25, wherein the first and second monocrystalline semiconductor material comprises silicon implanted by silicon ions.

27. The bipolar junction transistor for an integrated circuit of claim 25, further comprising:

a layer of epitaxial monocrystalline semiconductor material deposited on the second layer of monocrystalline semiconductor material.

28. The bipolar junction transistor for an integrated circuit of claim 25, wherein the handle wafer comprises silicon and the insulating bond layer comprises silicon dioxide.

29. The bipolar junction transistor for an integrated circuit of claim 25, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

30. The bipolar junction transistor for an integrated circuit of claim 25, wherein the second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm.

31. The bipolar junction transistor for an integrated circuit of claim 25, wherein the gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

32. The bipolar junction transistor for an integrated circuit of claim 25, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

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