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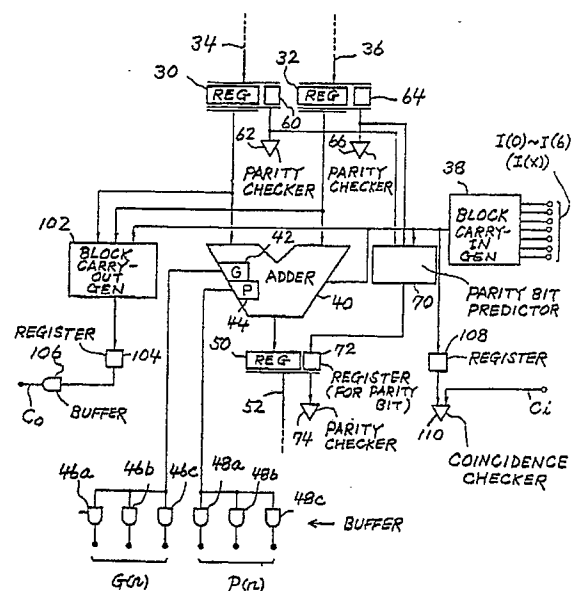
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54 **Digital arrangement for error checking in binary adder including block carry look-ahead units.**

57 A binary adder is comprised of a plurality of block carry look-ahead units. Each of the units includes a block carry-in generator (38), an adding section (40), a block carry-out generator (102) and a carry coincidence checker (110). The block carry-in generator (38) is arranged to receive a plurality of carry generate variables and a plurality of carry propagate variables from the other units, generating a carry-in using carry look-ahead scheme. The adding section (40) is coupled to receive the carry-in from said block carry-in generator (38) and further receives two operand data to be added and generates a resultant sum of the two operand data. The block carry-out generator (102) receives the two operand data and also receives the carry-in from the block carry-in generator (38). The block carry-out generator (102) produces a carry-out of the unit to be applied to a lower order block carry look-ahead unit. The carry coincidence checker (110) is arranged to receive the carry-in from the carry-in generator (38) and also receives a carry from another block carry look-ahead unit. The carry, which is applied from another unit, corresponds to the carry-out. The checker (110) performs a coincidence check between the carry-in and the carry applied from another unit.

FIG. 9



**EP 0 401 783 A3**



DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4 081 860 (MILLER) * the whole document * - - - -	1-12	G 06 F 7/50 G 06 F 11/00
A	US-A-4 084 253 (MILLER) * the whole document * - - - -	1-12	
A	US-A-3 925 647 (LOUIE) * the whole document * - - - -	1-12	
A	DE-A-1 524 141 (IBM) * the whole document * - - - -	1-12	
A	US-A-3 470 366 (GELLER) * column 13, line 64 - column 24, line 5; figures 164-183 * - - - -	1-12	
A	Proc. of the IEEE 1988 Custom Integrated Circuits Conference May 1988, Rochester, New York, USA pages 2451 - 2454; Keshlear et al.: "A high-speed 16-bit cascadable ALU using an aspect standard cell approach" * the whole document * - - - -	1-12	
A	PATENT ABSTRACTS OF JAPAN vol. 011, no. 084 (P-556) 13 March 1987, & JP-A-61 239331 (FUJITSU LTD) 24 October 1986, * the whole document * - - - - -	1,4,6,7, 10,12	TECHNICAL FIELDS SEARCHED (Int. Cl.5)  G 06 F
The present search report has been drawn up for all claims			
Place of search Berlin		Date of completion of search 27 August 91	Examiner DURAND J.
<p><b>CATEGORY OF CITED DOCUMENTS</b></p> <p>X: particularly relevant if taken alone  Y: particularly relevant if combined with another document of the same category  A: technological background  O: non-written disclosure  P: intermediate document  T: theory or principle underlying the invention</p> <p>E: earlier patent document, but published on, or after the filing date  D: document cited in the application  L: document cited for other reasons</p> <p>.....  &amp;: member of the same patent family, corresponding document</p>			