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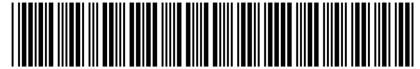

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(54) SILICIDED FIN JUNCTION FOR BACK-SIDE CONNECTION

(57) A semiconductor device comprising a fin structure (100) and a substrate (140) is disclosed. The fin structure comprises a first source/drain region (110), a second source/drain region (120), and a channel region (130). The channel region is arranged between the first source/drain region and the second source/drain region to separate the first source/drain region and the second source/drain region in a length direction of the fin structure. The first source/drain region (110) comprises a bottom portion (112) and a top portion (114), wherein the bottom portion (112) of the first source/drain region is fully silicided and the top portion (114) of the first source/drain region is partly silicided.

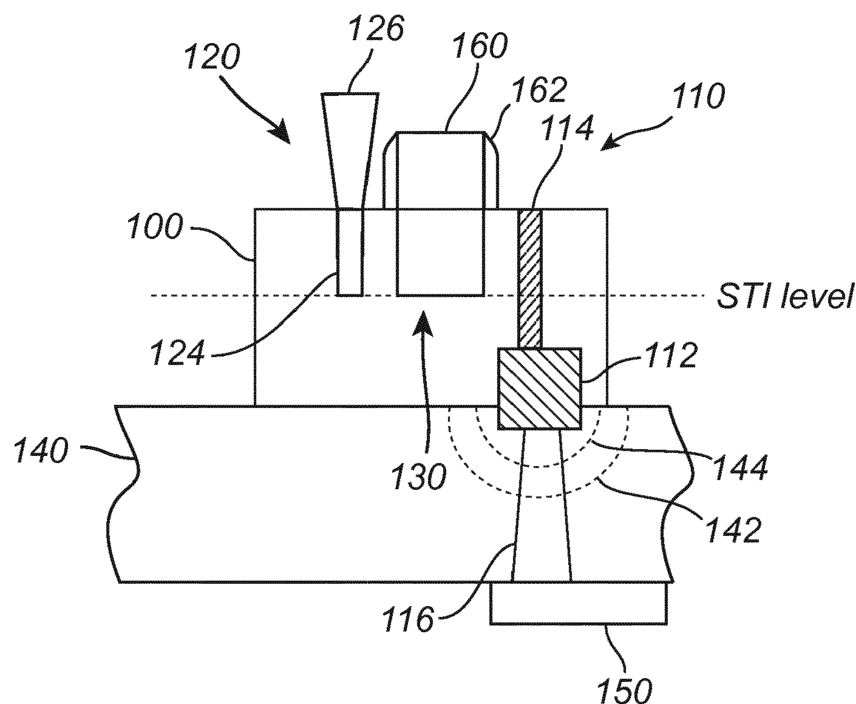

Fig. 1

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Description

Technical field

[0001] The present inventive concept relates generally to integrated circuit structures, and more particularly to techniques for power supply of semiconductor transistor devices.

Background

[0002] For the operation of integrated circuits, power must be supplied and distributed appropriately. With the ever increasing demand for smaller and more densely packed circuits, the challenges in design complexity and power routing has increased dramatically.

[0003] One attempt to address these challenges has been to introduce a backside interconnect structure to deliver power through the substrate to the front side of the integrated circuit. This technology employs a power distribution network, formed on the backside of the substrate, and a series of deep vias through the substrate to couple the power planes to front side metal lines.

[0004] Even though such technology may reduce the footprint of the integrated circuit, there is still a need for an improved technology for supplying semiconductor devices with power.

Summary

[0005] An objective of the present inventive concept is to provide a semiconductor device, and a method for forming such a device, having an improved power routing. The present inventive concept is described by the independent claims, whereas different embodiments are defined by the dependent claims.

[0006] Thus, according to a first aspect there is provided a semiconductor device comprising a fin structure and a substrate, wherein the fin structure comprises a first source/drain region, a second source/drain region, and a channel region. The channel region is arranged between the first source/drain region and the second source/drain region to separate the first source/drain region and the second source/drain region in a length direction of the fin structure. Further, the first source/drain region comprises a bottom portion and a top portion, wherein the bottom portion is arranged between the top portion and the substrate such that it shares a common boundary with the top portion. According to the present aspect, the bottom portion is fully silicided, whereas the top portion is partly silicided.

[0007] According to a second aspect, a method for forming a semiconductor device is disclosed. The method comprises:

forming a fin structure having a first source/drain region, a second source/drain region and a channel region, wherein the channel region is arranged between the first source/drain region and the second source/drain region, thereby separating the first source/drain region and the second source/drain region in a length direction of the fin structure, and wherein the first source/drain region comprises a bottom portion and a top portion, the bottom portion being arranged between the top portion and a substrate of the semiconductor device and such that the bottom portion shares a common boundary with the top portion;

depositing a first silicidation metal on the top portion of the first source/drain region;

annealing the material of the top portion of the first source/drain region to react the first silicidation metal with said material such that the top portion of the first source/drain region is partly silicided;

providing a second silicidation metal on the bottom portion of the first source/drain region; and

annealing the material of the bottom portion of the first source/drain region to react the second silicidation metal with said material such that the bottom portion of the first source/drain region is fully silicided.

[0008] The present inventive concept allows for the fin to be electrically contacted to directly from below, i.e., without having to go through a routing structure connecting the fin from the top. This allows for a more densely packed circuit, as the space otherwise required for the vertical routing between for example a backside interconnect structure and the top of the fin can be saved. Further, the direct connection to the bottom of the fin eliminates the resistance and parasitic capacitance associated with the routing to the top of the fin.

[0009] The electrical contacting of the fin from below is allowed due to the full silicidation of the bottom portion of the fin, combined with the partial silicidation of the top portion. The fully silicided bottom portion of the fin forms a landing pad for backside connections and may be used to bias the well, whereas the partially silicided top portion of the fin enables a large contact area to the fin and thus a reduced interface resistance.

[0010] The fin structure may be considered to have an active part, or device part, formed by at least a part of the top portion as mentioned above. The active part may be defined by the part of the fin that protrudes from an isolating structure, such as for example a shallow trench isolation (STI), and may constitute only a fraction of the total fin height as measured from the substrate. The bottom portion may be arranged under the active part, as seen from above the fin in a direction towards the substrate, and preferably in contact with the substrate. The top portion of the fin may be arranged directly on the bottom portion, such that the top portion and the bottom portion share a common boundary. In fact, the top portion and the bottom portion may be formed from the same fin structure, and be defined by the difference in degree of silicidation. The part of the fin that is fully silicided may

be referred to as the bottom portion, whereas the part of the fin that is only partly silicided may be referred to as the top portion.

[0011] The distance from the substrate to the top of the fin, as seen in an orthogonal direction from the substrate, may be referred to as the height of the fin, whereas the horizontal extension of the fin along a surface of the substrate may be referred to as the length of the fin. The fin may have a uniform height, or a height that varies along its length. Similarly, the height of the device part protruding from the isolating structure (if any), may either be uniform or vary along the length of the fin.

[0012] Given the above definitions, the top and bottom portions may be aligned above each other in the height direction of the fin, whereas the first source/drain region, channel region and the second source/drain region, which all may be formed in the device part of the fin, may be aligned after each other in the length direction of the fin.

[0013] The terms 'source/drain region' and 'channel region' relate to the parts of the fin in which the corresponding terminals of a transistor may be formed. It is therefore appreciated that the actual source/drain and channel of the resulting transistor device may form only a part of the source/drain and channel regions of the fin structure - the latter region may be referring to different parts or regions of the fin structure, and not necessarily to the terminals of the transistor.

[0014] The source/drain and channel of the transistor, which may be formed by parts of the material of the source/drain region and the channel region of the fin structure, may be connected to electrical contacting or connecting structures. The electrical contacting structure coupled to the channel may be referred to a gate or gate contact, and are used for modulating the channel conductivity.

[0015] In the present inventive concept, the electrical contacting structure at the first source/drain region is at least partly formed by the silicide of the fin structure.

[0016] The electrical contacting structures may include horizontal conductive lines and vertical conductive vias or metal vias that provide the signal routing required for operating the transistors.

[0017] As used herein, the term 'horizontal' denotes a direction parallel to a main plane of extension or a main surface, whereas the term 'vertical' denotes a direction transverse to the main plane of extension of the substrate. Accordingly, the terms 'top' and 'above' refer to a direction away from the substrate, along the vertical direction, whereas the terms 'bottom' and 'below' refers to a direction towards the substrate, along the vertical direction.

[0018] The term 'fully silicided' refers to a part of the fin structure being silicided all the way through the fin, such that not only the outer surfaces of the fin part has reacted with the silicidation metal to form a silicide, but also all the material within the fin part. The term 'partly silicided', on the other side, refers to a part of the fin structure in which only some of the material has reacted with the silicidation metal. Preferably, only the outer surfaces of the fin part have reacted with the silicidation metal, leaving at least some of the material within the fin part unaffected. In some example, the silicide may form a layer on the outside of the partly silicided portion.

[0019] In the above, the top portion of the first source/drain region is described as partly silicided. It will however be appreciated that also the top portion of the second source/drain region may be partly silicided as well, so as to facilitate contacting from above.

[0020] According to an embodiment, the semiconductor device may further comprise a first connecting structure for electrically contacting at least a part of the bottom portion of the first source/drain region, and a second connecting structure for electrically contacting at least a part of the top portion of the second source/drain region. The first connecting structure may for example comprise a trench or through silicon via, formed in the substrate and landing on the fully silicided portion of the fin structure, for providing an electrical connection to a backside contacting structure such as a power distribution network (PDN). The first connecting structure may thus be arranged to contact the fully silicided portion of the fin from below, i.e., the side of the fin facing the substrate, whereas the second connecting structure may be arranged to contact the (possibly partly silicided) fin from above, i.e., the side of the fin facing away from the substrate.

[0021] As previously mentioned, the partly silicided portion(s) of the fin structure may comprise an outer layer of silicide. In other words, the silicidation of those parts may be provided in the form of an outer layer of the fin, whereas at least part of the material of the fin structure arranged inside the layer is not silicided. It should be noted that the silicided outer layer need not necessarily cover the entire surface of the first source/drain region. The silicided layer may cover a surface portion that defines a contact area sufficiently large to provide a proper, functional contacting of the source/drain region of the fin.

[0022] According to an embodiment, the top portion of the first source/drain region may be arranged to fully overlap the bottom portion of the first source/drain region, as seen in a height direction of the fin structure. This allows for the top portion to be electrically connected from below through the underlying, fully silicided bottom portion of the fin, which hence may be considered as vertically aligned with the top portion.

[0023] According to an embodiment, the substrate may comprise a well that is doped with a dopant of a first dopant type. Further, a region of the well sharing a common boundary with the bottom portion of the first source/drain region may comprise a higher dopant concentration than the remaining regions of the well. A higher surface doping at the substrate/silicide dopant allows for a reduced electrical resistance between the substrate and the fin structure. By using a well, the fin structure can be connected to the substrate without using any tap cells. Further, the top portion of the first and second

source/drain regions, i.e., the partly silicided portions, may be doped with a second dopant type.

[0024] The doping may be formed by forming a recess in the substrate, adjacent to the fin structure, and at least partly filling the recess with a doped oxide. At least the bottom portion of at least one of the first and second source/drain regions may be doped in a solid-phase diffusion process.

[0025] According to an embodiment, at least a part of the top portion of the second source/drain region may be provided with an epitaxial contacting structure. The epitaxial contacting structure may form part of the second connecting structure for providing a routing from above, and may in some examples be provided with an outer layer of silicide so as to facilitate electrical connection and reduce interface resistance.

[0026] The partly and fully silicided portions of the fin structure may be provided in a two-part silicidation process, in which the first silicidation metal is deposited on the top portion of the first source in a first silicidation step and the second silicidation metal is provided on the bottom portion of the first source/drain region of the fin structure in a second silicidation step. In one embodiment, the second silicidation metal is provided by forming a recess exposing sidewalls of the bottom portion, and depositing the second silicidation metal in the recess. The recess may be formed in an STI arranged above the substrate.

[0027] According to an embodiment, the method may further comprise a step of removing the first silicidation metal from portion of the fin structure that have not been silicided. The unreacted silicidation metal may be removed so as to avoid shortcuts between different silicided portions.

[0028] According to an embodiment, the reacting of the second silicidation metal may be performed after an inter-layer dielectric (ILD) has been provided, so as to prevent the fin from collapsing during the silicidation process.

Brief description of the drawings

[0029] The above, as well as additional objects, features and advantages of the present inventive concept, will be better understood through the following illustrative and non-limiting detailed description, with reference to the appended drawings. In the drawings like reference numerals will be used for like elements unless stated otherwise.

Figure 1 is a schematic cross section taken along a fin structure.

Figure 2 is a schematic cross section taken across the first source/drain region of a fin structure.

Figures 3-7 schematically illustrate a method for forming a semiconductor device comprising a fin structure.

Figure 8 is a schematic perspective view of a semiconductor device.

Detailed description

[0030] Figure 1 is a cross section taken along a semiconductor device according to an embodiment of the present inventive concept. It should be noted that, owing to the schematic nature of the drawings, the relative dimensions of the various structures and layers are not drawn to scale. Rather the dimensions have been adapted for illustrational clarity and to facilitate understanding of the following description.

[0031] The semiconductor device according to the present example illustrated in figure 1 comprises a fin structure 100 supported by a substrate 140. The fin structure comprises a first source/drain region 110, a second source/drain region 120, and a channel region 130 arranged between the first source/drain region 110 and the second source/drain region 120 as seen in a length direction of the fin structure 100. Even though only one fin structure is illustrated in the present figure, it will be appreciated that the resulting semiconductor device may comprise a plurality of fin structure, which preferably are arranged parallel to each other. The fin structure(s) 100 may be formed by a fin pattering and fin cut process of the substrate 140.

[0032] The fin structure 100 may be at least partly embedded in a STI, such that only a portion of the fin structure 100 protrudes from the surface of the STI. The level of the STI surface in indicated by the dashed line in figure 1. The protruding portion of the fin structure 100 may be referred to as an active portion or device portion. The final device, such as a transistor device comprising a source, drain and gate terminal, may be formed in this device portion.

[0033] The first source/drain region 110 of the fin structure 100 may comprise a bottom portion 112, arranged in the portion of the fin closest to the substrate 140, and a top portion 114. The top portion 114 may thus be arranged on top of the bottom portion 112 such that the top portion 114 and the bottom portion 112 shares a common boundary or interface. In the present example, the bottom portion 112 of the first source/drain region 110 is fully silicided, whereas the top portion 114 is partly silicided. The bottom portion 112 may in other words comprise a silicide that extends all the way through the entire width of the fin structure 100, whereas the top portion 114 may comprise a silicide provided in the form of an outer layer on the fin structure (illustrated by the dashed area 114 in figure 1).

[0034] The substrate 140 may be doped to form a well 142 under the fin structure 100, an in particular the first source/drain region 110 indicated in figure 1. In the well 142 a region 144 of higher dopant concentration may be formed so as to improve the electrical connection between the fin structure 100 and the silicon of the well 140. The region 144 may hence be arranged such that it shares a common boundary with the silicide of the bottom portion 112 of the first source/drain region 110. The silicide of the bottom portion 112 may reach slightly into the

substrate 140 due to the nature of the silicidation process, which may consume some of the silicon of the substrate 140.

[0035] A first connecting structure 116, such as a trench or via filled with a metal or another electrically conductive material, may be arranged to connect the bottom portion 112 of the fin structure 100 from below. In the present example of figure 1, the trench is arranged under the first source/drain region 110 and extends through the substrate 140 so as to connect the first source/drain region 110 to a backside power distribution network, PDN 150.

[0036] The second source/drain region 120 may comprise a top portion 124 that is electrically connected to a second connecting structure 126, such as an interconnecting via or a metal line, for connecting the second source/drain region 120 from above.

[0037] The channel region 130 may be controlled by a gate electrode 160, separated from the surrounding structures such as the second connecting structure 126 by sidewall spacers 162. During operation of the transistor device, the gate electrode 160 may be used for controlling the flow of electrical carriers between the first source/drain region 110 and the second source/drain region 120.

[0038] Figure 2 is a schematic illustration of a cross section, taken across the first source/drain region 110 of a semiconductor device that may be similarly configured as the embodiment discussed in connection with figure 1. The present cross section illustrates an example of a fin structure 100 wherein the bottom portion 112 is fully silicided and the top portion 114 only partly silicided. The silicide is indicated by the dashed areas. The partly silicided top portion 114 comprises a silicide provided as a layer arranged on the outer surface of the fin structure 100, while the inner regions of the top portion are substantially unaffected by the deposited silicidation metal.

[0039] The fully silicided bottom portion 112, which hence may be considered as transformed into a silicide material, provides a landing pad for the trench 116 that connects the first source/drain region 110 from below - in the present example to a PDN 150. The silicided surface of the top portion 114 provides an electrical contacting of the active top part of the fin structure, allowing the source/drain region of the transistor device formed in the fin to be powered from the substrate rather than from a BEOL side.

[0040] A method for forming a semiconductor device, which may be similarly configured as the device illustrated in figures 1 and 2, will now be discussed with reference to figures 3 to 7.

[0041] At the stage of the method shown in figure 3, three parallel fin structures 100 have been provided. The fin structures 100 are supported by a substrate 140, which may be a semiconductor substrate of a conventional type, such as a silicon substrate 140. Other examples may be a germanium substrate or a SiGeOI substrate, a SiC substrate, a SOI substrate, or a GeOI substrate.

[0042] The fin structures 100 have been formed by a cut etch forming trenches that define the fin structures 100. An STI layer 20 may be formed such that only an uppermost portion of the fin structures 100 protrude from the surface of the STI layer 20. In the present figure, the STI layer 20 have been etched away from two of the fin structures 100, so as to expose the first source/drain regions 110 that are to be processed in the following illustrating disclosure.

[0043] As shown in figure 3, a dopant material, such as phosphor-silicate glass, PSG 10, may be conformally deposited over the structure.

[0044] The PSG 10 may then be recessed, for example by dry etching or wet etching, until the PSG 10 remains at the bottom of the two exposed fin structures 100. The result is shown in figure 4. The remaining structures, such as the STI layer 20 and the third fin structure 100, may be protected by a layer of e.g. silicon nitride, acting as a stopping layer for the etch process.

[0045] Thereafter, a first silicidation metal 30 may be deposited on the top portion 114 of the fin structures 110 and annealed so as to react the first silicidation metal 30 to form an outer layer of silicide. The silicidation metal 30 may be titanium, cobalt or nickel platinum, and may for example be added in a layer of a thickness of about 3 nm. The result is illustrated in figure 5, showing the fin structures 100 with partly silicided top portions 114 and, in the case of the two left fins that were not protected by the STI layer 20, a silicided layer also at the bottom portions 112. Any remaining first silicidation metal 30 at the STI layer 20 may be removed in an etch process.

[0046] In figure 6, a second silicidation metal 32 have been provided at the bottom portion 112 of the exposed fin structures 100, in this case in the trenched formed at the two left fin structures 100. The second silicidation metal 32 may for example be deposited by conformal coating and recessing until the second silicidation metal 32 remains at the bottom portions 112 that are to be silicided. Example of silicidation metals 32 include titanium, cobalt and nickel platinum.

[0047] In a subsequent step, following the deposition of the second silicidation metal 32 and prior to the annealing of the second silicidation metal 32, an isolating/supporting layer, such as an inter-layer dielectric, ILD 40, may be formed so as to support the fin structures during the silicidation process and reduce deformation. Figure 7 illustrates an example of the semiconductor device after the second silicidation metal 32 has been annealed and formed the silicide with the material of the bottom portion 112 of the fin structure 100. The silicide has been formed throughout the entire bottom portion 112 arranged closest to the substrate 140, and is electrically connected to the substrate 140 through the doped region provided by the PSG 10 described in figures 3 and 4. Due to the relatively thin layer of the first silicidation metal 30 that was deposited in connection with figure 5, the top portion 114 of the fins remains partly silicided.

[0048] Figure 8 is a perspective view of a semiconductor device according to an embodiment, which may be similarly configured as the devices shown in figures 1 and 2, and which may be formed in a similar process as illustrated in connection with figures 3-7.

[0049] Figure 8 shows four fin structures 100 extending horizontally along a substrate 140. The fin structures 100 and/or the substrate 140 may for example be formed of silicon. The fin structures 100 are embedded in an STI layer 20 of which, for illustrational clarity, only the top surface is illustrated in the present figure.

[0050] Each of the fin structures 100 comprises a first source/drain region 110, a channel region 130 and a second source/drain region 120, wherein the first and second source/drain regions 110, 120 are separated, in the length direction of the fin structures 100, by the channel region 130. The first source/drain region 110 of the fin structures 100 is electrically connected from below, i.e., the substrate side, by a completely silicided bottom portion 112 of the fin. The silicide of the bottom portion 112 may serve as a landing pad for a trench (not shown in figure 8) connecting the first source/drain portion to a backside contact, such as for example a PDN.

[0051] Further, as shown in the present example, the second source/drain regions 120 may be connected from above by means of a second connecting structure 126 extending across the fin structures 100. This may also apply to the channel region 130, which may be coupled to a gate electrode 160 extending along and across the channel regions 130 of the fin structures 100. The gate electrode 160 may be isolated from the connecting structure 126 of the second source/drain regions 120 by means of an isolating spacer 162 arranged at the sidewalls of the gate electrode 160.

[0052] In the above the inventive concept has mainly been described with reference to a limited number of examples. However, as is readily appreciated by a person skilled in the art, other examples than the ones disclosed above are equally possible within the scope of the inventive concept, as defined by the appended claims.

Claims

1. A semiconductor device comprising a fin structure (100) and a substrate (140), the fin structure comprising:

   a first source/drain region (110);
   a second source/drain region (120); and
   a channel region (130);

   wherein:

   the channel region is arranged between the first source/drain region and the second source/drain region, thereby separating the first source/drain region and the second source/drain region in a length direction of the fin structure;
   the first source/drain region (110) comprises a bottom portion (112) and a top portion (114), the bottom portion being arranged between the top portion and the substrate and such that it shares a common boundary with the top portion;
   the bottom portion (112) of the first source/drain region is fully silicided; and
   the top portion (114) of the first source/drain region is partly silicided.

2. The semiconductor device according to claim 1, wherein a top portion (124) of the second source/drain region (120) is partly silicided.

3. The semiconductor device according to claim 1 or 2, further comprising a first connecting structure (116) for electrically contacting at least a part of the bottom portion (112) of the first source/drain region (110) and a second connecting structure (126) for electrically contacting at least a part of a top portion (124) of the second source/drain region (120).

4. The semiconductor device according to claim 3, wherein:

   the first connecting structure (116) is configured to electrically contact the bottom portion (112) of the first source/drain region (110) from a side of the fin structure facing the substrate; and
   the second connecting structure (126) is configured to electrically contact a surface of the top portion (114) of the first source/drain region and/or a surface of the top portion (124) of the second source/drain region (120), said surface(s) facing away from the substrate.

5. The semiconductor device according to any of the previous claims, wherein the top portion (114) of the first source/drain region and/or the top portion (124) of the second source/drain region (120) comprises a silicided outer layer.

6. The semiconductor device according to any of the previous claims, wherein the top portion (114) of the first source/drain region (110) fully overlaps the bottom portion (112) of the first source/drain region (110) as seen in a direction transverse to a main plane of extension of the substrate (140).

7. The semiconductor device according to any of the previous claims, wherein the substrate comprises a well (142) doped with a dopant of a first dopant type, wherein a region (144) of the well sharing a common boundary with the bottom portion (112) of the first source/drain region (110) comprises a higher dopant concentration than the remaining regions of the well,

and wherein the top portion of the first and second source/drain regions are doped with a second dopant type.

8. The semiconductor device according to claim 3 or 4, wherein:

at least a part of the top portion (124) of the second source/drain region (120) is provided with an epitaxial contacting structure forming part of the second connecting structure (126).

9. A method for forming a semiconductor device, comprising:

forming a fin structure having a first source/drain region (110), a second source/drain region (120) and a channel region (130), wherein the channel region is arranged between the fist source/drain region and the second source/drain region, thereby separating the first source/drain region and the second source/drain region in a length direction of the fin structure, and wherein the first source/drain region (110) comprises a bottom portion (112) and a top portion (114), the bottom portion being arranged between the top portion and a substrate (140) of the semiconductor device and such that the bottom portion shares a common boundary with the top portion;
depositing a first silicidation metal on the top portion (114) of the first source/drain region (110);
annealing the material of the top portion (114) of the first source/drain region (110) to react the first silicidation metal with said material such that the top portion (114) of the first source/drain region (110) is partly silicided;
providing a second silicidation metal on the bottom portion (112) of the first source/drain region (110); and
annealing the material of the bottom portion (112) of the first source/drain region (110) to react the second silicidation metal with said material such that the bottom portion (112) of the first source/drain region (110) is fully silicided.

10. The method according to claim 9, wherein providing the second silicidation metal comprises:

forming a recess exposing sidewalls of the bottom portion (112) of the first source/drain region (110);
depositing the second silicidation metal in the recess.

11. The method according to claim 9 or 10, further comprising:

removing the first silicidation metal from portions of the fin structure that have not been silicided.

12. The method according to any one of claims 9 to 11, further comprising:

depositing an inter-layer dielectric, ILD, prior to reacting the second silicidation metal.

13. The method according to any one of claims 9-12, further comprising:

doping the substrate to form a well (142) such that a region (144) of the well sharing a common boundary with the bottom portion (112) of the first source/drain region (110) comprises a higher dopant concentration than the remaining regions of the well.

14. The method according to claim 13, wherein the doping comprises:

forming a recess in the substrate, the recess being positioned adjacent to the fin structure; and at least partly filling the recess with a doped oxide, wherein at least the bottom portion of at least one of the first and second source/drain regions are doped in a solid-phase diffusion process.

15. The method according to any one of claim 9-14, further comprising:

forming a first connecting structure (116) for electrically contacting at least a part of the bottom portion (112) of the first source/drain region (110);
forming a second connecting structure (126) for electrically contacting at least a part of the top portion (114) of the first source/drain region (110) and/or at least a part of a top portion (124) of the second source/drain region (120).

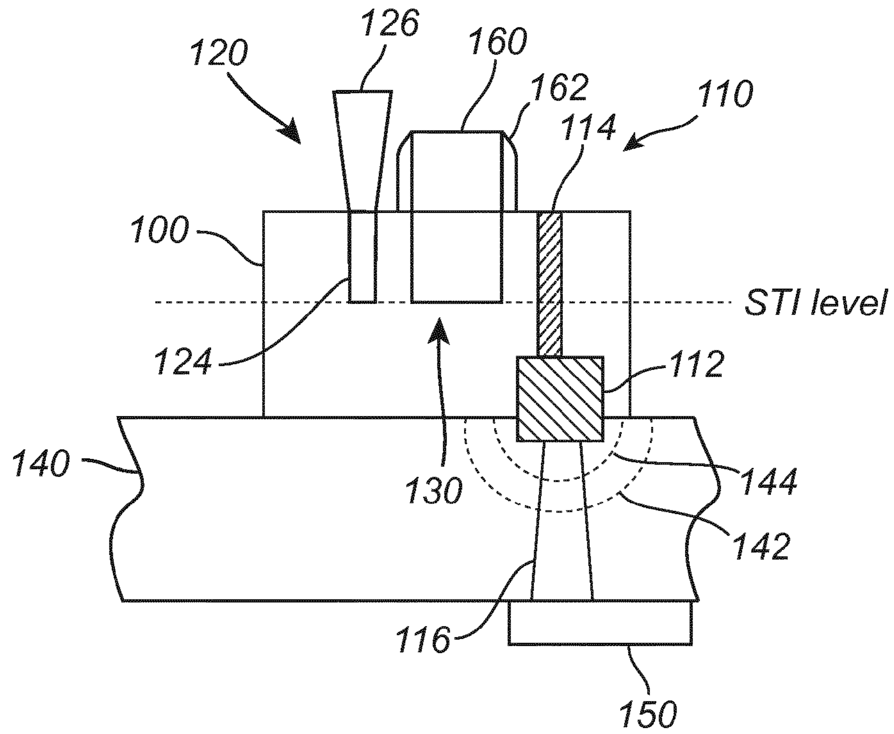

Fig. 1

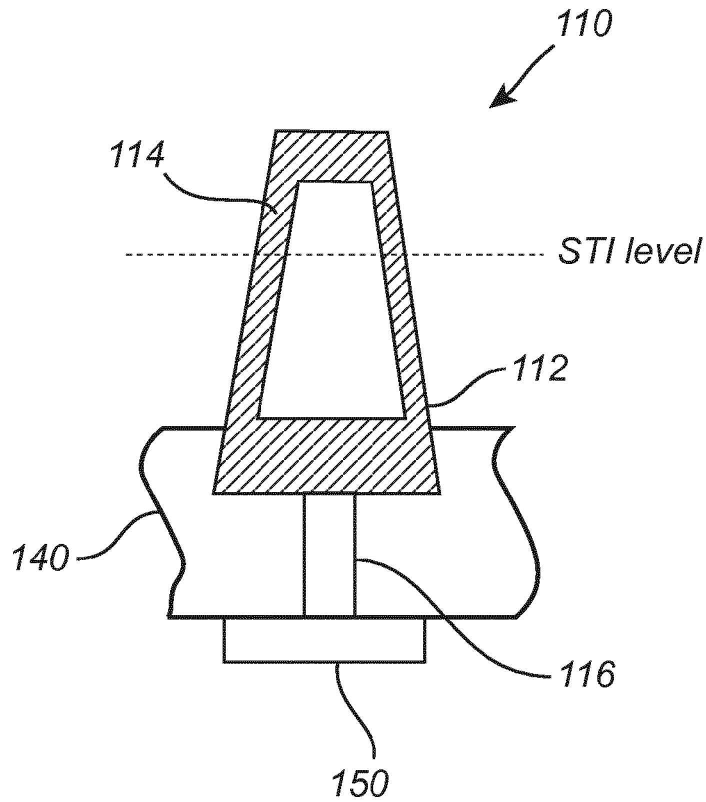

Fig. 2

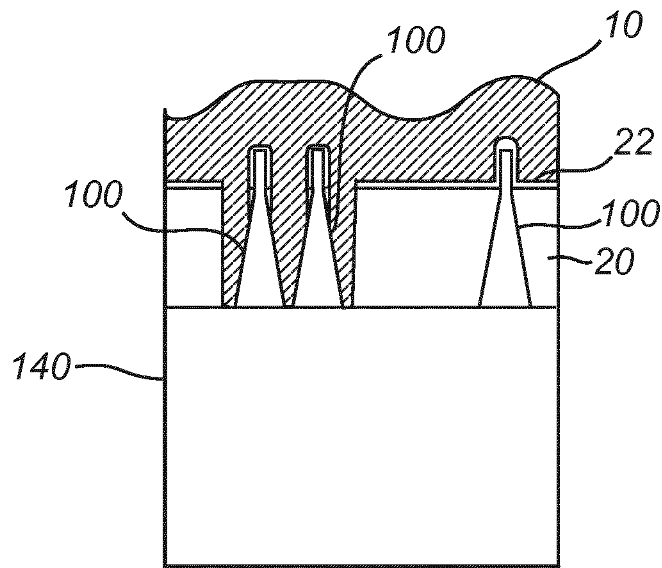

Fig. 3

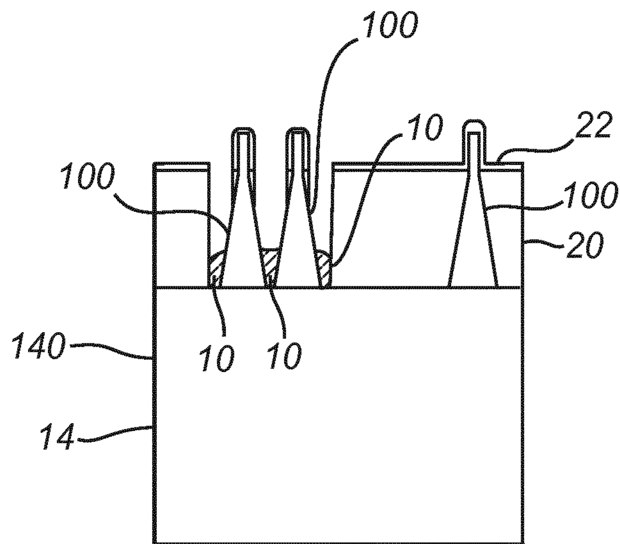

Fig. 4

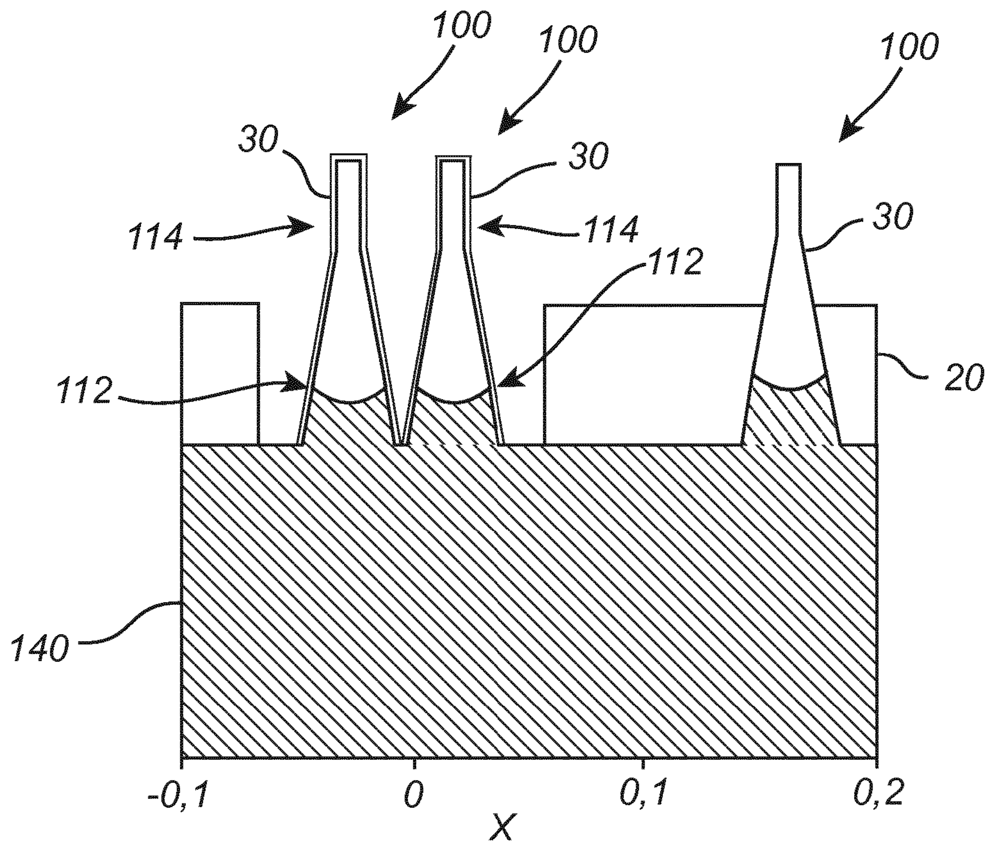

Fig. 5

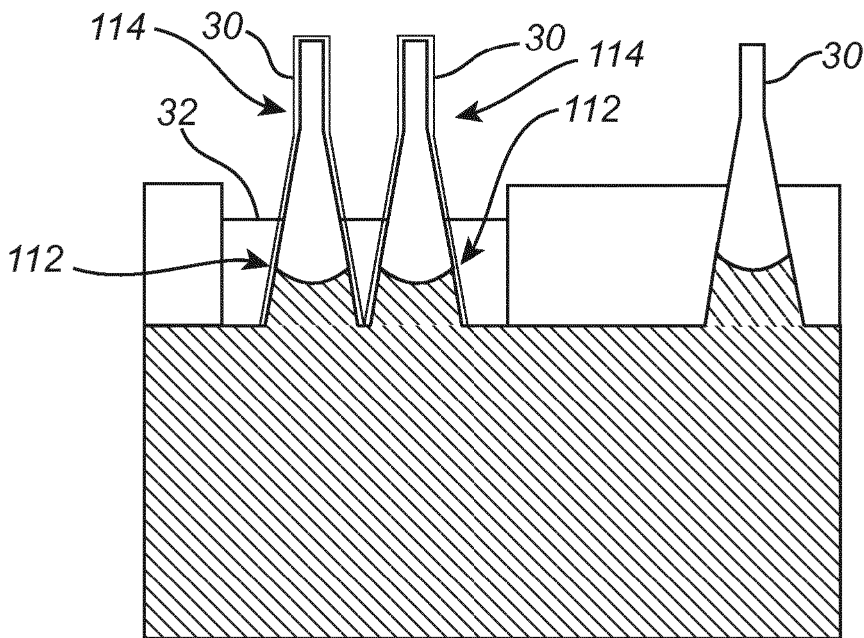

Fig. 6

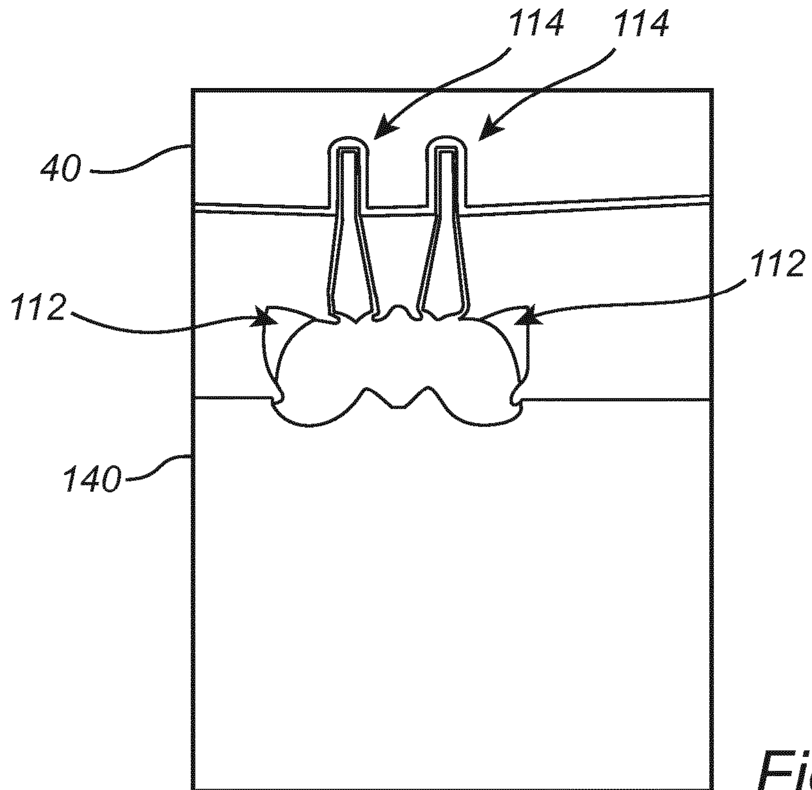

Fig. 7

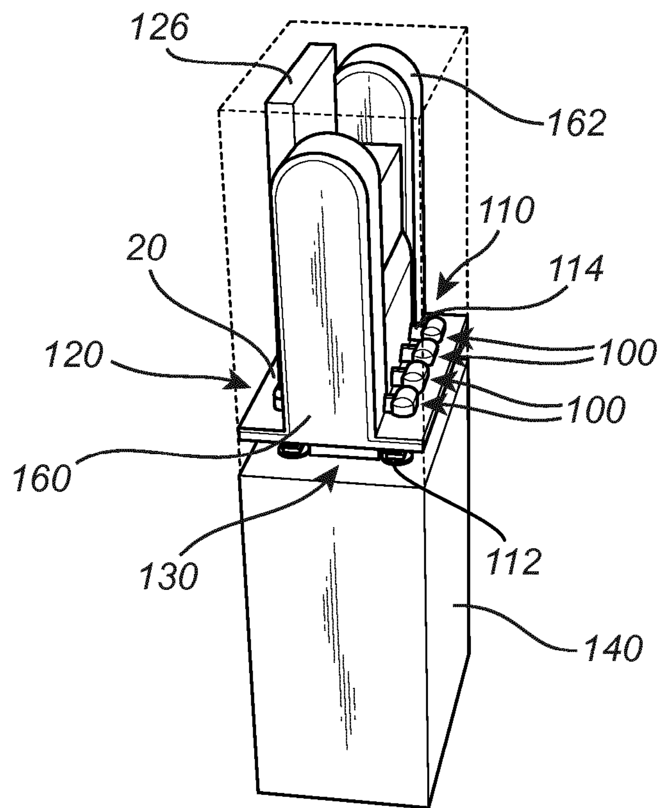

Fig. 8

EUROPEAN SEARCH REPORT

Application Number
EP 18 21 2336

5 10 15 20 25 30 35 40 45 50 55

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Place of search	Date of completion of the search	Examiner
Berlin	18 June 2019	Hoffmann, Niels

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