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(54) Improvements relating to digital data transmission

(57) Data bits such as digital samples of a sound signal are supplemented by error checking bits, e.g. provided by a Parity Generator, and these error bits are used to carry additional data bits (Extra Data) very securely by using the additional data bits to modify groups of the parity bits by way of a Pattern Generator and Parity Modifier. The additional data may be 3-bit scale factors applying to groups of digitally companded samples. The modification is detectable and reversible and may be selective inversion of all bits in a parity bit group. At the receiving end the Data and Parity bits are conventionally treated in a Parity Checker whose output can be recognised as groups of un-modified (non-inverted) and modified (inverted) bits by a Pattern Recogniser, using majority logic so that recognition is not upset by occasional bit errors. The Pattern Recogniser thus recovers the Extra Data and enables the actual parity bits to be recovered via a Pattern Generator and Parity Check Modifier. These bits are used conventionally in relation to Corrective Action on the main Data.

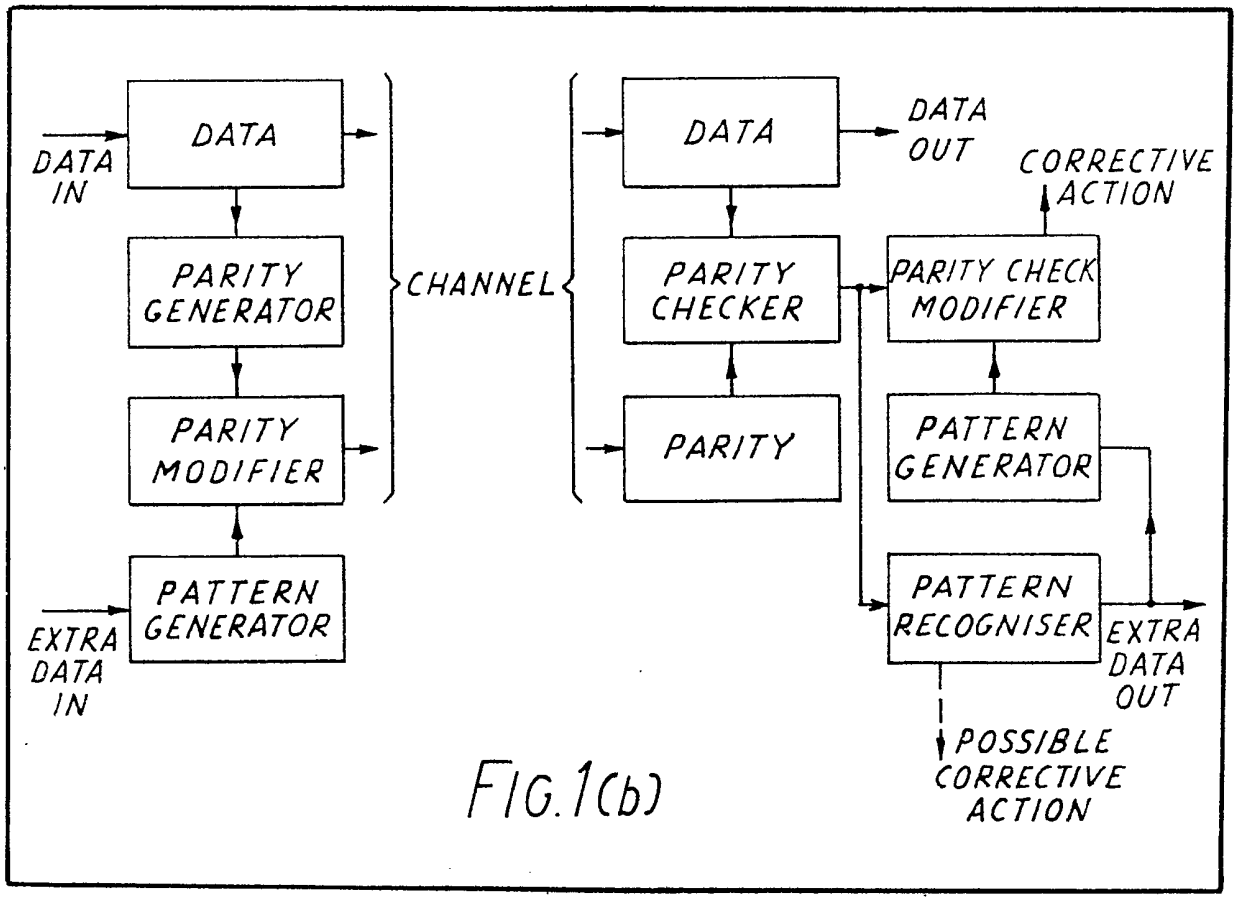

FIG. 1(b)

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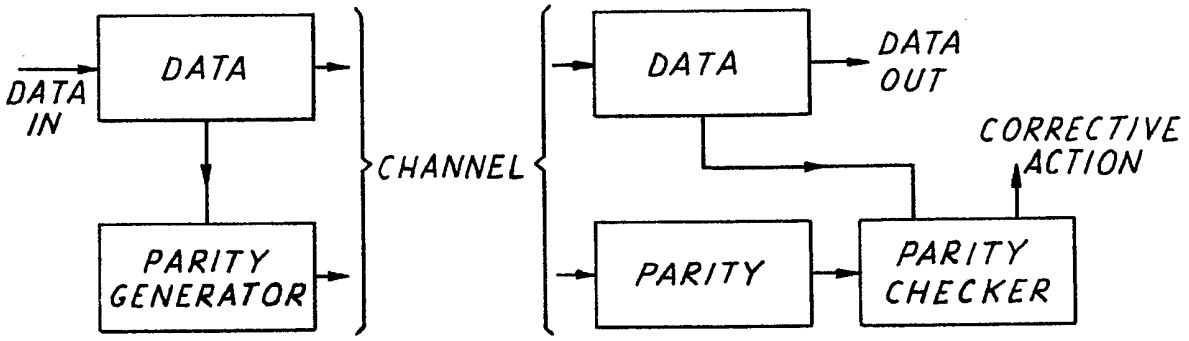
DATA IN
DATA
PARITY GENERATOR
CHANNEL
DATA
PARITY
DATA OUT
CORRECTIVE ACTION
PARITY CHECKER

FIG. 1(a)

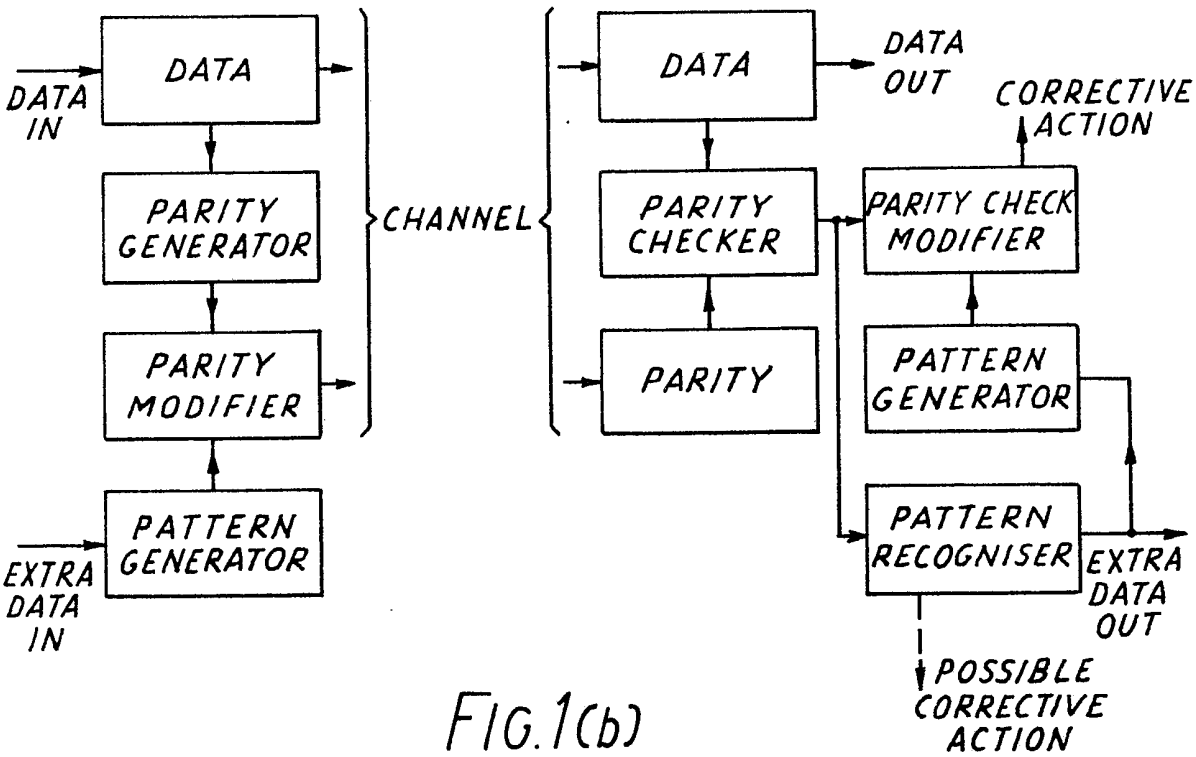
DATA IN
DATA
PARITY GENERATOR
PARITY MODIFIER
PATTERN GENERATOR
EXTRA DATA IN
CHANNEL
DATA
PARITY
DATA OUT
CORRECTIVE ACTION
PARITY CHECKER
PARITY CHECK MODIFIER
PATTERN GENERATOR
PATTERN RECOGNISER
EXTRA DATA OUT
POSSIBLE CORRECTIVE ACTION

FIG. 1(b)

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FIG. 2(a)

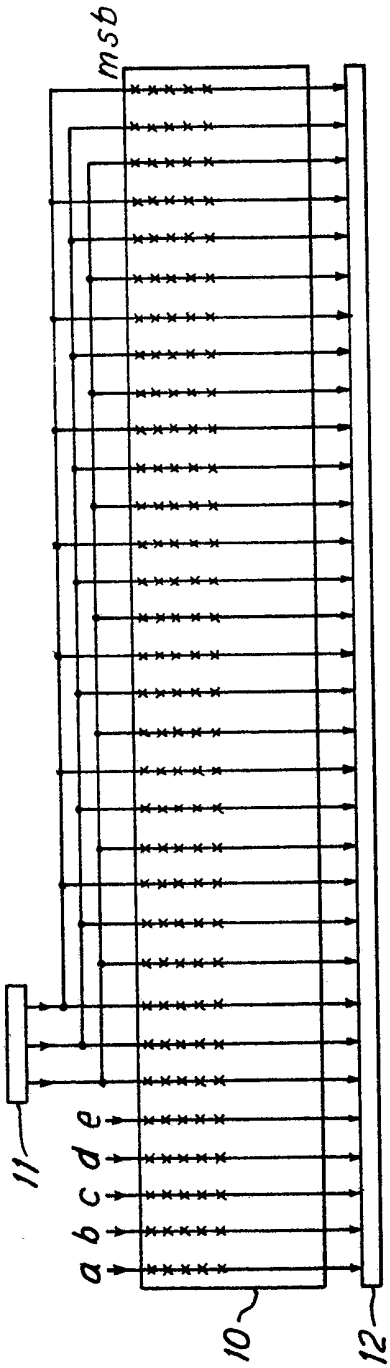
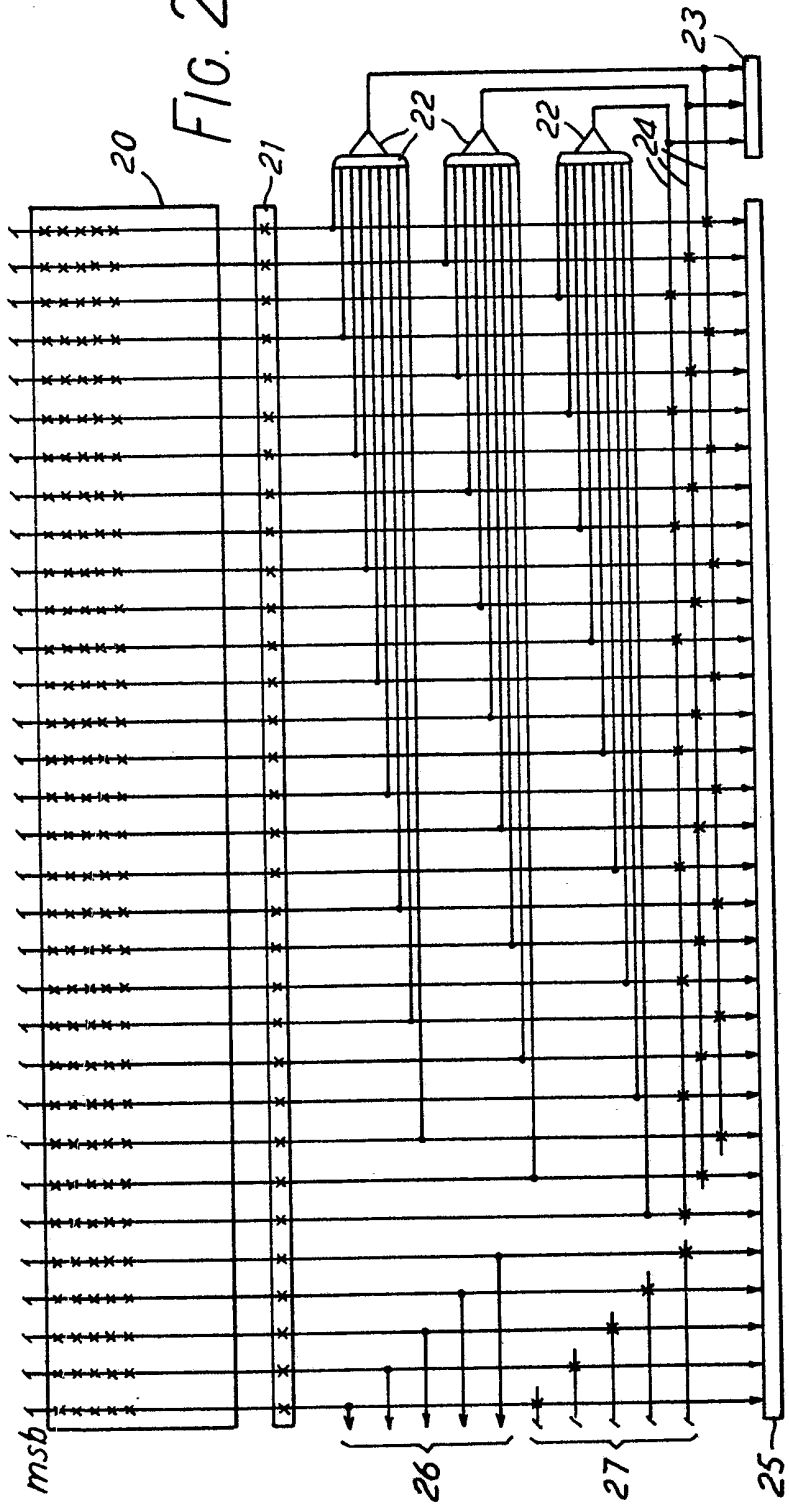


FIG. 2(b)



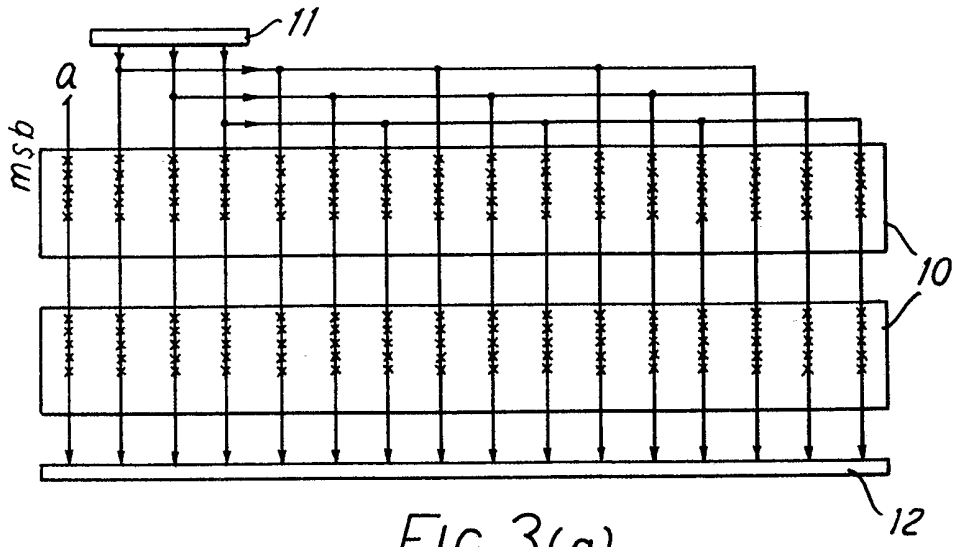


FIG. 3(a)

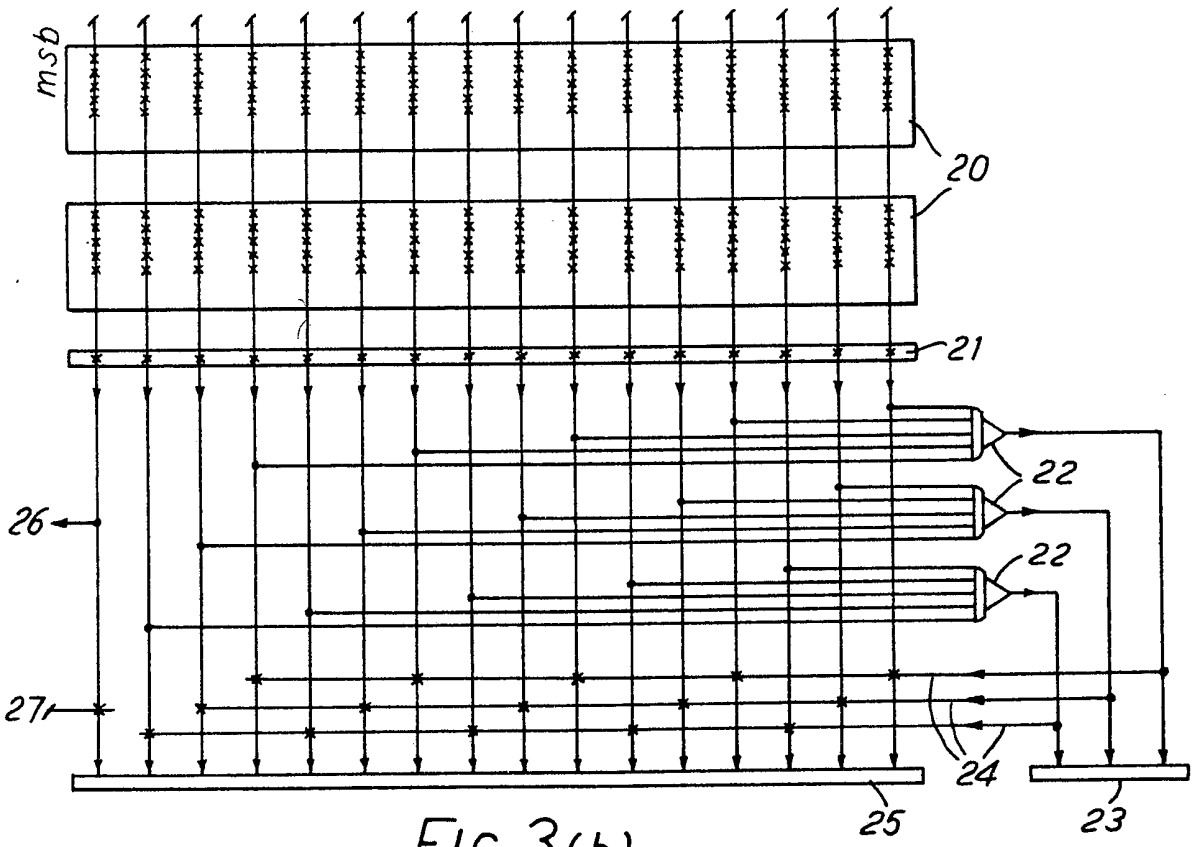


FIG. 3(b)

SPECIFICATION

Improvements relating to digital data transmission

The present invention relates to an improved method of digital data transmission and an improved transmitter and receiver. The object of the invention is to enhance the data-carrying capacity by utilizing parity and other error checking signals also to carry information signals. It is a further object of the invention to enable such supplementary information signals to be transmitted with a high degree of reliability.

For convenience, the present application refers simply to transmission of data. This may be transmission by transmission line, radio, optical fibre, etc. but may equally be transmission by a recording/playback process. The appended claims are to be interpreted accordingly. The medium whereby transmission takes place, i.e. any propagation or recording medium which involves delay and possible distortion, may be referred to as a channel.

When simple parity bits are added to data at the input to a channel and then checked afterwards, almost all the checks are correct if the channel contributes few errors to the data. It could be argued that the signalling capacity of the parity channel is then being wasted, as it is carrying very little information. The present invention proposes a general technique for using some of the information capacitiy of the parity channel, thereby increasing the overall efficiency of the data channel. The invention is defined in the appended claims.

Although described in terms of binary data, the principle can be applied directly to any digital data, for example data using a ternary or higher base number. Although described, in the example, in terms of simple parity check bits the invention can be applied to other error protection methods.

The invention will now be described in more detail, by way of example, with reference to the accompanying drawings, in which:

Figs. 1(a) and 1(b) are block diagrams of a conventional data transmission system and a system embodying the invention respectively,

Fig. 2(a) and 2(b) are schematic diagrams of the transmitter and receiver of a specific embodiment of the invention for use with a companded digital sound transmission system, and

Figs. 3(a) and 3(b) are schematic diagrams of the transmitter and receiver of a modified embodiment.

The technique is described in general terms by reference to Fig. 1. A conventional data channel with parity added at the input and checked at the output is shown in Fig. 1(a). A failure of a parity check implies the need for corrective action which, in practice, depends on the nature of the data and channel.

In Fig. 1(b) an extra data input is used to control a pattern generator; the patterns are distributed over several parity bits. The parity bits are then modified by the pattern before being transmitted. The modifier is, most simply, a modulo-2 ("exclusive or") sum of the parity and the pattern bit-by-bit. At the end of the channel a parity check is performed. In the absence of error this check would give, for example, all zeroes, but instead it now gives one of the patterns. The output of the checker is examined in a pattern recogniser where the nearest or identical pattern is converted back into extra data output. This pattern, corrected if necessary, is used to modify the output of the parity checker to restore its conventional significance. If because of channel errors, the pattern recogniser cannot give an equivocal decision about the extra data it may itself signal the need for corrective action. When, under high error rate conditions, the wrong pattern is recognised the consequent modification of the parity check will provide false information.

Practical examples of an embodiment of the technique will now be given. They relate to the near-instantaneous companded system of digital sound transmission such as described in Croll, M.G. Moffat M.E.B. & Osborne, D. W. 1973, "Nearly-instantaneous digital compander for transmitting six sound-programme signals in 2.048 Mbit/s multiplex", Electron. Letters, 1973, 9, 14, pp 298—300. Sound signals are sampled at 32kHz and the samples are uniformly quantised to 14-bit accuracy. Consecutive groups of 32 coded samples are examined and scaled by a factor 1, 2, 4, 8 or 16 to give a 10-bit signal whilst preserving the long-term dynamic range. This gives a saving in required channel bit-rate but it requires the scale factor for each group to be transmitted very reliably. This scale factor, one of five values, is conventionally coded as a three-bit number with some unused states. In order to protect the data corresponding to the five most significant bits of the companded samples, a simple parity check is used on each sample (32 parity bits per group) or on pairs of samples (16 parity bits per group). In the embodiments of the present invention, these parity bits are used to signal the scale factor, which would otherwise be sent as additional data requiring good protection.

In all of Figs. 2(a) to 3(b), crosses are employed to symbolize exclusive or operations. All operations are represented schematically and are of a well-known nature in themselves. As is equally well known, they may be implemented by dedicated circuits or by use of a programmed microprocessor.

Referring to the transmitter shown in Fig. 2(a), a block 10 of 32×10 bits is formed for transmission, in the known manner outlined above and the accompanying 3-bit scale factor is formed and latched in a register 11. In accordance with conventional practice, a 32-bit parity block would be formed in a register 12 solely by exclusive-or operations on the 5 most significant bits of each 10-bit sample in the block 10. However, in carrying out the invention, Fig. 2(a) shows how 27 of the 32 parity bits at the input are modified in three groups of nine

according to the three bits of the scale factor. The pattern for each extra data bit is nine parity bits either all changed or all unchanged. In the output decoder (Fig. .2(b)) the parity check is performed conventionally by performing exclusive or operations on the 5 most-significant bits of each sample in the received block 20 and then exclusive-or'ing with the bits in the received parity block 21. In a conventional system, all 32 outputs from the block 21 would (in the absence of errors) be all "0" or all "1" depending upon whether even or odd parity were employed. However, in performing the present invention, the three groups of nine checks are gathered together in majority logic gates 22 to give the scale factor bits. This is the pattern recogniser. The nine-input gates give an output according to which state is held by five or more of their inputs. The result of this pattern recognition, the three-bit scale factor, is latched in a register 23 and is moreover used to modify the appropriate three groups of nine parity checks to give a conventional result, as indicated by the exclusive-or operations on lines 24. The 32 parity bits are thus recovered in block 25 for use in the conventional manner. It will be appreciated that five or more of any particular group of nine parity checks would need to fail (each due to 1, 3, or 5 errors in the six bits tested) to give a wrong scale factor, At low error rates this probability is very low as indicated in the table below.

Figs. 2(a) and (b) show that the remaining five parity bits could be used to provide further signalling capacity using this technique, by application of further data to inputs *a* to *e*.

The corresponding outputs 26 would be applied to auxiliary data recovery circuits which will provide parity correction signals on lines 27. Alternatively, it would be beneficial to extend the three majority logic gates 22 to have 10, 11 and 11 inputs and so use all the 32 parity bits. This would give the greatest immunity to scale factor error. In the case of the 10-input gate there may be a situation with five inputs each way, this corresponds to the 'possible corrective action' shown in Fig. 1(b) and it would be clear in this case that that particular bit in the scale factor is in doubt. There may be application where this "no mans' land" area of operation can be used to monitor the behaviour of the channel and take corrective action whether or not there is an even number of inputs to the majority logic gates. The preferred allocation of the scale factor three-bit-codes to the five factors, and of the gate outputs to the bits of these codes, can be selected so as to yield best results, without affecting the principle of the invention.

Figs. 3(a) and (b) show similar diagrams where there are 16 parity bits each protecting the five most significant bits of a pair of samples. In this case, there are three groups of five parity bits used to send and recognise the pattern, and the immunity to scale factor error is reduced as each check is more likely to fail and only three failures in five are needed to alter the majority. Again there is possible advantage to be gained by using one 6-input gate to take advantage of 16 parity bits.

The computed failure rates of the two systems as drawn are given below. It is clear that at random bit error rates at which the sound samples themselves are not significantly degraded (i.e. less than about 10^{-4}) the scale factor failure rate is insignificant.

Random channel bit error rate	*Wrong scale factor code rate*	
	Figure 2	*Figure 3*
10^{-2}	1.9×10^{-4}	2.4×10^{-2}
10^{-3}	3×10^{-9}	4×10^{-5}
10^{-4}	3×10^{-14}	4×10^{-8}
10^{-5}	3×10^{-19}	4×10^{-11}

The technique for signalling in parity as described above could find many applications particularly where a small amount of well-protected additional data needs to be sent. The example of the companding scale factor detailed above is of immediate relevance to broadcasting; other potential applications include the control of digital multiplexers, in particular framing and adjusting for different bit rates ("bit stuffing").

In the case of binary data the invention can be seen to reside in a data transmission system transmitter and receiver. In the transmitter a group of error checking bits is used to transmit a supplementary data bit by leaving the group of bits unchanged for one supplementary bit value and subjecting the group to a predetermined, detectable and reversible transformation for the other supplementary bit value. In the specific case of a group of parity bits, the transformation can be inversion of all parity bits within the group.

At the receiver the group of bits is tested to ascertain whether or not the transformation has been applied. Specifically it is determined whether the majority of parity bits give a false or true parity check. The supplementary bit value is thus determined and the normal error checking and/or correcting procedures are applied on the basis of the received group of bits when it is determined that the transformation has not been applied and on the basis of the received group of bits subjected to the reverse (inverse) transformation when it is determined that the transformation has been applied.

Examples of transformations of the error checking signals have been given with reference to Figs. 2(a) to 3(b) but there are naturally many other possibilities. One advantageous example is to use distanced codes as the second digital information signals, for example the six codes described in our copending application 8226590 (Serial No) may be transmitted by enclusive or'ing with the 16 parity check bits. This gives full "majority of nine" benefit as explained in the said application when only 16 signalling bits are available.

Claims

1. A method of transmitting digital data wherein first digital information signals are processed to derive error checking signals, groups of the error checking signals are selectively subjected to at least one predetermined, detectable and reversible transformation in dependence upon second digital information signals, and the first digital information signals are transmitted accompanied by the selectively transformed error checking signals.

2. A method according to claim 1, wherein the transmitted signals are received, the selective transformations are detected to recover the second digital information signals, the error signals are selectively subjected to reverse transformation in dependence upon the detected transformations to recover the original error checking signals, and error checks are carried out in accordance with those error checking signals in conjunction with the first digital information signals.

3. A method according to claim 1 or 2, wherein the data is binary data and the or each reversible transformation consists in forming an exclusive or function between a group of bits of the first digital information signals and a predetermined pattern of bits.

4. A method according to claim 3, wherein the predetermined pattern is all ones, whereby the transformation consists in bit-wise inversion of the bits of the said group.

5. A method according to claim 3 or 4, wherein the received data and error checking signals are processed in accordance with the algorithm upon which the error checking is based to recover groups of bits which, in the absence of errors introduced during transmission, will possess a first predetermined pattern if not subject to transformation before transmission and will possess a different predetermined pattern for the or each transformation selectively effected before transmission, each recovered group of bits is assigned to that pattern to which it is closest, thereby to recover the second digital information signals, and errors are detected and/or corrected on the basis of any bit discrepancies between the recovered groups of bits and the patterns to which they are assigned.

6. A binary transmitter comprising means responsive to first binary data signals to form error checking bits, means responsive to second binary data signals to subject groups of the error checking bits selectively to detectable, reversible transformations, and means for transmitting the first binary data signals accompanied by the selectively transformed groups of error checking bits.

7. A transmitter according to claim 6, wherein the means responsive to the second binary data signals use each bit thereof to leave a corresponding group of error checking bits unchanged for one value of the said bit and, for the other value of the bit, to form an exclusive or function between the group of bits and a predetermined pattern of bits.

8. A binary data receiver for use with a transmitter according to claim 6, comprising means responsive to received binary data signals and error checking bits to form groups of recovered bits, means for matching the groups of recovered bits with a plurality of predetermined patterns so as to assign each group to its closest pattern, means providing further binary data signals corresponding to the assignations of the groups, and means providing error detecting and/or correcting bits in accordance with any discrepancies between the groups of bits and the patterns to which they are assigned.

9. A method according to claim 1 or 2, wherein the first digital information signals comprise data using a ternary or higher base number.

10. A method according to claim 3, wherein a plurality of different patterns of bits are employed to transmit distanced codes as the second digital information signals.

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