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(54) **METHOD FOR MAKING A SEMI-CONDUCTING SUBSTRATE LOCATED ON AN INSULATION LAYER**

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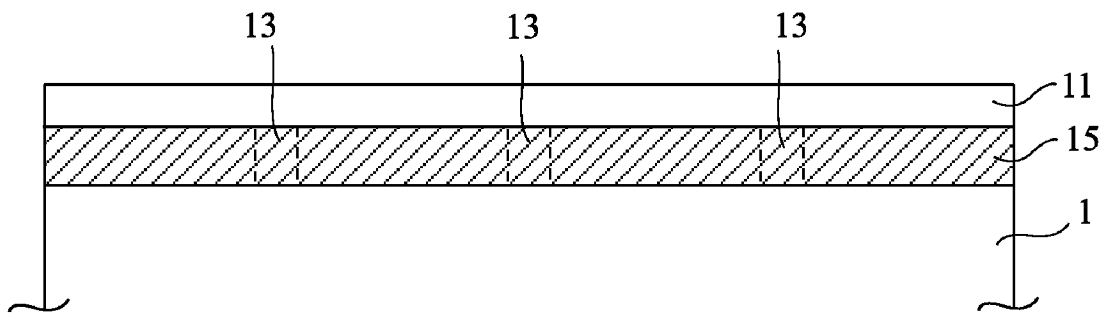
(57) **ABSTRACT**

A method for making a silicon layer extending on an insulation layer, including the steps of forming a silicon-germanium layer on at least a portion of a silicon wafer; transforming portions of the silicon-germanium layer into porous silicon pads; growing a monocrystalline silicon layer on the silicon-germanium layer and on the porous silicon pads; removing the silicon-germanium layer; oxidizing the porous silicon pads; and depositing an insulation material on the silicon layer.



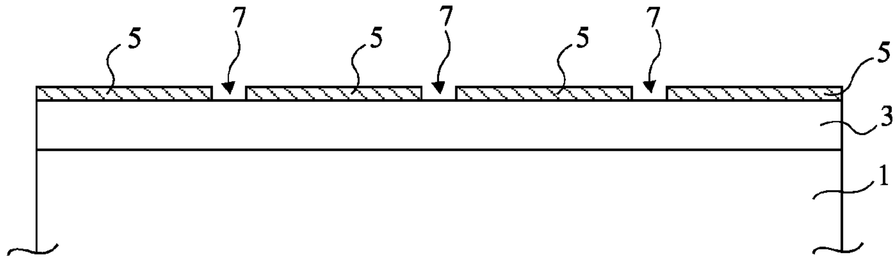


Fig 1A

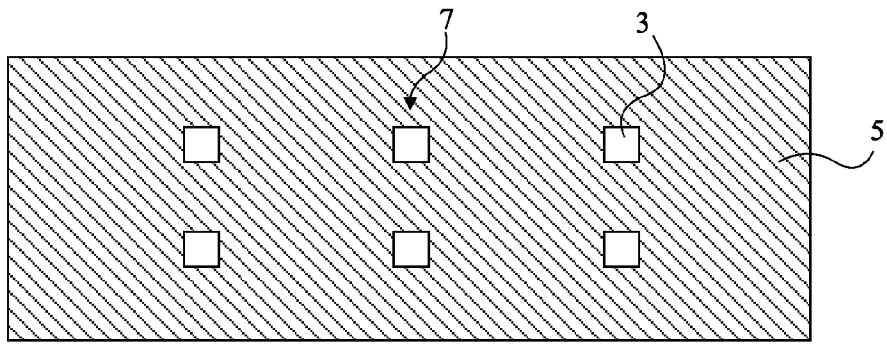


Fig 1B

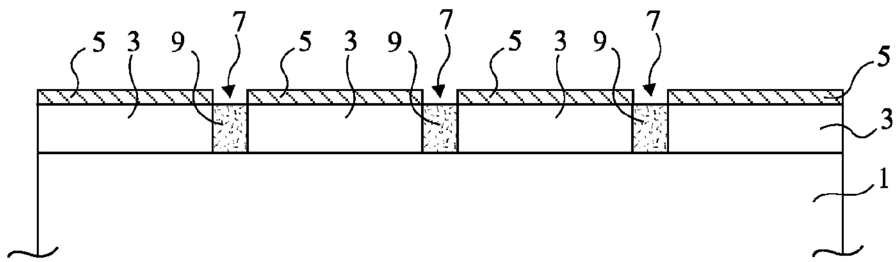


Fig 1C

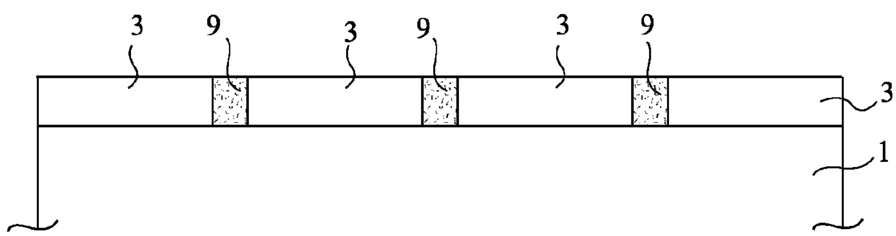


Fig 1D

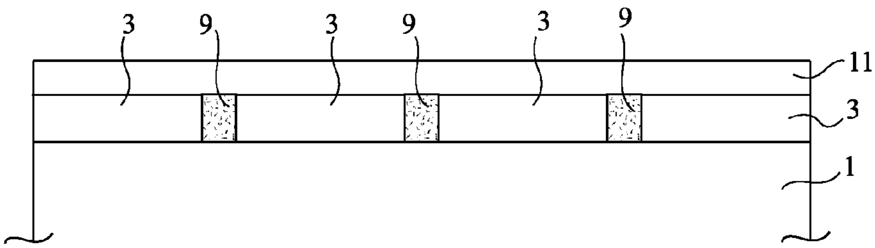


Fig 1E

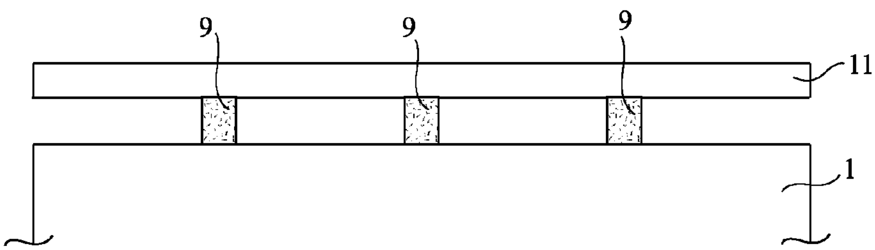


Fig 1F

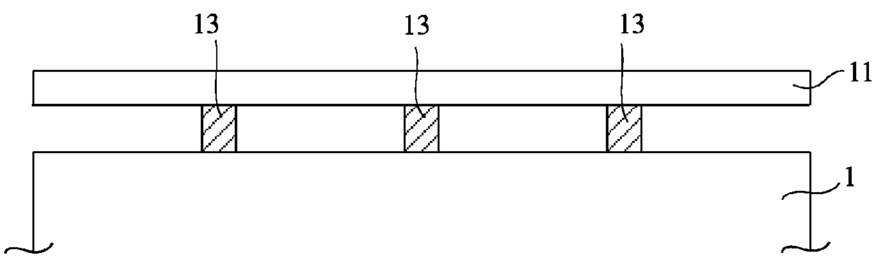


Fig1G

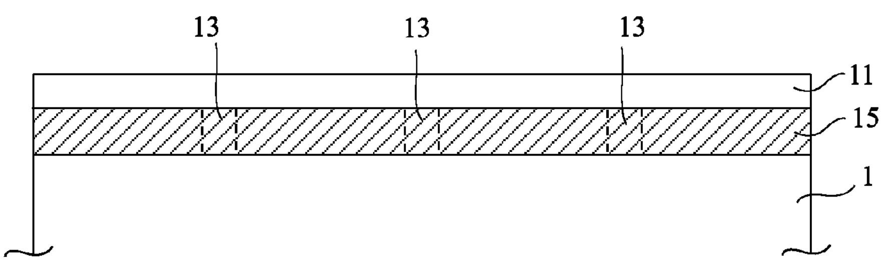


Fig1H

METHOD FOR MAKING A SEMI-CONDUCTING SUBSTRATE LOCATED ON AN INSULATION LAYER

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a U.S. national stage patent application based on PCT application number PCT/FR2008/051717, entitled "Method For Making A Semi-Conducting Substrate Located On An Insulation Layer", filed on Sep. 26, 2008 which application claims priority to French patent application number 07/57916, filed on Sep. 28, 2007, entitled "Method For Making A Semi-Conducting Substrate Located On An Insulation Layer" which applications are hereby incorporated by reference to the maximum extent allowable by law.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to structures comprising a semiconductor substrate formed locally on a semiconductor wafer with an interposed insulating layer and, more specifically, to a method for manufacturing such a structure.

[0004] 2. Discussion of the Related Art

[0005] Currently, semiconductor components are formed either in a solid semiconductor wafer, or in a semiconductor layer formed on an insulating layer, these latter substrates being generally called SOI substrates (for "Silicon On Insulator").

[0006] Substrates formed on a semiconductor support with an interposed insulating layer have the advantage of enabling for the components formed in and on these substrates to be insulated from the support, which avoids biasing said support and avoids interference between the components via the support. A disadvantage of known methods for manufacturing such substrates is that these substrates are formed on an entire surface of the support.

SUMMARY OF THE INVENTION

[0007] An embodiment of the present invention aims at a method for manufacturing, on a semiconductor wafer, a local structure formed of a portion of semiconductor layer formed on an insulating layer portion.

[0008] Thus, an embodiment provides a method for manufacturing a silicon layer extending on an insulating layer, comprising the steps of: forming a silicon-germanium layer on at least a portion of a silicon wafer; transforming portions of the silicon-germanium layer into porous silicon pads; growing a single-crystal silicon layer on the silicon-germanium layer and on the porous silicon pads; eliminating the silicon-germanium layer; oxidizing the porous silicon pads; and depositing an insulating material under the silicon layer.

[0009] According to an embodiment, the transforming of the portions of the silicon-germanium layer into porous silicon pads comprises the steps of: forming, on the silicon-germanium layer, a mask comprising openings; performing an electrolysis of the silicon-germanium layer; and removing the mask.

[0010] According to an embodiment, the transforming of the portions of the silicon-germanium layer into porous silicon pads comprises the steps of: forming, on the silicon-germanium layer, a mask comprising openings; etching the silicon-germanium layer down to the silicon wafer at the level of the openings; growing by epitaxy silicon portions on the wafer in the etched portions of the silicon-germanium layer; performing an electrolysis of the silicon portions; and removing the mask.

[0011] According to an embodiment, the thickness of the silicon layer and the thickness of the insulating layer range between 10 and 20 nm.

[0012] According to an embodiment, the porous silicon pads have dimensions smaller than 1 μm and are spaced apart from one another by 10 μm.

[0013] An embodiment further provides a structure comprising a silicon layer hung above a silicon wafer by porous silicon pads.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The foregoing and other objects, features, and advantages of the present invention will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

[0015] FIGS. **1**A and **1**C to **1**H are cross-section views illustrating steps of a method according to an embodiment of the present invention, FIG. **1**B being a top view corresponding to the cross-section view of FIG. **1**A.

[0016] For clarity, the same elements have been designated with the same reference numerals in the different drawings and, further, as usual in the representation of semiconductor structures, the various drawings are not to scale.

DETAILED DESCRIPTION

[0017] Successive steps of a method for obtaining a single-crystal silicon layer on an insulating layer resting on a silicon wafer according to an embodiment will be described in relation with FIGS. **1**A to **1**H.

[0018] As illustrated in FIGS. **1**A and **1**B, respectively in cross-section view and in top view, it is started from a silicon wafer **1** on which a local silicon-germanium layer **3** is formed. As an example, silicon-germanium layer **3** may be formed by epitaxial growth under a gas flow, for example, of silane and germane. Also as an example, layer **3** may have a thickness ranging between 10 and 20 nm. A mask **5** is then formed above silicon-germanium layer **3**. Mask **5** comprises openings **7** nearly in the form of points and, preferably, regularly spaced apart. In the example of FIG. **1**B, openings **7** are, in top view, small squares. As an example, openings **7** may have dimensions of approximately 1 μm and be spaced apart by a distance of approximately 10 μm. Mask **5** may be formed by the deposition of an insulating layer of the silicon-germanium layer, followed by the deposition of a resist which is insolated through a pattern comprising adapted openings. The insolated resist is etched and the insulating layer is then etched at the level of the resist openings. The resist layer is then removed. This method enables forming a mask **5** of an insulating material, presently called a "hard mask".

[0019] At the step illustrated in FIG. **1**C, an electrolysis has been performed. This electrolysis transforms the portions of silicon-germanium layer **3** located opposite to openings **7** of mask **5** into porous silicon **9**. It should be noted that, generally, during the electrolysis, the germanium atoms in the transformed portions of silicon-germanium layer **3** migrate in the electrolytic liquid, whereby porous material **9** is essentially silicon.

[0020] As a variation, to obtain the structure of FIG. **1**C from the structure of FIGS. **1**A and **1**B, it is possible to carry out the successive steps of:

[0021] etching silicon-germanium layer **3** at the level of openings **7** down to silicon wafer **1** (for example, by plasma etch);

[0022] growing, by selective epitaxy, silicon portions on silicon wafer **1** in the previously-formed openings; and

[0023] performing an electrolysis of the silicon portions thus formed to transform them into porous silicon **9**.

[0024] As compared with the steps of the previously-described method in which silicon-germanium layer **3** is directly transformed into porous silicon **9** at the level of openings **7** of mask **5**, this variation has the advantage of enabling a greater flexibility in the selection of the used technologies.

[0025] At the step illustrated in FIG. **1**D, mask **5** has been removed, for example, by etching.

[0026] At the step illustrated in FIG. **1**E, a single-crystal silicon layer **11** has been grown by epitaxy over silicon-germanium layer **3** and porous silicon portions **9** altogether. Silicon layer **11** forms the substrate in and on which electronic components will be formed. The growth by epitaxy of single-crystal silicon layer **11** is possible since porous silicon portions **9** keep the initial crystal structure of the silicon-germanium of layer **3**. As an example, silicon layer **11** may have a thickness ranging between 10 and 20 nm.

[0027] At the step of FIG. **1**F, silicon-germanium layer **3** has been eliminated by selective etching with respect to porous silicon **9** and to the single-crystal silicon of wafer **1** and of layer **11**. This etching may be a plasma etching and it may be performed from the sides of silicon-germanium portion **3** or via openings, not shown, formed in silicon layer **11**. A structure comprising a silicon layer **11** hung above silicon wafer **1** by porous silicon pillars or pads **9** is thus obtained.

[0028] At the step of FIG. **1**G, an oxidation of the porous silicon of pads **9** has been carried out. Pads **9** are thus transformed into silicon oxide pads **13**. The oxidation may comprise a first low-temperature oxidation step (300-400° C.) for a time period of approximately one hour under an oxygen flow, followed by a second oxidation step at higher temperature (700-800° C.). These two steps enable stabilizing the oxidized porous silicon structure and preventing its degradation.

[0029] FIG. **1**H shows the structure obtained after having filled the empty space under silicon layer **11** with an insulator **15**. This filling of the space under layer **11** between pads **13** may be performed under a gas flow. As an example, the insulator deposited during this step may be silicon oxide (SiO_2). A structure comprising a single-crystal silicon portion **11** formed on a portion of insulating layer **13**, **15** which itself extends on single-crystal silicon wafer **1** is thus obtained.

[0030] To obtain a structure identical to that provided herein, a method comprising the growth, on a semiconductor wafer, of a portion of a silicon-germanium layer topped with a portion of a silicon layer may have been used. Then, an etching is performed, from a side of the silicon-germanium layer or from a hole formed in the silicon layer, to remove a portion of silicon-germanium layer. The silicon layer is then maintained above the semiconductor wafer by the remaining portion of the silicon-germanium layer. An insulator is then deposited, in the same way as in the step of FIG. **1**H, under the silicon layer and the remaining silicon-germanium is etched. However, if it is desired to form the stacking of the insulating layer portion and of the silicon layer portion on a relatively large surface area of the wafer, there is a risk for the silicon layer to collapse, due to its weight, once the etching of a portion of the silicon-germanium has been performed. The method according to an embodiment of the present invention enables avoiding this collapse phenomenon since, when silicon-germanium layer **3** is etched at the step of FIG. **1**F, silicon layer **11** is maintained at several points by porous silicon pads **9**. To avoid the collapse, the distance separating pads **9** must be properly specified. This enables forming, on a significant surface area of wafer **1**, a structure comprising the stacking of insulating layer **15** and of silicon layer portion **11**.

[0031] A structure formed of a silicon layer **11** extending on an insulating layer **15** formed on a portion only of a semiconductor wafer **1** has been described previously. However, this structure may also be formed on the entire surface of the semiconductor wafer.

[0032] Specific embodiments of the present invention have been described. Variation alterations, modifications and improvements will occur to those skilled in the art. In particular, openings **7** formed in mask **5** have been defined as having a square shape in top view. However, any other shape of openings then enabling obtaining holding pads may be envisaged, for example, rounded or hexagonal shapes. As a variation, openings **7** may also be strips in top view. In all cases, pads **9** must be close enough to avoid a collapsing of silicon layer **11** in the etch step of FIG. **1**F, and they must not prevent the etching of the entire silicon-germanium layer **3**.

[0033] As a variation, the insulating material of layer **15** may be any insulating material other than silicon oxide, for example, a nitride or a metal oxide having a high dielectric constant (so-called "high-k" material) such as hafnium dioxide (HfO_2) or zirconium dioxide (ZrO_2).

[0034] An advantage of the present invention is to enable forming, on a same silicon wafer, components directly formed in this silicon wafer, currently designed in the art as "bulk components" and components formed in a thin silicon-on-insulator layer.

[0035] Such alterations, modifications and improvements are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The invention is limited only as defined in the following claims and the equivalent thereto.

What is claimed is:

1. A method for manufacturing a silicon layer extending on an insulating layer, comprising the steps of:

forming a silicon-germanium layer on at least a portion of a silicon wafer;

transforming portions of the silicon-germanium layer into porous silicon pads;

growing a single-crystal silicon layer on the silicon-germanium layer and on the porous silicon pads;

eliminating the silicon-germanium layer;

oxidizing the porous silicon pads; and

depositing an insulating material under the silicon layer.

2. The method of claim **1**, wherein the transforming of the portions of the silicon-germanium layer into porous silicon pads comprises the steps of:

forming, on the silicon-germanium layer, a mask comprising openings;

performing an electrolysis of the silicon-germanium layer; and

removing the mask.

3. The method of claim **1**, wherein the transforming of the portions of the silicon-germanium layer into porous silicon pads comprises the steps of:

forming, on the silicon-germanium layer, a mask comprising openings;

etching the silicon-germanium layer down to the silicon wafer at the level of the openings;

growing by epitaxy silicon portions on the wafer in the etched portions of the silicon-germanium layer;

performing an electrolysis of the silicon portions; and removing the mask.

4. The method of claim **1**, wherein the thickness of the silicon layer and the thickness of the insulating layer range between 10 and 20 nm.

5. The method of claim **1**, wherein the porous silicon pads have dimensions smaller than 1 μm and are spaced apart from one another by 10 μm.

6. A structure comprising a silicon layer hung above a silicon wafer by porous silicon pads.

* * * * *