US 20140063636A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2014/0063636 A1**

(43) **Pub. Date: Mar. 6, 2014**

Zhang et al.

(54) **SYSTEMS AND METHODS FOR CONDITIONAL POSITIVE FEEDBACK DATA DECODING**

(75) Inventors: **Fan Zhang**, Milpitas, CA (US); **Shaohua Yang**, San Jose, CA (US)

(73) Assignee: **LSI Corporation**

(21) Appl. No.: **13/596,947**

(22) Filed: **Aug. 28, 2012**

Publication Classification

(51) **Int. Cl.**

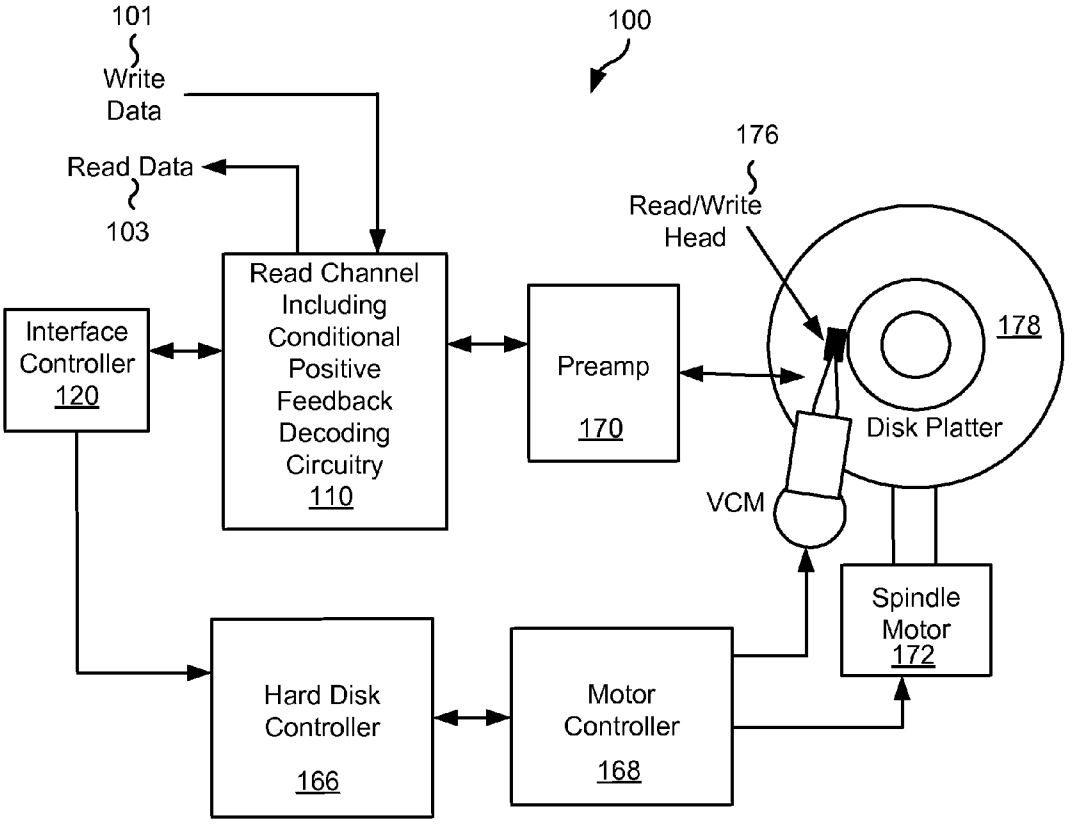
H03M 7/00	(2006.01)
H04L 27/06	(2006.01)
G11B 5/035	(2006.01)

(52) **U.S. Cl.**

USPC **360/65**; 375/340; 341/50

(57) **ABSTRACT**

The present inventions are related to systems and methods for information data processing included selective decoder message determination.



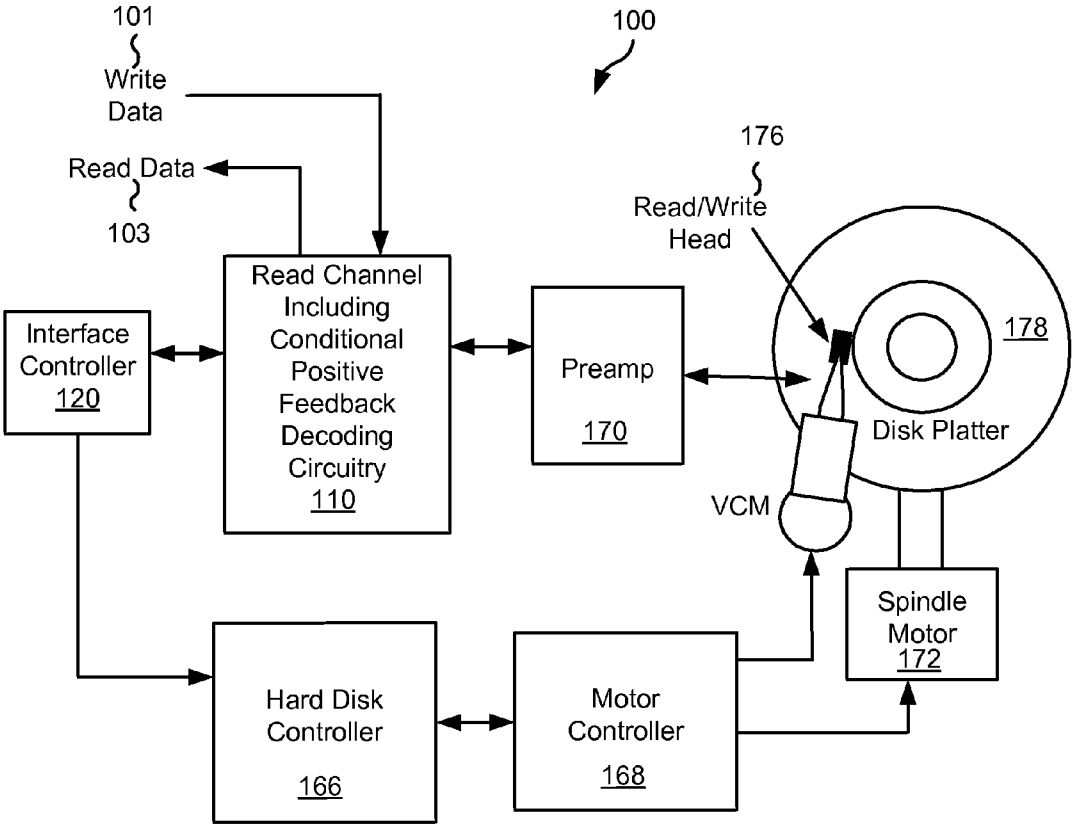

101
Write Data
Read Data
103
100
176
Read/Write Head
Read Channel Including Conditional Positive Feedback Decoding Circuitry 110
Interface Controller 120
Preamp 170
178
Disk Platter
VCM
Spindle Motor 172
Hard Disk Controller 166
Motor Controller 168

Fig. 1

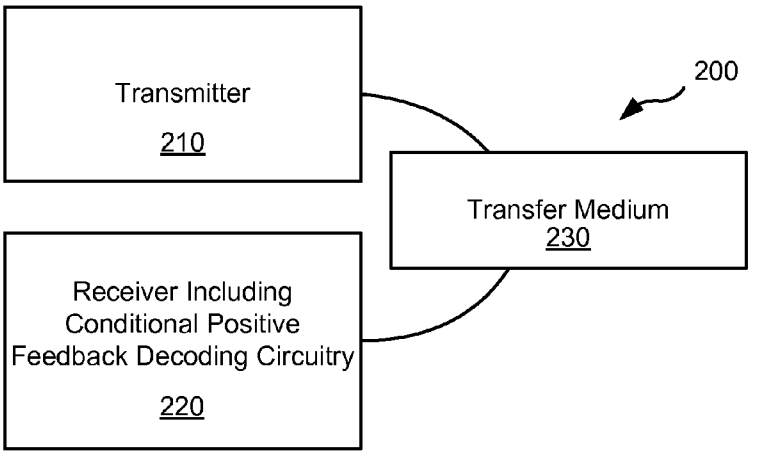

Transmitter 210
200
Transfer Medium 230
Receiver Including Conditional Positive Feedback Decoding Circuitry 220

Fig. 2

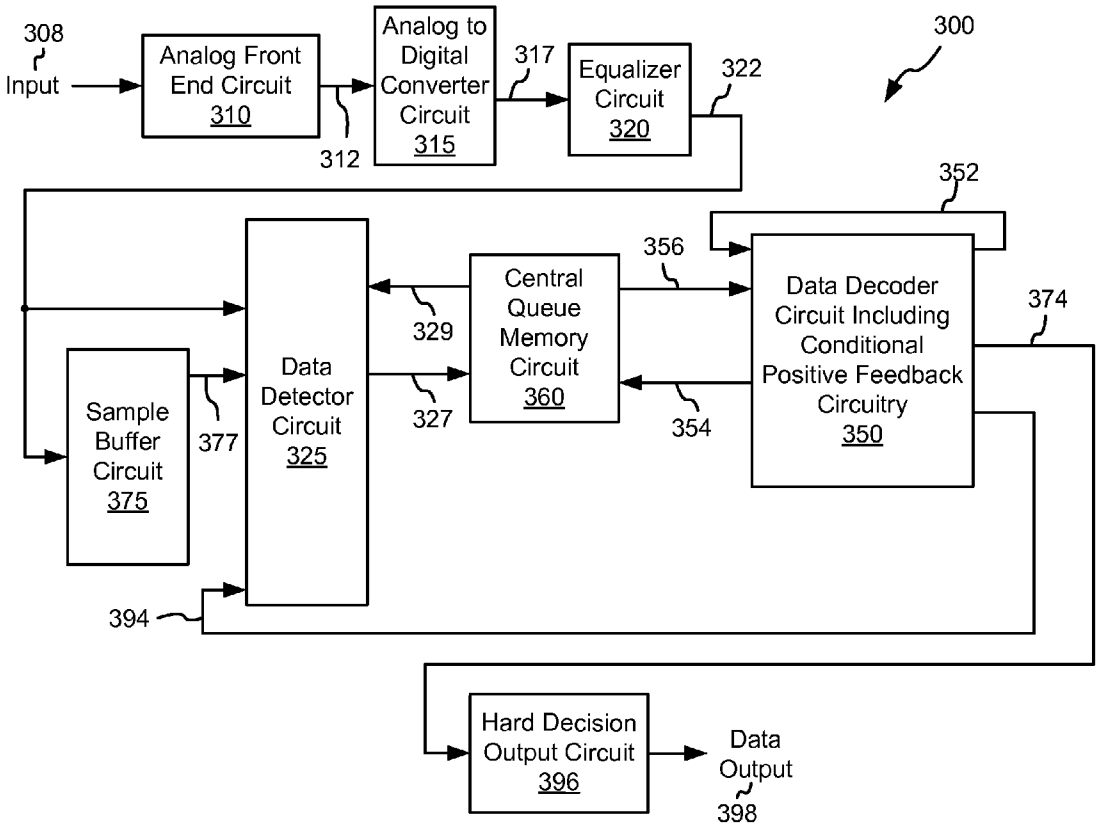

308
Input
Analog Front End Circuit 310
312
Analog to Digital Converter Circuit 315
317
Equalizer Circuit 320
322
300
352
356
Central Queue Memory Circuit 360
329
327
354
Data Decoder Circuit Including Conditional Positive Feedback Circuitry 350
374
Sample Buffer Circuit 375
377
Data Detector Circuit 325
394
Hard Decision Output Circuit 396
Data Output
398

Fig. 3a

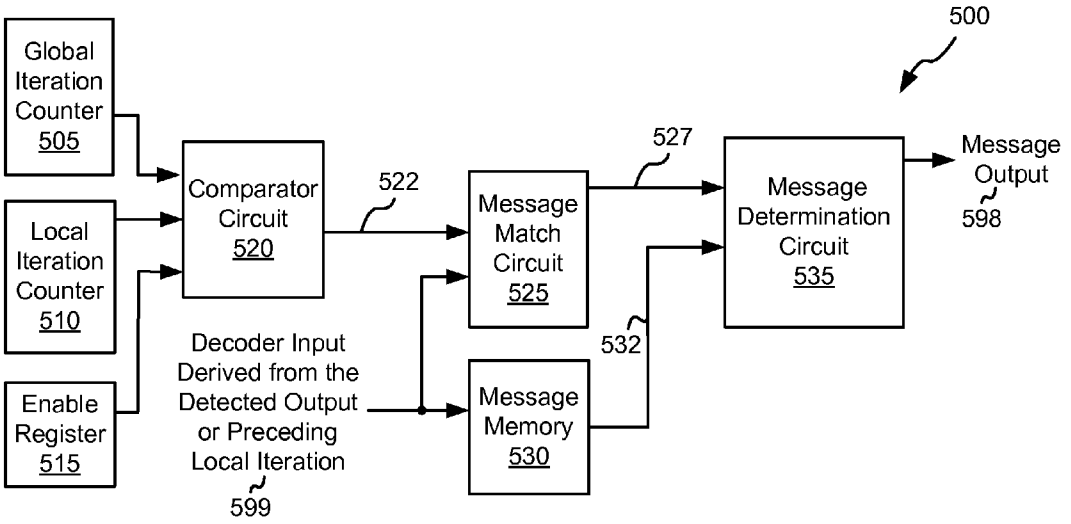


Fig. 3b

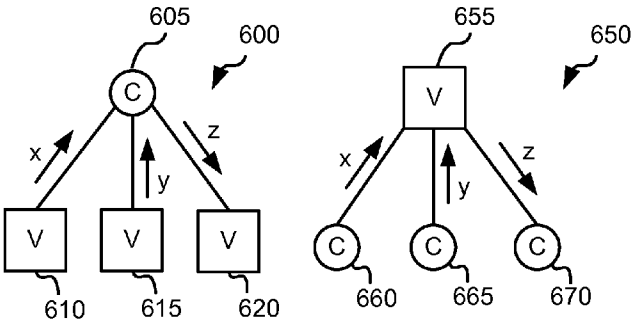


Fig. 3c

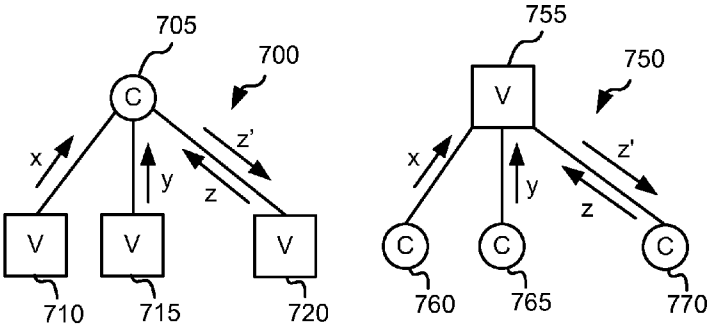


Fig. 3d

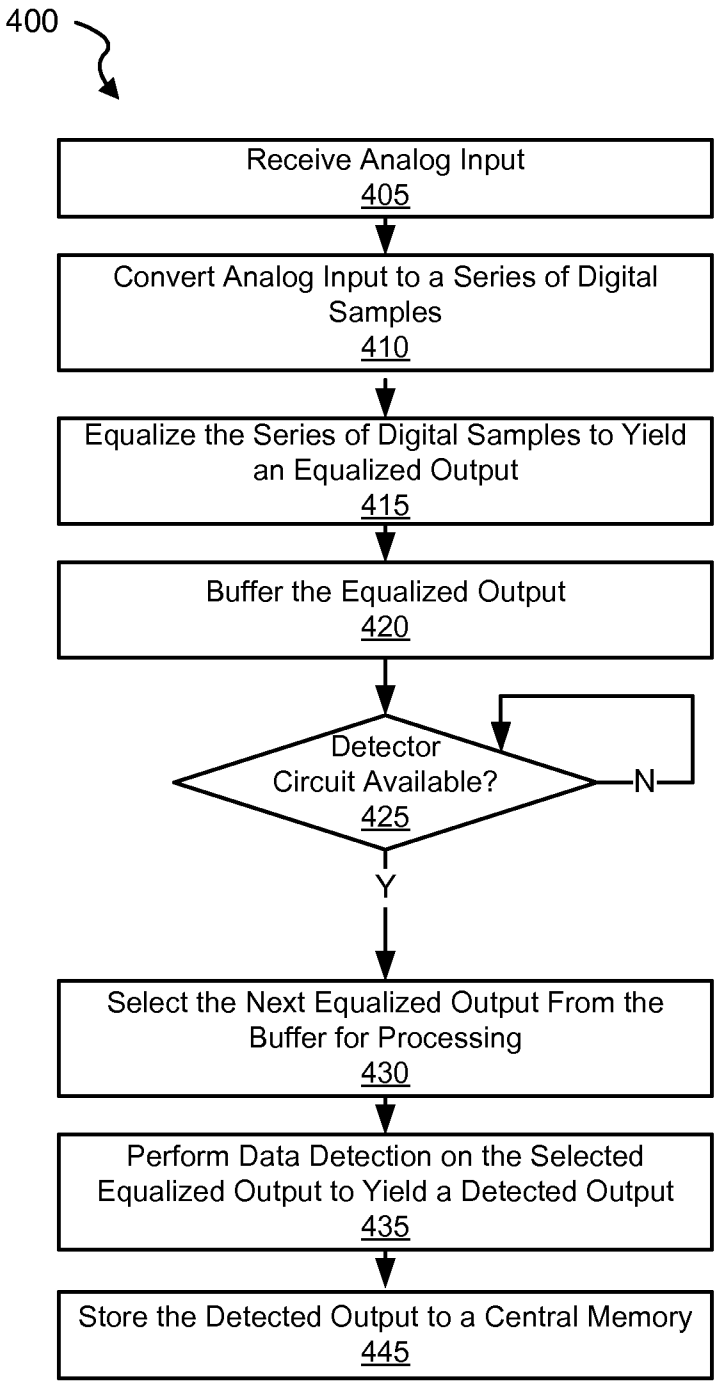

400
Receive Analog Input
405
Convert Analog Input to a Series of Digital Samples
410
Equalize the Series of Digital Samples to Yield an Equalized Output
415
Buffer the Equalized Output
420
Detector Circuit Available?
425
N
Y
Select the Next Equalized Output From the Buffer for Processing
430
Perform Data Detection on the Selected Equalized Output to Yield a Detected Output
435
Store the Detected Output to a Central Memory
445

Fig. 4a

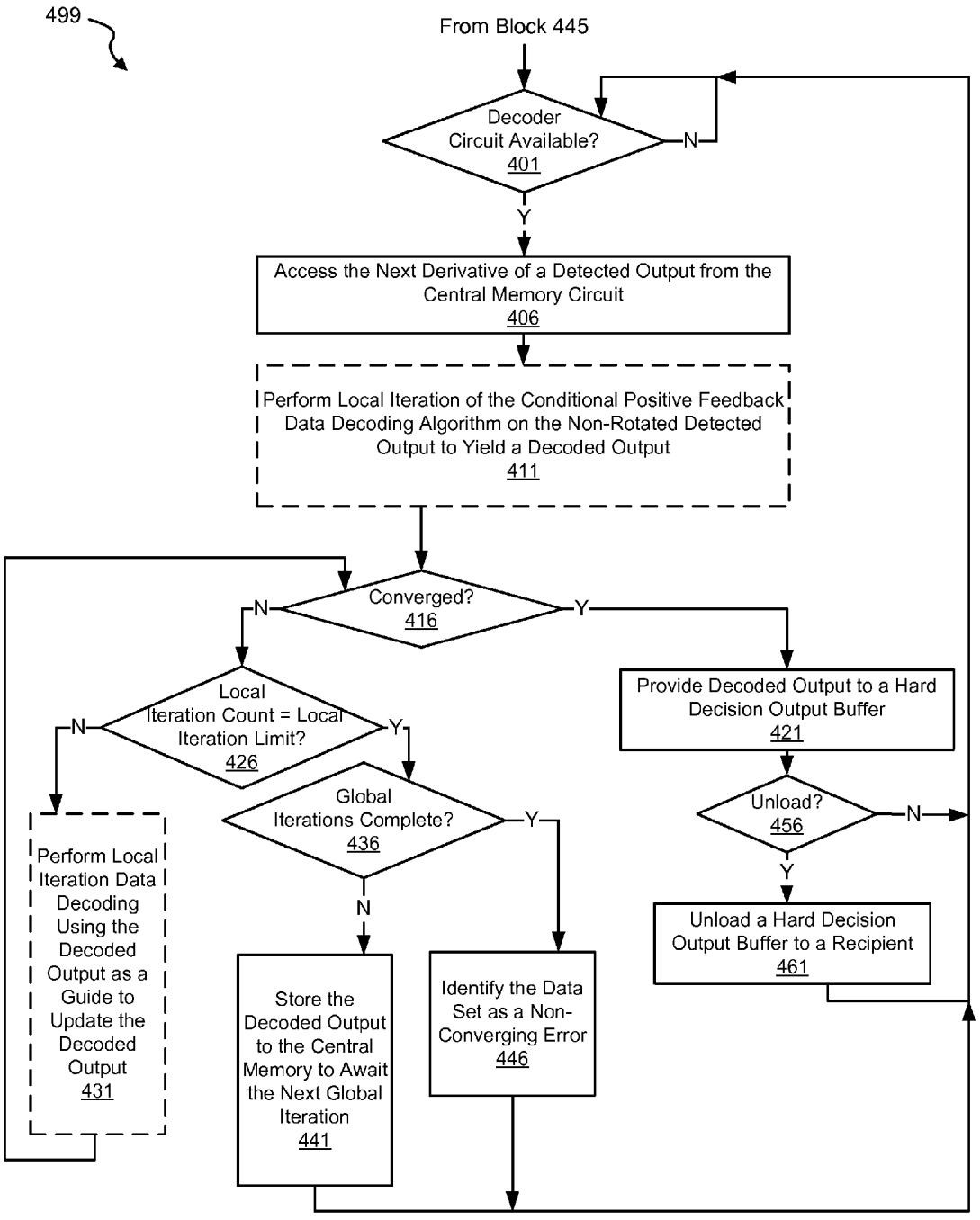

499
From Block 445
Decoder Circuit Available? 401
N
Y
Access the Next Derivative of a Detected Output from the Central Memory Circuit 406
Perform Local Iteration of the Conditional Positive Feedback Data Decoding Algorithm on the Non-Rotated Detected Output to Yield a Decoded Output 411
Converged? 416
N
Y
Local Iteration Count = Local Iteration Limit? 426
N
Y
Global Iterations Complete? 436
Y
N
Perform Local Iteration Data Decoding Using the Decoded Output as a Guide to Update the Decoded Output 431
Store the Decoded Output to the Central Memory to Await the Next Global Iteration 441
Identify the Data Set as a Non-Converging Error 446
Provide Decoded Output to a Hard Decision Output Buffer 421
Unload? 456
N
Y
Unload a Hard Decision Output Buffer to a Recipient 461

Fig. 4b

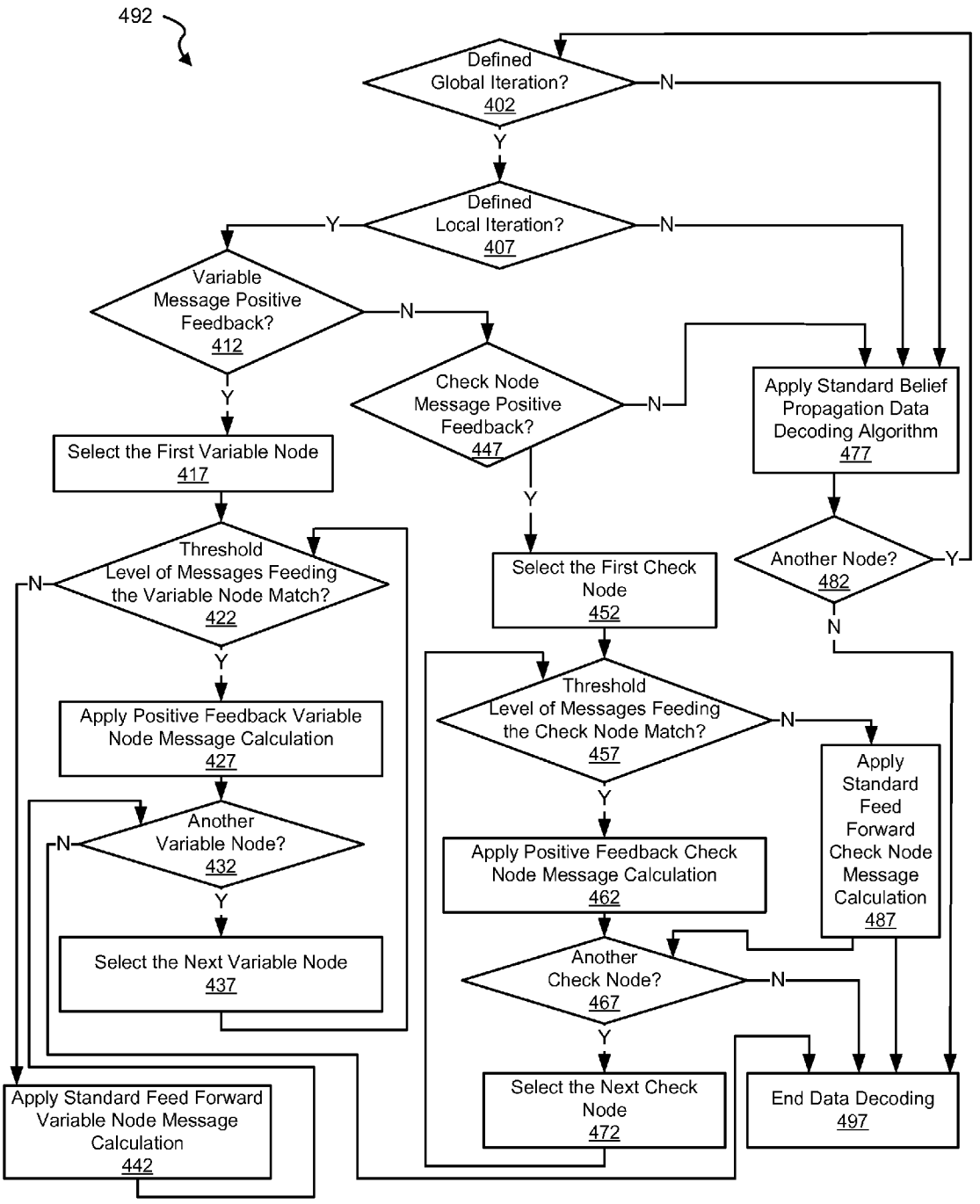

492
Defined Global Iteration? 402
N
Y
Defined Local Iteration? 407
Y
N
Variable Message Positive Feedback? 412
N
Y
Check Node Message Positive Feedback? 447
N
Y
Apply Standard Belief Propagation Data Decoding Algorithm 477
Another Node? 482
Y
N
Select the First Variable Node 417
Threshold Level of Messages Feeding the Variable Node Match? 422
N
Y
Apply Positive Feedback Variable Node Message Calculation 427
Another Variable Node? 432
N
Y
Select the Next Variable Node 437
Apply Standard Feed Forward Variable Node Message Calculation 442
Select the First Check Node 452
Threshold Level of Messages Feeding the Check Node Match? 457
N
Y
Apply Positive Feedback Check Node Message Calculation 462
Apply Standard Feed Forward Check Node Message Calculation 487
Another Check Node? 467
N
Y
Select the Next Check Node 472
End Data Decoding 497

Fig. 4c

SYSTEMS AND METHODS FOR CONDITIONAL POSITIVE FEEDBACK DATA DECODING

BACKGROUND OF THE INVENTION

[0001] The present inventions are related to systems and methods for data processing, and more particularly to systems and methods for data decoding.

[0002] Various data transfer systems have been developed including storage systems, cellular telephone systems, radio transmission systems. In each of the systems data is transferred from a sender to a receiver via some medium. For example, in a storage system, data is sent from a sender (i.e., a write function) to a receiver (i.e., a read function) via a storage medium. In some cases, the data processing function uses a variable number of iterations through a data detector circuit and/or data decoder circuit depending upon the characteristics of the data being processed. Depending upon a number of factors, different data sets require more or fewer iterations through the data detector circuit and/or the data decoder circuit. In some cases, more iterations alone do not allow for convergence of the processing data set.

[0003] Hence, for at least the aforementioned reasons, there exists a need in the art for advanced systems and methods for data processing.

BRIEF SUMMARY OF THE INVENTION

[0004] The present inventions are related to systems and methods for data processing, and more particularly to systems and methods for data decoding.

[0005] Various embodiments of the present invention provide data processing systems include a data decoder circuit that is operable to apply a conditional data decoding algorithm to a data set to yield a decoded output. The conditional decoding algorithm is operable to calculate node messages using either a first message determination mechanism, and a second message determination mechanism. The selection between the first message determination mechanism and the second message determination mechanism is based upon a condition.

[0006] This summary provides only a general outline of some embodiments of the invention. The phrases "in one embodiment," "according to one embodiment," "in various embodiments", "in one or more embodiments", "in particular embodiments" and the like generally mean the particular feature, structure, or characteristic following the phrase is included in at least one embodiment of the present invention, and may be included in more than one embodiment of the present invention. Importantly, such phases do not necessarily refer to the same embodiment. Many other embodiments of the invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] A further understanding of the various embodiments of the present invention may be realized by reference to the figures which are described in remaining portions of the specification. In the figures, like reference numerals are used throughout several figures to refer to similar components. In some instances, a sub-label consisting of a lower case letter is associated with a reference numeral to denote one of multiple similar components. When reference is made to a reference numeral without specification to an existing sub-label, it is intended to refer to all such multiple similar components.

[0008] FIG. **1** shows a storage system including conditional positive feedback decoding circuitry in accordance with various embodiments of the present invention;

[0009] FIG. **2** depicts a data transmission system including conditional positive feedback decoding circuitry in accordance with one or more embodiments of the present invention;

[0010] FIG. **3***a-d* shows a data processing circuit including a data decoder circuit with conditional positive feedback circuitry in accordance with some embodiments of the present invention; and

[0011] FIGS. **4***a*-**4***c* are flow diagrams showing a method for conditional positive feedback processing in accordance with some embodiments of the present invention.

DETAILED DESCRIPTION OF SOME EMBODIMENTS OF THE INVENTION

[0012] The present inventions are related to systems and methods for data processing, and more particularly to systems and methods for data decoding.

[0013] It has been discovered that introducing positive feedback in decoder messaging can create a system perturbation sufficient to move an iterative data processing algorithm away from a trapping set or other impediment to convergence. In some embodiments of the present invention, such positive feedback is applied to decoder message determination whenever a defined condition is achieved. The condition may include, for example, a particular global and local iteration during which a defined threshold of messages used in the determination match each other. Where this condition is met, positive feedback is applied in the message determination of the data decoder circuit.

[0014] Various embodiments of the present invention provide data processing systems include a data decoder circuit that is operable to apply a conditional data decoding algorithm to a data set to yield a decoded output. The conditional decoding algorithm is operable to calculate node messages using either a first message determination mechanism, and a second message determination mechanism. The selection between the first message determination mechanism and the second message determination mechanism is based upon a condition. In some instances of the aforementioned embodiments, the condition includes a global iteration count applied to the data set. In one or more instances of the aforementioned embodiments, the condition includes a local iteration count applied to the data set. In various instances of the aforementioned embodiments, includes a number of messages feeding a given node that match. In some such instances, the number of messages is a majority of messages feeding the given node. In one or more such instances, the given node is selected as one of a check node and a variable node. In various cases, the first message determination mechanism is a feed forward determination mechanism, and the second message determination message is a positive feedback determination mechanism. In some such cases, the condition is based at least in part on a number of messages feeding a given node that match, and the positive feedback determination mechanism includes setting the value of the messages for a next iteration equal to the value of the messages that correspond to the message used in the number of messages feeding the given node.

[0015] Other embodiments of the present invention provide methods for data processing that includes: receiving a data

set; determining a processing condition; and applying a data decoding algorithm by a data decoder circuit to the data set to yield a decoded output. Applying the data decoding algorithm includes: selecting one of a first message determination mechanism and a second message determination mechanism as a selected message determination mechanism based at least in part on the processing condition; and performing the selected message determination mechanism. In some instances of the aforementioned embodiments, the processing condition is based upon at least one of: a global iteration count applied to the data set, a local iteration count applied to the data set, and a number of messages feeding a given node that match. In some cases, the processing condition is based upon a combination of at least two of: the global iteration count applied to the data set, the local iteration count applied to the data set, and the number of messages feeding the given node that match. In particular cases, the given node is selected from a group consisting of: a check node, and a variable node. In one or more cases, the first message determination mechanism is a feed forward determination mechanism, and the second message determination message is a positive feedback determination mechanism. In various cases, the processing condition is based at least in part on a number of messages feeding a given node that match; and the positive feedback determination mechanism includes setting the value of the messages for a next iteration equal to the value of the messages that correspond to the message used in the number of messages feeding the given node.

[0016] Turning to FIG. **1**, a storage system **100** including a read channel circuit **110** having conditional positive feedback decoding circuitry is shown in accordance with various embodiments of the present invention. Storage system **100** may be, for example, a hard disk drive. Storage system **100** also includes a preamplifier **170**, an interface controller **120**, a hard disk controller **166**, a motor controller **168**, a spindle motor **172**, a disk platter **178**, and a read/write head **176**. Interface controller **120** controls addressing and timing of data to/from disk platter **178**, and interacts with a host controller **190** that includes out of order constraint command circuitry. The data on disk platter **178** consists of groups of magnetic signals that may be detected by read/write head assembly **176** when the assembly is properly positioned over disk platter **178**. In one embodiment, disk platter **178** includes magnetic signals recorded in accordance with either a longitudinal or a perpendicular recording scheme.

[0017] In a typical read operation, read/write head assembly **176** is accurately positioned by motor controller **168** over a desired data track on disk platter **178**. Motor controller **168** both positions read/write head assembly **176** in relation to disk platter **178** and drives spindle motor **172** by moving read/write head assembly to the proper data track on disk platter **178** under the direction of hard disk controller **166**. Spindle motor **172** spins disk platter **178** at a determined spin rate (RPMs). Once read/write head assembly **176** is positioned adjacent the proper data track, magnetic signals representing data on disk platter **178** are sensed by read/write head assembly **176** as disk platter **178** is rotated by spindle motor **172**. The sensed magnetic signals are provided as a continuous, minute analog signal representative of the magnetic data on disk platter **178**. This minute analog signal is transferred from read/write head assembly **176** to read channel circuit **110** via preamplifier **170**. Preamplifier **170** is operable to amplify the minute analog signals accessed from disk platter **178**. In turn, read channel circuit **110** decodes and digitizes the received analog signal to recreate the information originally written to disk platter **178**. This data is provided as read data **103** to a receiving circuit. A write operation is substantially the opposite of the preceding read operation with write data **101** being provided to read channel circuit **110**. This data is then encoded and written to disk platter **178**.

[0018] As part of processing the received information, read channel circuit **110** applies a data detection algorithm by a data detector circuit to the received data set to yield a detected output. The detected output is provided to a data decoder circuit that applies a data decoding algorithm to yield a decoded output. This decoded output may be fed back to data detector circuit where it guides re-application of the data detection algorithm. This iterative process may continue until either a timeout condition is achieved, or until the original data is recovered. During this processing, the data decoder circuit generally applies a feed forward message determination process. However where a defined condition is met, a positive feedback is added to the standard feed forward message determination. In some cases, the read channel circuit may be implemented similar to that discussed in relation to FIGS. **3***a*-**3***d;* and/or may operate similar to the methods discussed below in relation to FIGS. **4***a*-**4***c*.

[0019] It should be noted that storage system **100** may be integrated into a larger storage system such as, for example, a RAID (redundant array of inexpensive disks or redundant array of independent disks) based storage system. Such a RAID storage system increases stability and reliability through redundancy, combining multiple disks as a logical unit. Data may be spread across a number of disks included in the RAID storage system according to a variety of algorithms and accessed by an operating system as if it were a single disk. For example, data may be mirrored to multiple disks in the RAID storage system, or may be sliced and distributed across multiple disks in a number of techniques. If a small number of disks in the RAID storage system fail or become unavailable, error correction techniques may be used to recreate the missing data based on the remaining portions of the data from the other disks in the RAID storage system. The disks in the RAID storage system may be, but are not limited to, individual storage systems such as storage system **100**, and may be located in close proximity to each other or distributed more widely for increased security. In a write operation, write data is provided to a controller, which stores the write data across the disks, for example by mirroring or by striping the write data. In a read operation, the controller retrieves the data from the disks. The controller then yields the resulting read data as if the RAID storage system were a single disk.

[0020] A data decoder circuit used in relation to read channel circuit **110** may be, but is not limited to, a low density parity check (LDPC) decoder circuit as are known in the art. Such low density parity check technology is applicable to transmission of information over virtually any channel or storage of information on virtually any media. Transmission applications include, but are not limited to, optical fiber, radio frequency channels, wired or wireless local area networks, digital subscriber line technologies, wireless cellular, Ethernet over any medium such as copper or optical fiber, cable channels such as cable television, and Earth-satellite communications. Storage applications include, but are not limited to, hard disk drives, compact disks, digital video disks, magnetic tapes and memory devices such as DRAM, NAND flash, NOR flash, other non-volatile memories and solid state drives.

[0021] In addition, it should be noted that storage system **100** may be modified to include solid state memory that is used to store data in addition to the storage offered by disk platter **178**. This solid state memory may be used in parallel to disk platter **178** to provide additional storage. In such a case, the solid state memory receives and provides information directly to read channel circuit **110**. Alternatively, the solid state memory may be used as a cache where it offers faster access time than that offered by disk platted **178**. In such a case, the solid state memory may be disposed between interface controller **120** and read channel circuit **110** where it operates as a pass through to disk platter **178** when requested data is not available in the solid state memory or when the solid state memory does not have sufficient storage to hold a newly written data set. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of storage systems including both disk platter **178** and a solid state memory.

[0022] Turning to FIG. **2**, a data transmission system **291** including a receiver **295** having conditional positive feedback decoding circuitry is shown in accordance with various embodiments of the present invention. Data transmission system **291** includes a transmitter **293** that is operable to transmit encoded information via a transfer medium **297** as is known in the art. The encoded data is received from transfer medium **297** by a receiver **295**. Receiver **295** processes the received input to yield the originally transmitted data.

[0023] As part of processing the received information, receiver **295** applies a data detection algorithm by a data detector circuit to the received data set to yield a detected output. The detected output is provided to a data decoder circuit that applies a data decoding algorithm to yield a decoded output. This decoded output may be fed back to data detector circuit where it guides re-application of the data detection algorithm. This iterative process may continue until either a timeout condition is achieved, or until the original data is recovered. During this processing, the data decoder circuit generally applies a feed forward message determination process. However where a defined condition is met, a positive feedback is added to the standard feed forward message determination. In some cases, the read channel circuit may be implemented similar to that discussed in relation to FIGS. **3***a*-**3***d;* and/or may operate similar to the methods discussed below in relation to FIGS. **4***a*-**4***c*.

[0024] FIG. **3** shows a data processing circuit **300** a data decoder circuit with conditional positive feedback circuitry in accordance with some embodiments of the present invention. Data processing circuit **300** includes an analog front end circuit **310** that receives an analog signal **308**. Analog front end circuit **310** processes analog signal **308** and provides a processed analog signal **312** to an analog to digital converter circuit **315**. Analog front end circuit **310** may include, but is not limited to, an analog filter and an amplifier circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of circuitry that may be included as part of analog front end circuit **310**. In some cases, analog input signal **308** is derived from a read/write head assembly (not shown) that is disposed in relation to a storage medium (not shown). In other cases, analog input signal **308** is derived from a receiver circuit (not shown) that is operable to receive a signal from a transmission medium (not shown). The transmission medium may be wired or wireless. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of source from which analog input signal **308** may be derived.

[0025] Analog to digital converter circuit **315** converts processed analog signal **312** into a corresponding series of digital samples **317**. Analog to digital converter circuit **315** may be any circuit known in the art that is capable of producing digital samples corresponding to an analog input signal. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of analog to digital converter circuits that may be used in relation to different embodiments of the present invention. Digital samples **317** are provided to an equalizer circuit **320**. Equalizer circuit **320** applies an equalization algorithm to digital samples **317** to yield an equalized output **322**. In some embodiments of the present invention, equalizer circuit **320** is a digital finite impulse response filter circuit as are known in the art. It may be possible that equalized output **322** may be received directly from a storage device in, for example, a solid state storage system. In such cases, analog front end circuit **310**, analog to digital converter circuit **315** and equalizer circuit **320** may be eliminated where the data is received as a digital data input. Equalized output **322** is stored to a sample buffer circuit **375** that includes sufficient memory to maintain one or more codewords until processing of that codeword is completed through a data detector circuit **325** and a data decoder circuit **350** including, where warranted, multiple "global iterations" defined as passes through both data detector circuit **325** and data decoder circuit **350** and/or "local iterations" defined as passes through data decoding circuit **350** during a given global iteration. Sample buffer circuit **375** stores the received data as buffered data **377**.

[0026] Data detector circuit **325** may be any data detector circuit known in the art that is capable of producing a detected output **327**. As some examples, data detector circuit **325** may be, but is not limited to, a Viterbi algorithm detector circuit or a maximum a posteriori detector circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detector circuits that may be used in relation to different embodiments of the present invention. Detected output **325** may include both hard decisions and soft decisions. The terms "hard decisions" and "soft decisions" are used in their broadest sense. In particular, "hard decisions" are outputs indicating an expected original input value (e.g., a binary '1' or '0', or a non-binary digital value), and the "soft decisions" indicate a likelihood that corresponding hard decisions are correct. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of hard decisions and soft decisions that may be used in relation to different embodiments of the present invention.

[0027] Detected output **327** is provided to a central queue memory circuit **360** that operates to buffer data passed between data detector circuit **325** and data decoder circuit **350**. When data decoder circuit **350** is available, data decoder circuit **350** receives detected output **327** from central queue memory **360** as a decoder input **356**. Data decoder circuit **350** applies a data decoding algorithm to decoder input **356** in an attempt to recover originally written data. Application of the data decoding algorithm includes passing messages between variable and check nodes as is known in the art. In most cases, the message passing includes standard belief propagation or feed forward messaging where two or more messages feeding the variable or check node are used to calculate or determine a message to be passed to another node. A graphic **600** of FIG.

3*c* shows an example of such standard belief propagation where three variable nodes are connected to one check node. In this situation, a message x from a variable node **610** and a message y from a variable node **615** are passed to a check node **605**. In turn, check node **605** calculates a message z that is passed to a variable node **620**. Similarly, a graphic **650** of FIG. 3*c* shows another example of such standard belief propagation where three check nodes are connected to one variable node. In this situation, a message a from x check node **660** and a message y from a check node **665** are passed to a variable node **655**. In turn, variable node **655** calculates a message c that is passed to a check node **670**.

[0028] In contrast, where a defined condition is met, the message passing includes novel positive feedback message determination. A graphic **700** of FIG. 3*d* shows an example of such novel positive feedback message determination where three variable nodes are connected to one check node. In this situation, a message x from a variable node **710** and a message y from a variable node **715**, and a message z from variable node **720** are passed to a check node **705**. In turn, check node **705** calculates a message z' that is passed to variable node **720**. Similarly, a graphic **750** of FIG. 3*d* shows another example of such standard belief propagation where three check nodes are connected to one variable node. In this situation, a message x from a check node **760**, a message y from a check node **765**, and a message z from check node **770** are passed to a variable node **755**. In turn, variable node **755** calculates a message z' that is passed to check node **770**.

[0029] Various conditions may be used to trigger the positive feedback message determination. Such conditions may be determined based upon circuit simulations that reveal conditions specific to a given circuit when the positive feedback message determination would be advantageous. For example, positive feedback message determination may be considered advantageous when the probability that a majority of the messages received by a given node are correct is twice the probability that the same majority of messages is incorrect. In such a condition, it has been found that positive feedback message determination results in a reduction in errors when compared to standard belief propagation or feed forward message determination. Using such a metric applied to the two input graphics **700**, **750** described above in relation to FIG. 3*d*, positive feedback message determination is applied when, for example, x=y=Value (i.e., a majority of the input messages match). Further, this positive feedback message determination may be limited to application only during particular global/local iterations through data detector circuit **325** and data decoder circuit **350**. For example, in one particular embodiment of the present invention, positive feedback message determination may be applied when a majority of the messages to a node (i.e., either a variable node or check node) match during any local iteration of either the first global iteration or the tenth global iteration. Where the condition is met, the messages for the succeeding local iteration (i.e., x', y', z') are all set equal to the value of the majority of messages (i.e., Value). Using the graphics of FIG. **7** as an example, where x=y=Value during a defined global/local iteration, the preceding messages are set in accordance with the following equation: x'=y'=z'=Value. Doing so effectuates the positive feedback message determination prescribed when the condition is met.

[0030] Turning to FIG. 3*b*, an example message determination circuit **500** that may be used as part of data decoder circuit **350**. Message determination circuit **500** includes a global iteration counter **505** operable to indicate the number of global iterations (i.e., passes through both data detector circuit **325** and data decoder circuit **350**) that have been applied to a currently processing data set, and a local iteration counter **510** operable to indicate the number of local iterations (i.e., passes through data decoder circuit **350** during any given global iteration). An enable register **515** is a user programmable register operable to receive an indication of which combinations of global and local iterations that positive feedback message determination is enabled. The combinations of global and local iterations from enable register **515** are provided to a comparator circuit **520** where they are compared against the current global and local iteration number from global iteration counter **505** and local iteration counter **510** being applied to the currently processing data set. Where there is a match, comparator circuit **520** asserts an iteration enable **522** to a message match circuit **525**.

[0031] Message match circuit **525** compares the messages received for a given node. Thus, for example, using the graphics of FIGS. **6** and **7**, message match circuit **525** compares messages x and y for a given check node or variable node. Where a majority of the messages match and iteration enable **522** is asserted, message match circuit **525** asserts a message match enable **527**. Otherwise, message match circuit **525** de-asserts message match enable **527**. Again, using the graphics of FIGS. **6** and **7**, where message x equals message y and iteration enable **522** is asserted, message match circuit **525** asserts message match enable **527**. Alternatively, where either iteration enable **522** is not asserted or message x is not equal to message y, message match circuit **525** de-asserts message match enable **527**.

[0032] Message match enable **527** is provided to message determination circuit **535**. A message memory **530** stores messages from a preceding global iteration (i.e., a preceding decoder input derived from the detected output **599**) that are provided as the message output **532** (e.g., x, y, z) to message determination circuit **535**. In addition, decoder input **599** derived from the detected output is provided to message determination circuit **535**. Where match enable **527** is not asserted, message determination circuit **535** provides a message output **598** calculated using standard belief propagation or feed forward message determination as graphically depicted in FIG. **6**. Alternatively, where match enable **527** is asserted indicating a majority of the messages for the given node (i.e., check node or variable node) matched (e.g., x=y=Value), then message determination circuit **535** sets the next messages equal to the majority value (e.g, x'=y'=z'=Value) which is provided as message output **598**.

[0033] Returning to FIG. 3*a*, the result of the data decoding algorithm is provided as a decoded output **354**. Similar to detected output **327**, decoded output **354** may include both hard decisions and soft decisions. For example, data decoder circuit **350** may be any data decoder circuit known in the art that is capable of applying a decoding algorithm to a received input. Data decoder circuit **350** may be, but is not limited to, a low density parity check decoder circuit or a Reed Solomon decoder circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data decoder circuits that may be used in relation to different embodiments of the present invention. Where the original data is recovered (i.e., the data decoding algorithm converges) or a timeout condition occurs, data decoder circuit **350** provides the result of the data decoding algorithm as a data output **374**. Data output **374** is provided to

a hard decision output circuit **396** where the data is reordered before providing a series of ordered data sets as a data output **398**.

[0034] One or more iterations through the combination of data detector circuit **325** and data decoder circuit **350** may be made in an effort to converge on the originally written data set. As mentioned above, processing through both the data detector circuit and the data decoder circuit is referred to as a "global iteration". For the first global iteration, data detector circuit **325** applies the data detection algorithm without guidance from a decoded output. For subsequent global iterations, data detector circuit **325** applies the data detection algorithm to buffered data **377** as guided by decoded output **354**. Decoded output **354** is received from central queue memory **360** as a detector input **329**.

[0035] During each global iteration it is possible for data decoder circuit **350** to make one or more local iterations including application of the data decoding algorithm to decoder input **356**. For the first local iteration, data decoder circuit **350** applies the data decoder algorithm without guidance from a decoded output **352**. For subsequent local iterations, data decoder circuit **350** applies the data decoding algorithm to decoder input **356** as guided by a previous decoded output **352**. In some embodiments of the present invention, a default of ten local iterations is allowed for each global iteration.

[0036] Turning to FIGS. **4***a*-**4***c* are flow diagrams **400**, **499**, **492** showing a method for conditional positive feedback processing in accordance with some embodiments of the present invention. Following flow diagram **400** of FIG. **4***a*, an analog input is received (block **405**). The analog input may be derived from, for example, a storage medium or a data transmission channel. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of sources of the analog input. The analog input is converted to a series of digital samples (block **410**). This conversion may be done using an analog to digital converter circuit or system as are known in the art. Of note, any circuit known in the art that is capable of converting an analog signal into a series of digital values representing the received analog signal may be used. The resulting digital samples are equalized to yield an equalized output (block **415**). In some embodiments of the present invention, the equalization is done using a digital finite impulse response circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of equalizer circuits that may be used in place of such a digital finite impulse response circuit to perform equalization in accordance with different embodiments of the present invention. The equalized output is buffered (block **420**).

[0037] It is determined whether a data detector circuit is available to process a data set (block **425**). Where a data detector circuit is available to process a data set (block **425**), the next equalized output from the buffer is accessed for processing (block **430**). The data detector circuit may be, for example, a Viterbi algorithm data detector circuit or a maximum a posteriori data detector circuit. The next equalized output selected for processing by the available data detector circuit (block **430**), is selected based upon a quality metric that is calculated as more fully discussed below in relation to block **440**. A data detection algorithm is applied to the accessed equalized output by the data detector circuit to yield a detected output (block **435**). The detected output is stored to a central queue memory circuit where it awaits processing by a data decoder circuit (block **445**).

[0038] Turning to FIG. **4***b* and following flow diagram **499**, it is determined whether a data decoder circuit is available (block **401**) in parallel to the previously described data detection process of FIG. **4***a*. The data decoder circuit may be, for example, a low density parity check data decoder circuit as are known in the art. Where the data decoder circuit is available (block **401**) the next derivative of a detected output is selected from the central queue memory circuit (block **406**). The derivative of the detected output may be, for example, an interleaved (shuffled) version of a detected output from the data detector circuit. A first local iteration of a data decoding algorithm is applied by the data decoder circuit to the selected detected output to yield a decoded output (block **411**). The data decoding algorithm includes conditionally application positive feedback message determination. Block **411** is shown in dashed lines indicating that further detail of the conditional processing is set forth in relation to flow diagram **492** of FIG. **4***c*. It is then determined whether the decoded output converged (e.g., resulted in the originally written data as indicated by the lack of remaining unsatisfied checks) (block **416**).

[0039] Where the decoded output converged (block **416**), it is provided as a decoded output codeword to a hard decision output buffer (e.g., a re-ordering buffer) (block **421**). It is determined whether the received output codeword is either sequential to a previously reported output codeword in which case reporting the currently received output codeword immediately would be in order, or that the currently received output codeword completes an ordered set of a number of codewords in which case reporting the completed, ordered set of codewords would be in order (block **456**). Where the currently received output codeword is either sequential to a previously reported codeword or completes an ordered set of codewords (block **456**), the currently received output codeword and, where applicable, other codewords forming an in order sequence of codewords are provided to a recipient as an output (block **461**).

[0040] Alternatively, where the decoded output failed to converge (e.g., errors remain) (block **416**), it is determined whether the number of local iterations already applied equals the maximum number of local iterations (block **426**). In some cases, a default seven local iterations are allowed per each global iteration. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize another default number of local iterations that may be used in relation to different embodiments of the present invention. Where another local iteration is allowed (block **426**), the data decoding algorithm is applied to the selected data set using the decoded output as a guide to update the decoded output (block **431**). Again, the data decoding algorithm includes conditionally application positive feedback message determination. Block **431** is shown in dashed lines indicating that further detail of the conditional processing is set forth in relation to flow diagram **492** of FIG. **4***c*. The processes of blocks starting at block **416** are repeated for the next local iteration.

[0041] Alternatively, where all of the local iterations have occurred (block **426**), it is determined whether all of the global iterations have been applied to the currently processing data set (block **436**). Where the number of global iterations has not completed (block **436**), the decoded output is stored to the central queue memory circuit to await the next global iteration (block **441**). Alternatively, where the number of

global iterations has completed (block **436**), an error is indicated and the data set is identified as non-converging (block **446**).

[0042] Turning to flow diagram **492** of FIG. **4***c*, conditional positive feedback message determination is discussed. Following flow diagram **492**, it is determined whether the current global iteration for the processing data set is equal to a defined global iteration (block **402**). The defined global iteration may be user programmable and selected based upon circuit simulation. Where the current global iteration for the processing data set is not equal to the defined global iteration (block **402**), standard feed forward or belief propagation message determination is performed as part of the decoding algorithm (block **477**). It is then determined whether another node remains to be analyzed (block **482**). Where another node remains (block **482**), the process starting at block **402** is repeated for the next node. Otherwise, where no additional node remains to be analyzed (block **482**), the data decoding algorithm ends (block **497**).

[0043] Where, on the other hand, it is determined whether the current global iteration for the processing data set is equal to a defined global iteration (block **402**), It is determined whether the current local iteration for the processing data set is equal to the defined local iteration (block **407**). The defined local iteration may be user programmable and selected based upon circuit simulation. Where the current local iteration for the processing data set is not equal to the defined local iteration (block **407**), standard feed forward or belief propagation message determination is performed as part of the decoding algorithm (block **477**). It is then determined whether another node remains to be analyzed (block **482**). Where another node remains (block **482**), the process starting at block **402** is repeated for the next node. Otherwise, where no additional node remains to be analyzed (block **482**), the data decoding algorithm ends (block **497**).

[0044] Alternatively, where the current local iteration for the processing data set is equal to the defined local iteration (block **407**), it is determined whether a variable node is being processed and conditional positive feedback is allowed for variable nodes (block **412**). Where a variable node is being processed (block **412**), an initial variable node is selected (block **417**), and it is determined whether a threshold level of the messages feeding the variable node match (block **422**). In some embodiments of the present invention, the threshold level is a majority. Using the graphics of FIG. **7** as an example, where x=y=Value during a defined global/local iteration, then the threshold level is met. Where the threshold level of matching messages is met (block **422**), a positive feedback variable node message determination is performed (block **427**). Such positive feedback variable node message determination includes assigning the messages for the next variable node equal to the value common to the majority messages. Using the graphics of FIG. **7** as an example, where x=y=Value during a defined global/local iteration, then the values x', y', z' for the next local iteration are set equal to Value.

[0045] It is then determined whether another variable node remains to be processed (block **432**). Where another variable node remains to be processed (block **432**), the next variable node is selected (block **437**), and the processes of blocks **422-437** are repeated for the next variable node. Otherwise, where another variable node does not remain (block **432**), the data decoding algorithm ends (block **497**). Alternatively, where the threshold level of messages is not met (block **422**), standard feed forward or belief propagation message determination is performed as part of the decoding algorithm (block **442**).

[0046] Alternatively, it is determined whether a check node is being processed and conditional positive feedback is allowed for check nodes (block **447**), an initial check node is selected (block **452**), and it is determined whether a threshold level of the messages feeding the check node match (block **457**). In some embodiments of the present invention, the threshold level is a majority. Using the graphics of FIG. **7** as an example, where x=y=Value during a defined global/local iteration, then the threshold level is met. Where the threshold level of matching messages is met (block **457**), a positive feedback check node message determination is performed (block **462**). Such positive feedback check node message determination includes assigning the messages for the next variable node equal to the value common to the majority messages. Using the graphics of FIG. **7** as an example, where x=y=Value during a defined global/local iteration, then the values x', y', z' for the next local iteration are set equal to Value.

[0047] It is then determined whether another check node remains to be processed (block **467**). Where another variable node remains to be processed (block **467**), the next check node is selected (block **472**), and the processes of blocks **457-467** are repeated for the next check node. Otherwise, where another check node does not remain (block **467**), the data decoding algorithm ends (block **497**). Alternatively, where the threshold level of messages is not met (block **457**), standard feed forward or belief propagation message determination is performed as part of the decoding algorithm (block **487**).

[0048] Where, on the other hand, a check node is not being processed or conditional positive feedback is not allowed for check nodes (block **447**), standard feed forward or belief propagation message determination is performed as part of the decoding algorithm (block **477**). It is then determined whether another node remains to be analyzed (block **482**). Where another node remains (block **482**), the process starting at block **402** is repeated for the next node. Otherwise, where no additional node remains to be analyzed (block **482**), the data decoding algorithm ends (block **497**).

[0049] It should be noted that the various blocks discussed in the above application may be implemented in integrated circuits along with other functionality. Such integrated circuits may include all of the functions of a given block, system or circuit, or a subset of the block, system or circuit. Further, elements of the blocks, systems or circuits may be implemented across multiple integrated circuits. Such integrated circuits may be any type of integrated circuit known in the art including, but are not limited to, a monolithic integrated circuit, a flip chip integrated circuit, a multichip module integrated circuit, and/or a mixed signal integrated circuit. It should also be noted that various functions of the blocks, systems or circuits discussed herein may be implemented in either software or firmware. In some such cases, the entire system, block or circuit may be implemented using its software or firmware equivalent. In other cases, the one part of a given system, block or circuit may be implemented in software or firmware, while other parts are implemented in hardware.

[0050] In conclusion, the invention provides novel systems, devices, methods and arrangements for out of order data processing. While detailed descriptions of one or more

embodiments of the invention have been given above, various alternatives, modifications, and equivalents will be apparent to those skilled in the art without varying from the spirit of the invention. Therefore, the above description should not be taken as limiting the scope of the invention, which is defined by the appended claims.

What is claimed is:

1. A data processing system, the data processing system comprising:

a data decoder circuit operable to apply a conditional data decoding algorithm to a data set to yield a decoded output; wherein the conditional decoding algorithm is operable to calculate node messages using an approach selected from a group consisting of: a first message determination mechanism, and a second message determination mechanism; and wherein one of the first message determination mechanism and the second message determination mechanism is selected based upon a condition.

2. The data processing system of claim **1**, wherein the condition includes a global iteration count applied to the data set.

3. The data processing system of claim **1**, wherein the condition includes a local iteration count applied to the data set.

4. The data processing system of claim **1**, wherein the condition includes a number of messages feeding a given node that match.

5. The data processing system of claim **4**, wherein the number of messages is a majority of messages feeding the given node.

6. The data processing system of claim **4**, wherein the given node is selected from a group consisting of: a check node, and a variable node.

7. The data processing system of claim **1**, wherein the first message determination mechanism is a feed forward determination mechanism, and wherein the second message determination message is a positive feedback determination mechanism.

8. The data processing system of claim **7**, wherein the condition is based at least in part on a number of messages feeding a given node that match; and wherein the positive feedback determination mechanism includes setting the value of the messages for a next iteration equal to the value of the messages that correspond to the message used in the number of messages feeding the given node.

9. The data processing system of claim **1**, wherein the data processing system further comprises:

a data detector circuit operable to apply a data detection algorithm to an input to yield a detected output, and wherein the data set is derived from the detected output.

10. The data processing system of claim **9**, wherein the data detector circuit is selected from a group consisting of: a maximum a posteriori data detector circuit, and a Viterbi algorithm data detector circuit.

11. The data processing system of claim **1**, wherein the data decoder circuit is a low density data decoder circuit.

12. The data processing system of claim **1**,wherein the system is implemented as an integrated circuit.

13. The data processing system of claim **1**, wherein the system is implemented as part of device selected from a group consisting of: a storage device, and a communication device.

14. A method for data processing, the method comprising:

receiving a data set;

determining a processing condition; and

applying a data decoding algorithm by a data decoder circuit to the data set to yield a decoded output, wherein applying the data decoding algorithm includes:

selecting one of a first message determination mechanism and a second message determination mechanism as a selected message determination mechanism based at least in part on the processing condition; and

performing the selected message determination mechanism.

15. The method of claim **14**, wherein the processing condition is based upon at least one of: a global iteration count applied to the data set, a local iteration count applied to the data set, and a number of messages feeding a given node that match.

16. The method of claim **15**, wherein the processing condition is based upon a combination of at least two of: the global iteration count applied to the data set, the local iteration count applied to the data set, and the number of messages feeding the given node that match.

17. The method of claim **15**, wherein the given node is selected from a group consisting of: a check node, and a variable node.

18. The method of claim **14**, wherein the first message determination mechanism is a feed forward determination mechanism, and wherein the second message determination message is a positive feedback determination mechanism.

19. The method of claim **18**, wherein the processing condition is based at least in part on a number of messages feeding a given node that match; and wherein the positive feedback determination mechanism includes setting the value of the messages for a next iteration equal to the value of the messages that correspond to the message used in the number of messages feeding the given node.

20. A storage device, the storage device comprising:

a storage medium;

a head assembly disposed in relation to the storage medium and operable to provide a sensed signal corresponding to a data set on the storage;

a read channel circuit including:

an analog front end circuit operable to provide an analog signal corresponding to the sensed signal;

an analog to digital converter circuit operable to sample the analog signal to yield a series of digital samples;

an equalizer circuit operable to equalize the digital samples to yield a sample set;

a data detector circuit operable to apply a data detection algorithm to a the sample set to yield a detected output;

a central memory operable to store a decoder input derived from the detected output;

a data decoder circuit operable to apply a conditional data decoding algorithm to a data set to yield a decoded output; wherein the conditional decoding algorithm is operable to calculate node messages using an approach selected from a group consisting of: a first message determination mechanism, and a second message determination mechanism; and wherein one of the first message determination mechanism and the second message determination mechanism is selected based upon a condition.

* * * * *