(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 295 935 B1**

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification: **23.12.92**

(51) Int. Cl.5: **G11C 16/04**, H01L 27/105

(21) Application number: **88305544.4**

(22) Date of filing: **17.06.88**

(54) **Electrically erasable programmable read only memory.**

(30) Priority: **19.06.87 US 65040**

(43) Date of publication of application:
21.12.88 Bulletin 88/51

(45) Publication of the grant of the patent:
23.12.92 Bulletin 92/52

(84) Designated Contracting States:
DE FR GB NL

(56) References cited:
EP-A- 0 202 785
US-A- 4 377 857
US-A- 4 654 825

IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-20, no. 2, April 1985, New York, US; R. CUPPENS et al.: "An EEPROM for Microprocessors and Custom Logic", pages 603-608

(73) Proprietor: **ADVANCED MICRO DEVICES, INC.**
901 Thompson Place P.O. Box 3453
Sunnyvale, CA 94088(US)

(72) Inventor: **Logie, Stewart**
1090 Tanland Dr. No. 107
Palo Alto California 94303(US)

(74) Representative: **Jones, Ian et al**
POLLAK MERCER & TENCH High Holborn House 52-54 High Holborn
London WC1V 6RY(GB)

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid (Art. 99(1) European patent convention).

EP 0 295 935 B1

Rank Xerox (UK) Business Services

Description

The invention relates to an electrically erasable programmable read only memory (EEPROM).

The most recent generation of memories is the EEPROM, which allows its programmed contents to be electrically erased, thereby allowing reprogramming. Unlike typical erasable programmable read only memories (EPROMs), which are usually erased in bulk by exposure to ultra-violet light, an EEPROM allows electrical erasure, typically within ten milliseconds.

A typical prior art EEPROM is described by Tickle, U.S. Patent No. 4,377,857, issued March 22, 1983. A typical prior art EEPROM cell is shown in Figure 1a and 1b of the accompanying drawings, in which Figure 1a is a cross-sectional view of a prior art EEPROM memory cell, and Figure 1b is a schematic circuit diagram showing the EEPROM cell of Figure 1a in an EEPROM memory circuit with a word line coupling transistor. The prior art memory cell includes transistor 100 having source 101 and drain 102 formed in silicon substrate 99, source 101 and drain 102 being of a conductivity type opposite to that of substrate 99, and having channel region 103 formed therebetween. Gate insulation 104 electrically insulates polycrystalline silicon floating gate 105 from channel 103 and drain 102. A very thin tunnel oxide region 106 electrically insulates a small portion of floating gate 105 from drain 102. This prior art structure further includes control gate 108, and insulation layer 107 formed between floating gate 105 and control gate 108.

Also shown in Figure 1a are the various capacitances which inherently form in the cell: capacitance C_{ch} is the capacitance formed between floating gate 105 and channel region 103: capacitance C_{pp} is the capacitance formed between control gate 108 and floating gate 105; and capacitance C_t is the capacitance formed between floating gate 105 and drain 102.

Shown in Figure 1b is a schematic circuit diagram of a prior art EEPROM which uses transistor 100, shown in Figure 1a, and word coupling transistor 200. Control gate (CG) 108, word line (WL) 205, bit line (BL) 210, connections to substrate 99, and source 101 and drain 102 of transistor 100 are shown. Word line 205 is connected to the control gate of transistor 200. Described below is the operation of such a prior art EEPROM.

Table 1 shows the various voltages applied to the circuit of Figure 1b.

TABLE 1

	WL	BL	CG	Source	Substrate
Read	V_{cc}	V_{sense}	V_r	ground	ground
Write	V_{pp}	ground	V_{pp}	ground	ground
Erase	V_{pp}	V_{pp}	ground	float	ground

In order to store a logical 0 in the EEPROM, electrons are injected into floating gate 105 to provide a negative voltage on floating gate 105, thus increasing the control gate threshold voltage needed to turn on transistor 100. This injection of electrons on floating gate 105 is accomplished, for example, by Fowler-Nordheim tunneling. One technique to achieve this electron tunneling is to place high voltage V_{pp} (typically 15-20 volts) on control gate 108, grounding drain 102 by applying high voltage V_{pp} toword line 205 and grounding bit line 210, and grounding source 101 and substrate 99. This causes electrons to tunnel from drain region 102, through tunneling oxide 106, to floating gate 105, which is capacitively coupled to control gate 108. After this programming of the cell to a logical 0, sufficient electrons are stored within floating gate 105 to increase control gate threshold voltage V_t of transistor 100 (typically to greater than 5 volts) such that transistor 100 will not turn on in response to read voltage V_r applied to control gate 108.

Reading of the state of transistor 100 is accomplished by applying operating voltage V_{cc} (typically five volts) to word line 205 (turning on transistor 200), applying sense voltage V_{sense} (typically $V_{cc}/2$) to bit line 210, applying read voltage V_r to control gate 108, and grounding source 101 of transistor 100. If a logical 0 is stored in the EEPROM (i.e., floating gate 105 is negatively charged) transistor 100 will not turn on in response to read voltage V_r, and no current flows between bit line 210 and source 101 of transistor 100, indicating a logical 0.

In order to erase the EEPROM or, in other words, to change the state of the EEPROM from a logical 0 to a logical 1, floating gate 105 is discharged. This is accomplished, for example, by placing control gate 108 at ground, applying high positive voltage V_{pp} to drain 102 (typically 20 volts) by applying a high voltage to word line 205 and bit line 210, disconnecting source 101 (i.e., source 101 is "floating"), and connecting substrate 99 to ground. This causes electrons to flow from floating gate 105, through tunnel oxide 106, to drain 102, thereby discharging floating gate 105. Discharging floating gate 105 decreases control gate

threshold voltage V_t, and stores a logical 0 in the memory cell. Applying read voltage V_r to control gate 108 will turn on transistor 100 and current will flow between bit line 210 and source 101 of transistor 100, indicating a logical 1.

Using the structure of Figure 1a and the circuit of Figure 1b, programming can also be accomplished by storing a positive charge on floating gate 105. This is done by drawing free electrons from floating gate 105, through tunnel oxide 106, and into drain 102. Erasing is accomplished by drawing electrons back through tunnel oxide 106 from drain 102 and into floating gate 105. Using this method, reading of the cell does not require a voltage to control gate 108 since transistor 100 is already on if floating gate 105 is positively charged (indicating a logical 1) and off if floating gate 105 has no charge (indicating a logical 0). The various voltage levels are shown in Table 2.

TABLE 2

	WL	BL	CG	Source	Substrate
Read	V_{cc}	V_{sense}	ground	ground	ground
Write	V_{pp}	V_{pp}	ground	float	ground
Erase	V_{pp}	ground	V_{pp}	ground	ground

The speed of charging floating gate 105 (i.e., programming the cell) and discharging floating gate (i.e., erasing the cell) is determined by the magnitude of the electric field across tunnel oxide 106. This in turn is dependent on the magnitude of voltage V_{pp}, which is applied between control gate 108 and drain 102, as well as the coupling ratio of the cell. Coupling ratio defines what portion of the applied voltage V_{pp} appears across tunnel oxide 106 between floating gate 105 and drain 102. For the EEPROM shown in Figure 1, the voltage V_f between floating gate 105 and drain 102, during programming, may be expressed as a fraction of the programming voltage V_{pp} as follows:

$$V_f = V_{pp} (C_{pp})/(C_{pp} + C_t + C_{ch})$$

or

$$V_f = V_{pp} \times PCR$$

where PCR is the programming coupling ratio. During erasing, control gate 108 and substrate 99 are grounded, and the voltage V_f between floating gate 105 and drain 102 during erasing may be expressed as follows:

$$V_f = V_{pp} (C_{pp} + C_{ch})/(C_{pp} + C_{ch} + C_t)$$

or

$$V_f = V_{pp} \times ECR$$

where ECR is the erasing coupling ratio.

Since it is desirable to provide an EEPROM cell having high programming and erasing speeds, it is desirable to construct the cell such that the programming and erasing coupling ratios are as close to unity as possible. To accomplish this, the value of capacitance C_t should be made as small as possible, capacitance C_{pp} should be as large as possible, and capacitance C_{ch} should be small during programming and large during erasing. Capacitance is calculated using the equation:

$C = AK\epsilon_0/t$, where

- C is the capacitance
- ϵ_0 is the permittivity of empty space (8.85×10^{-2} $coul^2/newton^2\text{-}m^2$)
- K is the dielectric constant (3.9 for SiO_2)
- A is the plate area, and
- t is the dielectric thickness.

Limiting factors in reducing C_t are that present technology is only capable of producing plate areas down to a minimum of 1 micron^2, and that the thickness of tunnel oxide 106 must be made sufficiently small to allow efficient tunneling to occur between floating gate 105 and drain 102. Capacitance C_{pp} can be increased without limit by reducing dielectric thickness or increasing plate area, thus aiding the efficiency of the cell, however, achieving a consistent thin dielectric thickness over a large area is difficult, and maintaining a small cell size is critical. In the prior art, C_{ch} is not alterable between programming and erasing operations. Thus, there is a tradeoff to be made between reduced cell size versus increased programming and erasing efficiencies. Furthermore, increasing the programming and erasing voltage V_{pp} will increase the speed of programming and erasing the EEPROM cell. However, it is also highly desirable to minimize the programming and erasing voltage V_{pp} to prevent circuit failure due to undesired voltage breakdowns, as well as to avoid the generation of V_{pp} to be unduly burdensome.

Also, manufacturing of prior art EEPROMs involves the relatively complex and time consuming process of forming two separate gates: the floating gate and control gate. Any teaching to eliminate the control gate would reduce cell size, by eliminating contact electrode area, and ease manufacturing complexity and cost. Some prior art EEPROMs, such as that described by R. Cuppens et al. in the article, "An EEPROM for Microprocessors and Custom Logic", IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 2, April 1985, and described by J. Miyamoto et al. in the article, "An Experimental 5-V-Only 256-Kbit CMOS EEPROM with a High Performance Single-Polysilicon Cell", IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, October 1986, use a single layer of polycrystalline silicon (poly-Si) to act as a floating gate and use an N+ diffused area to act as a control gate, which is capacitively coupled to the poly-Si layer. This, however, requires extra substrate surface to form the N+ diffused control gate region.

Finally, prior art devices require the word line transistor, such as that shown in Figure 1b as transistor 200, to operate quickly so reading can be accomplished quickly. Since these word line transistors must be sufficiently large to handle the high programming and erasing voltages, the word line transistors cannot be freely reduced in size for increased speed for reading. One way to decrease the reaction time of the cell is to increase the width of the sense transistor channel. However, this increase in channel width increases capacitance between the floating gate and the substrate, thus, decreasing coupling ratio, and also increases the cell area.

In accordance with the present invention, a single layer of polycrystalline silicon (poly-Si) is used in an EEPROM structure, which obviates the need to form a separate control gate and floating gate. The EEPROM utilizes three separate transistors: a write transistor, a read transistor, and a sense transistor. In the preferred embodiment, the write transistor is an NMOS transistor which has a control gate connected to a word line, the control gate being insulated from a P type channel region by a gate oxide layer. N+ source and drain regions of the write transistor are located at the ends of the channel. When a high positive voltage is applied to the word line, the write transistor turns on. A thin tunnel oxide layer separates the source region of the write transistor from an N doped poly-Si layer and capacitively couples this source region to the poly-Si layer. A relatively thick field oxide layer insulates this poly-Si layer from a substrate region separating the write transistor from the sense transistor. The poly-Si layer extends over the N+ source region of the sense transistor and is capacitively coupled to the source region of the sense transistor via a thin gate oxide insulating layer. This poly-Si layer continues to extend over a channel region separating the N+ source and N+ drain regions of the sense transistor, the poly-Si layer being separated from the channel via the thin gate oxide insulating layer. The drain of the sense transistor also acts as the source of the read transistor, which is also an NMOS transistor. The N+ source and N+ drain of the read transistor are separated by a channel region which conducts when a high positive voltage is applied, via the word line, to a control gate overlying the channel of the read transistor and being insulated from the channel region by the gate oxide layer. In the above structure, the poly-Si layer acts as the floating gate over the channel of the sense transistor.

Since the poly-Si floating gate is both capacitively coupled to the source of the sense transistor and to the source of the write transistor, no separate control gate or control gate electrode is needed (the source of the sense transistor acts as the control gate) and the resulting EEPROM requires less processing steps and less chip area. The structure also enables a higher coupling ratio during erasing, thus allowing faster erase times by coupling a higher voltage onto the poly-Si floating gate. Also, since the read transistor is separate from the write transistor, the read transistor can be made smaller thus allowing faster reading speeds.

The invention will then be seen to provide an EEPROM which is simple to manufacutre, relatively inexpensive, may be programmed and erased dusing a lower voltage than prior art EEPROMS, can be read extremely fast, and uses up less chip surface area.

The invention is further described below, by way of example, with reference to the remaining figures of the accompanying drawings, in which:

Figure 2 is a cross-sectional view of an EEPROM, using a single poly-Si layer, in accordance with the preferred embodiment of the invention,

Figure 3 is a schematic circuit diagram showing the EEPROM of Figure 2 as three separate transistors,

Figure 4 is a cross-sectional view of an EEPROM in accordance with an alternative embodiment of the invention using two poly-Si layers,

Figure 5 is a cross-sectional view of an EEPROM in accordance with an alternative embodiment of the invention using a single poly-Si layer with a separate control region,

Figure 6 is a graph showing the voltage threshold of the sense transistor in Figure 2 given various erase voltages and pulse widths, and

Figure 7 is a graph showing current through the sense transistor of Figure 2 given certain programming voltages and pulse widths.

Figure 2 shows an EEPROM memory cell 10 in accordance with the preferred embodiment of the invention. A P- type substrate 5 has five N+ type regions formed on and below its surface by standard diffusion techniques. These N+ type regions correspond to the source and drain regions of the three transistors which make up the EEPROM memory circuit. Write transistor 20 comprises drain 22, source 24, channel region 25, gate oxide layer 27 and control gate 28. Sense transistor 30 comprises drain 32, source 34, channel region 35, gate oxide layer 37, and N type polycrystalline silicon (poly-Si) floating gate 38. Read transistor 40 comprises drain 41, source 32, which is also the drain of sense transistor 30, channel region 45, gate oxide layer 47, and control gate 48. Poly-Si floating gate 38 is capacitively coupled to source 34 of sense transistor 30, via gate oxide layer 37 (approximately 300Å in thickness), and capacitively coupled to source 24 of write transistor 20 via tunnel oxide layer 55 (approximately 90Å in thickness). Poly-Si floating gate 38 also extends over channel region 35 of sense transistor 30 so that when a sufficient positive charge is on poly-Si floating gate 38, channel 35 will invert and conduct current between source 34 and drain 32 of sense transistor 30. Field oxide layer 57 insulates floating gate 38 from the underlying substrate 5 separating sense transistor 30 and write transistor 20.

Operation of the memory cell 10 will be described with reference to Figures 2 and 3. In Figure 3 word line WL is connected to control gates 28 and 48 of write transistor 20 and read transistor 40, respectively. Tunnel oxide layer 55 is represented by capacitor C_t while gate oxide layer 37 between source 34 of sense transistor 30 and poly-Si floating gate 38 is represented by capacitor C_g. Drain and source contacts are represented by D and S, respectively.

The three operations of the memory circuit are write, erase, and read. The various voltages applied to the circuit of Figure 3 is shown in Table 3.

TABLE 3

	WL	Write	Read	Source	Substrate
Read	V_{cc}	ground	V_{sense}	ground	ground
Write	V_{pp}	V_{pp}	ground	ground	ground
Erase	V_{pp}	ground	V_{pp}	V_{pp}	ground

When N type poly-Si floating gate 38 is written upon, or programmed, floating gate 38 is given a positive charge by removing free electrons from floating gate 38. To accomplish this, first, a high programming voltage V_{pp} is applied to word line WL, which turns on write and read transistors 20 and 40. By turning on transistor 20, a write signal applied to drain 22 of write transistor 20 is coupled to source 24 of write transistor 20. Similarly, when transistor 40 is on, a read signal applied to drain 41 of read transistor 40 is coupled to source 32 of read transistor 40. Next, in order to program sense transistor 30, high programming voltage V_{pp} is applied to drain 22 of write transistor 20, and source 34 of sense transistor 30, as well as drain 41 of read transistor 40 and substrate 5, is grounded. Since source 24 of write transistor 20 is at a high voltage and source 34 of sense transistor 30 is grounded, voltage is capacitively coupled to poly-Si floating gate 38 due to the electric field created between source 24 and source 34 through gate oxide layer 37 and tunnel oxide layer 55.

Since the capacitance between source 24 and floating gate 38 across tunnel oxide layer 55 is very small (on the order of 0.004pF), and the capacitance between source 34 and floating gate 38 across gate oxide layer 37 is about ten times greater, a large percentage (on the order of 90%) of the voltage difference between source 24 and source 34 (i.e., V_{pp}) appears between source 24 and floating gate 38 across tunnel oxide layer 55. This voltage is sufficient to cause electron tunneling from floating gate 38 to source 24 of write transistor 20 through tunnel oxide layer 55, resulting in a net positive charge on floating gate 38. The

positive charge is sufficient to turn on sense transistor 30 because floating gate 38 extends over channel region 35 of sense transistor 30. This indicates a logical 1 since current can flow through sense transistor 30 during a read operation.

To erase floating gate 38, high programming voltage V_{pp} is applied to word line WL as well as source 34 of sense transistor 30 and drain 41 of read transistor 40, while drain 22 of write transistor 20 and substrate 5 are grounded. In this biasing arrangement, the high voltage at source 34 of sense transistor 30 is capacitively coupled to floating gate 38 and almost all of high programming voltage V_{pp} appears across tunnel oxide layer 55 between floating gate 38 and grounded drain 24. This causes electrons from drain 24 to tunnel through tunnel oxide layer 55, resulting in a net negative charge on floating gate 38. Thus, channel 35 of sense transistor 30 is not inverted and sense transistor 30 is shut off.

When reading the state of sense transistor 30, operating voltage V_{cc}, which is less than programming voltage V_{pp}, is applied to word line WL, and voltage V_{sense} (usually $V_{cc}/2$) is applied to drain 41 of read transistor 40. Drain 22 of write transistor 20, as well as source 34 of sense transistor 30 and substrate 5, are grounded. A current flows between drain 41 and source 34 if sense transistor 30 is on, indicating a logical 1. If sense transistor 30 is off, current does not flow, indicating a logical 0.

Since sense transistor 30 and read transistor 40 are not subject to high voltage V_{pp} between their source and drain regions, their channel lengths may be made short to increase reading speed.

During the erase operation, source 34 and drain 32 of sense transistor 30 are at a high voltage while substrate 5 is grounded. This drives channel 35 into deep depletion, thus reducing the undesired parasitic capacitance between floating gate 38 and channel 35 and, hence, creating a higher coupling ratio during the erase operation, enabling faster erase times. During the writing operation, both source 34 and channel region 35 are grounded so no undesired parasitic capacitances exist.

Prior art cells which use a separate control gate above the floating gate, such as that shown in Figure 1, and apply the voltages shown in Table 2, incur a higher undesired capacitance between the floating gate and the substrate during erasing. This is because, during erasing of the floating gate, the source is floating or at a ground potential to prevent current from flowing through the transistor during erasing, and, consequently, the channel is not driven into deep depletion. To offset this higher capacitance between the floating gate and the substrate, a higher capacitance must be created between the control gate and the floating gate by increasing the area of the control gate. This undesirably increases the size of the EEPROM itself.

Prior art cells such as that shown in Figure 1 which apply the voltages shown in Table 1, incur a similar undesired capacitance between the floating gate and the substrate, as discussed above, but during the write operation.

Since the memory cell couples a greater voltage to floating gate 38, the tunnel oxide area under tunnel oxide layer 55 may be made smaller than the prior art tunnel oxide area, thus allowing less chance of defects in the formation of the thin tunnel oxide layer. In the preferred embodiment, the tunnel oxide area is approximately 1 micron^2. Prior art tunnel oxide areas are typically 10-15 microns^2. Thus,the invention enables an EEPROM to be formed which requires less chip area (approximately 200 microns^2) than prior art devices, has faster read times, can be formed with less chance of defects, and can be made with less processing steps than prior art devices requiring a separate control gate.

In an alternative embodiment, shown in Figure 4, the EEPROM of Figure 2 uses a separate poly-Si control gate 36 to capacitively couple voltage to floating gate 38. Insulating, or coupling, layer 50 insulates control gate 36 and floating gate 38 from each other, and its thickness can be adjusted to obtain the desired capacitance between control gate 36 and floating gate 38. In this configuration, control gate 36 has applied to it the same voltages as the "Source" in Table 3. The added capacitive coupling from control gate 36 increases the coupling ratio during the write and erase operations. During erase, channel 35 is in deep depletion, further increasing the coupling ratio. In this alternative embodiment, coupling layer 50 is 300Å, with the remainder of the dimensions identical to the preferred embodiment described with reference to Figure 2.

In another embodiment, almost identical to that of Figure 4, in which two separate poly-Si layers are used, source 34 is not capacitively coupled to floating gate 38, and the voltage applied to it is irrelevant except during the read operations. However, the same reading, writing, and erasing voltages shown in Table 3 are applied to the remainder of the structure. The control gate has applied to it the same voltages as the "Source" in Table 3. To make negligible the capacitive coupling between source 34 and floating gate 38, a thick insulating layer such as field oxide layer 57, shown in Figure 4, extends over source 34 and separates source 34 from floating gate 38. In this embodiment, as in the embodiments shown in Figures 2 and 4, channel region 35 is in deep depletion during erasing, resulting in an increased coupling ratio and more efficient erasing of the charge on floating gate 38.

In another embodiment, shown in Figure 5, there is a separate N+ diffusion region 39, which acts as a control gate similar to control gate 36 in Figure 4, to capacitively couple voltage to floating gate 38. Insulating, or coupling, layer 37 insulates control gate 39 from floating gate 38. In this configuration, control gate 39 has applied to it the same voltages as the "Source" in Table 3. As in all embodiments, during erase, channel 35 is in deep depletion, and, thus, there is negligible parasitic capacitance between channel 35 and floating gate 38.

Tests performed on an EEPROM in accordance with the preferred embodiment of Figure 2 showed that programming and erasing of the EEPROM can be satisfactorily accomplished using a programming and erasing voltage (V_{pp}) of 14 volts with a pulse width of about 300µs. These results are shown in Figures 6 and 7. Figure 6 shows the resulting threshold voltage of sense transistor 30 when various V_{pp} voltages are applied to the EEPROM at various pulse widths. When the threshold voltage is a positive voltage, sense transistor 30 is off, indicating a logical 0 during the read operation. As seen from Figure 6, a V_{pp} of 14 volts for 300µs, while the EEPROM is biased in the erase mode, will raise the threshold voltage of sense transistor 30 to approximately 2 volts. Figure 7 shows the current through sense transistor 30, given a read voltage (V_{sense}) of 2 volts and a word line voltage (V_{cc}) of 5 volts. As seen, a V_{pp} of 14 volts for 300µs, while the EEPROM is biased in the programming, or write, mode, will enable a current of approximately 250µA to flow through sense transistor 30, indicating that sense transistor 30 is on and, thus, indicating a logical 1.

The preferred and alternative embodiments described are manufactured using well-known techniques, and their method of manufacture will be obvious to those skilled in the art.

This invention is by no means limited to the preferred and alternative embodiments described. While the invention has been particularly shown and described with reference to these preferred and alternative embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the scope of the invention as defined in the appended claims.

Claims

1. An EEPROM comprising a semiconductor substrate (5) of a first conductivity type having a top surface, first (34), second (32), and third (24) regions of a conductivity type opposite that of said substrate formed on and below said surface of said substrate, a channel region (35) between said first and second regions, and a gate oxide layer (37) formed over said channel region (35), characterized by

a tunnel oxide layer (55) formed over said third region (24); and

a floating gate (38) formed over said channel region (35), said floating gate (38) being capacitively coupled to said first region (34) via said gate oxide layer (37) and capacitively coupled to said third region (24) via said tunnel oxide layer (55), said tunnel oxide layer (55) being of a thickness to allow electron tunneling upon incurrence of a sufficient voltage potential between said floating gate (38) and said third region (24).

2. An EEPROM comprising:

a semiconductor substrate (5) of a first conductivity type having a top surface;

a first source region (24) of a write transistor (20) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a first drain region (22) of said write transistor (20) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a first channel region (25) of said write transistor (20) between said first source region (24) and said first drain region (22);

a first control gate (28) formed over and insulated from said first channel region (25);

a second source region (34) of a sense transistor (30) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a second drain region (32) of said sense transistor (30) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a second channel region (35) of said sense transistor (30) between said second source region (34) and said second drain region (32);

a gate oxide layer (37) formed over said second channel region (35) and said second source region (34) of said sense transistor (30);

a third source region (32) of a read transistor (40) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate, said third source region (32) also acting as said second drain region (32) of said sense transistor (30);

a third drain region (41) of said read transistor (40) of a conductivity type opposite that of said

substrate formed on and below said surface of said substrate;
a third channel region (45) of said read transistor (40) between said third source region (32) and said third drain region (41) of said read transistor (40); and
a third control gate (48) formed over and insulated from said third channel region (45),
characterized by
a tunnel oxide layer (55) formed over said first source region (24) of said write transistor (20); and
a floating gate (38) formed over and insulated from said second channel region (35), said second source region (34) of said sense transistor (30) and said first source region (24) of said write transistor (20), said floating gate (38) being capacitively coupled to said second source region (34) via said gate oxide layer (37) and capacitively coupled to said first source region (24) via said tunnel oxide layer (55) of a thickness to allow electron tunneling upon incurrence of a sufficient voltage potential between said floating gate (38) and said first source region (24) of said write transistor (20).

3. An EEPROM comprising:
a semiconductor substrate (5) of a first conductivity type having a top surface;
a first source region (24) of a write transistor (20) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;
a first drain region (22) of said write transistor (20) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;
a first channel region (25) between said first source region (24) and said first drain region (22);
a first control gate (28) overlying and insulated from said first channel region (25);
a second source region (34) of a sense transistor (30) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;
a second drain region (32) of said sense transistor (30) of a conductivity type opposite than of said substrate formed on and below said surface of said substrate;
a second channel region (35) of said sense transistor (30) between said second source region (34) and said second drain region (32);
a gate oxide layer (37) formed over said second channel region (35);
a third source region (32) of a read transistor (40) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate, said third source region (32) also acting as said second drain region (32) of said sense transistor (30);
a third drain region (41) of said read transistor (40) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;
a third channel region (45) of said read transistor (40) between said third source region (32) and said third drain region (41) of said read transistor (40); and
a third control gate (48) formed over and insulated from said third channel region (45),
characterized by
a tunnel oxide layer (55) formed over said first source region (24) of said write transistor (20);
a floating gate (38) formed over and insulated from said second channel region (35) and said first source region (24) of said write transistor (20), said floating gate being capacitively coupled to said first source region (24) of said write transistor (20) via said tunnel oxide layer (55) of a thickness to allow electron tunneling upon incurrence of a sufficient voltage potential between said floating gate (38) and said first source region (24) of said write transistor (20);
an insulating coupling layer (50) formed over said floating gate (38);
a second control gate (36) formed over said coupling layer (50), said second control gate (36), being capacitively coupled to said floating gate (38) via said coupling layer (50).

4. An EEPROM as claimed in claim 3 wherein said floating gate (38) is also formed over and insulated from said second source region (34) of said sense transistor (30) and capacitively coupled to said second source region (34) via said gate oxide layer (37).

5. An EEPROM comprising:
a semiconductor substrate (5) of a first conductivity type having a top surface;
a first source region (24) of a write transistor (20) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;
a first drain region (22) of said write transistor (20) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;
a first channel region (25) between said first source region (24) and said first drain region (22);

a first control gate (28) formed over and insulated from said first channel region (25);

a first control gate region (39) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a second source region (34) of a sense transistor (30) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a second drain region (32) of said sense transistor (30) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a second channel region (35) of said sense transistor (30) between said second source region (34) and said second drain region (32);

a gate oxide layer (37) formed over said second channel region (35) and said first control gate region (39);

a third source region (32) of a read transistor (40) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate, said third source region (32) also acting as said second drain region (32) of said sense transistor (30);

a third drain region (41) of said read transistor (40) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a third channel region (45) of said read transistor (40) between said third source region (32) and said third drain region (41) of said read transistor (40); and

a third control gate (48) formed over and insulated from said third channel region (45),

characterized by

a tunnel oxide layer (55) formed over said first source region (24) of said write transistor (20);

a floating gate (38) formed over and insulated from said second channel region (35), said first control gate region (39) and said first source region (24) of said write transistor (20), said floating gate (38) being capacitively coupled to said first control gate region (39) via said gate oxide layer (37) and capacitively coupled to said first source region (24) of said write transistor (20) via said tunnel oxide layer (55) of a thickness to allow electron tunneling upon incurrence of a sufficient voltage potential between said floating gate (38) and said first source region (24) of said write transistor (20).

6. An EEPROM as claimed in claim 5 characterized in that said gate oxide layer (37) is also formed over said second source region (34) of said sense transistor (30), and said second source region (34) is also capacitively coupled to said floating gate (38).

7. An EEPROM as claimed in any preceding claim wherein said first conductivity type is a P type so that during drawing electrons to said floating gate (38), said second channel region (35) is reverse biased with respect to said second source region (34) and said second drain region (32), thus creating a deep depletion region in said second channel region (35).

Patentansprüche

1. EEPROM mit einem Halbleitersubstrat (5) eines ersten Leitfähigkeittyps, das eine obere Außenfläche aufweist, einem ersten (34), einem zweiten (32) und einem dritten Bereich (24) eines Leitfähigkeittyps, der dem des Substrates entgegengesetzt ist, die an und unter der oberen Außenfläche des Substrates ausgebildet sind, einem Kanalbereich (35) zwischen dem ersten und dem zweiten Bereich und einer Gateoxidschicht (37), die über dem Kanalbereich (25) ausgebildet ist, gekennzeichnet durch

eine Tunneloxidschicht (55), die über dem dritten Bereich (24) ausgebildet ist, und

ein schwebendes Gate (38), das über dem Kanalbereich (35) ausgebildet ist, wobei das schwebende Gate (38) über die Gateoxidschicht (37) kapazitiv mit dem ersten Bereich (34) und über die Tunneloxidschicht (55) kapazitiv mit dem dritten Bereich (24) gekoppelt ist und die Tunneloxidschicht (55) eine derartige Stärke hat, daß beim Anliegen eines ausreichenden Spannungspotentials zwischen dem schwebenden Gate (38) und dem dritten Bereich (24) ein Elektronentunneln möglich ist.

2. EEPROM mit

einem Halbleitersubstrat (5) eines ersten Leitfähigkeitstyps, das eine obere Außenfläche aufweist,

einem ersten Sourcebereich (24) eines Schreibtransistors (20) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,

einem ersten Drainbereich (22) des Schreibtransistors (20) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet

ist,
einem ersten Kanalbereich (25) des Schreibtransistors (20) zwischen dem ersten Sourcebereich (24) und dem ersten Drainbereich (22),
einem ersten Steuergate (28), das über dem ersten Kanalbereich (25) ausgebildet ist und demgegenüber isoliert ist,
einem zweiten Sourcebereich (34) eines Abfragetransistors (30) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,
einem zweiten Drainbereich (32) des Abfragetransistors (30) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,
einem zweiten Kanalbereich (35) des Abfragetransistors (30) zwischen dem zweiten Sourcebereich (34) und dem zweiten Drainbereich (32),
einer Gateoxidschicht (37), die über dem zweiten Kanalbereich (35) und dem zweiten Sourcebereich (34) des Abfragetransistors (30) ausgebildet ist,
einem dritten Sourcebereich (32) eines Lesetransistors (40) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist, wobei der dritte Sourcebereich (32) auch als zweiter Drainbereich (32) des Abfragetransistors (30) arbeitet,
einem dritten Drainbereich (41) des Lesetransistors (40) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,
einem dritten Kanalbereich (45) des Lesetransistors (40) zwischen dem dritten Sourcebereich (32) und dem dritten Drainbereich (41) des Lesetransistors (40), und
einem dritten Steuergate (48), das über dem dritten Kanalbereich (45) ausgebildet und demgegenüber isoliert ist,
gekennzeichnet durch
eine Tunneloxidschicht (55), die über dem ersten Sourcebereich (24) des Schreibtransistors (20) ausgebildet ist, und
ein schwebendes Gate (38), das über dem zweiten Kanalbereich (35), dem zweiten Sourcebereich (34) des Abfragetransistors (30) und dem ersten Sourcebereich (24) des Schreibtransistors (20) ausgebildet und demgegenüber isoliert ist, wobei das schwebende Gate (38) über die Gateoxidschicht (37) mit dem zweiten Sourcebereich (34) kapazitiv gekoppelt ist und über die Tunneloxidschicht (55), die eine derartige Stärke hat, daß beim Anliegen eines ausreichenden Spannungspotentials zwischen dem schwebenden Gate (38) und dem ersten Sourcebereich (24) des Schreibtransistors (20) ein Elektronentunneln möglich ist, kapazitiv mit dem ersten Sourcebereich (24) gekoppelt ist.

3. EEPROM mit
einem Halbleitersubstrat (5) eines ersten Leitfähigkeitstyps, das eine obere Außenfläche hat,
einem ersten Sourcebereich (24) eines Schreibtransistors (20) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,
einem ersten Drainbereich (22) des Schreibtransistors (20) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,
einem ersten Kanalbereich (25) zwischen dem ersten Sourcebereich (24) und dem ersten Drainbereich (22),
einem ersten Steuergate (28), das über dem ersten Kanalbereich (25) liegt und demgegenüber isoliert ist,
einem zweiten Sourcebereich (34) eines Abfragetransistors (30) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,
einem zweiten Drainbereich (32) des Abfragetransistors (30) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,
einem zweiten Kanalbereich (35) des Abfragetransistors (30) zwischen dem zweiten Sourcebereich (34) und dem Zweiten Drainbereich (32),
einer Gateoxidschicht (37), die über dem zweiten Kanalbereich (35) ausgebildet ist,

einem dritten Sourcebereich (32) eines Lesetransistors (40) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist, wobei der dritte Sourcebereich (32) auch als zweiter Drainbereich (32) des Abfragetransistors (30) arbeitet,

einem dritten Drainbereich (41) des Lesetransistors (40) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,

einem dritten Kanalbereich (45) des Lesetransistors (40) zwischen dem dritten Sourcebereich (32) und dem dritten Drainbereich (41) des Lesetransistors (40) und

einem dritten Steuergate (48), das über dem dritten Kanalbereich (45) ausgebildet und demgegenüber isoliert ist,

gekennzeichnet durch

eine Tunneloxidschicht (55), die über dem ersten Sourcebereich (24) des Schreibtransistors (20) ausgebildet ist,

ein schwebendes Gate (38), das über dem zweiten Kanalbereich (35) und dem ersten Sourcebereich (24) des Schreibtransistors (20) ausgebildet und demgegenüber isoliert ist, wobei das schwebende Gate über die Tunneloxidschicht (55), die eine derartige Stärke hat, daß beim Anliegen eines ausreichenden Spannungspotentials zwischen dem schwebenden Gate (38) und dem ersten Sourcebereich (24) des Schreibtransistors (20) ein Elektronentunneln möglich ist, kapazitiv mit dem ersten Sourcebereich (24) des Schreibtransistors (20) gekoppelt ist,

eine isolierende Kopplungsschicht (50), die über dem schwebenden Gate (38) ausgebildet ist, und

ein zweites Steuergate (36), das über der Kopplungsschicht (50) ausgebildet ist, wobei das zweite Steuergate (36) über die Kopplungsschicht (50) kapazitiv mit dem schwebenden Gate (38) gekoppelt ist.

4. EEPROM nach Anspruch 3, bei dem das schwebende Gate (38) auch über dem zweiten Sourcebereich (34) des Abfragetransistors (30) ausgebildet und demgegenüber isoliert ist und über die zweite Gateoxidschicht (37) mit dem zweiten Sourcebereich (34) kapazitiv gekoppelt ist.

5. EEPROM mit

einem Halbleitersubstrat (5) eines ersten Leitfähigkeitstyps, das eine obere Außenfläche aufweist,

einem ersten Sourcebereich (24) eines Schreibtransistors (20) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,

einem ersten Drainbereich (22) des Schreibtransistors (20) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des oberen Substrates ausgebildet ist,

einem ersten Kanalbereich (25) zwischen dem ersten Sourcebereich (24) und dem ersten Drainbereich (22),

einem ersten Steuergate (28), das über dem ersten Kanalbereich (25) ausgebildet und demgegenüber isoliert ist,

einem ersten Steuergatebereich (39) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,

einem zweiten Sourcebereich (34) eines Abfragetransistors (30) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,

einem zweiten Drainbereich (32) des Abfagetransistors (30) eines Leitfähigkeitstyps, der dem der Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,

einem zweiten Kanalbereich (35) des Abfagetransistors (30) zwischen dem zweiten Sourcebereich (34) und dem zweiten Drainbereich (32),

einer Gateoxidschicht (37), die über dem zweiten Kanalbereich (35) und dem ersten Steuergatebereich (39) ausgebildet ist,

einem dritten Sourcebereich (32) eines Lesetransistors (40) eines Leitfähigkeitstyps, der dem des Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist, wobei der dritte Sourcebereich (32) auch als zweiter Drainbereich (32) des Abfragetransistors (30) arbeitet,

einem dritten Drainbereich (41) des Lesetransistors (40) eines Leitfähigkeitstyps, der dem des

Substrates entgegengesetzt ist, der an und unter der oberen Außenfläche des Substrates ausgebildet ist,

einem dritten Kanalbereich (45) des Lesetransistors (40) zwischen dem dritten Sourcebereich (32) und dem dritten Drainbereich (41) des Lesetransistors (40) und

einem dritten Steuergate (48), das über dem dritten Kanalbereich (45) ausgebildet und demgegenüber isoliert ist, gekennzeichnet durch

eine Tunneloxidschicht (55), die über dem ersten Sourcebereich (24) des Schreibtransistors (20) ausgebildet ist, und

ein schwebendes Gate (38), das über dem zweiten Kanalbereich (35), dem ersten Steuergatebereich (39) und dem ersten Sourcebereich (24) des Schreibtransistors ausgebildet und demgegenüber isoliert ist, wobei das schwebende Gate (38) über die Gateoxidschicht (37) kapazitiv mit dem ersten Steuergatebereich (39) gekoppelt ist und über die Tunneloxidschicht (55), die eine derartige Stärke hat, daß beim Anliegen eines ausreichenden Spannungspotentials zwischen dem schwebenden Gate (38) und dem ersten Sourcebereich (24) des Schreibtransistors (20) ein Elektronentunneln möglich ist, kapazitiv mit dem ersten Sourcebereich (24) des Schreibtransistors (20) gekoppelt ist.

6. EEPROM nach Anspruch 5, dadurch gekennzeichnet, daß die Gateoxidschicht (37) auch über dem zweiten Sourcebereich (34) des Abfragetransistors (30) ausgebildet ist und der zweite Sourcebereich (34) kapazitiv auch mit dem schwebenden Gate (38) gekoppelt ist.

7. EEPROM nach einem der vorhergehenden Ansprüche bei dem der erste Leitfähigkeitstyp der P Leitfähigkeitstyp ist, so daß beim Ziehen von Elektronen in das schwebende Gate (38) der zweite Kanalbereich (35) in Sperrichtung bezüglich des zweiten Sourcebereiches (34) und des zweiten Drainbereiches (32) vorgespannt wird, so daß ein tiefer Sperrbereich im zweiten Kanalbereich (35) erzeugt wird.

Revendications

1. EEPROM comprenant un substrat semi-conducteur (5) d'un premier type de conductivité, présentant une surface supérieure, des première (34), deuxième (32) et troisième (24) régions d'un type de conductivité opposé à celui dudit substrat, formées sur et au dessous de ladite surface dudit substrat, une région du canal (35) entre lesdites première et seconde régions, et une couche d'oxyde de porte (37), formée au dessus de ladite région de canal (35),
caractérisée par
une couche d'oxyde de tunnel (55) formée au dessus de ladite troisième région (24) ; et
une porte flottante (38) formée au dessus de ladite région de canal (35), ladite porte flottante (38) étant couplée par capacité à ladite première région (34) au travers de ladite couche d'oxyde de porte (37) et couplée par capacité à ladite troisième région (24) au travers de ladite couche d'oxyde de tunnel (55), ladite couche d'oxyde de tunnel étant d'une épaisseur permettant l'effet de tunnel électronique en présence d'un potentiel de tension suffisant entre ladite porte flottante (38) et ladite troisième région (24).

2. EEPROM comprenant :
un substrat semi-conducteur (5) d'un premier type de conductivité, présentant une surface supérieure ;
une première région de source (24) d'un transistor d'écriture (20) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat ;
une première région de drain (22) dudit transistor d'écriture (20) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat ;
une première région de canal (25) dudit transistor d'écriture (20) entre ladite première région de source (24) et ladite première région de drain (22) ;
une première porte de commande (28), formée au dessus et isolée de ladite première région de canal (25) ;
une seconde région de source (34) d'un transistor de détection (30), d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de la surface dudit substrat ;
une seconde région de drain (32) dudit transistor de détection (30) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de la surface dudit substrat ;
une seconde région de canal (35) dudit transistor de détection (30) entre ladite seconde région de

source (34) et ladite seconde région de drain (32) ;

une couche d'oxyde de porte (37), formée au dessus de ladite seconde région de canal (35) et de ladite seconde région de source (34) dudit transistor de détection (30) ;

une troisième région de source (32) d'un transistor de lecture (40) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat, ladite troisième région de source (32) jouant aussi le rôle dedite seconde région de drain (32) dudit transistor de détection (30) ;

une troisième région de drain (41) dudit transistor de lecture (40) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat ;

une troisième région de canal (45) dudit transistor de lecture (40) entre ladite troisième région de source (32) et ladite troisième région de drain (41) dudit transistor de lecture (40) ; et

une troisième porte de commande (48), formée au dessus et isolée de ladite troisième région de canal (45) ;

caractérisée par

une couche d'oxyde de tunnel (55), formée au dessus de ladite première région de source (24) dudit transistor d'écriture (20) ; et

une porte flottante (38), formée au dessus et isolée de ladite seconde région de canal (35), de ladite seconde région de source (34) dudit transistor de mesure (30) et de ladite première région de source (24) dudit transistor d'écriture (20), ladite porte flottante (38) étant couplée par capacité à ladite seconde région de source (34) au travers de ladite couche d'oxyde de porte (37) et couplée par capacité à ladite première région de source (24) au travers de ladite couche d'oxyde de tunnel (55) d'une épaisseur permettant l'effet de tunnel électronique en présence d'un potentiel de tension suffisant entre ladite porte flottante (38) et ladite première région de source (24) dudit transistor d'écriture (20).

3. EEPROM comprenant :

un substrat semi-conducteur (5) d'un premier type de conductivité, présentant une surface supérieure ;

une première région de source (24) d'un transistor d'écriture (20) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat ;

une première région de drain (22) dudit transistor d'écriture (20) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat ;

une première région de canal (25) entre ladite première région de source (24) et ladite première région de drain (22) ;

une première porte de commande (28), superposée à et isolée de ladite première région de canal (25) ;

une seconde région de source (34) d'un transistor de détection (30), d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de la surface dudit substrat ;

une seconde région de drain (32) dudit transistor de détection (30) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de la surface dudit substrat ;

une seconde région de canal (35) dudit transistor de détection (30) entre ladite seconde région de source (34) et ladite seconde région de drain (32) ;

une couche d'oxyde de porte (37), formée sur de ladite seconde région de canal (35) ;

une troisième région de source (32) d'un transistor de lecture (40) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat, ladite troisième région de source (32) jouant aussi le rôle de seconde région de drain (32) dudit transistor de détection (30) ;

une troisième région de drain (41) dudit transistor de lecture (40) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat ;

une troisième région de canal (45) dudit transistor de lecture (40) entre ladite troisième région de source (32) et ladite troisième région de drain (41) dudit transistor de lecture (40) ; et

une troisième porte de commande (48), formée au dessus et isolée de ladite troisième région de canal (45) ;

caractérisée par

une couche d'oxyde de tunnel (55) formée au dessus de ladite première région de source (24) dudit transistor d'écriture (20) ; et

une porte flottante (38), formée au dessus et isolée de ladite seconde région de canal (35) et de ladite première région de source (24) dudit transistor d'écriture (20), ladite porte flottante étant couplée par capacité à ladite première région de source (24) dudit transistor d'écriture (20) au travers de ladite

couche d'oxyde de tunnel (55) d'une épaisseur permettant l'effet de tunnel électronique en présence d'un potentiel de tension suffisant entre ladite porte flottante (38) et ladite première région de source (24) dudit transistor d'écriture (20) ; et

une couche isolante de couplage (50), formée au dessus de ladite porte flottante (38) ;

5 une seconde porte de commande (36), formée au dessus de ladite couche de couplage (50), ladite seconde porte de commande (36) étant couplée par capacité à ladite porte flottante (38) au travers de ladite couche de couplage (50).

4. EEPROM selon la revendication 3, dans laquelle ladite porte flottante (38) est également formée au
10 dessus et isolée de ladite région de source (34) dudit transistor de mesure (30) et couplée par capacité à ladite seconde région de source (34) au travers de ladite couche d'oxyde de porte (37).

5. EEPROM comprenant :

un substrat semi-conducteur (5) d'un premier type de conductivité, présentant une surface
15 supérieure ;

une première région de source (24) d'un transistor d'écriture (20) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat ;

une première région de drain (22) dudit transistor d'écriture (20) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat ;

20 une première région de canal (25) entre ladite première région de source (24) et ladite première région de drain (22) ;

une première porte de commande (28), formée au dessus et isolée de ladite première région de canal (25) ;

une première région de porte de commande (39) d'un type de conductivité opposé à celui dudit
25 substrat formée sur et au dessous de ladite surface dudit substrat ;

une seconde région de source (34) d'un transistor de détection (30), d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de la surface dudit substrat ;

une seconde région de drain (32) dudit transistor de détection (30) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat ;

30 une seconde région de canal (35) dudit transistor de détection (30) entre ladite seconde région de source (34) et ladite seconde région de drain (32) ;

une couche d'oxyde de porte (37), formée au dessus de ladite seconde région de canal (35) et de ladite première région de porte de commande (39) ;

une troisième région de source (32) d'un transistor de lecture (40) d'un type de conductivité
35 opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat, ladite troisième région de source (32) jouant aussi le rôle dedite seconde région de drain (32) dudit transistor de détection (30) ;

une troisième région de drain (41) dudit transistor de lecture (40) d'un type de conductivité opposé à celui dudit substrat, formée sur et au dessous de ladite surface dudit substrat ;

40 une troisième région de canal (45) dudit transistor de lecture (40) entre ladite troisième région de source (32) et ladite troisième région de drain (41) dudit transistor de lecture (40) ; et

une troisième porte de commande (48), formée au dessus et isolée de ladite troisième région de canal (45) ;

caractérisée par

45 une couche d'oxyde de tunnel (55), formée au dessus de ladite première région de source (24) dudit transistor d'écriture (20) ; et

une porte flottante (38), formée au dessus et isolée de ladite seconde région de canal (35), de ladite première région de porte de commande (39) et de ladite première région de source (24) dudit transistor d'écriture (20), ladite porte flottante (38) étant couplée par capacité à ladite première région
50 de porte de commande au travers de ladite couche d'oxyde de porte (37) et couplée par capacité à ladite première région de source (24) dudit transistor d'écriture (20) au travers de ladite couche d'oxyde de tunnel (55) d'une épaisseur permettant l'effet de tunnel électronique en présence d'un potentiel de tension suffisant entre ladite porte flottante (38) et ladite première région de source (24) dudit transistor d'écriture (20).

55

6. EEPROM selon la revendication 5, caractérisée en ce que ladite couche d'oxyde de porte (37) est également formée au dessus de ladite seconde région de source (34) dudit transistor de détection (30), et en ce que ladite seconde région de source (34) est également couplée par capacité à ladite porte

flottante (38).

7. EEPROM selon l'une quelconque des revendications précédentes, dans laquelle le premier type de conductivité est un type P de sorte que pendant l'extraction d'électrons vers ladite porte flottante (38), ladite seconde région de canal est en polarisation inverse par rapport à ladite seconde région de source (34) et à ladite seconde région de drain (32), ce qui crée une région profonde de déplétion dans ladite seconde région de canal (35).

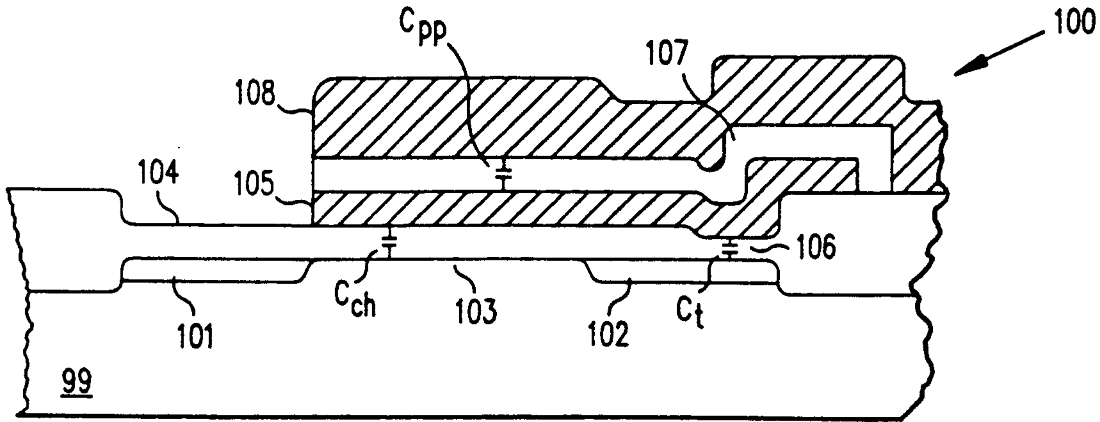

FIG. 1a
(Prior Art)

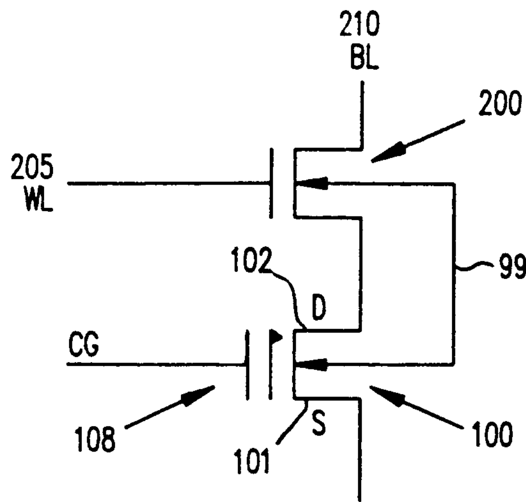

FIG. 1b
(Prior Art)

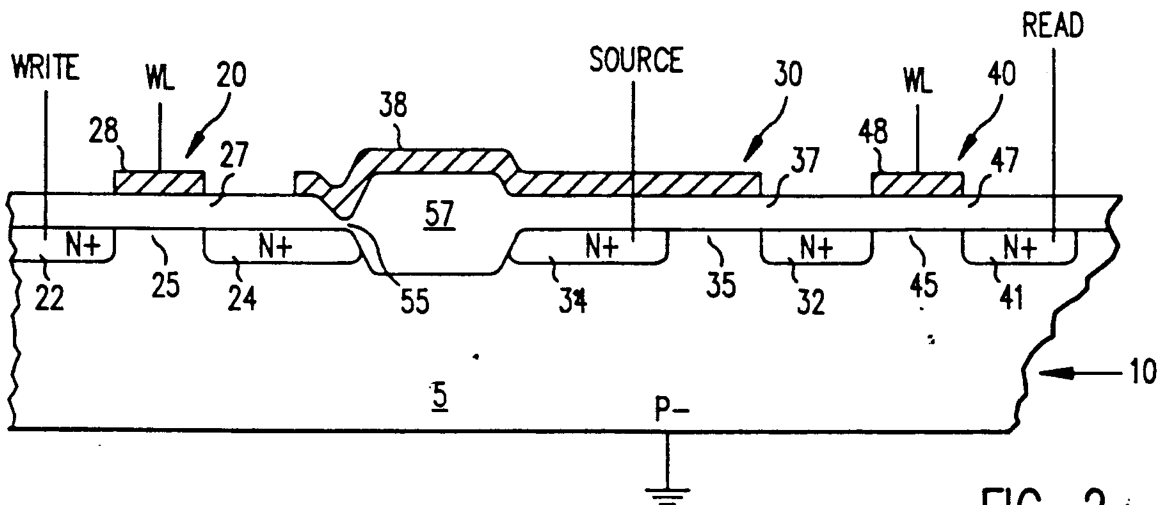

FIG. 2

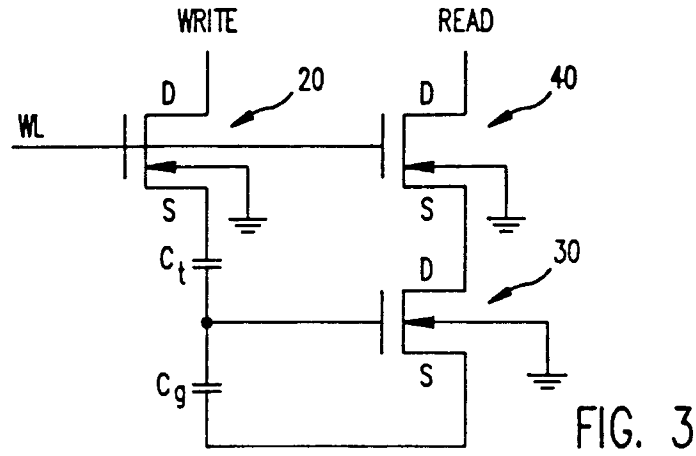

FIG. 3

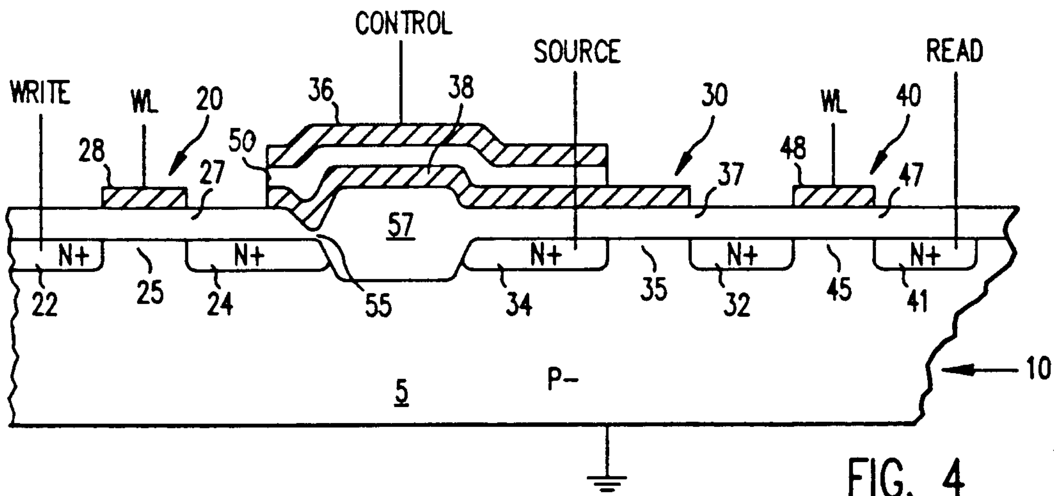

FIG. 4

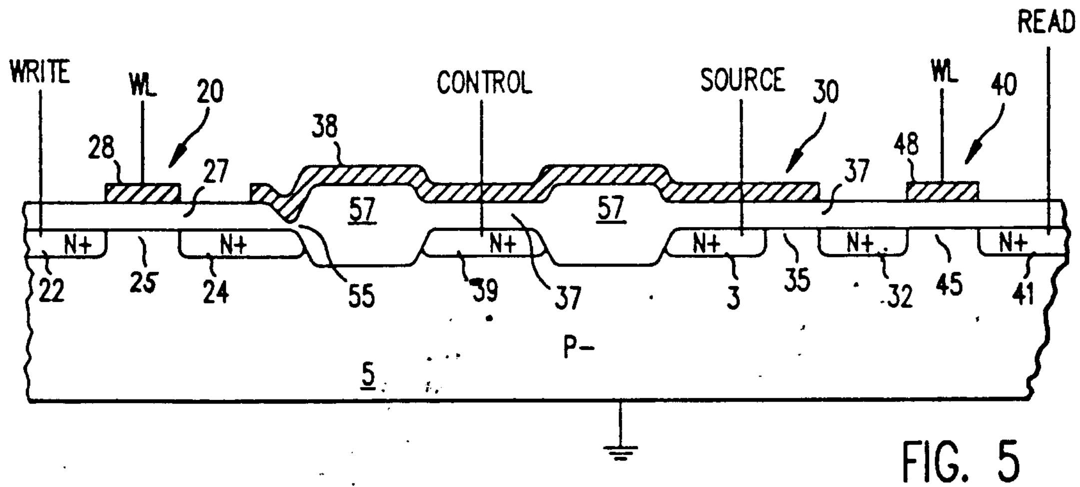

FIG. 5

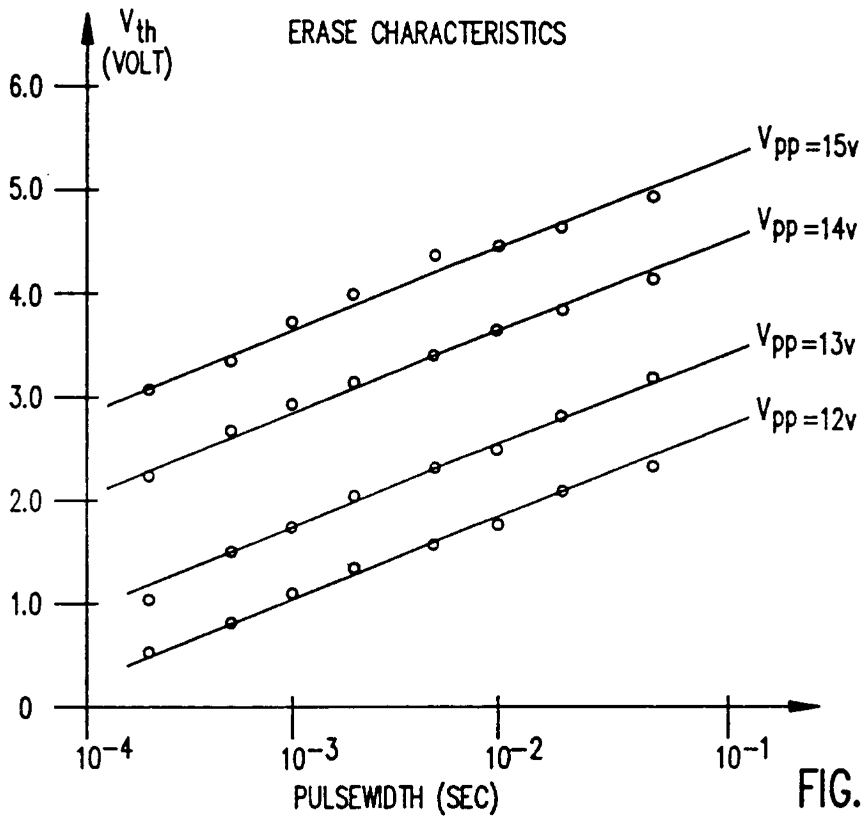

FIG. 6

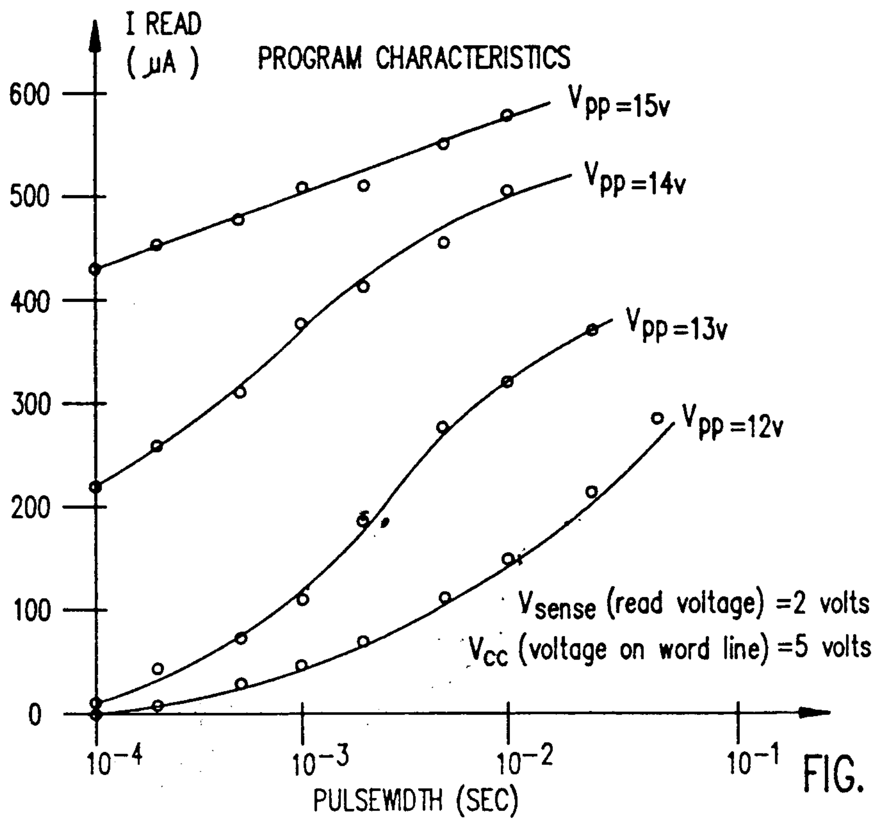

FIG. 7